TPS6113x Synchronous SEPIC and Flyback Converter With 1.1-A Switch and Integrated LDO

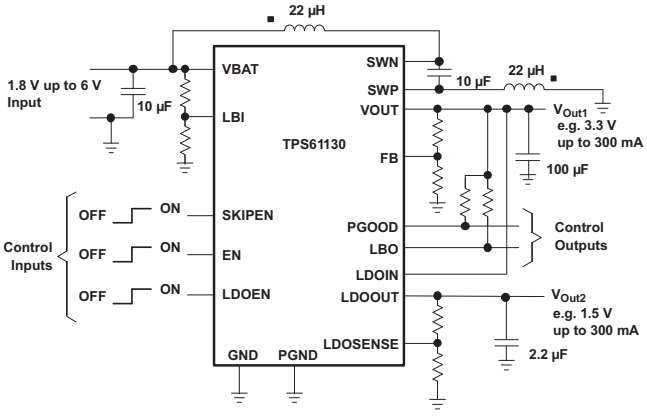
1 Features

- Synchronous, Up to 90% Efficient, SEPIC Converter With 300-mA Output Current From 2.5-V Input
- Integrated 200-mA Reverse Voltage Protected LDO for DC-DC Output Voltage Post Regulation or Second Output Voltage
- 40-µA (Typical) Quiescent Current
- Input Voltage Range: 1.8 V to 5.5 V
- Fixed and Adjustable Output Voltage Options up to 5.5 V
- Power Save Mode for Improved Efficiency at Low-Output Power
- Low Battery Comparator
- Power Good Output
- Low EMI-Converter (Integrated Antiringing Switch)
- Load Disconnect During Shutdown
- Overtemperature Protection
- Available in a Small 4-mm × 4-mm VQFN-16 or in a TSSOP-16 Package

2 Applications

- All Single Cell Li, Dual or Triple Cell Battery or USB Powered Products as MP-3 Player, PDAs, and Other Portable Equipment
- Dual Input or Dual Output Mode
- High Efficient Li-Ion to 3.3-V Conversion

Typical Application Schematic



3 Description

The TPS6113x devices provide a complete power supply solution for products powered by either a one-cell Li-Ion or Li-Polymer, or two- to four-cell Alkaline, NiCd, or NiMH batteries. The devices can generate two regulated output voltages. It provides a simple and efficient buck-boost solution for generating 3.3 V out of an input voltage that can be both higher and lower than the output voltage. The converter provides a maximum output current of at least 300 mA with supply voltages down to 1.8 V. The implemented SEPIC converter is based on a fixed frequency, pulse-width-modulation (PWM) controller using a synchronous rectifier to obtain maximum efficiency. The maximum peak current in the SEPIC switch is limited to a value of 1600 mA.

The converter can be disabled to minimize battery drain. During shutdown, the load is completely disconnected from the battery. A low-EMI mode is implemented to reduce ringing, and in effect, lower radiated electromagnetic energy when the converter enters the discontinuous conduction mode. A power good output at the SEPIC stage provides additional control of any connected circuits like cascaded power supply stages, or microprocessors.

The built-in LDO can be used for a second output voltage derived either from the SEPIC output or directly from the battery. The output voltage of this LDO can be programmed by an external resistor divider or is fixed internally on the chip. The LDO can be enabled separately, that is, using the power good of the SEPIC stage. The device is packaged in a 16-pin VQFN package measuring 4 mm × 4 mm (RSA) or in a 16-pin TSSOP (PW) package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61130	TSSOP (16)	5.00 mm × 4.40 mm
	VQFN (16)	4.00 mm × 4.00 mm
TPS61131	TSSOP (16)	5.00 mm × 4.40 mm
TPS61132		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (January 2008) to Revision C	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

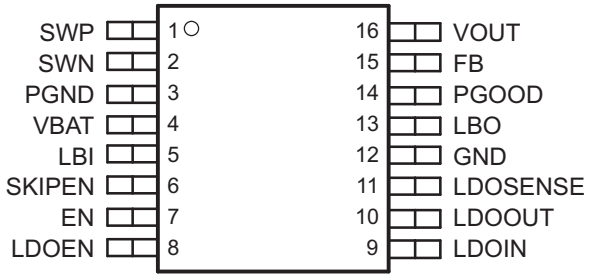
5 Available Output Voltage Options(1)

PART NUMBER(1)	OUTPUT VOLTAGE DC-DC	OUTPUT VOLTAGE LDO
TPS61130PW	Adjustable	Adjustable
TPS61131PW	3.3 V	3.3 V
TPS61132PW	3.3 V	1.5 V
TPS61130RSA	Adjustable	Adjustable
TPS61132RSA	3.3 V	1.5 V

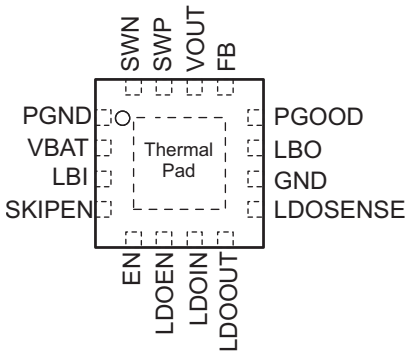
(1) Contact the factory to check availability of other fixed output voltage versions.
(1) The packages are available taped and reeled. Add R suffix to device type (for example, TPS61130PWR or TPS61130RSAR) to order quantities of 2000 devices per reel for the TSSOP (PW) package and 3000 devices per reel for the QFN (RSA) package.

6 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



RSA Package
16-Pin VQFN With Thermal Pad
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	TSSOP	VQFN		
EN	7	5	I	DC-DC-enable input. (1/VBAT enabled, 0/GND disabled)
FB	15	13	I	DC-DC voltage feedback of adjustable versions
GND	12	10	—	Control/logic ground
LBI	5	3	I	Low battery comparator input (comparator enabled with EN)
LBO	13	11	O	Low battery comparator output (open drain)
LDOEN	8	6	I	LDO-enable input (1/LDOIN enabled, 0/GND disabled)
LDOOUT	10	8	O	LDO output
LDOIN	9	7	I	LDO input
LDOSENSE	11	9	I	LDO feedback for voltage adjustment, must be connected to LDOOUT at fixed output voltage versions.
PGND	3	1	—	Power ground
PGOOD	14	12	O	DC-DC output power good (1:good, 0:failure) (open drain)
SKIPEN	6	4	I	Enable/disable power save mode (1/VBAT enabled, 0/GND disabled)
SWN	2	16	I	DC-DC switch input
SWP	1	15	I	DC-DC rectifying switch input
VBAT	4	2	I	Supply pin
VOUT	16	14	O	DC-DC output
Thermal Pad			—	Must be soldered to achieve appropriate power dissipation. Should be connected to PGND.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Input voltage on FB	–0.3	3.6	V
Input voltage on SWN	–0.3	12	V
Input voltage on SWP	–7	7	V
Maximum voltage between SWP and VOUT		–12	V
Input voltage on VOUT, LDOIN, LDOOUT, LDOEN, LDOSENSE, PGOOD, LBO, VBAT, LBI, SKIPEN, EN	–0.3	7	V
Operating virtual junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage at VBAT	1.8		6.5	V
Operating free air temperature range, T_A	–40		85	°C
Operating virtual junction temperature, T_J	–40		125	°C

7.4 Thermal Information

THERMAL METRIC (1)		TPS61130, TPS61131, TPS61132	TPS61130	UNIT
		PW (TSSOP)	RSA (VQFN)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	100.5	33.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.9	36.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.4	11	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.6	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44.8	11	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC-DC STAGE							
V_I	Input voltage range			1.8		6.5	V
V_O	Adjustable output voltage range (TPS61130)			2.5		5.5	V
V_{ref}	Reference voltage			485	500	515	mV
f	Oscillator frequency			400	500	600	kHz
I_{SW}	Switch current limit		VOUT = 3.3 V	1100	1300	1600	mA
	Start-up current limit				0.4 x I_{SW}		mA
	SWN switch on resistance		VOUT = 3.3 V		200	350	mΩ
	SWP switch on resistance		VOUT = 3.3 V		250	500	mΩ
	Total accuracy (including line and load regulation)					±3%	
	DC-DC quiescent current	into VBAT	I_O = 0 mA, V_{EN} = VBAT = 1.8 V, VOUT = 3.3 V, ENLDO = 0 V		10	25	µA
		into VOUT	I_O = 0 mA, V_{EN} = VBAT = 1.8 V, VOUT = 3.3 V, ENLDO = 0 V		10	25	µA
	DC-DC shutdown current		V_{EN}= 0 V		0.2	1	µA
LDO STAGE							
$V_{I(LDO)}$	Input voltage range			1.8		7	V
$V_{O(LDO)}$	Adjustable output voltage range (TPS61130)			0.9		5.5	V
$I_{O(max)}$	Output current			200	320		mA
	LDO short circuit current limit					500	mA
	Minimum voltage drop		I_O = 200 mA			300	mV
	Total accuracy (including line and load regulation)		I_O ≥ 1 mA			±3%	
	Line regulation		LDOIN change from 1.8 V to 2.6 V at 100 mA, LDOOUT = 1.5 V			0.6%	
	Load regulation		Load change from 10% to 90%, LDOIN = 3.3 V			0.6%	
	LDO quiescent current		LDOIN = 7 V, VBAT = 1.8 V, EN = VBAT		20	30	µA
	LDO shutdown current		LDOEN = 0 V, LDOIN = 7 V		0.1	1	µA
CONTROL STAGE							
V_{IL}	LBI voltage threshold		V_{LBI} voltage decreasing	490	500	510	mV
	LBI input hysteresis				10		mV
	LBI input current		EN = VBAT or GND		0.01	0.1	µA
	LBO output low voltage		V_O = 3.3 V, I_{OI} = 100 µA		0.04	0.4	V
	LBO output low current				100		µA
	LBO output leakage current		V_{LBO} = 7 V		0.01	0.1	µA
V_{IL}	EN, SKIPEN input low voltage					0.2 × VBAT	V
V_{IH}	EN, SKIPEN input high voltage			0.8 × VBAT			V
V_{IL}	LDOEN input low voltage					0.2 × V_{LDOIN}	V
V_{IH}	LDOEN input high voltage			0.8 × V_{LDOIN}			V
	EN, SKIPEN input current		Clamped on GND or VBAT		0.01	0.1	µA
	Power-Good threshold		V_O = 3.3 V	0.9 × V_o	0.92 × V_o	0.95 × V_o	V

Electrical Characteristics (continued)

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power-Good delay			30		µs
Power-Good output low voltage	V_O = 3.3 V, I_{OI} = 100 µA		0.04	0.4	V
Power-Good output low current			100		µA
Power-Good output leakage current	V_{PG} = 7 V		0.01	0.1	µA
Overtemperature protection			140		°C
Overtemperature hysteresis			20		°C

7.6 Typical Characteristics

Table 1. Table of Graphs

SEPIC CONVERTER		FIGURE
Maximum output current	vs Input voltage (TPS61130) (V_O = 3.3 V, 5 V, 2.5 V)	Figure 1 Figure 2
Efficiency	vs Output current (TPS61130) (V_O = 2.5 V, V_I = 1.8 V)	Figure 3
	vs Output current (TPS61132) (V_O = 3.3 V, V_I = 1.8 V, 3.8 V)	Figure 4
	vs Output current (TPS61130) (V_O = 5 V, V_I = 3.6 V, 6 V)	Figure 2
	vs Input voltage (TPS61132)	Figure 5
Output voltage	vs Output current (TPS61132)	Figure 6
No-load supply current into VBAT	vs Input voltage (TPS61132)	Figure 7
No-load supply current into VOUT	vs Input voltage (TPS61132)	Figure 8
LDO		
Maximum output current	vs Input voltage (V_O = 2.5 V, 3.3 V)	Figure 9
	vs Input voltage (V_O = 1.5 V, 1.8 V)	Figure 10
Output voltage	vs Output current (TPS61131)	Figure 11
Dropout voltage	vs Output current (TPS61131, TPS61132)	Figure 12
Supply current into LDOIN	vs LDOIN input voltage (TPS61132)	Figure 13
PSRR	vs Frequency (TPS61132)	Figure 14

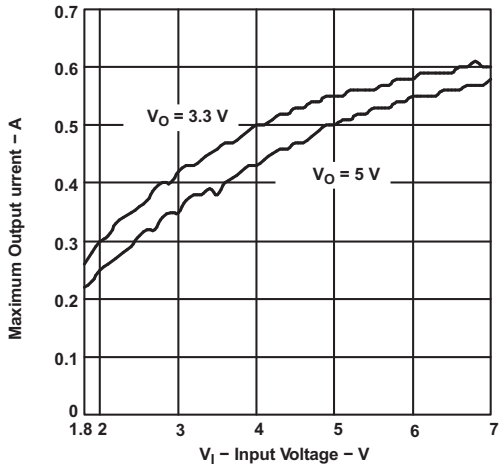


Figure 1. TPS61130 Maximum SEPIC Converter Output Current vs Input Voltage

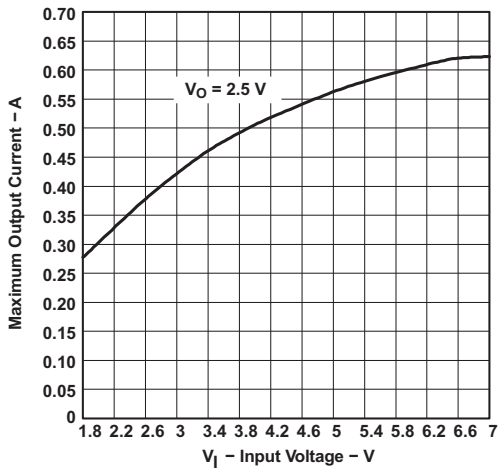


Figure 2. TPS61130 Maximum SEPIC Converter Output Current vs Input Voltage

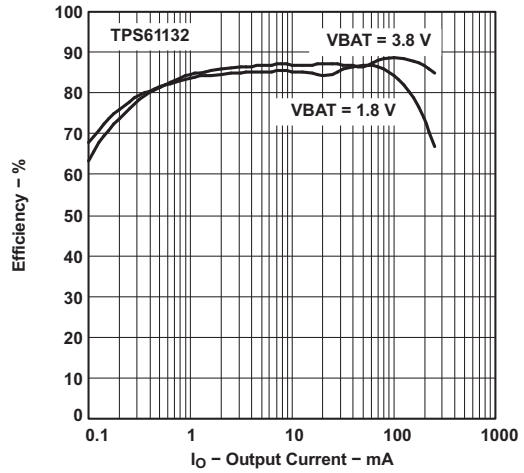


Figure 3. TPS61132 SEPIC Converter Efficiency vs Output Current

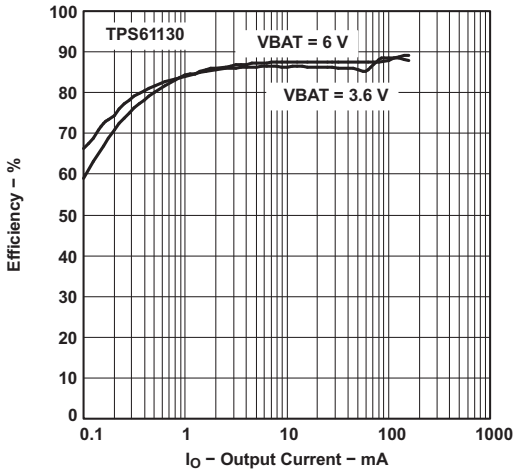


Figure 4. TPS61130 SEPIC Converter Efficiency vs Output Current

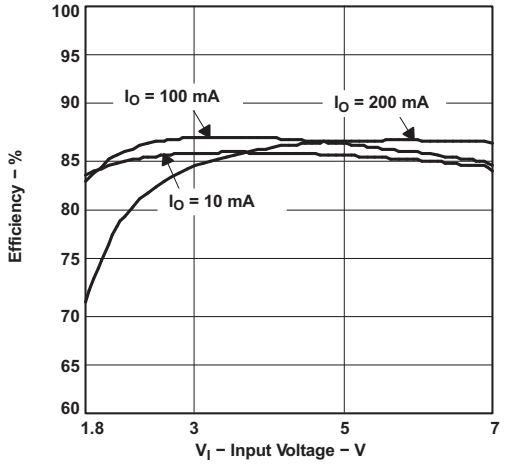


Figure 5. TPS61132 SEPIC Converter Efficiency vs Input Voltage

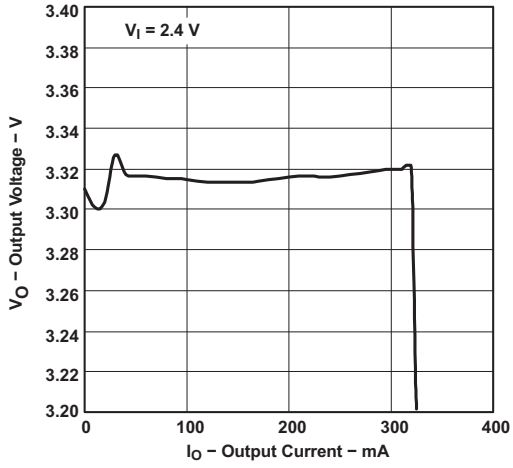


Figure 6. TPS61132 SEPIC Converter Output Voltage vs Output Current

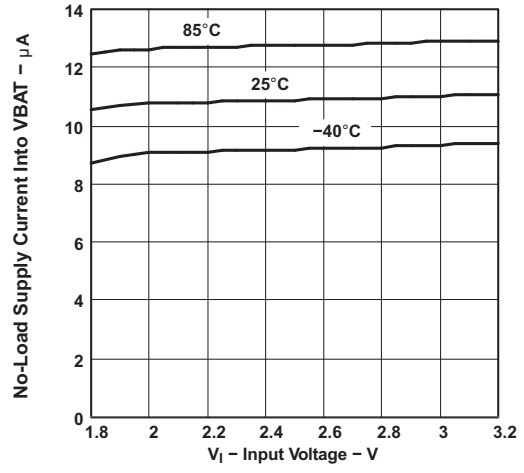


Figure 7. TPS61132 No-Load Supply Current Into VBAT vs Input Voltage

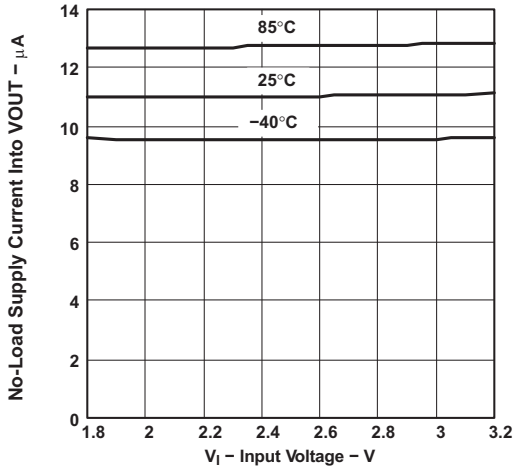


Figure 8. TPS61132 No-Load Supply Current Into VOUT vs Input Voltage

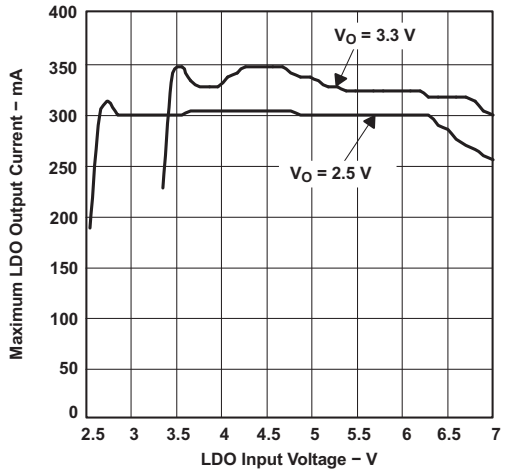


Figure 9. Maximum LDO Output Current vs LDO Input Voltage

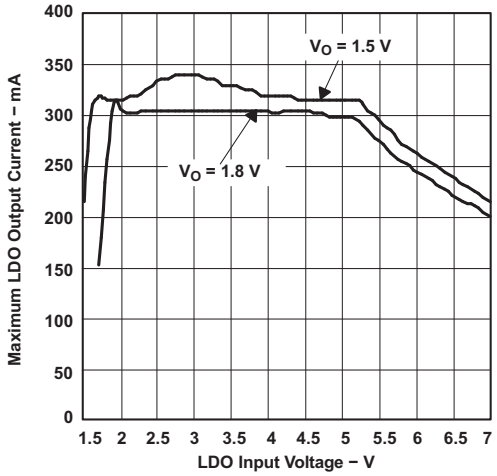


Figure 10. TPS61130 Maximum LDO Output Current vs LDO Input Voltage

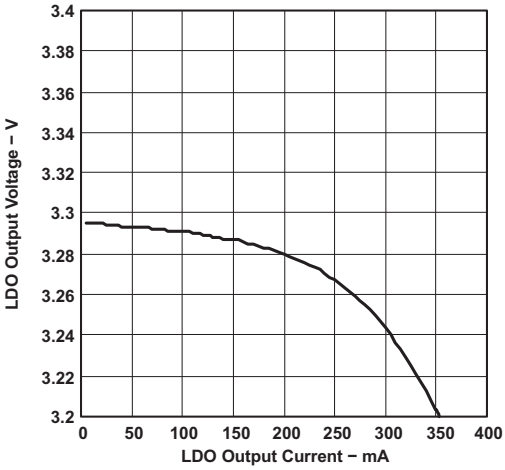


Figure 11. TPS61131 LDO Output Voltage vs LDO Output Current

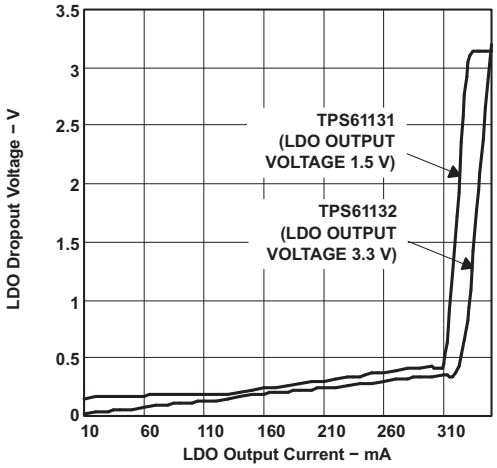


Figure 12. LDO Dropout Voltage vs LDO Output Current

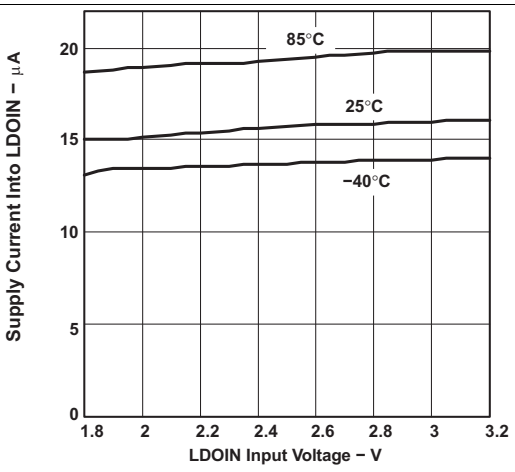


Figure 13. TPS61132 Supply Current Into LDOIN vs LDOIN Input Voltage

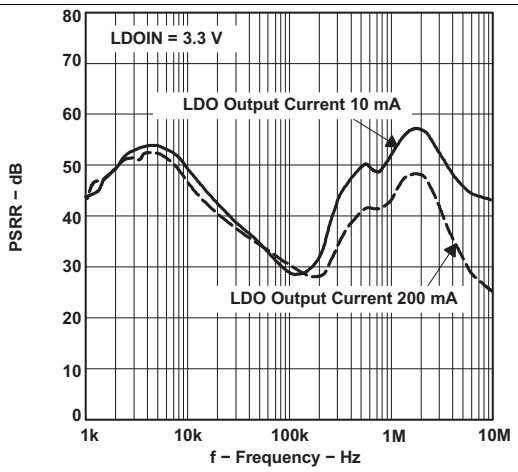
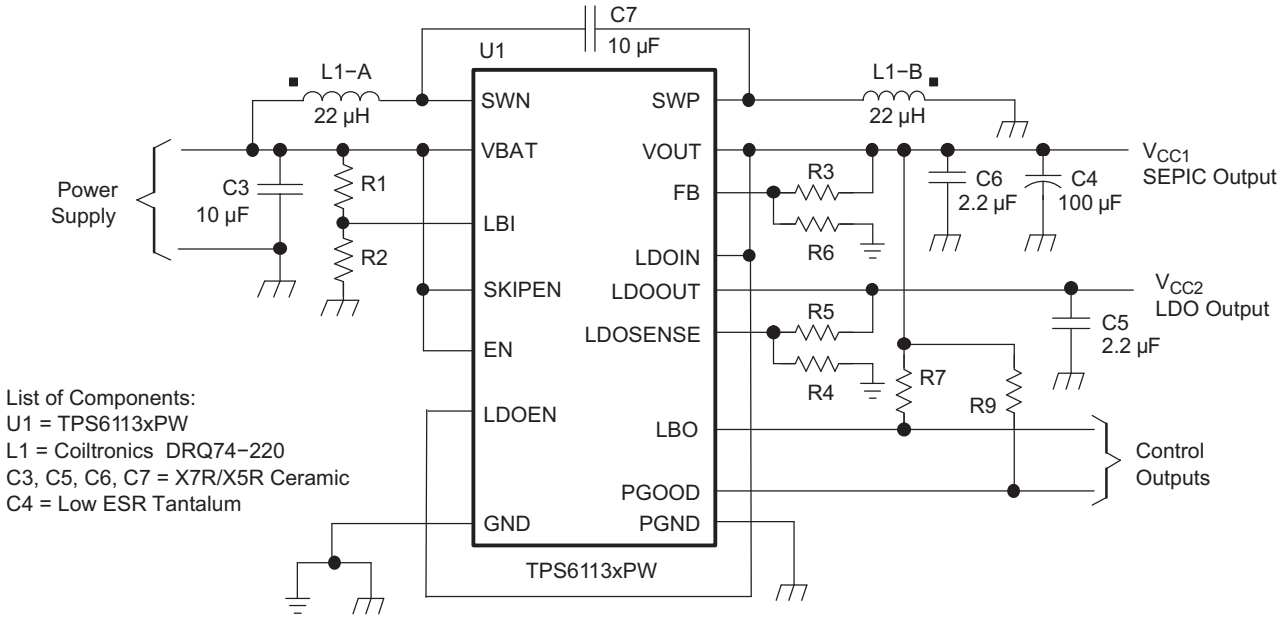


Figure 14. TPS61132 PSRR vs Frequency

8 Parameter Measurement Information

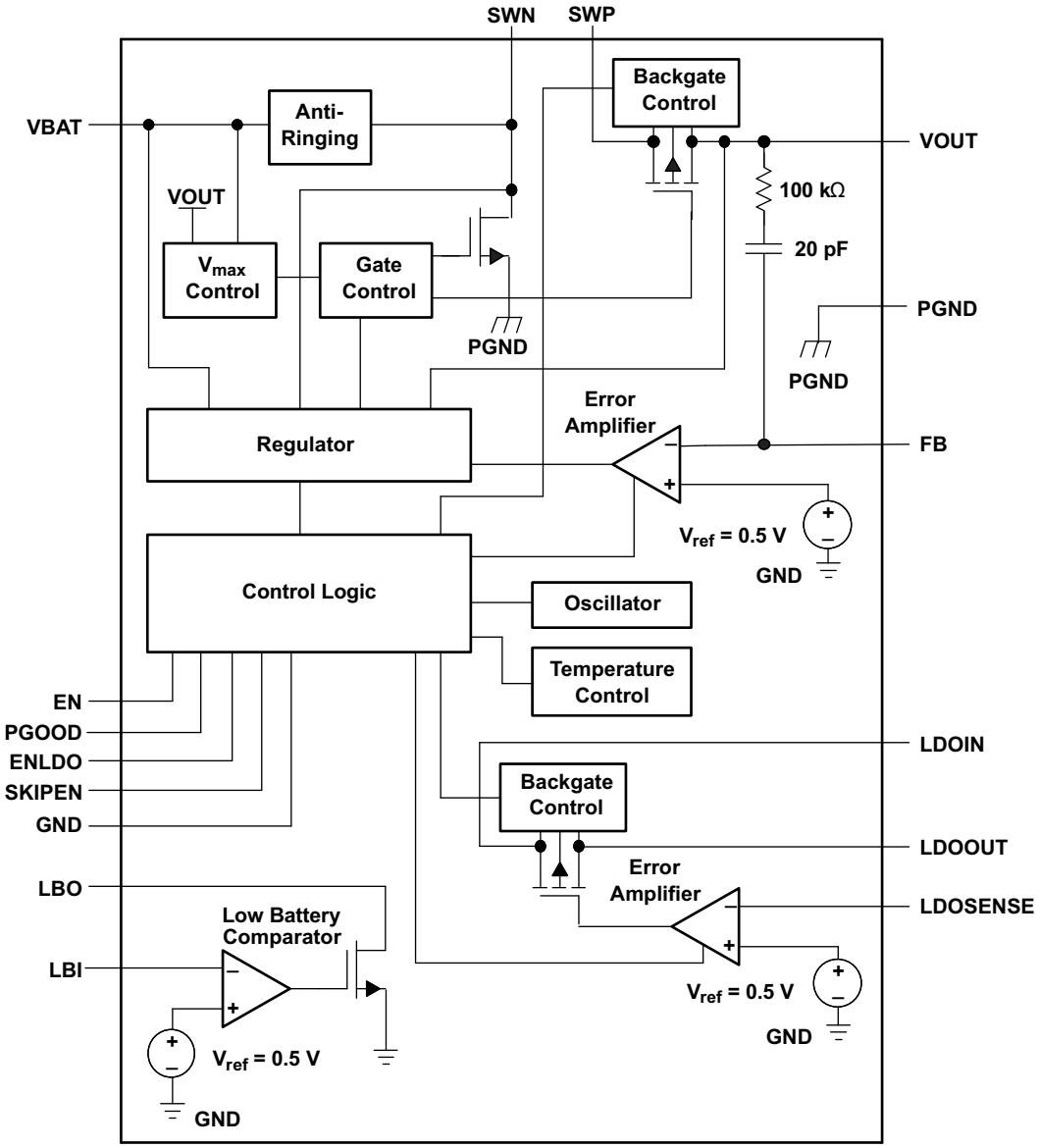


9 Detailed Description

9.1 Overview

The TPS6113x synchronous step-up converter typically operates at a 500-kHz frequency pulse width modulation (PWM) at moderate to heavy load currents. The converter enters Power Save mode at low load currents to maintain a high efficiency over a wide load. The Power Save mode can also be disabled, forcing the converter to operate at a fixed switching frequency. The device includes an additional built-in LDO which can be used to generate a second output voltage derived from the output of the TPS6113x or an external power supply. Additionally, TPS6113x integrated the low-battery detector circuit is used to supervise the battery voltage and to generate an error flag when the battery voltage drops below a user-set threshold voltage.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Controller Circuit

The controller circuit of the device is based on a fixed frequency multiple feedforward controller topology. Input voltage, output voltage, and voltage drop on the NMOS switch are monitored and forwarded to the regulator. So changes in the operating conditions of the converter directly affect the duty cycle and must not take the indirect and slow way through the control loop and the error amplifier. The control loop, determined by the error amplifier, only must handle small signal errors. The input for it is the feedback voltage on the FB pin or, at fixed output voltage versions, the voltage on the internal resistor divider. It is compared with the internal reference voltage to generate an accurate and stable output voltage.

The peak current of the NMOS switch is also sensed to limit the maximum current flowing through the switch and the inductor. The typical peak current limit is set to 1300 mA. An internal temperature sensor prevents the device from getting overheated in case of excessive power dissipation.

9.3.2 Synchronous Rectifier

The device integrates an N-channel and a P-channel MOSFET transistor to realize a synchronous rectifier. Because the commonly used discrete Schottky rectifier is replaced with a low RDS(ON) PMOS switch, the power conversion efficiency reaches 90%. To avoid ground shift due to the high currents in the NMOS switch, two separate ground pins are used. The reference for all control functions is the GND pin. The source of the NMOS switch is connected to PGND. Both grounds must be connected on the PCB at only one point close to the GND pin. Due to the nature of the SEPIC topology, there is no DC path from the battery to the output. No additional components must be added in a SEPIC or Flyback topology to make sure the battery is disconnected from the output of the converter.

Nevertheless, the backgate diode of the high-side PMOS which is forward biased in standard operation, is turned off in shutdown. This is done by a special circuit which takes the cathode of the backgate diode of the high-side PMOS and disconnects it from the source when the regulator is not enabled (EN = low).

9.3.3 Device Enable

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND. In shutdown mode, the regulator stops switching, all internal control circuitry including the low-battery comparator is switched off, and the backgate diode of the rectifying switch is turned off (as described in the Synchronous Rectifier Section). This also means that the output voltage can drop below the input voltage during shutdown. During start-up of the converter, the duty cycle and the peak current are limited to avoid high peak currents drawn from the battery.

9.3.4 Undervoltage Lockout

An undervoltage lockout function prevents device start-up if the supply voltage on VBAT is lower than approximately 1.6 V. When in operation and the battery is being discharged, the device automatically enters the shutdown mode if the voltage on VBAT drops below approximately 1.6 V. This undervoltage lockout function is implemented to prevent the malfunctioning of the converter.

9.3.5 Soft-Start

When the SEPIC section is enabled, the internal start-up cycle starts with switching at a duty cycle of 50%. After the output voltage has reached approximately 1.4 V the device continues switching with a variable duty cycle. Until the programmed output voltage is reached, the main switch current limit is set to 40% of its nominal value to avoid high peak inrush currents at the battery during start-up. Also the maximum output power during output short circuit conditions is reduced. When the programmed output voltage is reached, the regulator takes control and the switch current limit is set back to 100%.

9.3.6 Power Good

The PGOOD pin stays high impedance when the DC-DC converter delivers an output voltage within a defined voltage window. So it can be used to enable any connected circuitry such as cascaded converters (LDO) or microprocessor circuits.

Feature Description (continued)

9.3.7 Low Battery Detector Circuit—LBI/LBO

The low-battery detector circuit is typically used to supervise the battery voltage and to generate an error flag when the battery voltage drops below a user-set threshold voltage. The function is active only when the device is enabled. When the device is disabled, the LBO pin is high-impedance. The switching threshold is 500 mV at LBI. During normal operation, LBO stays at high impedance when the voltage, applied at LBI, is above the threshold. It is active low when the voltage at LBI goes below 500 mV.

The battery voltage, at which the detection circuit switches, can be programmed with a resistive divider connected to the LBI pin. The resistive divider scales down the battery voltage to a voltage level of 500 mV, which is then compared to the LBI threshold voltage. The LBI pin has a built-in hysteresis of 10 mV. See *Application and Implementation* for more details about the programming of the LBI threshold. If the low-battery detection circuit is not used, the LBI pin should be connected to GND (or to VBAT) and the LBO pin can be left unconnected. Do not let the LBI pin float.

9.3.8 Low-EMI Switch

The device integrates a circuit that removes the ringing that typically appears on the SW node when the converter enters discontinuous current mode. In this case, the current through the inductor ramps to zero and the rectifying PMOS switch is turned off to prevent a reverse current flowing from the output capacitors back to the battery. Due to the remaining energy that is stored in parasitic components of the semiconductor and the inductor, a ringing on the SW pin is induced. The integrated antiringing switch clamps this voltage to VBAT and therefore dampens ringing.

9.4 Device Functional Modes

9.4.1 Power Save Mode

The SKIPEN pin can be used to select different operation modes. To enable the power save mode, SKIPEN must be set high. Power save mode is used to improve efficiency at light loads. In power save mode, the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with several pulses, and goes again into power save mode once the output voltage exceeds the set threshold voltage. The power save mode can be disabled by setting the SKIPEN to GND.

9.4.2 LDO

The built-in LDO can be used to generate a second output voltage derived from the DC-DC converter output, from the battery, or from another power source like an AC adapter or a USB power rail. The LDO is capable of being back biased. This allows the user just to connect the outputs of DC-DC converter and LDO. So the device is able to supply the load through DC-DC converter when the energy comes from the battery and efficiency is most important and from another external power source through the LDO when lower efficiency is not critical. The LDO must be disabled if the LDOIN voltage drops below LDOOUT to block reverse current flowing. The status of the DC-DC stage (enabled or disabled) does not matter.

9.4.3 LDO Enable

The LDO can be separately enabled and disabled by using the LDOEN pin in the same way as the EN pin at the DC-DC converter stage described above. This is completely independent of the status of the EN pin. The voltage levels of the logic signals which must be applied at LDOEN are related to LDOIN.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS6113x DC-DC converters are intended for systems powered by a dual or triple cell NiCd or NiMH battery with a typical terminal voltage from 1.8 V to 5.5 V. They can also be used in systems powered by one-cell Li-Ion with a typical stack voltage from 2.5 V to 4.2 V. Additionally, two or three primary and secondary alkaline battery cells can be the power source in systems where the TPS6113x is used. The built-in LDO can be used to generate a second output voltage derived from the DC-DC converter output, from the battery, or from another power source like an AC adapter or a USB power rail. The maximum programmable output voltage at the LDO is 5.5 V.

10.2 Typical Applications

10.2.1 Typical Application Circuit for Adjustable Output Voltage Option

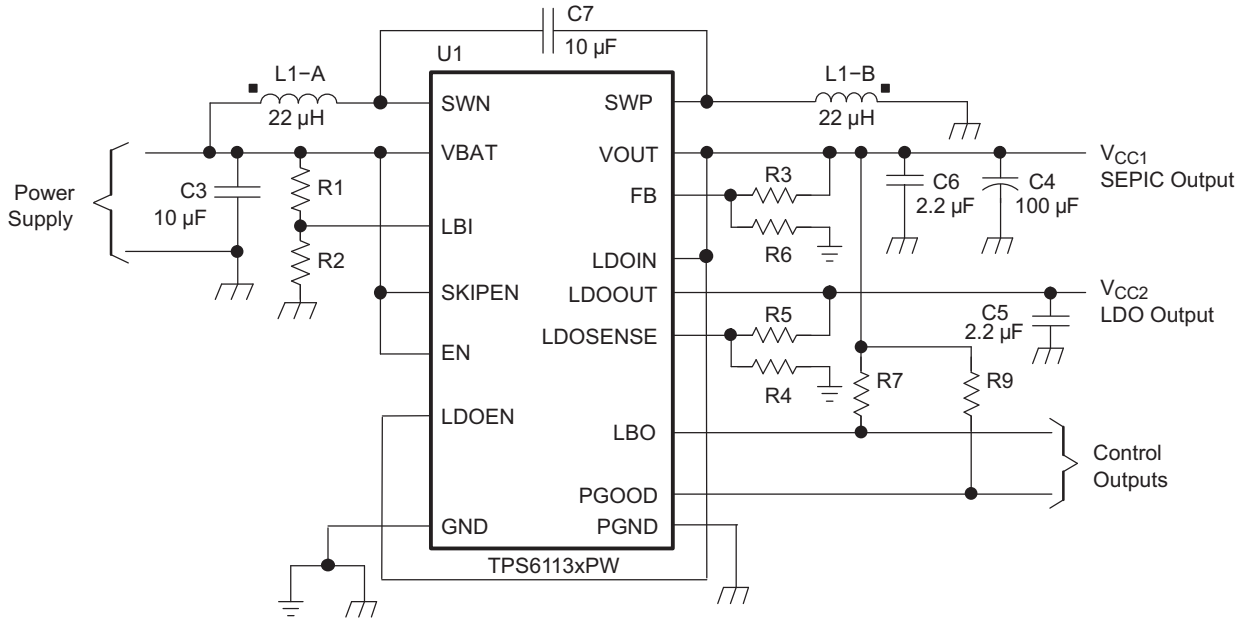


Figure 15. Typical Application Circuit for Adjustable Output Voltage Option

10.2.1.1 Design Requirements

Table 2 shows the design parameters for Figure 15.

Table 2. TPS6113x 3.3-V Output Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	1.8 V to 5.5 V
Output voltage boost	3.3 V
Output voltage LDO	1.5 V
Output voltage ripple	±3% VOUT

10.2.1.2 Detailed Design Procedure

The TPS6113x DC-DC converters are intended for systems powered by a dual up to 4 cell NiCd or NiMH battery with a typical terminal voltage from 1.8 V to 6.5 V. They can also be used in systems powered by one-cell Li-Ion with a typical stack voltage from 2.5 V to 4.2 V. Additionally, two up to four primary alkaline battery cells can be the power source in systems where the TPS6113x is used.

10.2.1.2.1 Programming the Output Voltage

10.2.1.2.1.1 DC-DC Converter

The output voltage of the TPS61130 DC-DC converter section can be adjusted with an external resistor divider. The typical value of the voltage on the FB pin is 500 mV. The maximum recommended value for the output voltage is 5.5 V. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01 µA and the voltage across R6 is typically 500 mV. Based on those two values, the recommended value for R6 should be lower than 500 kΩ, to set the divider current at 1 µA or higher. Because of internal compensation circuitry the value for this resistor should be in the range of 200 kΩ. From that, the value of resistor R3, depending on the needed output voltage (V_O), can be calculated using Equation 1:

$$R3 = R6 \times \left(\frac{V_O}{V_{FB}} - 1 \right) = 180\ k\Omega \times \left(\frac{V_O}{500\ mV} - 1 \right) \quad (1)$$

If as an example, an output voltage of 3.3 V is needed, a 1-MΩ resistor should be chosen for R3. If for any reason the value for R6 is chosen significantly lower than 200 kΩ additional capacitance in parallel to R3 is recommended. The required capacitance value can be easily calculated using Equation 2.

$$C_{parR3} = 20\ pF \times \left(\frac{200\ k\Omega}{R6} - 1 \right) \quad (2)$$

10.2.1.2.2 LDO

Programming the output voltage of the LDO follows almost the same rules as at the dc/dc converter section. The maximum recommended output voltage of the LDO is 5.5 V. Because reference and internal feedback circuitry are similar, as they are at the DC-DC converter section, R4 also should be in the 200-kΩ range. The calculation of the value of R5 can be done using the following Equation 3:

$$R5 = R4 \times \left(\frac{V_O}{V_{FB}} - 1 \right) = 180\ k\Omega \times \left(\frac{V_O}{500\ mV} - 1 \right) \quad (3)$$

If as an example, an output voltage of 1.5 V is needed, a 360-kΩ resistor should be chosen for R5.

10.2.1.2.3 Programming the LBI/LBO Threshold Voltage

The current through the resistive divider should be about 100 times greater than the current into the LBI pin. The typical current into the LBI pin is 0.01 µA, and the voltage across R2 is equal to the LBI voltage threshold that is generated on-chip, which has a value of 500 mV. The recommended value for R2 is therefore in the range of 500 kΩ. From that, the value of resistor R1, depending on the desired minimum battery voltage $V_{BAT,}$ can be calculated using Equation 4.

$$R1 = R2 \times \left(\frac{V_{BAT}}{V_{LBI-threshold}} - 1 \right) = 390\ k\Omega \times \left(\frac{V_{BAT}}{500\ mV} - 1 \right) \quad (4)$$

The output of the low battery supervisor is a simple open-drain output that goes active low if the dedicated battery voltage drops below the programmed threshold voltage on LBI. The output requires a pullup resistor with a recommended value of 1 MΩ. The maximum voltage which is used to pull up the LBO outputs should not exceed the output voltage of the DC-DC converter. If not used, the LBO pin can be left floating or tied to GND.

10.2.1.2.4 Inductor Selection

A SEPIC converter normally requires three main passive components for storing energy during the conversion. Two inductors, a flying capacitor, and a storage capacitor at the output are required. To select the two inductors, TI recommends keeping the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. For example, the typical current limit threshold of the TPS6113x's switch is 1300 mA at an output voltage of 3.3 V. The highest peak current through the switch is the sum of the two inductor currents and depends on the output load, the input (V_{BAT}), and the output voltage (V_{OUT}). Estimation of the maximum average inductor current of each inductor can be done using Equation 5:

$$I_{L1-A} = I_{L1-B} = I_{OUT} \times \frac{V_{OUT}}{V_{BAT} \times 0.8} \quad (5)$$

For example, for an output current of 300 mA at 3.3 V, at least 680 mA of average current flows through each of the inductors at a minimum input voltage of 1.8 V.

The second parameter for choosing the inductor is the desired current ripple in the inductor. Normally, it is advisable to work with a ripple of around ±20% of the average inductor current. A smaller ripple reduces the magnetic hysteresis losses in the inductor, as well as output voltage ripple and EMI. But in the same way, regulation time at load changes rises. In addition, a larger inductor increases the total system costs. With those parameters, it is possible to calculate the value for the inductor by using Equation 6:

$$L1-A = L1-B = \frac{V_{BAT} \times V_{OUT}}{\Delta I_L \times f \times (V_{OUT} + V_{BAT})} \quad (6)$$

Parameter ***f*** is the switching frequency andΔ I_L is the ripple current in the inductor, that is, 40% Δ I_L. In this example, the desired inductance is in the range of 20 µH. With this calculated value and the calculated currents, it is possible to choose a suitable inductor. In typical applications, TI recommends an inductance of 22 µH. The device has been optimized to operate with inductance values from 10 µH to 47 µH. Nevertheless operation with higher inductance values may be possible in some applications. TI recommends a detailed stability analysis. Take care so that load transients and losses in the circuit can lead to higher currents as estimated in Equation 6. Also, the losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

The following inductor series from different suppliers have been used with the TPS6113X converters:

Table 3. List of Inductors

VENDOR	RECOMMENDED INDUCTOR SERIES	COUPLED INDUCTOR SERIES
Coilcraft	LPS4012	LPD4012
	LPS3015	—
Cooper Electronics Technologies	DR73	DRQ73
	DR74	DRQ74
EPCOS	B82462G	—
Sumida	CDRH5D18	—
Wurth Electronik	7447789___	744878220
	7447779___	744877220

10.2.1.2.5 Capacitor Selection

10.2.1.2.5.1 Input Capacitor

TI recommends at least a 10-µF input capacitor to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor or a tantalum capacitor with a 100-nF ceramic capacitor in parallel, placed close to the IC, is recommended.

10.2.1.2.5.2 Flying Capacitor DC-DC Converter

In the normal operating mode, the *flying* capacitor (C7) must be large enough so that the voltage across the capacitor is small. This means the resonance frequency formed by the *flying* capacitor and the inductors must be at least ten times lower than the switching frequency (see Equation 7).

$$C_{min} = \frac{100}{4\pi^2 f^2 L} \quad (7)$$

Where L is the inductance of L1-A or L1-B.

To optimize efficiency, TI recommends capacitors with very low ESR such as ceramic capacitors. The voltage rating of the *flying* capacitor must be higher than the input voltage V_{BAT}.

10.2.1.2.5.3 Output Capacitor DC-DC Converter

The major parameter necessary to define the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero, by using Equation 8:

$$C_{min} = \frac{I_{OUT} \times V_{OUT}}{f \times \Delta V \times (V_{OUT} + V_{BAT})} \quad (8)$$

Parameter *f* is the switching frequency and ΔV is the maximum allowed ripple.

With a chosen ripple voltage of 15 mV, a minimum capacitance of 26 µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 9:

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR} \quad (9)$$

An additional ripple of 24 mV is the result of using a tantalum capacitor with a low ESR of 80 mΩ. The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. In this example, the total ripple is 39 mV. Additional ripple is caused by load transients. This means that the output capacitance must be larger than calculated above to meet the total ripple requirements. The output capacitor must completely supply the load during the charging phase of the inductor. A reasonable value of the output capacitance depends on the speed of the load transients and the load current during the load change. With the calculated minimum value of 26 µF and load transient considerations, the recommended output capacitance value is in a 100-µF range. For economical reasons this usually is a tantalum capacitor. Because of this the control loop has been optimized for using output capacitors with an ESR of greater than 30 mΩ. The minimum value for the output capacitor is 22 µF.

10.2.1.2.5.4 Small Signal Stability

When using output capacitors with lower ESR, like ceramics, TI recommends using the adjustable voltage version. The missing ESR can be easily compensated there in the feedback divider. Typically a capacitor in the range of 10 pF in parallel with R3 helps to obtain small signal stability, with the lowest ESR output capacitors. For more detailed analysis the small signal transfer function of the error amplifier and regulator, which is given in Equation 10, can be used.

$$A_{REG} = \frac{d}{V_{FB}} = \frac{10 \times (R3 + R6)}{R6 \times (1 + i \times \omega \times 1.6\ \mu s)} \quad (10)$$

10.2.1.2.5.5 Output Capacitor LDO

To ensure stable output regulation, it is required to use an output capacitor at the LDO output. TI recommends using ceramic capacitors in the range from 1 µF up to 4.7 µF. At 4.7 µF and above, TI recommends using standard ESR tantalum. There is no maximum capacitance value.

10.2.1.3 Application Curves

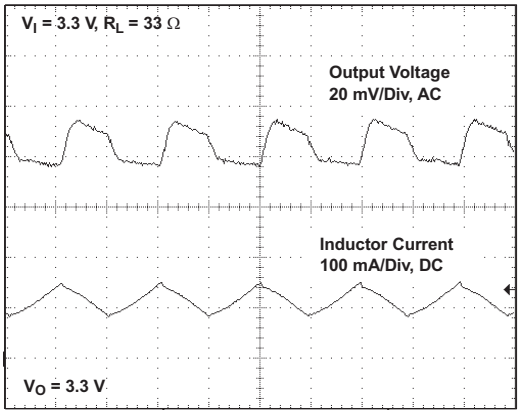


Figure 16. TPS61132 SEPIC Converter Output Voltage in Continuous Mode

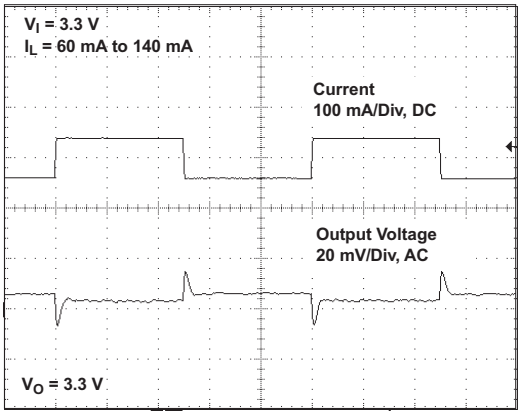


Figure 17. TPS61132 SEPIC Converter Load Transient Response

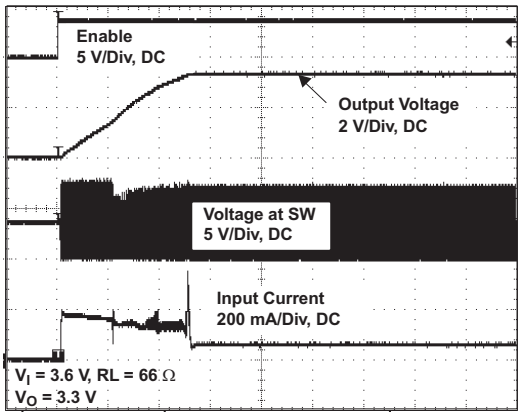


Figure 18. TPS61132 SEPIC Converter Start-Up After Enable

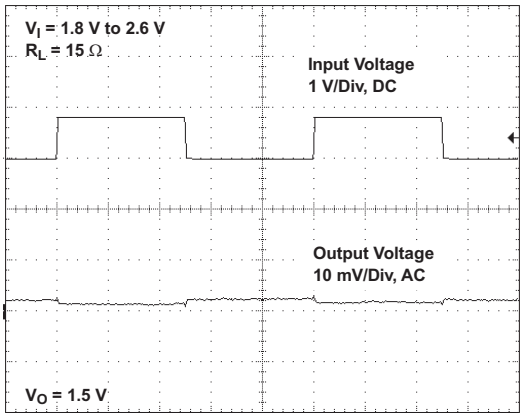


Figure 19. TPS61132 LDO Line Transient Response

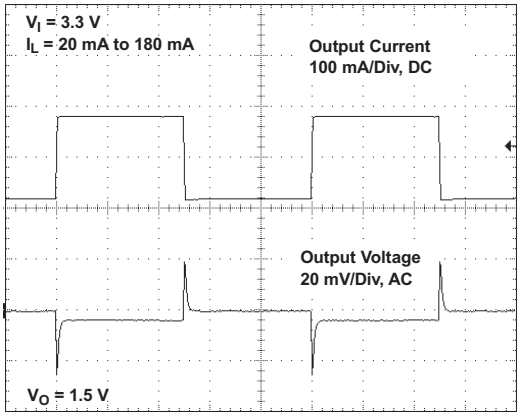


Figure 20. TPS61132 LDO Load Transient Response

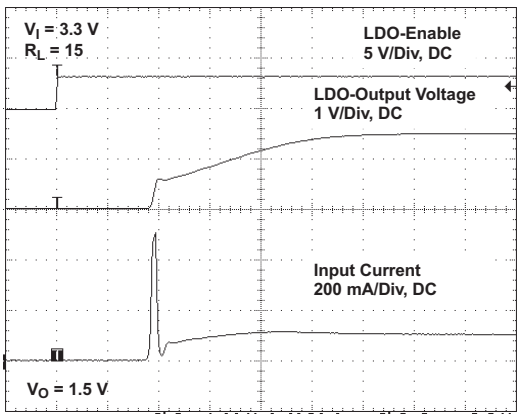


Figure 21. TPS61132 LDO Start-Up After Enable

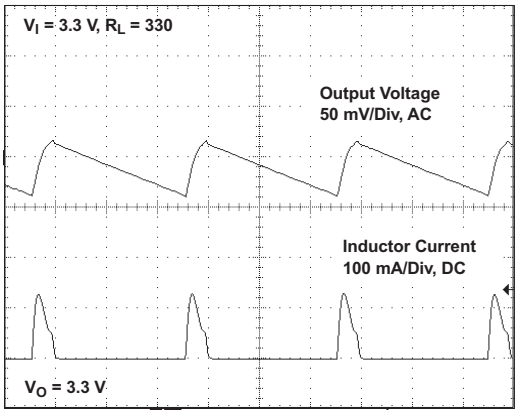


Figure 22. TPS61132 SEPIC Converter Output Voltage in Power Save Mode

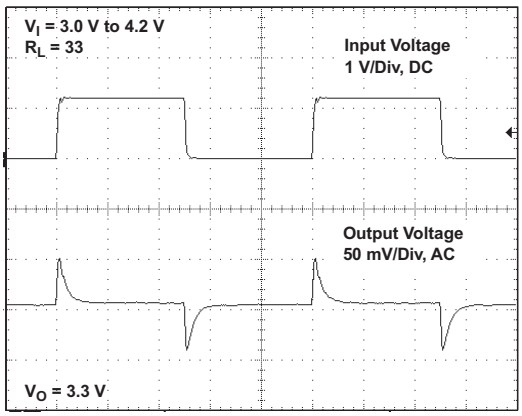


Figure 23. TPS61132 SEPIC Converter Line Transient Response

10.2.2 Solution for Maximum Output Power

The TPS6113x boost converter with LDO features two independent output voltages. An efficient synchronous boost converter provides a 3.3-V VOUT1 with output currents more than 250 mA. A >120-mA LDO regulator generates a 1.5-V VOUT2. The two outputs can be used independently from each other.

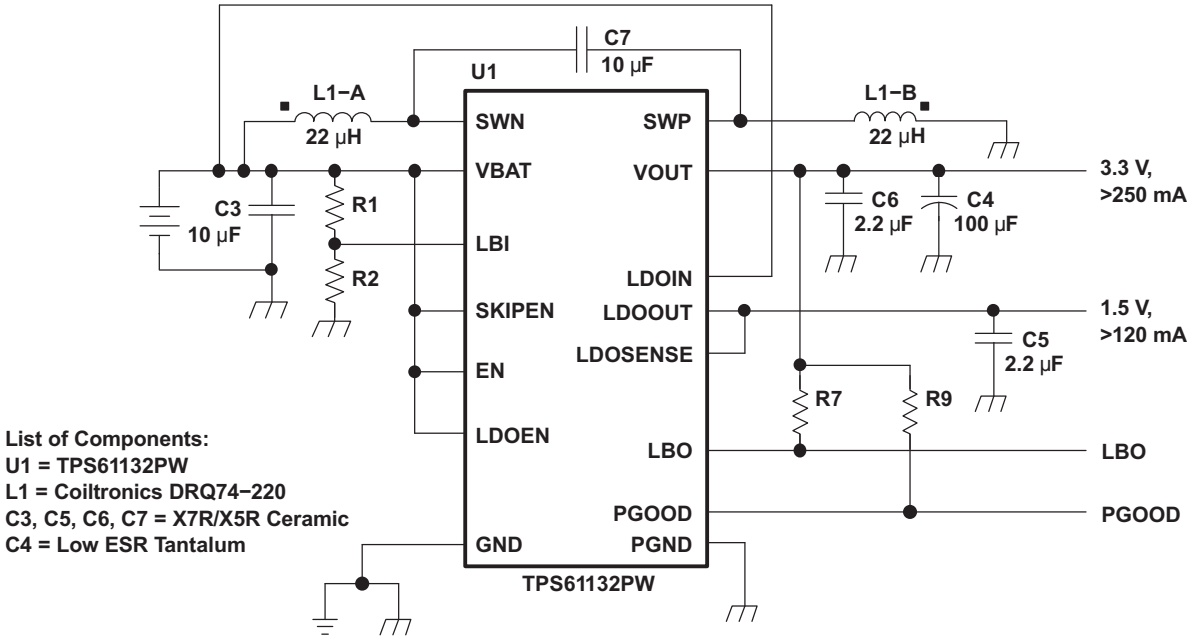


Figure 24. Solution for Maximum Output Power

10.2.3 Low Profile Solution, Maximum Height 1.8 mm

The TPS6113x boost converter with LDO features two independent output voltages. An efficient synchronous boost converter provides a 3.3-V VOUT1 and followed by a post-LDO generates a 1.5-V VOUT2.

TPS6113x could support low profile inductor with a height of 1.8 mm.

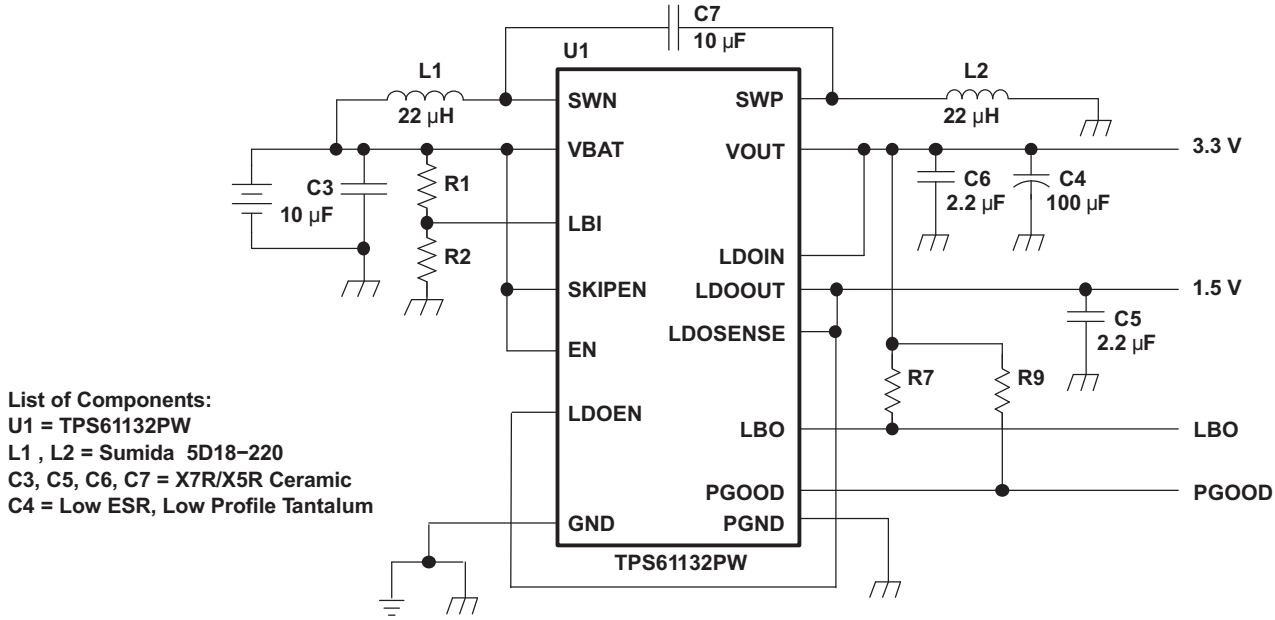


Figure 25. Low Profile Solution, Maximum Height 1.8 mm

10.2.4 Single Output Using LDO as Filter

The TPS6113x could provide a linear output of 3.3 V with the input from the output of the boost converter to enable lower noise output.

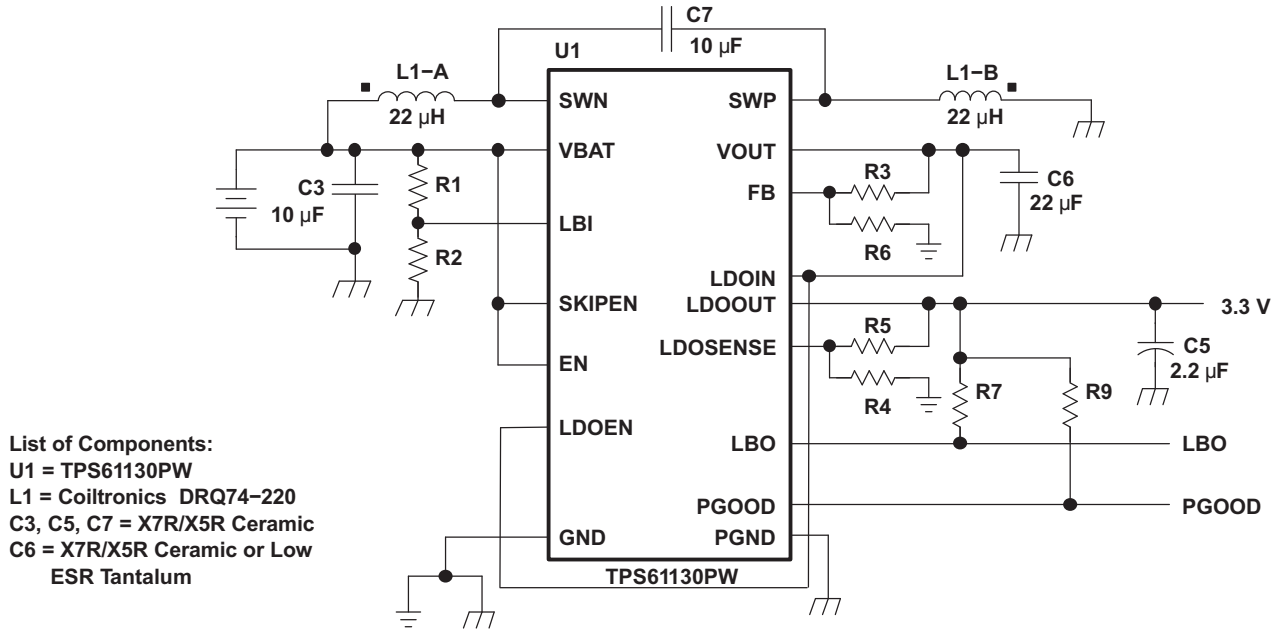


Figure 26. Single Output Using LDO as Filter

10.2.5 Dual Input Power Supply Solution

The TPS6113x boost converter can support dual input power supply, one input for boost converter to generate a 3.3 Vout, while the other input for LDO to generate the second 3.3 Vout independently.

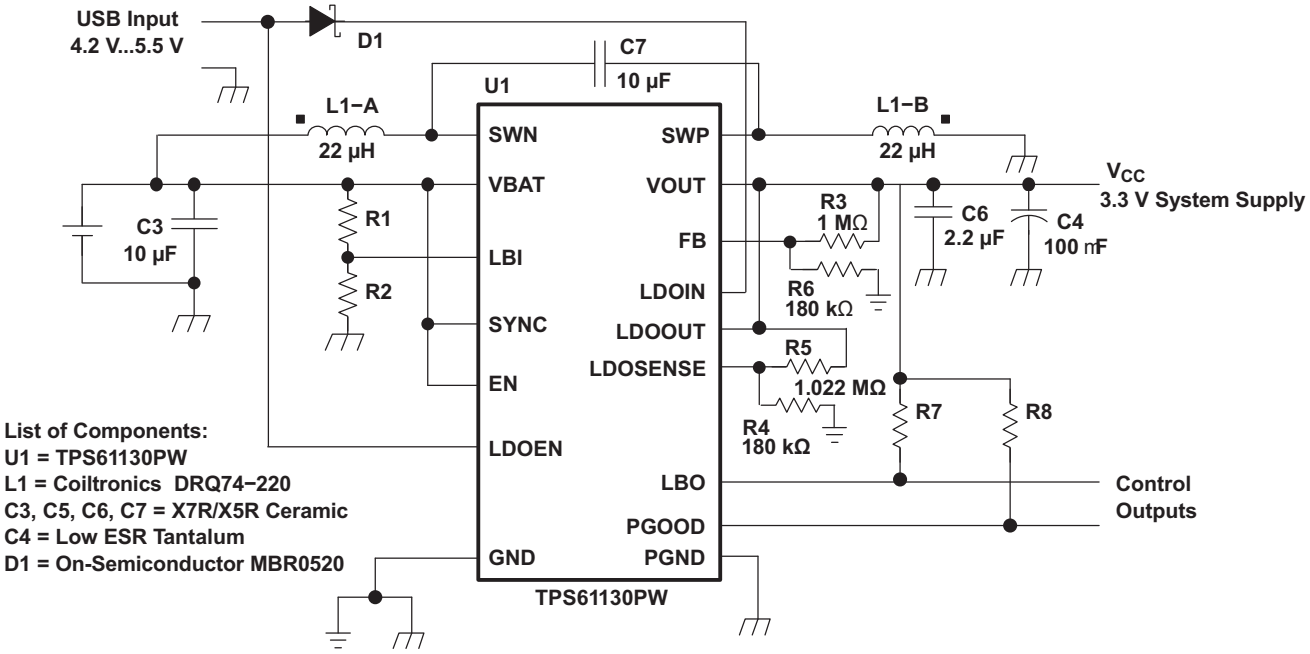


Figure 27. Dual Input Power Supply Solution

11 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 1.8 V to 5.5 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

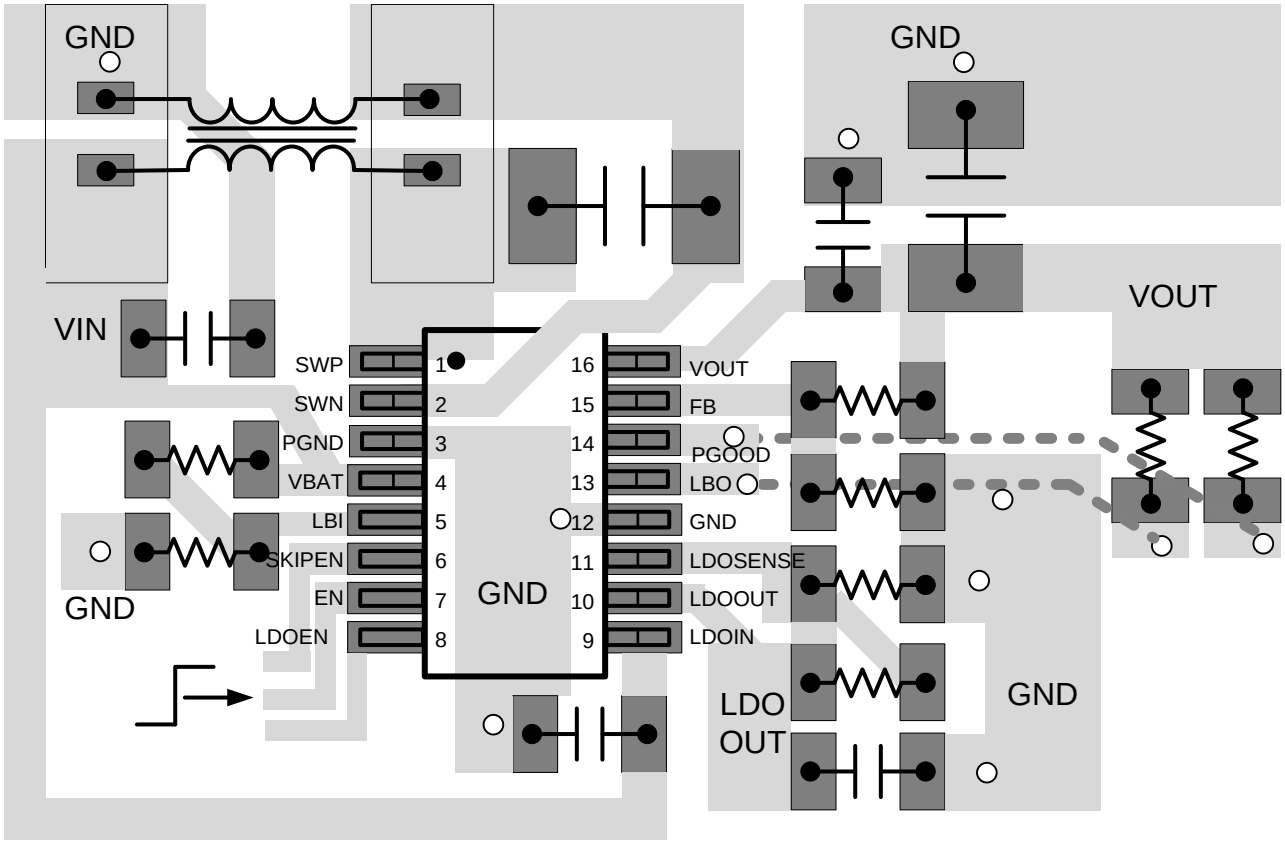
12 Layout

12.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor must be placed as close as possible to the device. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the device.

The feedback divider must be placed as close as possible to the control ground pin of the device. To lay out the control ground, TI recommends using short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

12.2 Layout Example



12.3 Thermal Consideration

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Follow these three basic approaches for enhancing thermal performance.

- Improving the power dissipation capability of the PCB design.
- Improving the thermal coupling of the component to the PCB.
- Introducing airflow in the system.

The maximum recommended junction temperature (T_J) of the TPS6113x devices is 150°C. The thermal resistance of the 16-pin TSSOP package (PW) is $R_{\Theta JA}$ = 100.5 °C/W. The 16-pin VQFN package (RSA) with exposed thermal pad has a thermal resistance of $R_{\Theta JA}$ = 33.9°C/W, if the thermal pad is soldered and the board layout is optimized. Specified regulator operation is assured to a maximum ambient temperature T_A of 85°C. Therefore, the maximum power dissipation is about 647 mW for the TSSOP (PW) package and 1917 mW for the VQFN (RSA) package. More power can be dissipated if the maximum ambient temperature of the application is lower (see Equation 11).

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} \tag{11}$$

If designing for a lower junction temperature of 125°C, which TI recommends, maximum heat dissipation is lower. Using the above Equation 11 results in 1917-mW power dissipation for the RSA package and 647 mW for the PW package.

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Related Links

The following table lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS61130	Click here	Click here	Click here	Click here	Click here
TPS61131	Click here	Click here	Click here	Click here	Click here
TPS61132	Click here	Click here	Click here	Click here	Click here

13.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61130PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS61130	Samples
TPS61130PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS61130	Samples
TPS61130RSAR	ACTIVE	QFN	RSA	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS6 1130	Samples
TPS61131PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS61131	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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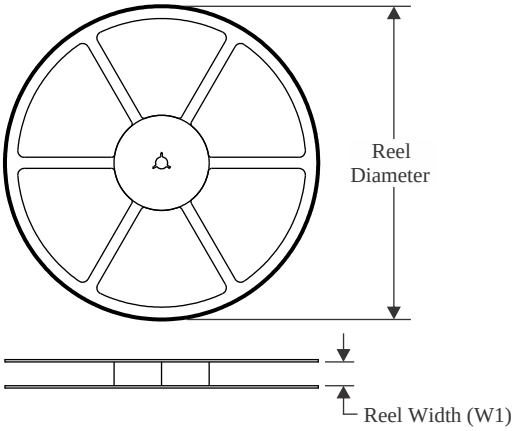
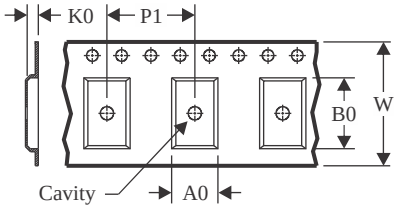
TAPE AND REEL INFORMATION

REEL DIMENSIONS

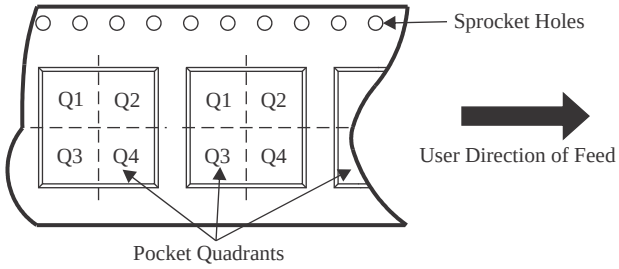


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

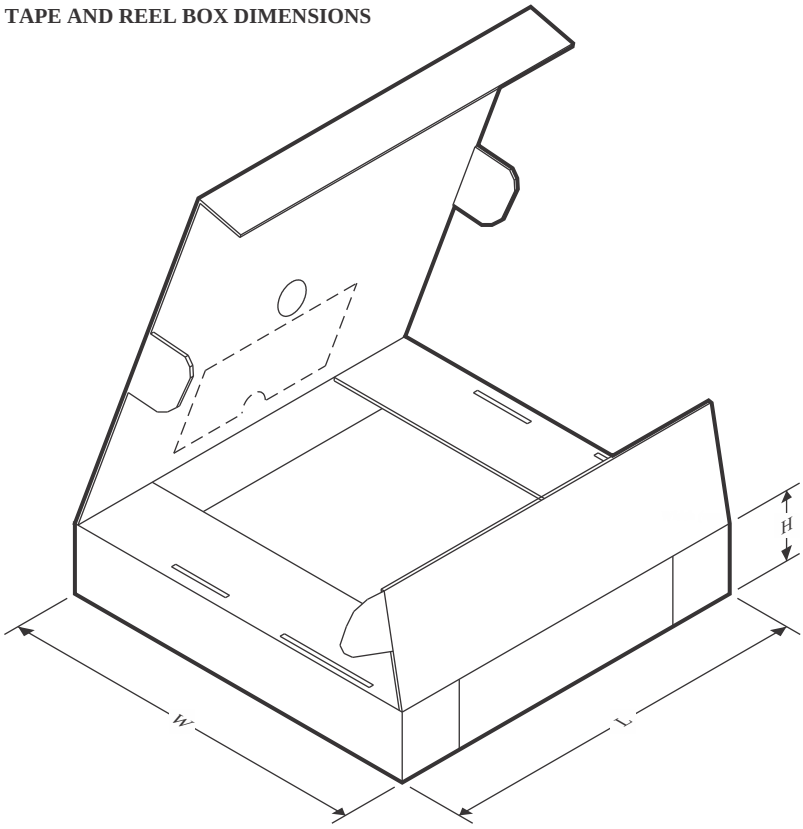
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61130PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

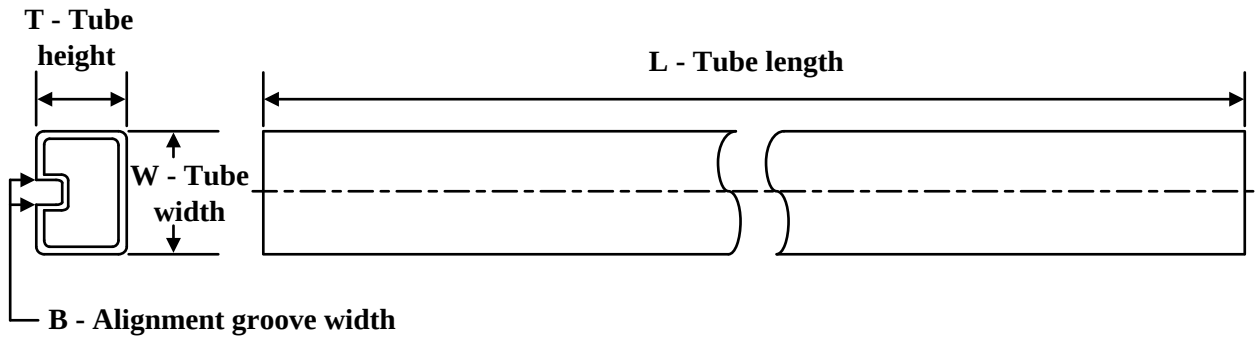
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61130PWR	TSSOP	PW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

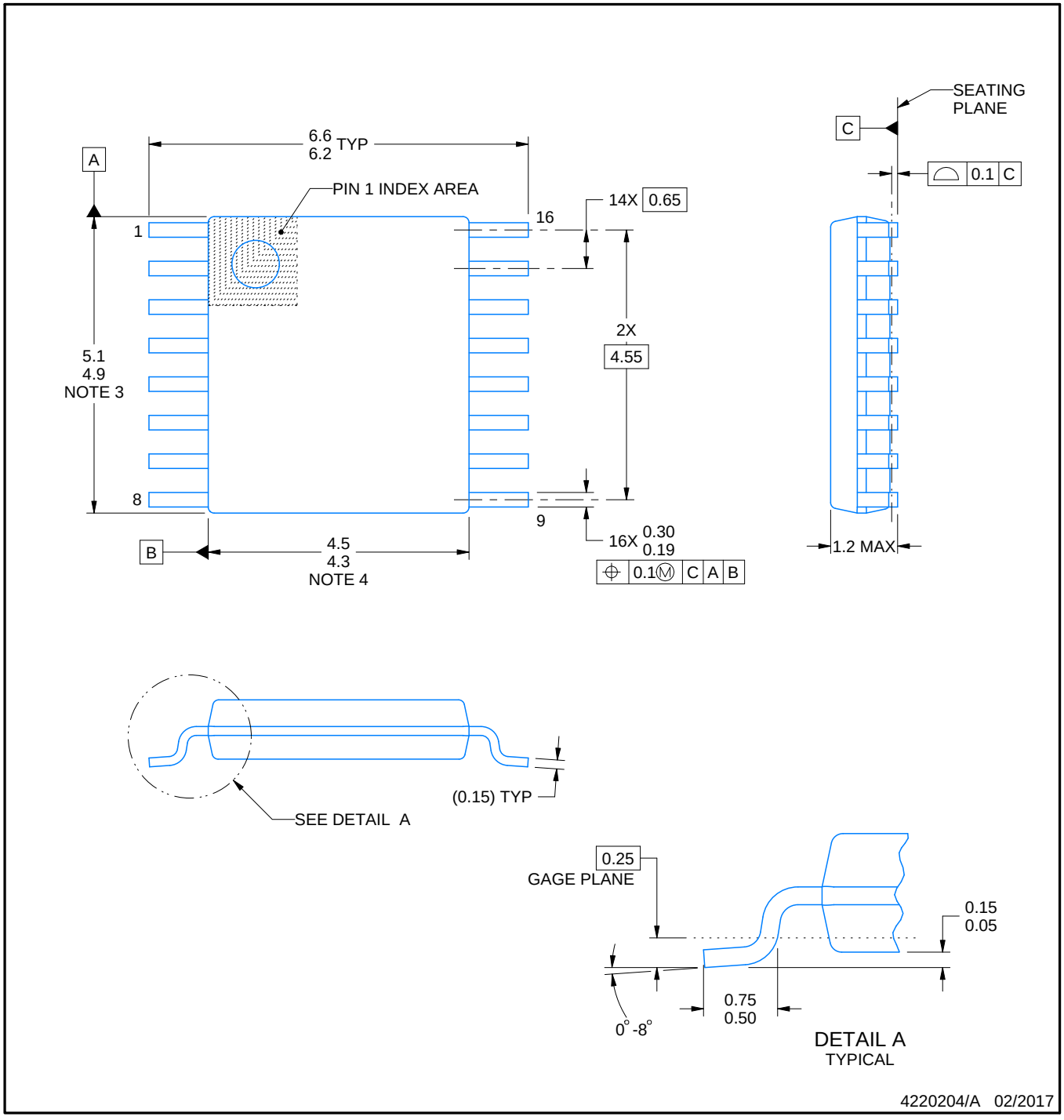
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS61130PW	PW	TSSOP	16	90	530	10.2	3600	3.5
TPS61131PW	PW	TSSOP	16	90	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0016A

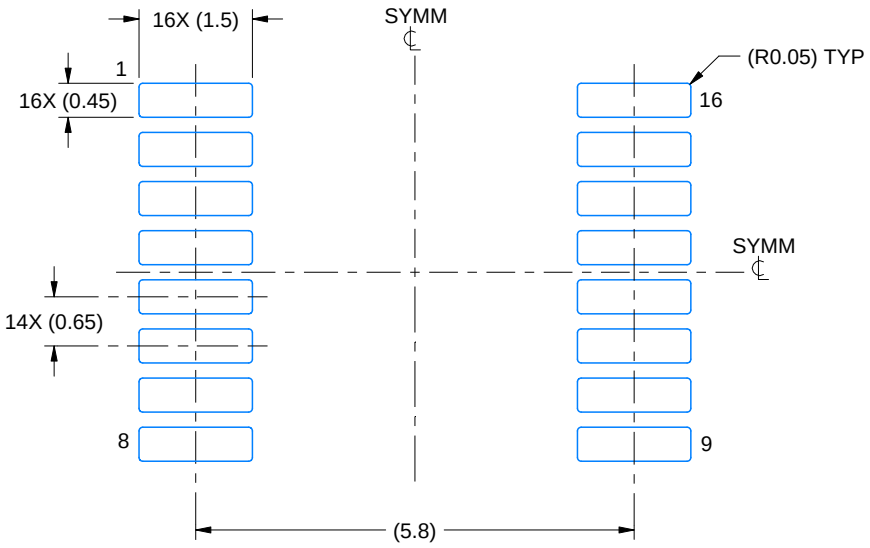
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

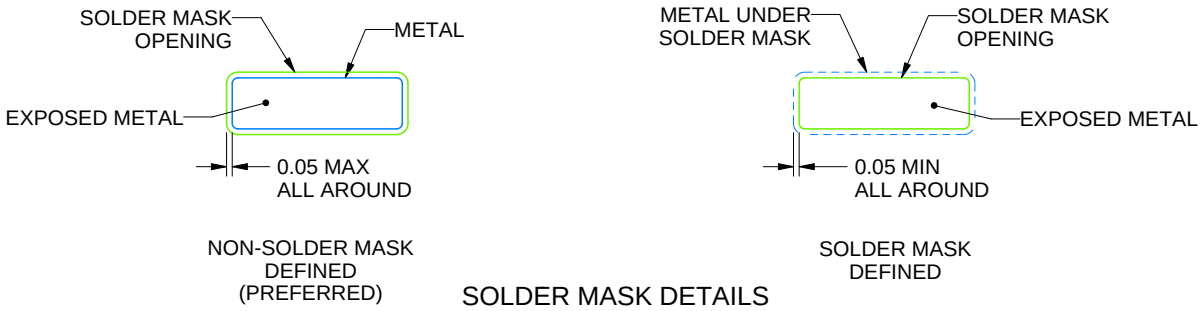


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

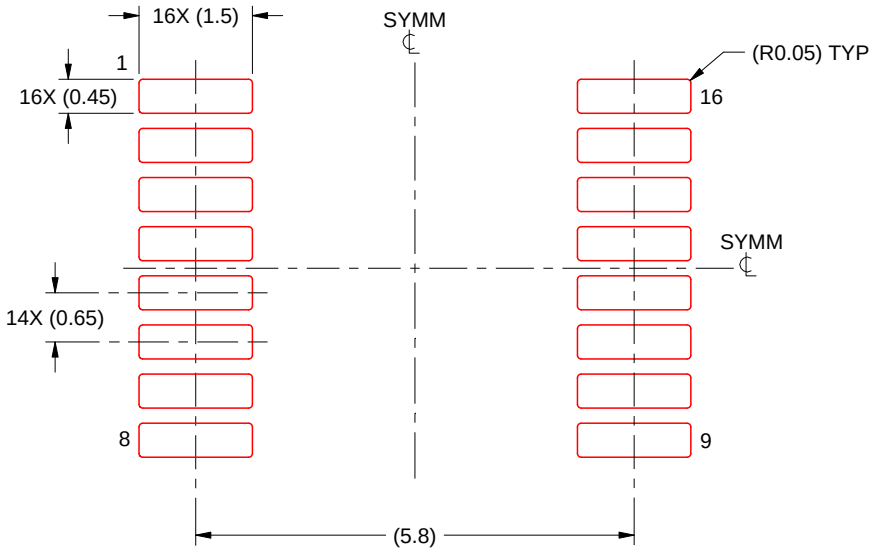


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



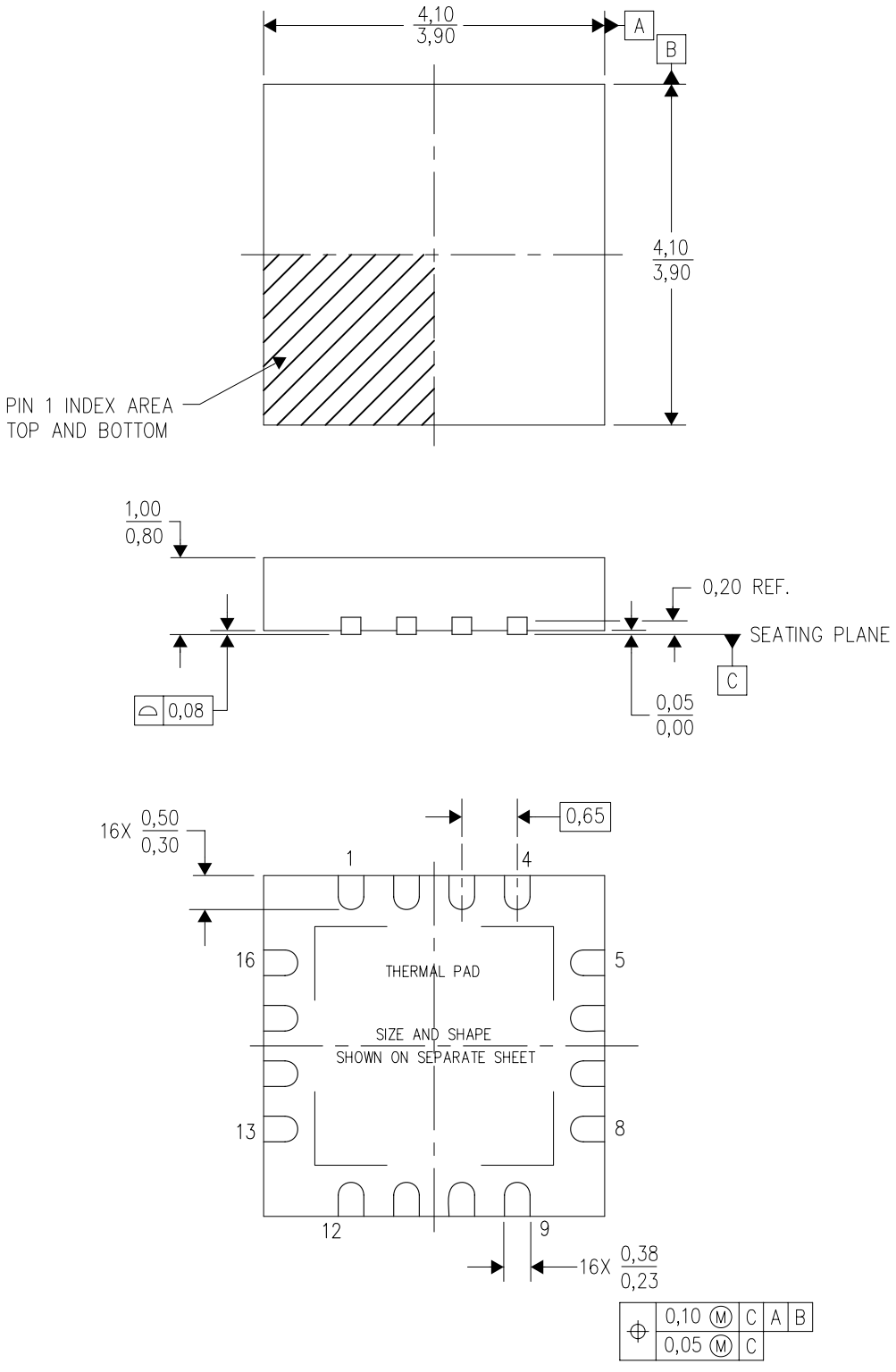
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

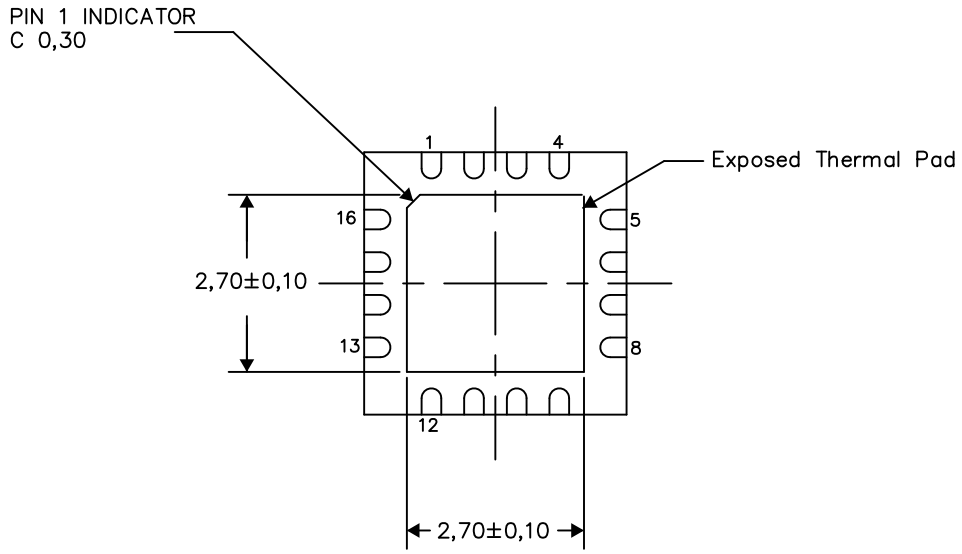
RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



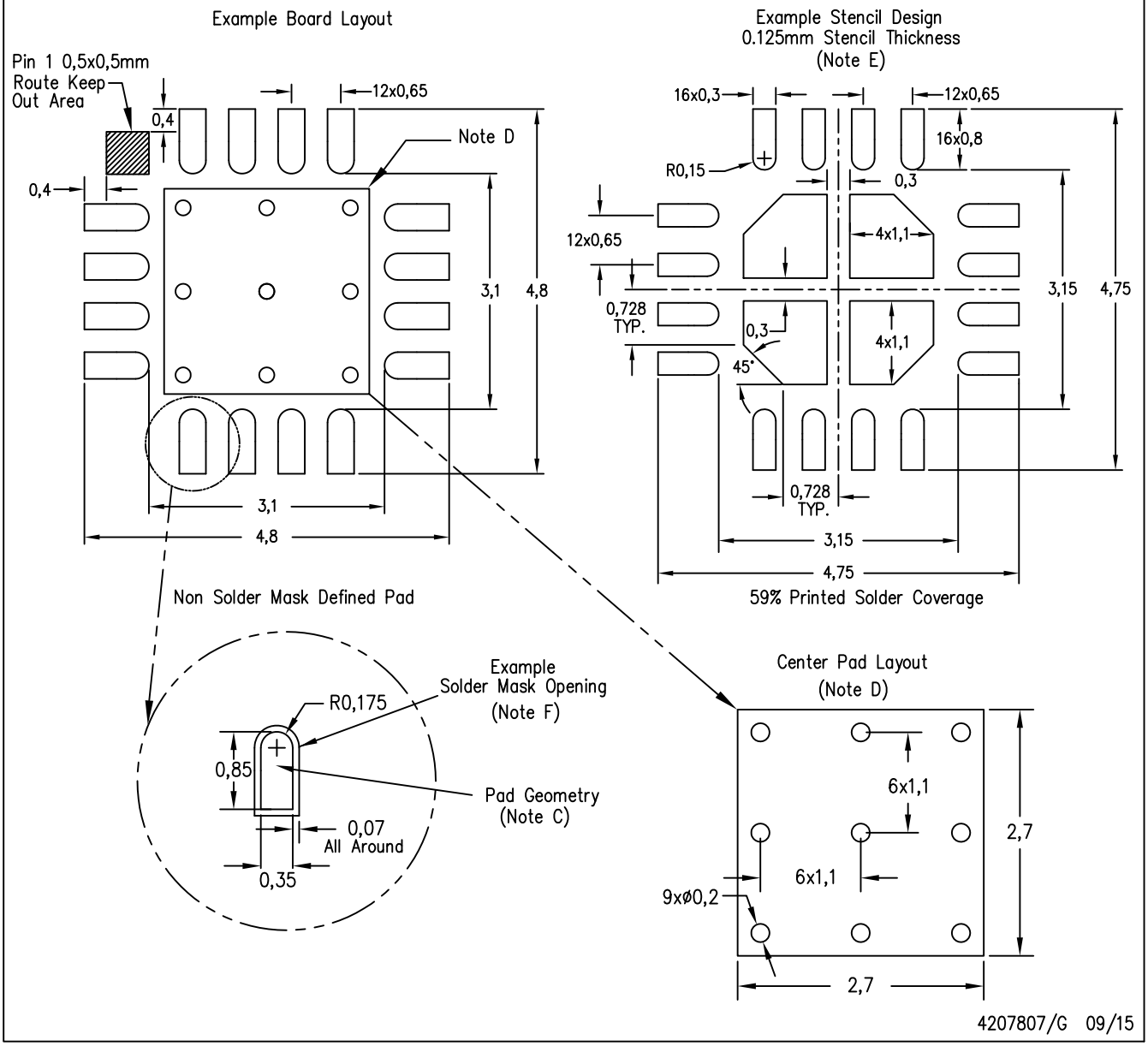
Bottom View

Exposed Thermal Pad Dimensions

4206364–2/0 09/15

NOTES:
A. All linear dimensions are in millimeters

RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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