NUS5530MN

Integrated Power MOSFET with PNP Low $V_{CE(sat)}$ Switching Transistor

This integrated device represents a new level of safety and board−space reduction by combining the 20 V P−Channel FET with a PNP Silicon Low $V_{CE(sat)}$ switching transistor. This newly integrated product provides higher efficiency and accuracy for battery powered portable electronics.

Features

- Low $R_{DS(on)}$ (MOSFET) and Low $V_{CE(sat)}$ (Transistor)
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive (MOSFET)
- Performance DFN Package
- This is a Pb−Free Device

Applications

- Power Management in Portable and Battery−Powered Products; i.e., Cellular and Cordless Telephones and PCMCIA Cards

MAXIMUM RATINGS FOR P−CHANNEL FET

(T_A = 25°C unless otherwise noted)

Rating	Symbol	5 sec	Steady State	Unit
Drain−Source Voltage	V_{DS}	−20		V
Gate−Source Voltage	V_{GS}	±12		V
Continuous Drain Current (T_J = 150°C) (Note 1) T_A = 25°C T_A = 85°C	I_D	 −5.3 −3.8	 −3.9 −2.8	A
Pulsed Drain Current	I_{DM}	±20		A
Continuous Source Current (Note 1)	I_S	−5.3	−3.9	A
Maximum Power Dissipation (Note 1) T_A = 25°C T_A = 85°C	P_D	 2.5 1.3	 1.3 0.7	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).

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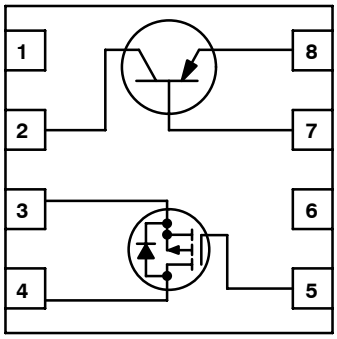
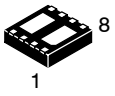


(Top View)



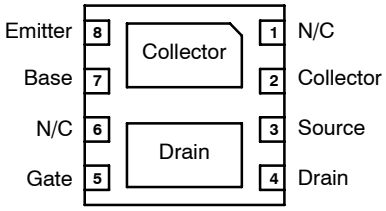
DFN8
CASE 506AL

MARKING DIAGRAM

A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



(Bottom View)

ORDERING INFORMATION

Device	Package	Shipping†
NUS5530MNR2G	DFN8 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MAXIMUM RATINGS FOR PNP TRANSISTORS (T_A = 25°C)

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	−35	Vdc
Collector-Base Voltage	V_{CBO}	−55	Vdc
Emitter-Base Voltage	V_{EBO}	−5.0	Vdc
Collector Current − Continuous	I_C	−2.0	Adc
Collector Current − Peak	I_{CM}	−7.0	A
Electrostatic Discharge	ESD	HBM Class 3 MM Class C	

THERMAL CHARACTERISTICS FOR P−CHANNEL FET

Characteristic	Symbol	Typ	Max	Unit
Maximum Junction−to−Ambient (Note 4) $t \leq 5$ sec Steady State	$R_{\theta JA}$	 40 80	 50 95	°C/W
Maximum Junction−to−Foot (Drain) Steady State	$R_{\theta JF}$	15	20	°C/W

THERMAL CHARACTERISTICS FOR PNP TRANSISTORS

Characteristic	Symbol	Max	Unit
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D (Note 1)	635 5.1	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$ (Note 1)	200	°C/W
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D (Note 2)	1.35 11	W mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$ (Note 2)	90	°C/W
Thermal Resistance, Junction−to−Lead #1	$R_{\theta JL}$	15	°C/W
Total Device Dissipation (Single Pulse < 10 sec)	$P_{Dsingle}$ (Notes 2 & 3)	2.75	W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

1. FR−4 @ 100 mm^2, 1 oz copper traces.
2. FR−4 @ 500 mm^2, 1 oz copper traces.
3. Thermal response.

ELECTRICAL CHARACTERISTICS FOR P−CHANNEL FET (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = −250 μA	−0.6		−1.2	V
Gate−Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±12 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −16 V, V_{GS} = 0 V			−1.0	μA
		V_{DS} = −16 V, V_{GS} = 0 V, T_J = 85°C			−5.0	
On−State Drain Current (Note 5)	$I_{D(on)}$	$V_{DS} \leq$ −5.0 V, V_{GS} = −4.5 V	−20			A
Drain−Source On−State Resistance (Note 5)	$r_{DS(on)}$	V_{GS} = −3.6 V, I_D = −1.0 A	−	0.050	0.06	Ω
		V_{GS} = −2.5 V, I_D = −1.0 A		0.070	0.083	
Forward Transconductance (Note 5)	g_{fs}	V_{DS} = −10 V, I_D = −3.9 A		12		Mhos
Diode Forward Voltage (Note 5)	V_{SD}	I_S = −2.1 A, V_{GS} = 0 V		−0.8	−1.2	V
Dynamic (Note 6)						
Total Gate Charge	Q_G	V_{DS} = −10 V, V_{GS} = −4.5 V, I_D = −3.9 A		9.7	22	nC
Gate−Source Charge	Q_{GS}			1.2		
Gate−Drain Charge	Q_{GD}			3.6		
Input Capacitance	C_{iss}	V_{DS} = −5.0 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz		710		pF
Output Capacitance	C_{oss}			400		
Reverse Transfer Capacitance	C_{rss}			140		
Turn−On Delay Time	$t_{d(on)}$	V_{DD} = −10 V, R_L = 10 Ω, $I_D \cong$ −1.0 A, V_{GEN} = −4.5 V, R_G = 6 Ω		14	30	ns
Rise Time	t_r			22	55	
Turn−Off Delay Time	$t_{d(off)}$			42	100	
Fall Time	t_f			35	70	
Source−Drain Reverse Recovery Time	t_{rr}	I_F = −1.1 A, di/dt = 100 A/μs		30	60	

4. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).
5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
6. Guaranteed by design, not subject to production testing.

ELECTRICAL CHARACTERISTICS FOR PNP TRANSISTORS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Collector – Emitter Breakdown Voltage (I_C = −10 mAdc, I_B = 0)	$V_{(BR)CEO}$	−35	−45	–	Vdc
Collector – Base Breakdown Voltage (I_C = −0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	−55	−65	–	Vdc
Emitter – Base Breakdown Voltage (I_E = −0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	−5.0	−7.0	–	Vdc
Collector Cutoff Current (V_{CB} = −35 Vdc, I_E = 0)	I_{CBO}	–	−0.03	−0.1	μAdc
Collector−Emitter Cutoff Current (V_{CES} = −35 Vdc)	I_{CES}	–	−0.03	−0.1	μAdc
Emitter Cutoff Current (V_{EB} = −6.0 Vdc)	I_{EBO}	–	−0.01	−0.1	μAdc
ON CHARACTERISTICS					
DC Current Gain (Note 7) (I_C = −1.0 A, V_{CE} = −2.0 V) (I_C = −1.5 A, V_{CE} = −2.0 V) (I_C = −2.0 A, V_{CE} = −2.0 V)	h_{FE}	 100 100 100	 200 200 200	 – 400 –	
Collector – Emitter Saturation Voltage (Note 7) (I_C = −0.1 A, I_B = −0.010 A) (I_C = −1.0 A, I_B = −0.010 A) (I_C = −2.0 A, I_B = −0.02 A)	$V_{CE(sat)}$	 – – –	 – – –	 −0.10 −0.15 −0.30	V
Base – Emitter Saturation Voltage (Note 7) (I_C = −1.0 A, I_B = −0.01 A)	$V_{BE(sat)}$	–	−0.68	−0.85	V
Base – Emitter Turn−on Voltage (Note 7) (I_C = −2.0 A, V_{CE} = −3.0 V)	$V_{BE(on)}$	–	−0.81	−0.875	V
Cutoff Frequency (I_C = −100 mA, V_{CE} = −5.0 V, f = 100 MHz)	f_T	100	–	–	MHz
Input Capacitance (V_{EB} = −0.5 V, f = 1.0 MHz)	Cibo	–	600	650	pF
Output Capacitance (V_{CB} = −3.0 V, f = 1.0 MHz)	Cobo	–	85	100	pF
Turn−on Time (V_{CC} = −10 V, I_{B1} = −100 mA, I_C = −1 A, R_L = 3 Ω)	t_{on}	–	35	–	nS
Turn−off Time (V_{CC} = −10 V, I_{B1} = I_{B2} = −100 mA, I_C = 1 A, R_L = 3 Ω)	t_{off}	–	225	–	nS

7. Pulsed Condition: Pulse Width = 300 μsec, Duty Cycle ≤ 2%

TYPICAL ELECTRICAL CHARACTERISTICS FOR P−CHANNEL FET

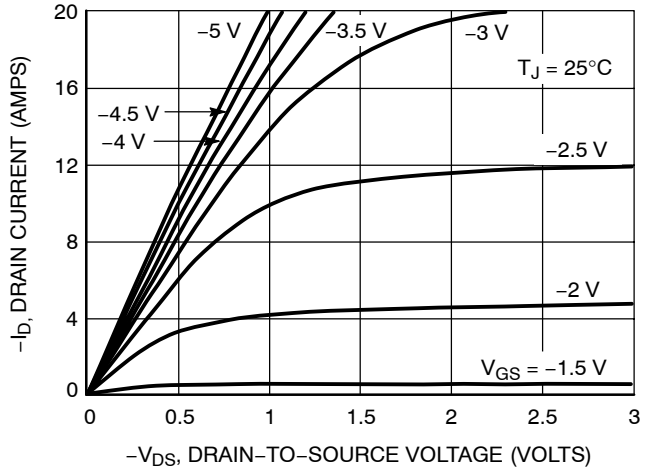


Figure 1. On−Region Characteristics

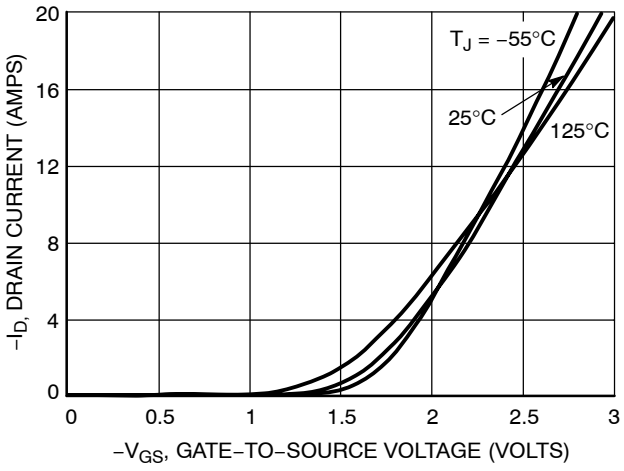


Figure 2. Transfer Characteristics

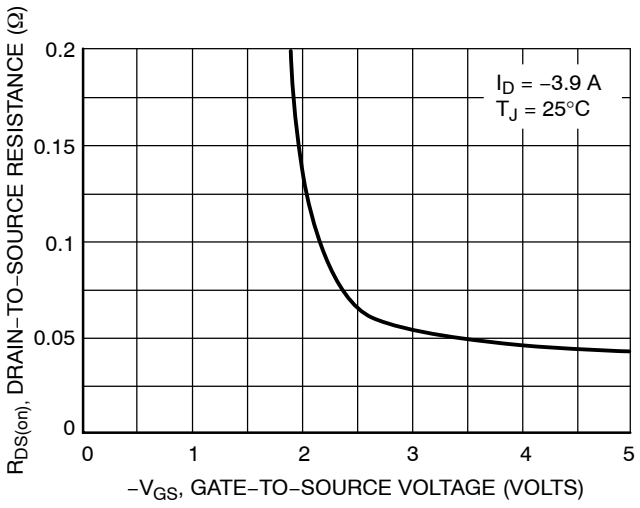


Figure 3. On−Resistance versus Gate−to−Source Voltage

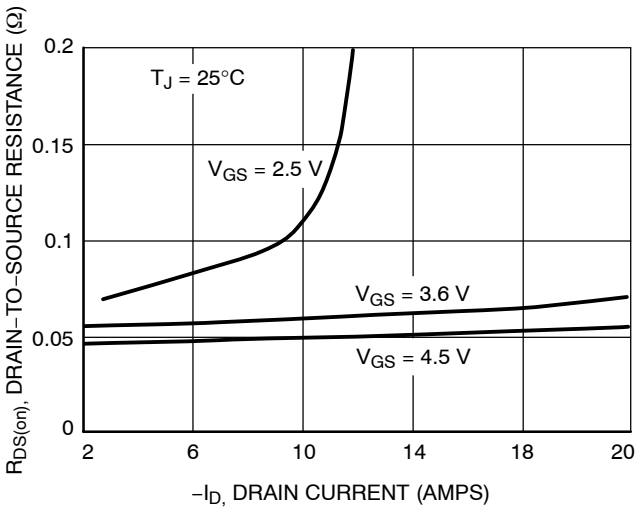


Figure 4. On−Resistance versus Drain Current and Gate Voltage

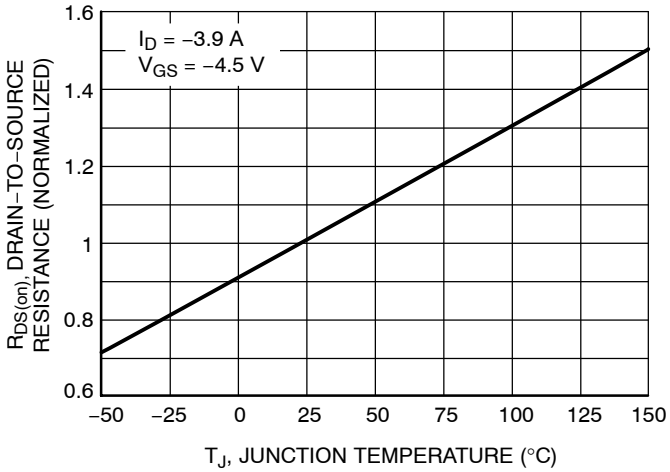


Figure 5. On−Resistance Variation with Temperature

TYPICAL ELECTRICAL CHARACTERISTICS FOR P−CHANNEL FET

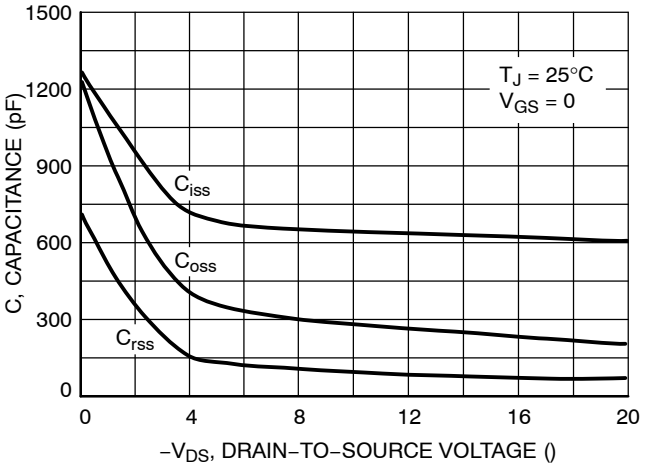


Figure 6. Capacitance Variation

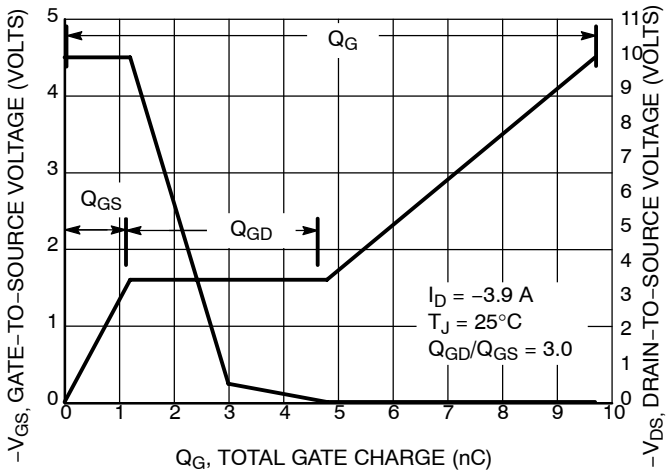


Figure 7. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

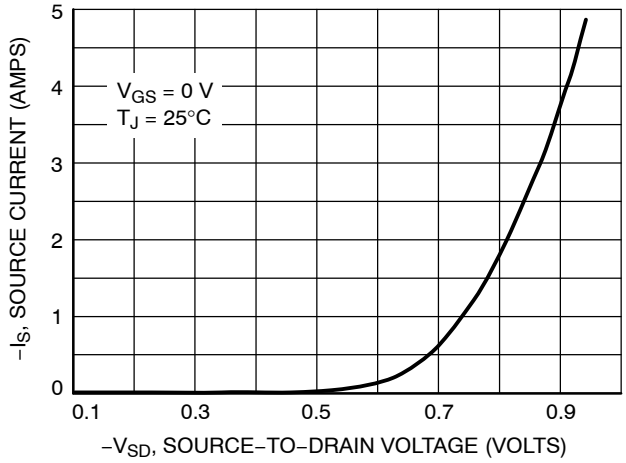


Figure 8. Diode Forward Voltage versus Current

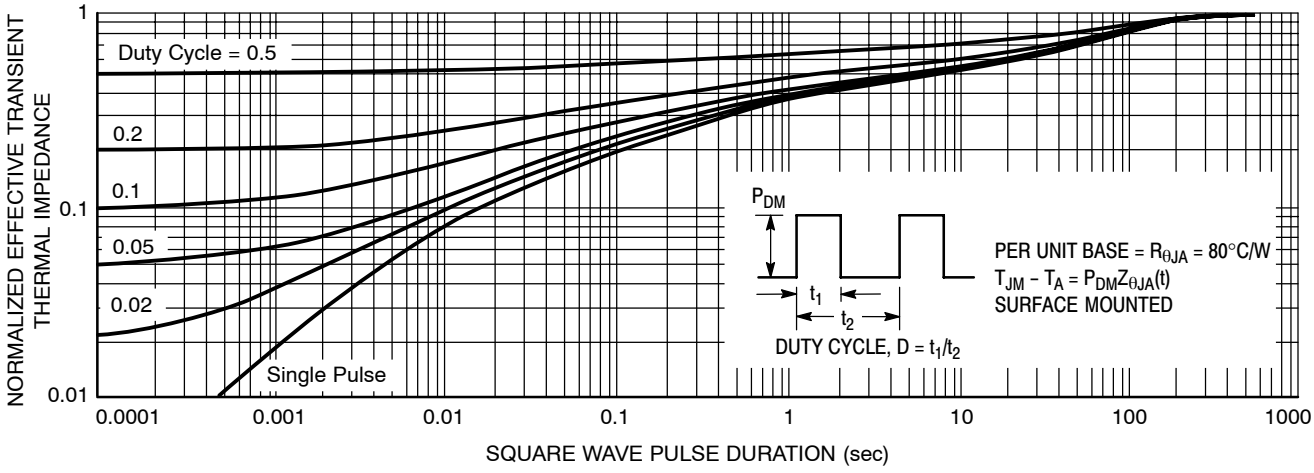


Figure 9. Normalized Thermal Transient Impedance, Junction−to−Ambient

TYPICAL ELECTRICAL CHARACTERISTICS FOR PNP TRANSISTOR

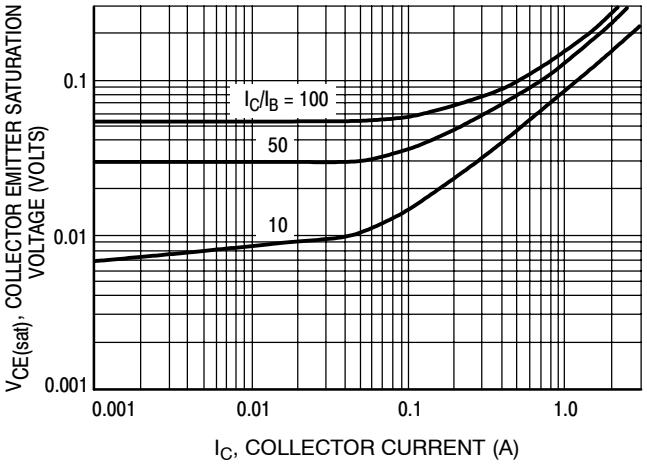


Figure 10. Collector Emitter Saturation Voltage versus Collector Current

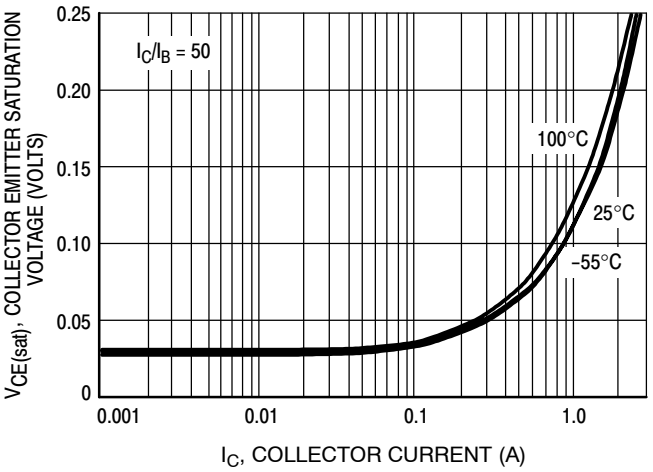


Figure 11. Collector Emitter Saturation Voltage versus Collector Current

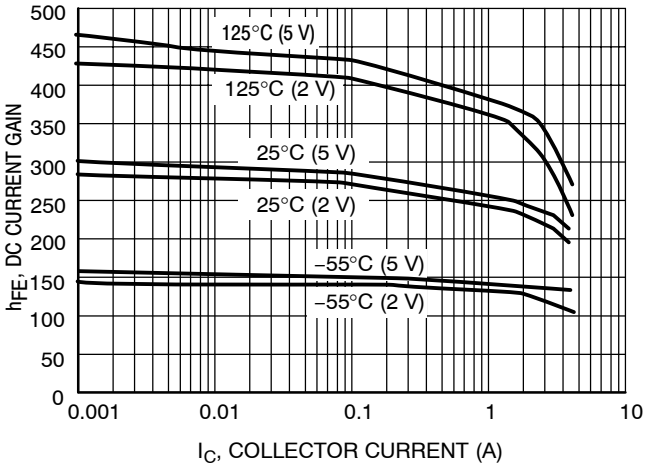


Figure 12. DC Current Gain versus Collector Current

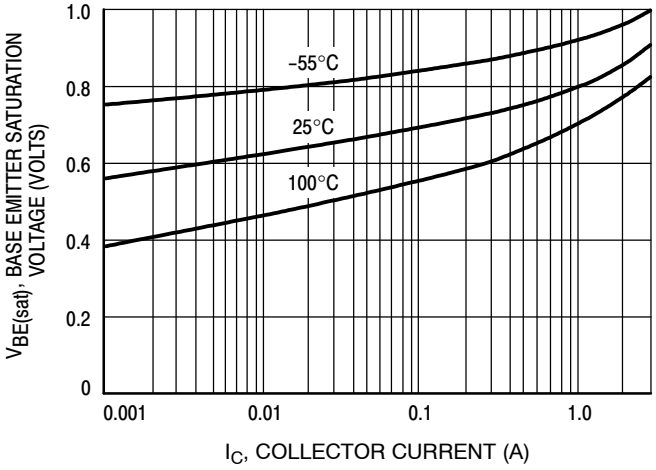


Figure 13. Base Emitter Saturation Voltage versus Collector Current

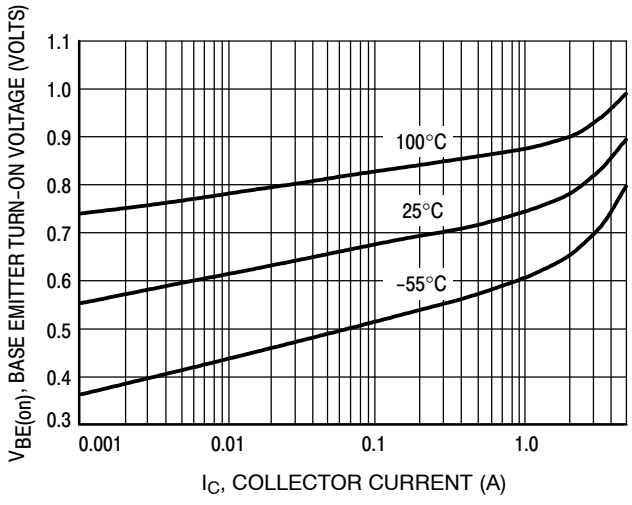


Figure 14. Base Emitter Turn−On Voltage versus Collector Current

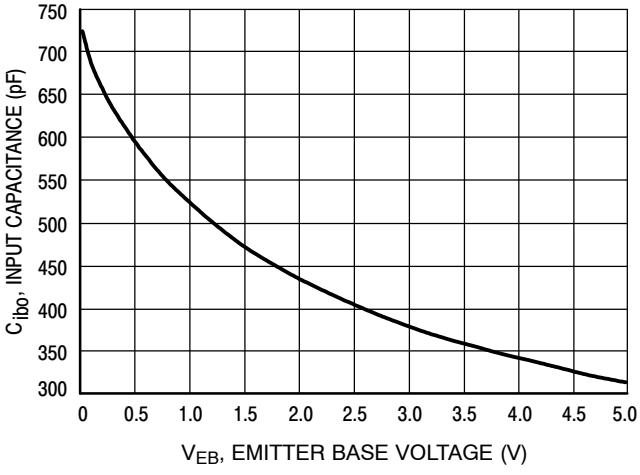


Figure 15. Input Capacitance

TYPICAL ELECTRICAL CHARACTERISTICS FOR PNP TRANSISTOR

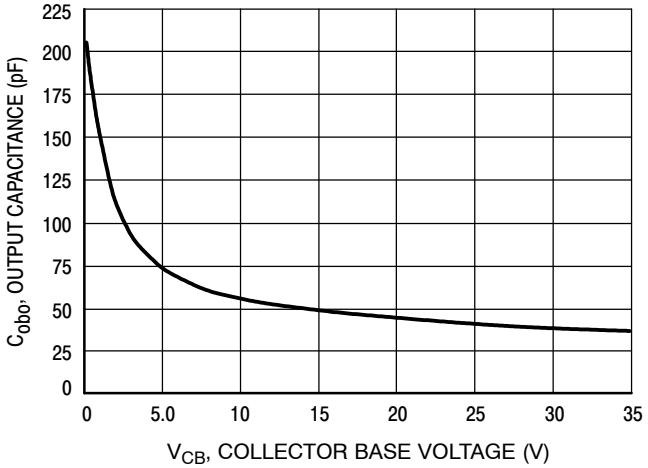


Figure 16. Output Capacitance

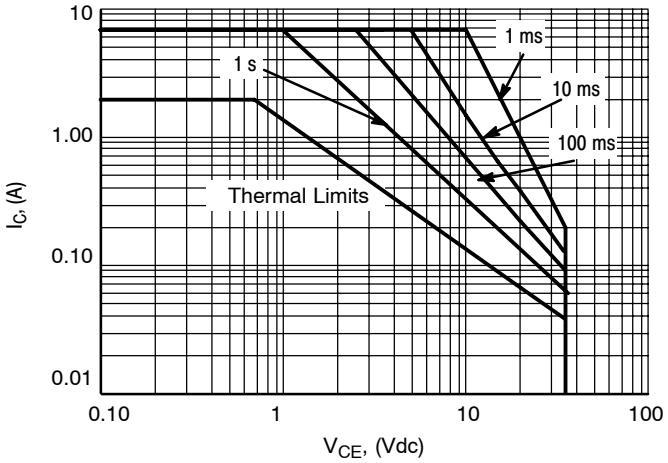


Figure 17. Safe Operating Area

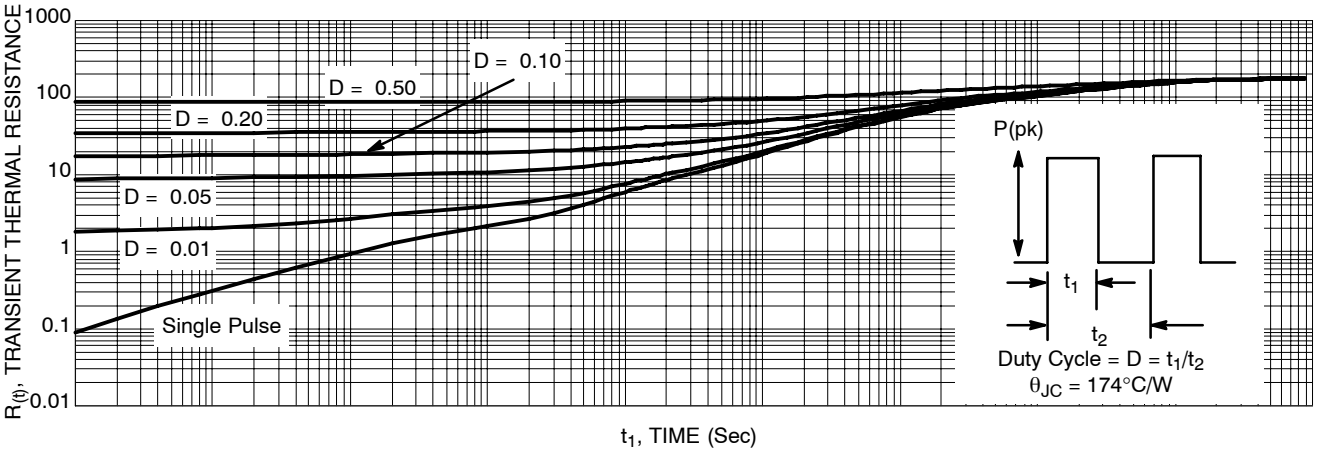
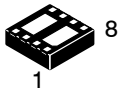


Figure 18. Normalized Thermal Response

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

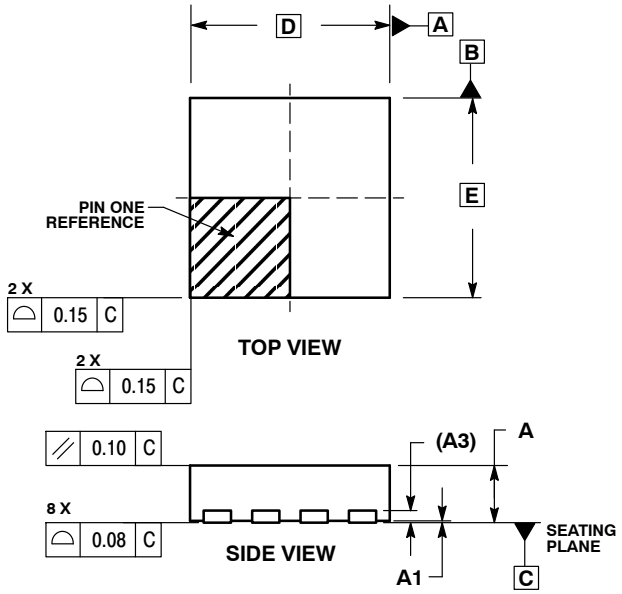
ON Semiconductor®

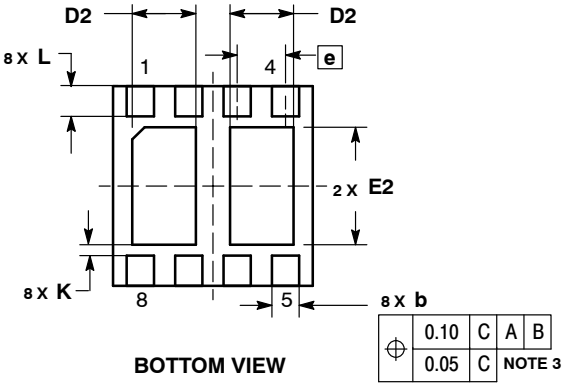


SCALE 2:1

DFN8
CASE 506AL−01
ISSUE A

DATE 20 DEC 2005





STYLE 1:
PIN 1. IN
2. GND
3. CNTRL
4. DRAIN
5. SOURCE
6. GATE
7. OUT
8. VCC

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

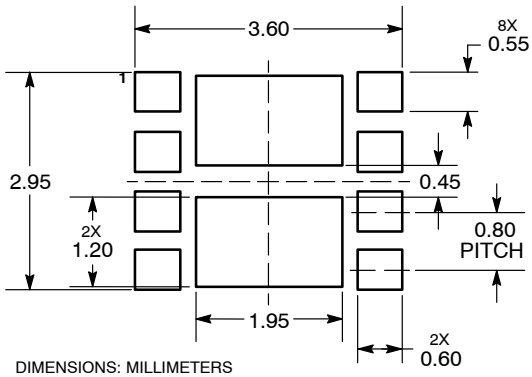
	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3		0.20 REF	
b	0.35	0.40	0.45
D		3.30 BSC	
D2	0.95	1.05	1.15
E		3.30 BSC	
E2	1.80	1.90	2.00
e		0.80 BSC	
K	0.21	---	---
L	0.30	0.40	0.50

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON20636D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**DFN8, 3.3X3.3 MM, 0.8 MM PITCH, DUAL FLAG**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

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For additional information, please contact your local Sales Representative

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