Class V, 14-BIT, 400-MSPS ANALOG-TO-DIGITAL CONVERTER

Check for Samples: ADS5474-SP

FEATURES

- **400 MSPS Sample Rate**
- **14 Bit Resolution, 10.9 Bits Effective Number of Bits (ENOB)**
- **5962R13208:**
  - **Radiation Hardness Assurance (RHA) up to TID 100 krad (Si)**
  - **Total Ionizing Dose 100 krad (Si)**
  - **ELDRS free 100 krad (Si)**
  - **SEL/SEU characterized**
- **1.28 GHz Input Bandwidth**
- **SFDR = 78 dBc at 230 MHz and 400 MSPS**
- **SNR = 69.8 dBFS at 230 MHz and 400 MSPS**
- **2.2 V_{PP} Differential Input Voltage**
- **LVDS-Compatible Outputs**
- **Total Power Dissipation: 2.5 W**
- **Power Down Mode: 50 mW**
- **Offset Binary Output Format**
- **Output Data Transitions on the Rising and Falling Edges of a Half-Rate Output Clock**
- **On-Chip Analog Buffer, Track-and-Hold, and Reference Circuit**
- **Available in a 84-Pin Ceramic Nonconductive Tie-Bar Package (HFG)**
- **Military Temperature Range: –55°C to +125°C T_{case}**
- **Engineering Evaluation (/EM) Samples are Available** (1)
- **Pin-Similar and Compatible With 12- and 14-Bit Family: ADS5463-SP and ADS5444-SP**

APPLICATIONS

- **Test and Measurement Instrumentation**
- **Software-Defined Radio**
- **Data Acquisition**
- **Power Amplifier Linearization**
- **Communication Instrumentation**
- **Radar**

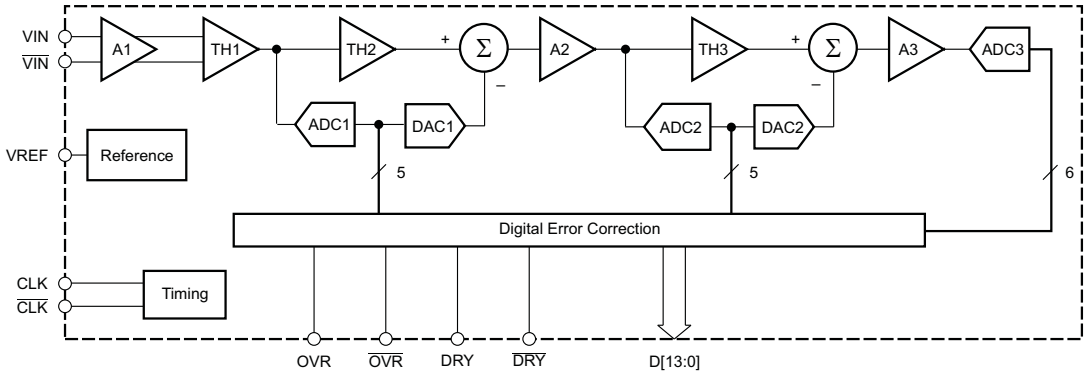
(1) These units are intended for engineering evaluation only. They are processed to a non-compliant flow (e.g. No Burn-In, etc.) and are tested to a temperature rating of 25°C only. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full MIL specified temperature range of -55°C to 125°C or operating life.

DESCRIPTION

The ADS5474 is a 14-bit, 400-MSPS analog-to-digital converter (ADC) that operates from both a 5-V supply and 3.3-V supply while providing LVDS-compatible digital outputs. This ADC is one of a family of 12-, 13-, 14-bit ADCs that operate from 210 MSPS to 500 MSPS. The ADS5474 input buffer isolates the internal switching of the onboard track and hold (T&H) from disturbing the signal source while providing a high-impedance input. An internal reference generator is also provided to simplify the system design.

Designed with a 1.4-GHz input bandwidth for the conversion of wide-bandwidth signals that exceed 400 MHz of input frequency at 400 MSPS, the ADS5474 has outstanding low noise performance and spurious-free dynamic range over a large input frequency range.

The ADS5474 is available in an 84-pin ceramic nonconductive tie-bar package (HFG). The device is built on Texas Instruments complementary bipolar process (BiCom3) and is specified over the full military temperature range (–55°C to +125°C T_{case}).



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		ADS5474-SP	UNIT
Supply voltage	AVDD5 to GND	6	V
	AVDD3 to GND	5	V
	DVDD3 to GND	5	V
Analog input to GND		–0.3 to (AVDD5 + 0.3)	V
Clock input to GND		–0.3 to (AVDD5 + 0.3)	V
CLK to $\overline{CLK}$		±2.5	V
Digital data output to GND		–0.3 to (DVDD3 + 0.3)	V
Operating case temperature range, T_C		–55 to +125	°C
Maximum junction temperature, T_J		+150	°C
Storage temperature range		–65 to +150	°C
ESD, human-body model (HBM)		2	kV

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. Kirkendall voidings and current density information for calculation of expected lifetime are available upon request.

THERMAL CHARACTERISTICS(1)

PARAMETER		TEST CONDITIONS	TYP	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Junction-to-case thermal resistance	21.81	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	MIL-STD-883 Test Method 1012	0.849	°C/W

(1) This CQFP package has built-in vias that electrically and thermally connect the bottom of the die to a pad on the bottom of the package. To efficiently remove heat and provide a low-impedance ground path, a thermal land is required on the surface of the PCB directly underneath the body of the package. During normal surface mount flow solder operations, the heat pad on the underside of the package is soldered to this thermal land creating an efficient thermal path. Normally, the PCB thermal land has a number of thermal vias within it that provide a thermal path to internal copper areas (or to the opposite side of the PCB) that provide for more efficient heat removal. TI typically recommends an 11,9 mm2 board-mount thermal pad. This allows maximum area for thermal dissipation, while keeping leads away from the pad area to prevent solder bridging. A sufficient quantity of thermal/electrical vias must be included to keep the device within recommended operating conditions. This pad must be electrically at ground potential.

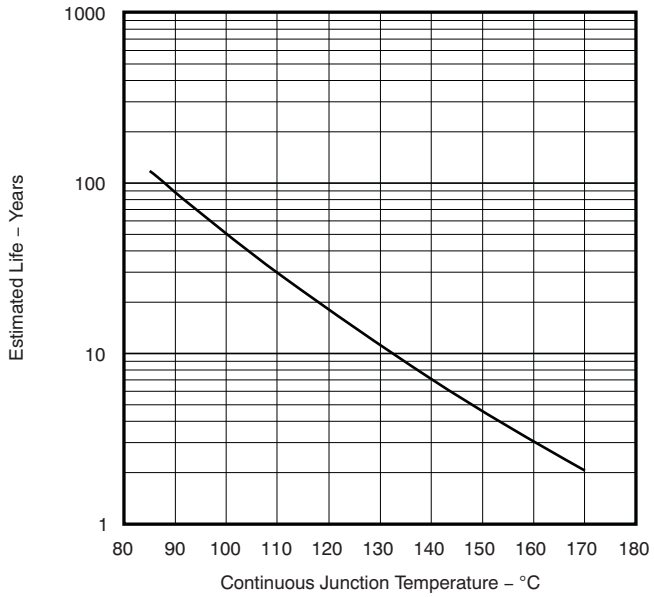


Figure 1. Operating Life Derating Chart, Electromigration Fail Mode

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
SUPPLIES					
AVDD5	Analog supply voltage	4.75	5	5.25	V
AVDD3	Analog supply voltage	3.1	3.3	3.6	V
DVDD3	Output driver supply voltage	3	3.3	3.6	V
ANALOG INPUT					
	Differential input range		2.2		V_{PP}
VCM	Input common mode		3.1		V
DIGITAL OUTPUT (DRY, DATA, OVR)					
	Maximum differential output load		10		pF
CLOCK INPUT (CLK)					
	CLK input sample rate (sine wave)	20(1)		400	MSPS
	Clock amplitude, differential sine wave(1)	0.5		5	V_{PP}
	Clock duty cycle (1)	40	50	60	%
T_C	Operating case temperature range	–55		+125	°C

(1) Parameters are assured by characterization, but not production tested.

ELECTRICAL CHARACTERISTICS

Typical values at T_C = +25°C: minimum and maximum values over full temperature range $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 400 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3 V_{PP} differential clock, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				14		Bits
ANALOG INPUTS						
	Differential input range			2.2		V_{PP}
	Analog input common-mode voltage	Self-biased; see VCM specification below		3.1		V
	Input resistance (dc)	Each input to VCM		500		Ω
	Input capacitance	Each input to GND		7.4		pF
	Analog input bandwidth (–3dB)			1.28		GHz
CMRR	Common-mode rejection ratio	Common-mode signal < 50 MHz (see Figure 28)		100		dB
INTERNAL REFERENCE VOLTAGE						
VREF	Reference voltage			2.4		V
VCM	Analog input common-mode voltage reference output	With internal VREF. Provided as an output via the VCM pin for dc-coupled applications.	2.9	3.1	3.3	V
	VCM temperature coefficient			–0.8		mV/°C
DYNAMIC ACCURACY						
	No missing codes			Assured		
DNL	Differential linearity error	f_{IN} = 10 MHz	–0.99	±0.7	2.5	LSB
INL	Integral linearity error	f_{IN} = 10 MHz	–7.0	±1.5	7.0	LSB
	Offset error		–16		16	mV
	Offset temperature coefficient			0.02		mV/°C
	Gain error		–5		5	%FS
	Gain temperature coefficient			–0.02		%FS/°C

ELECTRICAL CHARACTERISTICS (continued)

Typical values at T_C = +25°C: minimum and maximum values over full temperature range $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 400 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3 V_{PP} differential clock, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{AVDD5}	5-V analog supply current	V_{IN} = full-scale, f_{IN} = 70 MHz, f_S = 400 MSPS		338	380	mA
I_{AVDD3}	3.3-V analog supply current			185	210	mA
I_{DVDD3}	3.3-V digital supply current (includes LVDS)			75	85	mA
	Total power dissipation			2.5	2.835	W
	Power-up time	From turn-on of AVDD5		50		µs
	Wake-up time	From PDWN pin switched from HIGH (PDWN active) to LOW (ADC awake) (see Figure 29)		5		µs
	Power-down power dissipation	PDWN pin = logic HIGH		50	350	mW
PSRR	Power-supply rejection ratio, AVDD5 supply	Without 0.1 µF board supply capacitors, with < 1 MHz supply noise		75		dB
PSRR	Power-supply rejection ratio, AVDD3 supply			90		dB
PSRR	Power-supply rejection ratio, DVDD3 supply			110		dB
DYNAMIC AC CHARACTERISTICS						
SNR	Signal-to-noise ratio	f_{IN} = 30 MHz		70.5		dBFS
		f_{IN} = 70 MHz	65	68.7		
		f_{IN} = 130 MHz		69.9		
		f_{IN} = 230 MHz	65	69.8		
		f_{IN} = 351 MHz		69.2		
		f_{IN} = 451 MHz		68.8		
		f_{IN} = 651 MHz		67.3		
		f_{IN} = 751 MHz		66.6		
		f_{IN} = 999 MHz		64.4		
SFDR	Spurious-free dynamic range	f_{IN} = 30 MHz		79.4		dBc
		f_{IN} = 70 MHz	69	76.3		
		f_{IN} = 130 MHz		78.8		
		f_{IN} = 230 MHz	64.5	78		
		f_{IN} = 351 MHz		74.3		
		f_{IN} = 451 MHz		70.5		
		f_{IN} = 651 MHz		58.6		
		f_{IN} = 751 MHz		54.3		
		f_{IN} = 999 MHz		46		
HD2	Second-harmonic	f_{IN} = 30 MHz		92		dBc
		f_{IN} = 70 MHz		87		
		f_{IN} = 130 MHz		87		
		f_{IN} = 230 MHz		84		
		f_{IN} = 351 MHz		77		
		f_{IN} = 451 MHz		75		
		f_{IN} = 651 MHz		68		
		f_{IN} = 751 MHz		64		
		f_{IN} = 999 MHz		53		

ELECTRICAL CHARACTERISTICS (continued)

Typical values at T_C = +25°C: minimum and maximum values over full temperature range $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 400 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3 V_{PP} differential clock, unless otherwise noted.

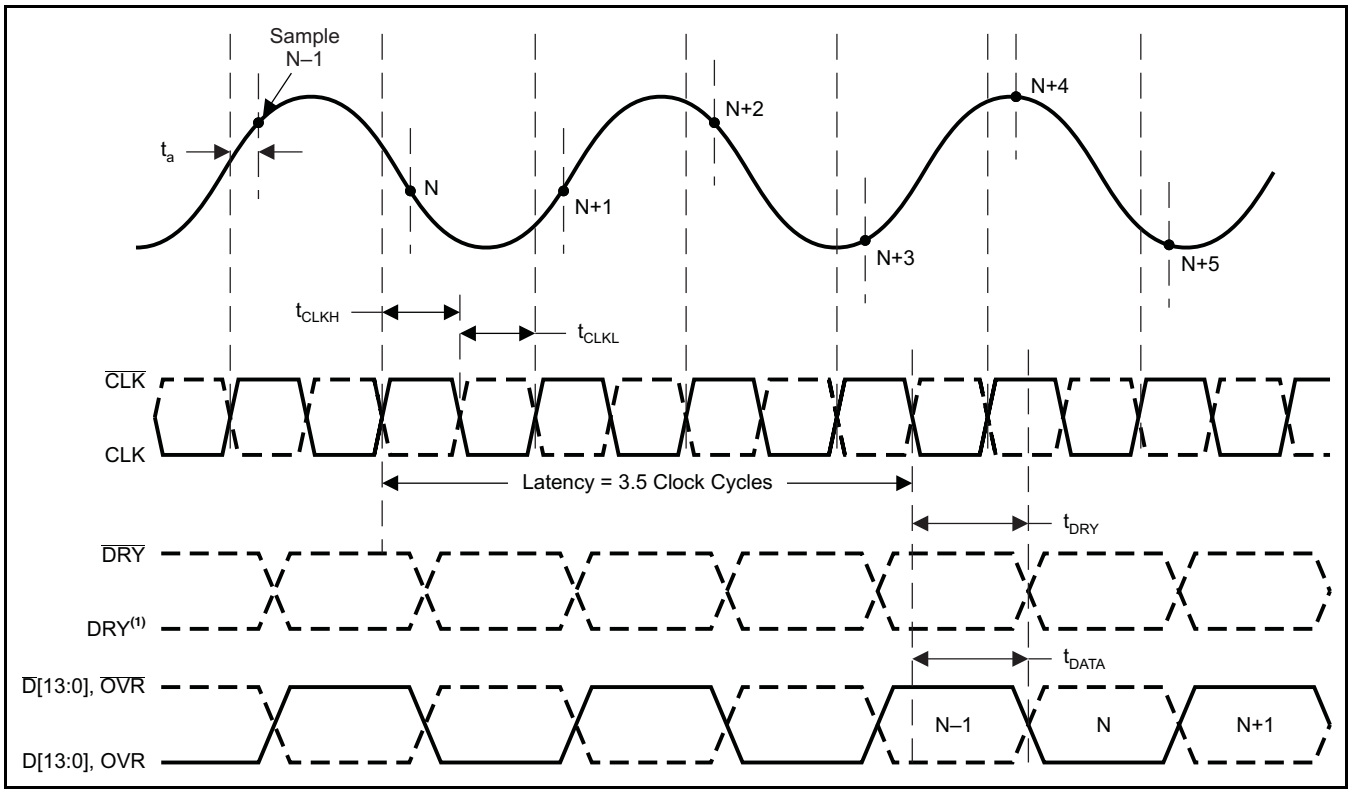
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC AC CHARACTERISTICS (continued)						
HD3	Third-harmonic	f_{IN} = 30 MHz		81		dBc
		f_{IN} = 70 MHz		86		
		f_{IN} = 130 MHz		80		
		f_{IN} = 230 MHz		80		
		f_{IN} = 351 MHz		76		
		f_{IN} = 451 MHz		72		
		f_{IN} = 651 MHz		60		
		f_{IN} = 751 MHz		56		
		f_{IN} = 999 MHz		48		
	Worst harmonic/spur (other than HD2 and HD3)	f_{IN} = 30 MHz		93		dBc
		f_{IN} = 70 MHz		91		
		f_{IN} = 130 MHz		91		
		f_{IN} = 230 MHz		88		
		f_{IN} = 351 MHz		87		
		f_{IN} = 451 MHz		87		
		f_{IN} = 651 MHz		91		
		f_{IN} = 751 MHz		87		
		f_{IN} = 999 MHz		80		
THD	Total harmonic distortion	f_{IN} = 30 MHz		77		dBc
		f_{IN} = 70 MHz		73.5		
		f_{IN} = 130 MHz		74.9		
		f_{IN} = 230 MHz		74.9		
		f_{IN} = 351 MHz		71.3		
		f_{IN} = 451 MHz		68.4		
		f_{IN} = 651 MHz		57.8		
		f_{IN} = 751 MHz		53.6		
		f_{IN} = 999 MHz		45		

ELECTRICAL CHARACTERISTICS (continued)

Typical values at T_C = +25°C: minimum and maximum values over full temperature range $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 400 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3 V_{PP} differential clock, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC AC CHARACTERISTICS (continued)						
SINAD	Signal-to-noise and distortion	f_{IN} = 30 MHz		69.8		dBc
		f_{IN} = 70 MHz	62.5	67.7		
		f_{IN} = 130 MHz		68.9		
		f_{IN} = 230 MHz	60.5	68.9		
		f_{IN} = 351 MHz		67.5		
		f_{IN} = 451 MHz		66.1		
		f_{IN} = 651 MHz		58.2		
		f_{IN} = 751 MHz		54.3		
		f_{IN} = 999 MHz		45.9		
	Two-tone SFDR	f_{IN1} = 69 MHz, f_{IN2} = 70 MHz, each tone at –7 dBFS		84.2		dBFS
		f_{IN1} = 69 MHz, f_{IN2} = 70 MHz, each tone at –16 dBFS		98.5		
		f_{IN1} = 297.5 MHz, f_{IN2} = 302.5 MHz, each tone at –7 dBFS		82.5		
		f_{IN1} = 297.5 MHz, f_{IN2} = 302.5 MHz, each tone at –16 dBFS		99		
ENOB	Effective number of bits	f_{IN} = 70 MHz	10.1	10.9		Bits
		f_{IN} = 230 MHz	9.77	10.5		
	RMS idle-channel noise	Inputs tied to common-mode		1.8		LSB
LVDS DIGITAL OUTPUTS						
V_{OD}	Differential output voltage (±)		247	350	454	mV
V_{OC}	Common-mode output voltage		1.115		1.375	V
DIGITAL INPUTS						
V_{IH}	High level input voltage	PWD (pin 33)	2.0			V
V_{IL}	Low level input voltage				0.8	V
I_{IH}	High level input current				1	µA
I_{IL}	Low level input current		-1			µA
C_{IN}	Input Capacitance			2.2		pF

TIMING INFORMATION



(1) Polarity of DRY is undetermined. For further information, see the Digital Outputs section.

Figure 2. Timing Diagram

TIMING CHARACTERISTICS(1)

Typical values at T_C = +25°C: minimum and maximum values over full temperature range $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = +125°C, sampling rate = 400 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3 V_{PP} differential clock, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_a	Aperture delay			200		ps
	Aperture jitter, rms	Internal jitter of the ADC		103		fs
	Latency			3.5		cycles
t_{CLK}	Clock period		2.5		50	ns
t_{CLKH}	Clock pulse duration, high		1			ns
t_{CLKL}	Clock pulse duration, low		1			ns
t_{DRY}	CLK to DRY delay(2)	Zero crossing, 10-pF parasitic loading to GND on each output pin	700	1600	2500	ps
t_{DATA}	CLK to DATA/OVR delay(2)	Zero crossing, 10-pF parasitic loading to GND on each output pin	650	1600	2600	ps
t_{SKEW}	DATA to DRY skew	t_{DATA} – t_{DRY}, 10-pF parasitic loading to GND on each output pin	-700	0	700	ps
t_{RISE}	DRY/DATA/OVR rise time	10-pF parasitic loading to GND on each output pin		500		ps
t_{FALL}	DRY/DATA/OVR fall time	10-pF parasitic loading to GND on each output pin		500		ps

(1) Timing parameters are assured by characterization, but not production tested.
(2) DRY, DATA, and OVR are updated on the falling edge of CLK. The latency must be added to t_{DATA} to determine the overall propagation delay.

PIN CONFIGURATION

HFG PACKAGE
(TOP VIEW)

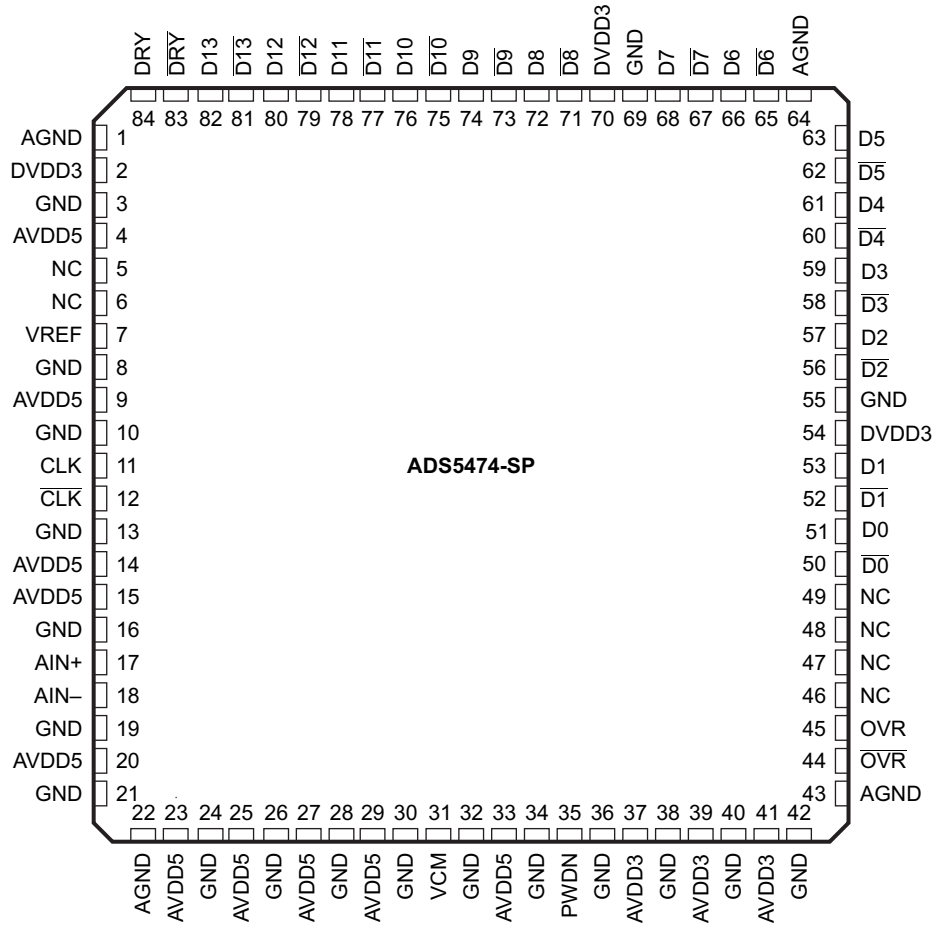


Table 1. TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
AIN	17	Differential input signal (positive)
$\overline{\text{AIN}}$	18	Differential input signal (negative)
AVDD5	4, 9, 14, 15, 20, 23, 25, 27, 29, 33	Analog power supply (5 V)
AVDD3	37, 39, 41	Analog power supply (3.3 V)
DVDD3	2, 54, 70	Digital and output driver power supply (3.3 V)
GND	1,3, 8, 10, 13, 16, 19, 21, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 42, 43, 55, 64, 69	Ground
CLK	11	Differential input clock (positive). Conversion is initiated on rising edge.
$\overline{\text{CLK}}$	12	Differential input clock (negative)
$\overline{\text{D0}}$, D0	50, 51	LVDS digital output pair, least-significant bit (LSB)
$\overline{\text{D1}}$, D1, $\overline{\text{D2}}$–D5, $\overline{\text{D6}}$-D7, $\overline{\text{D8}}$-D12	52, 53, 56–63, 65–68, 71–82	LVDS digital output pairs
$\overline{\text{D13}}$, D13	81, 82	LVDS digital output pair, most significant bit (MSB)
DRY, $\overline{\text{DRY}}$	84, 83	Data ready LVDS output pair
NC	5, 6, 46, 47, 48, 49	No connect
OVR, $\overline{\text{OVR}}$	45, 44	Overrange indicator LVDS output. A logic high signals an analog input in excess of the full-scale range.
VCM	31	Common-mode voltage output (3.1 V nominal). Commonly used in DC-coupled applications to set the input signal to the correct common-mode voltage. (This pin is not used on the ADS5463-SP and ADS5444-SP)
PDWN	35	Power-down (active high). Device is in sleep mode when PDWN pin is logic HIGH. ADC converter is awake when PDWN is logic LOW (grounded). (This pin is not used on the ADS5463-SP and ADS5444-SP)
VREF	7	Reference voltage input/output (2.4 V nominal)

TYPICAL CHARACTERISTICS

At T_A = +25°C, sampling rate = 400 MSPS, 50% clock duty cycle, 3-V_{PP} differential sinusoidal clock, analog input amplitude = –1 dBFS, AVDD5 = 5 V, AVDD3 = 3.3 V, and DVDD3 = 3.3 V, unless otherwise noted.

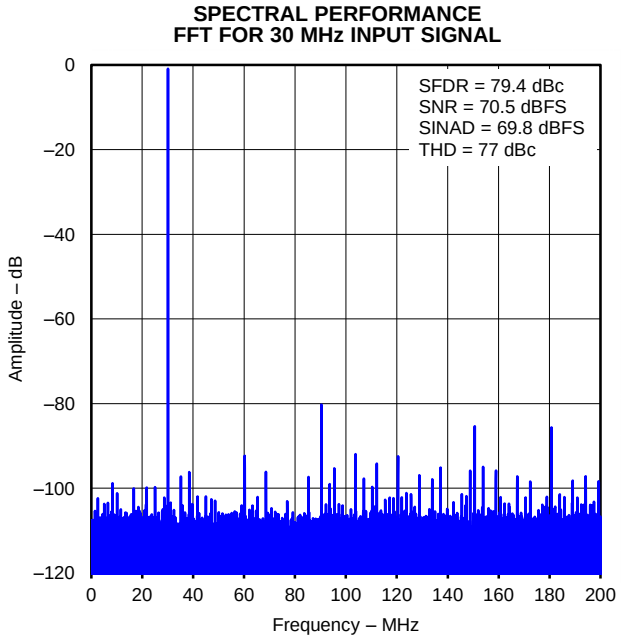


Figure 3.

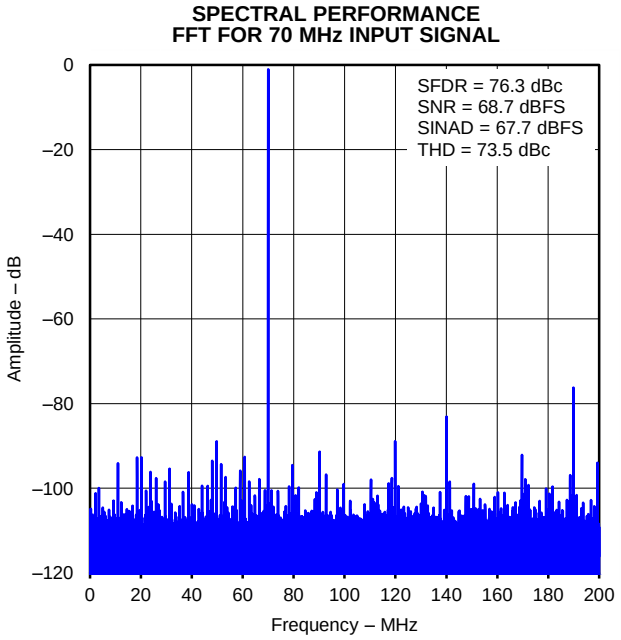


Figure 4.

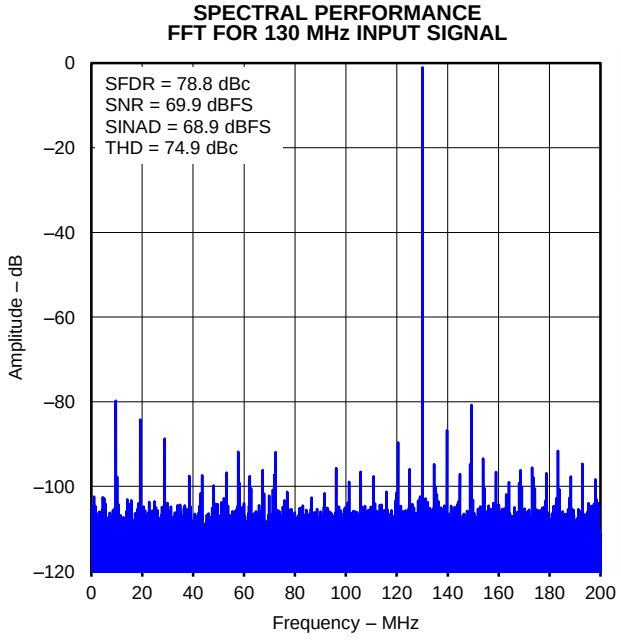


Figure 5.

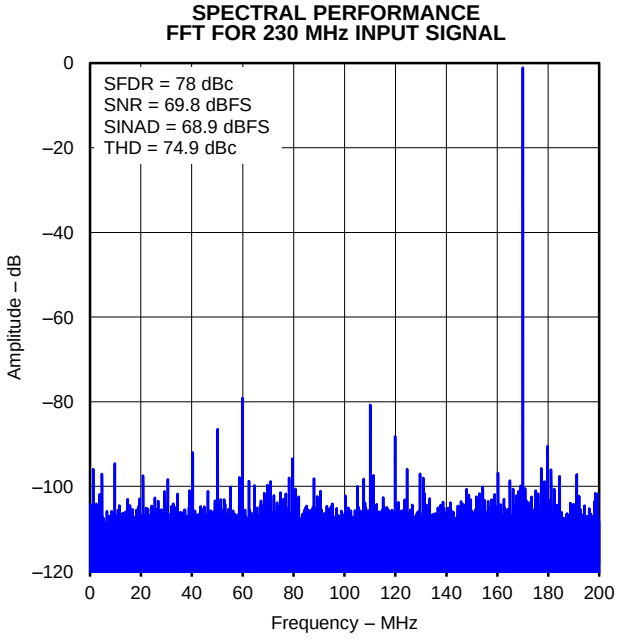


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, sampling rate = 400 MSPS, 50% clock duty cycle, 3-V_{PP} differential sinusoidal clock, analog input amplitude = –1 dBFS, AVDD5 = 5 V, AVDD3 = 3.3 V, and DVDD3 = 3.3 V, unless otherwise noted.

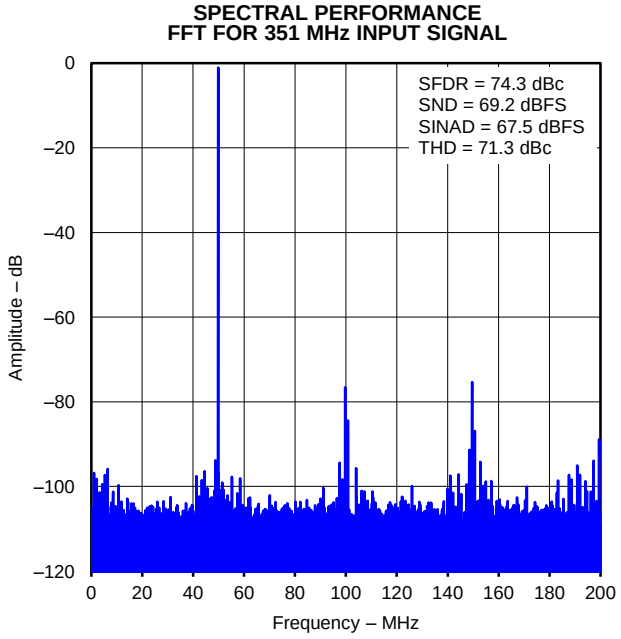


Figure 7.

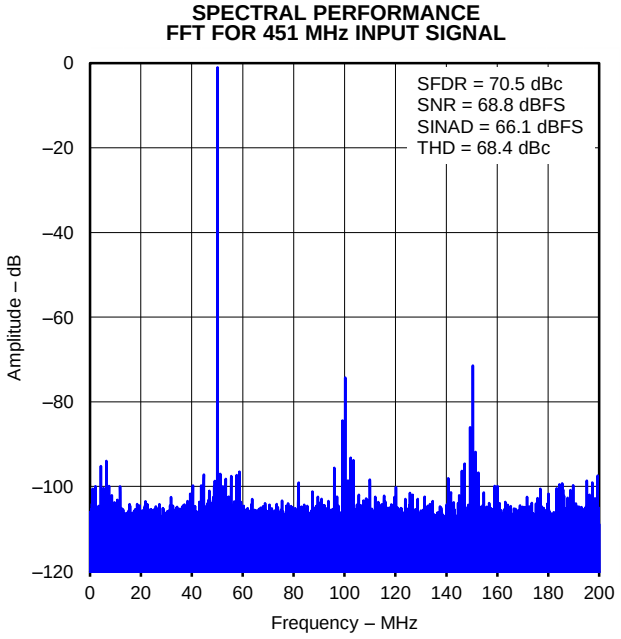


Figure 8.

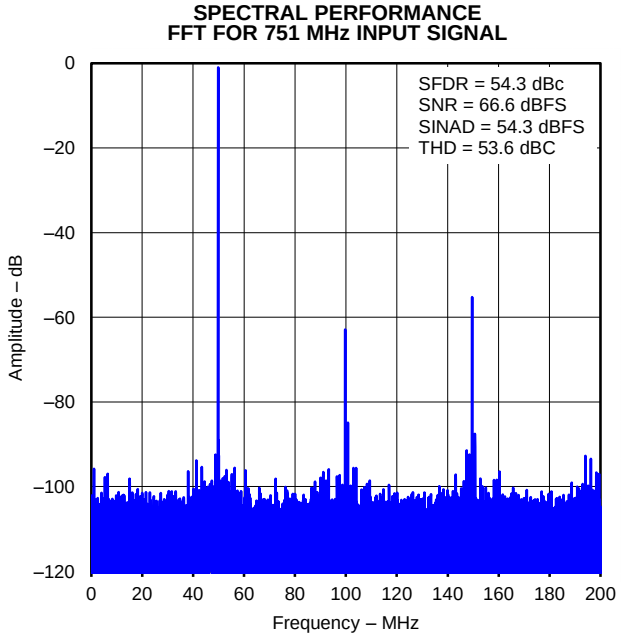


Figure 9.

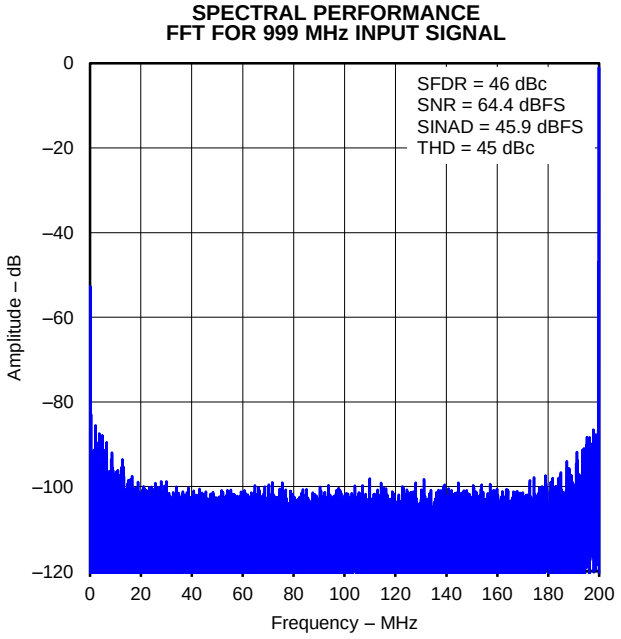


Figure 10.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, sampling rate = 400 MSPS, 50% clock duty cycle, 3-V_{PP} differential sinusoidal clock, analog input amplitude = –1 dBFS, AVDD5 = 5 V, AVDD3 = 3.3 V, and DVDD3 = 3.3 V, unless otherwise noted.

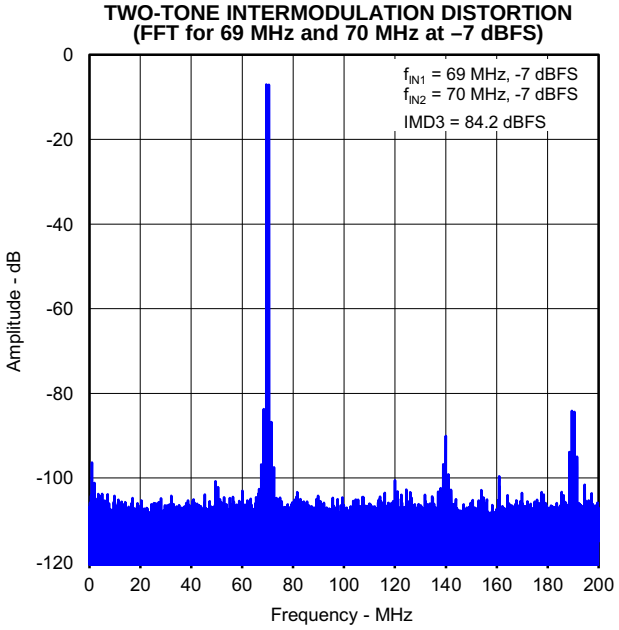


Figure 11.

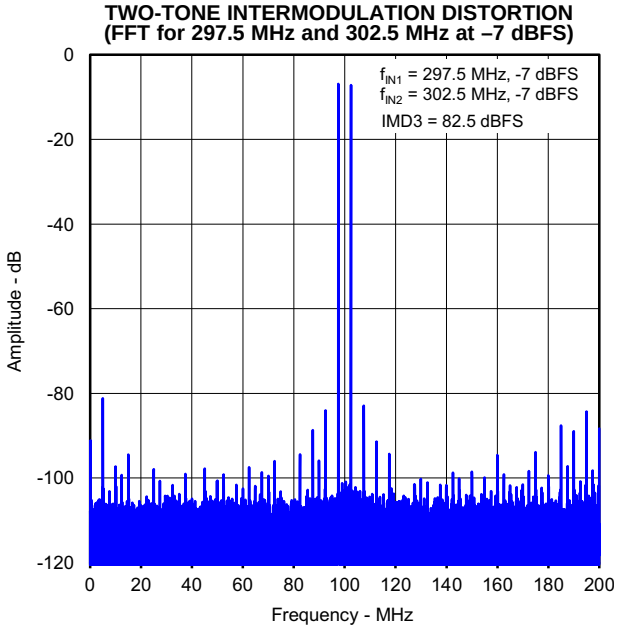


Figure 12.

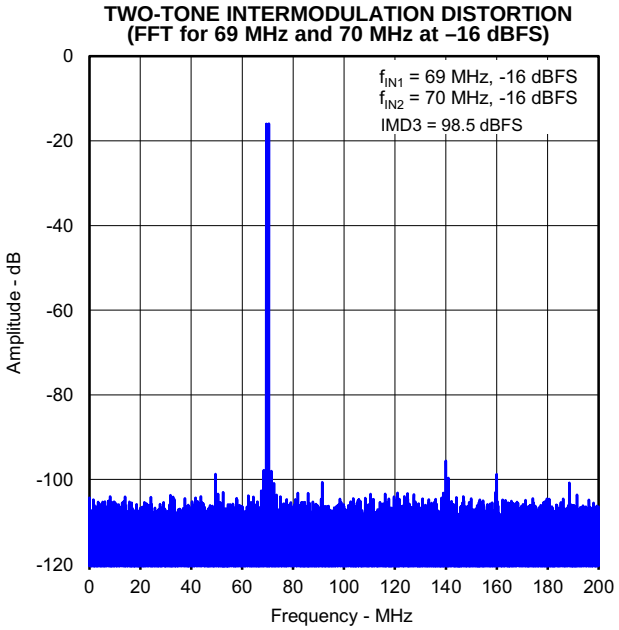


Figure 13.

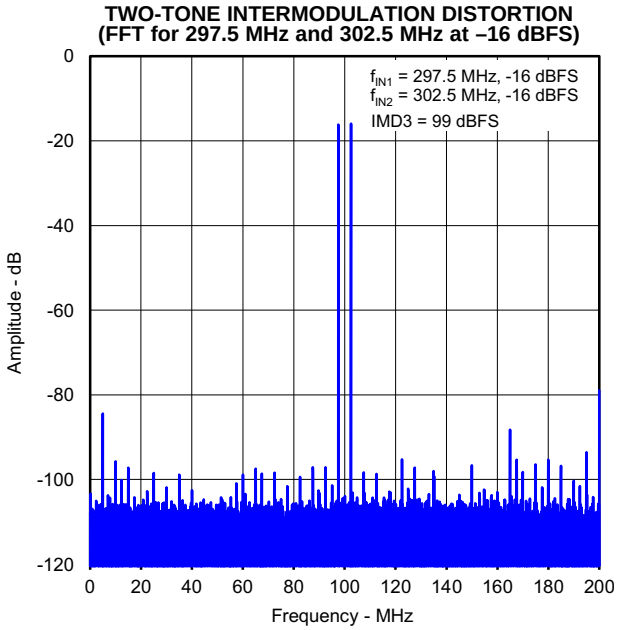


Figure 14.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, sampling rate = 400 MSPS, 50% clock duty cycle, 3-V_{PP} differential sinusoidal clock, analog input amplitude = –1 dBFS, AVDD5 = 5 V, AVDD3 = 3.3 V, and DVDD3 = 3.3 V, unless otherwise noted.

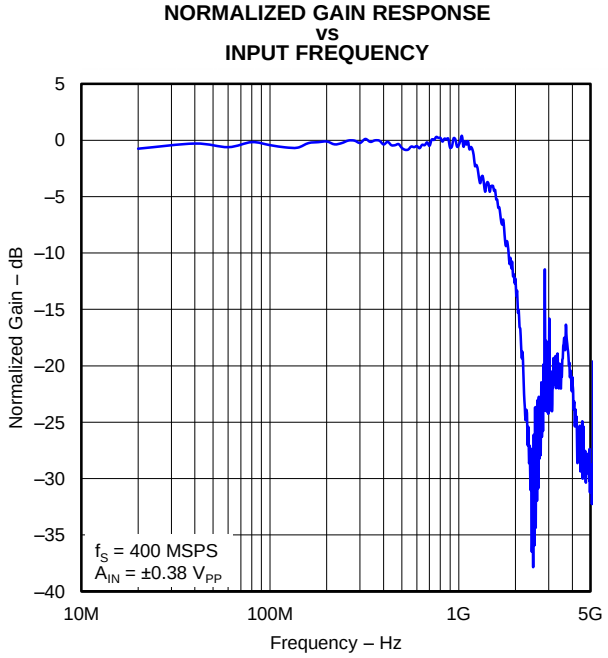


Figure 15.

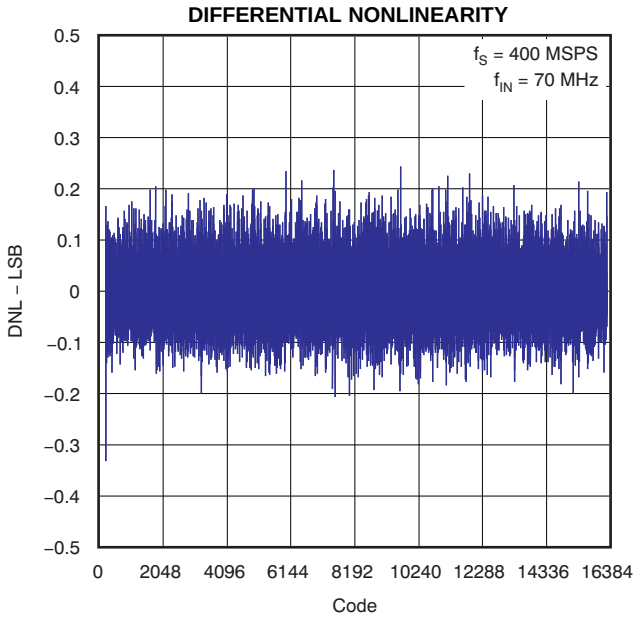


Figure 16.

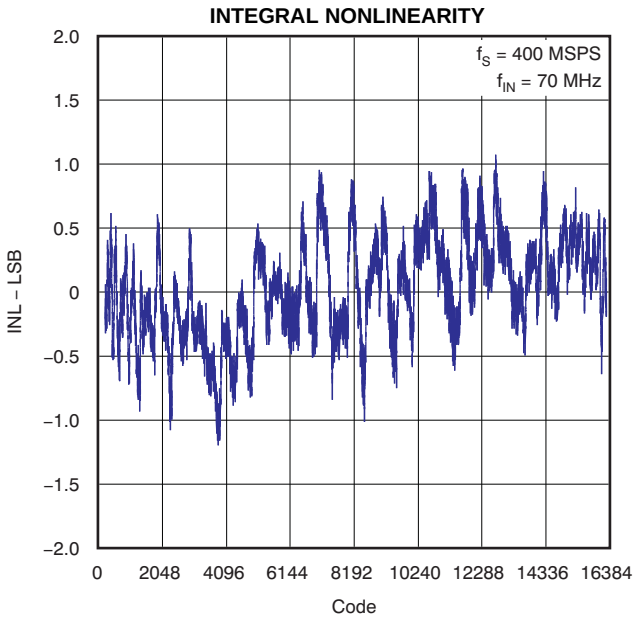


Figure 17.

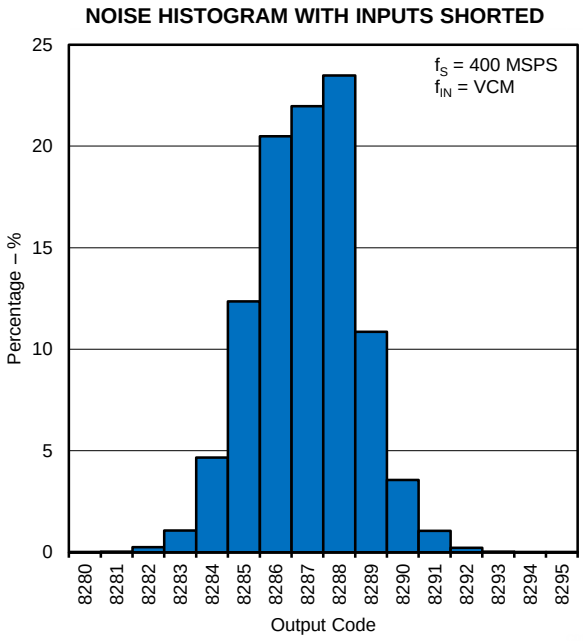


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, sampling rate = 400 MSPS, 50% clock duty cycle, 3-V_{PP} differential sinusoidal clock, analog input amplitude = –1 dBFS, AVDD5 = 5 V, AVDD3 = 3.3 V, and DVDD3 = 3.3 V, unless otherwise noted.

AC PERFORMANCE vs INPUT AMPLITUDE (70 MHz Input Signal)

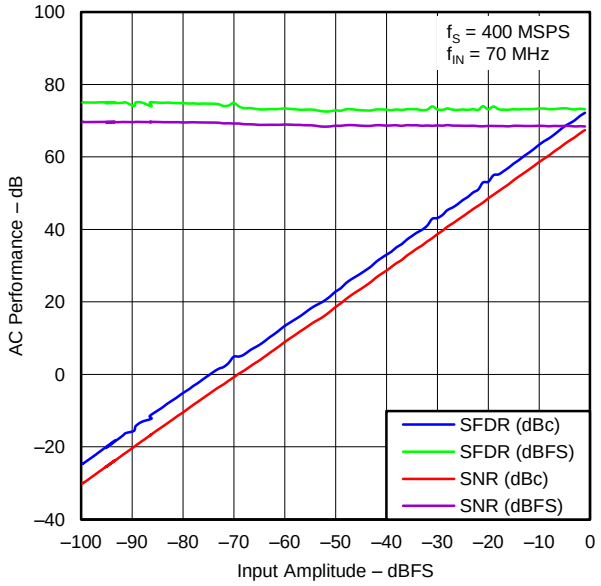


Figure 19.

AC PERFORMANCE vs INPUT AMPLITUDE (230 MHz Input Signal)

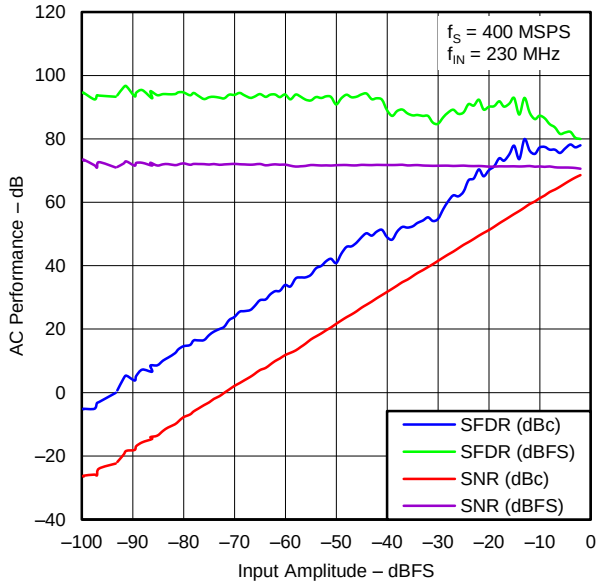


Figure 20.

TWO-TONE PERFORMANCE vs INPUT AMPLITUDE (f_1 = 297.5 MHz and f_2 = 302.5 MHz)

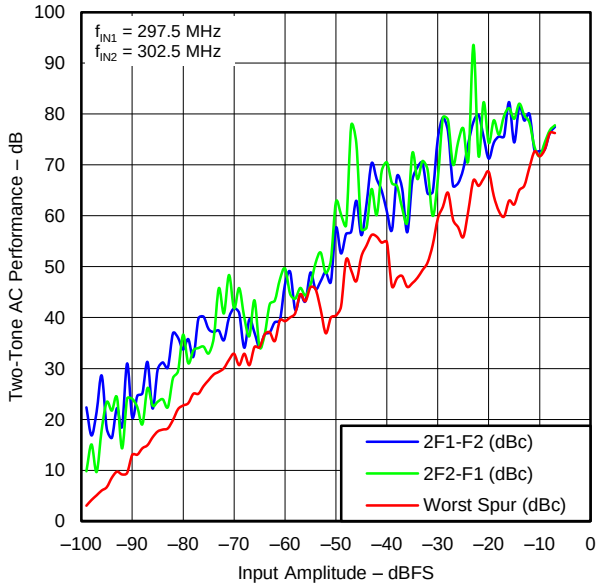


Figure 21.

SFDR vs AVDD5 OVER TEMPERATURE

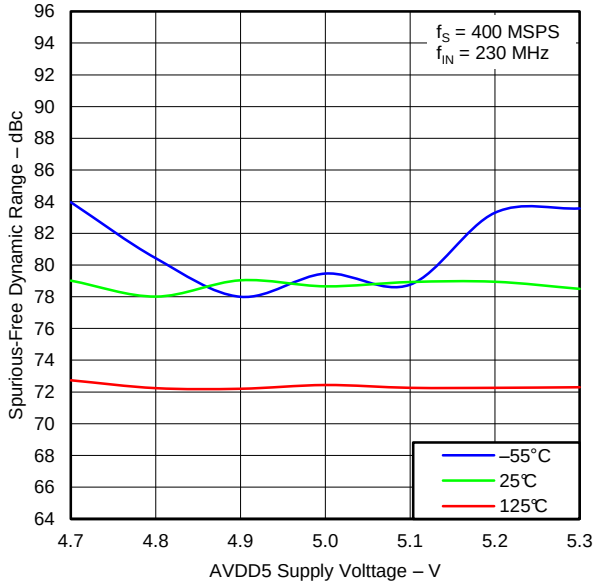


Figure 22.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, sampling rate = 400 MSPS, 50% clock duty cycle, 3-V_{PP} differential sinusoidal clock, analog input amplitude = –1 dBFS, AVDD5 = 5 V, AVDD3 = 3.3 V, and DVDD3 = 3.3 V, unless otherwise noted.

SNR vs AVDD5 OVER TEMPERATURE

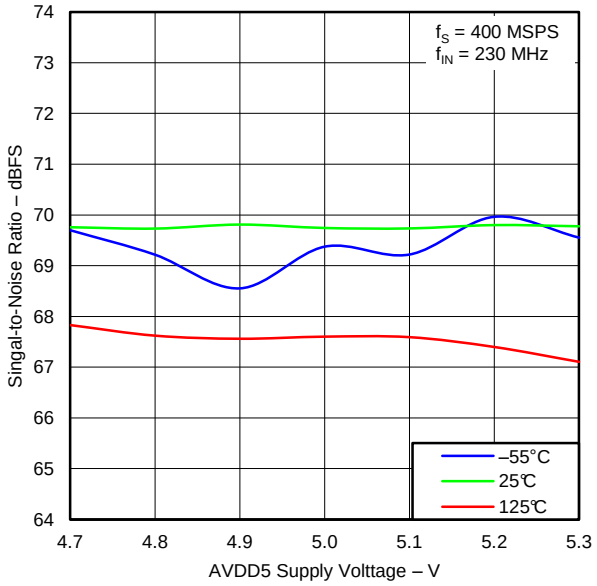


Figure 23.

SFDR vs AVDD33 OVER TEMPERATURE

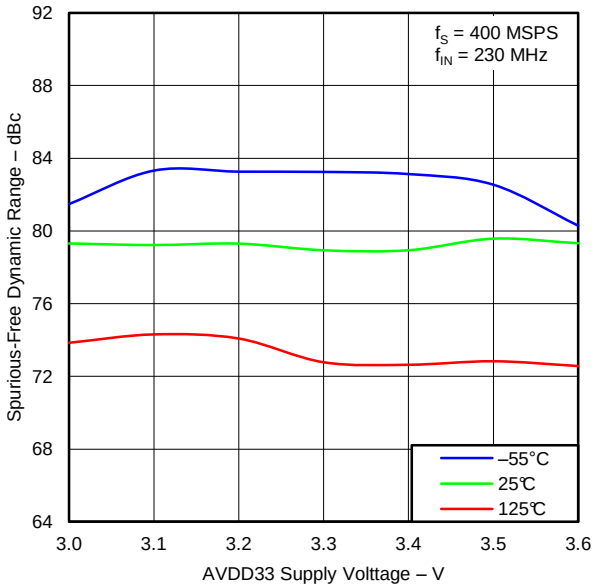


Figure 24.

SNR vs AVDD33 OVER TEMPERATURE

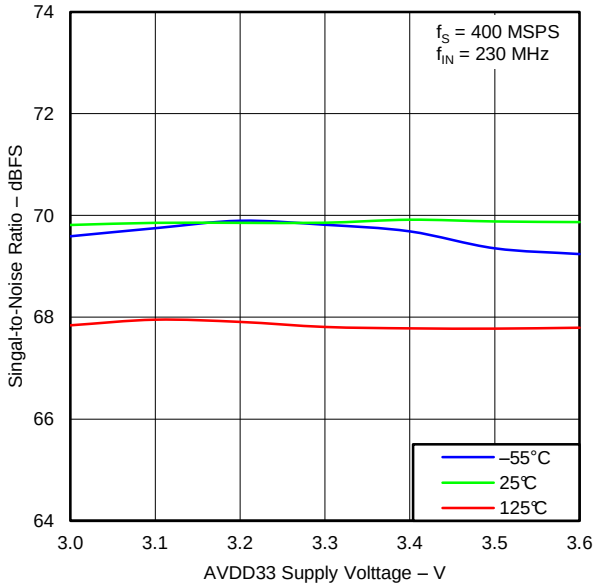


Figure 25.

SFDR vs DVDD18 OVER TEMPERATURE

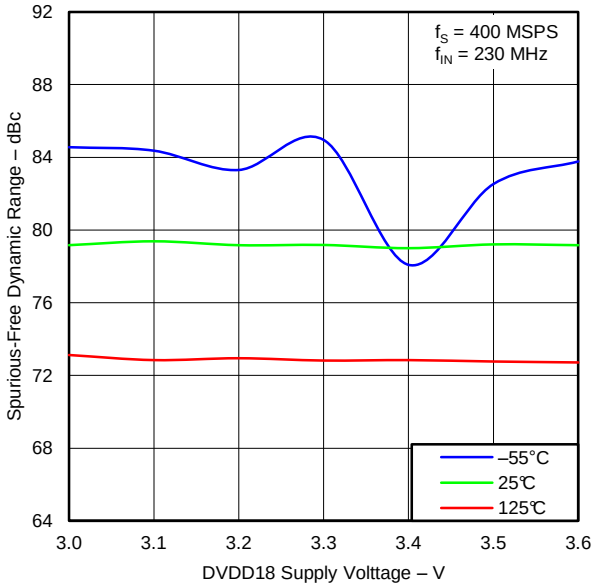


Figure 26.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, sampling rate = 400 MSPS, 50% clock duty cycle, 3-V_{PP} differential sinusoidal clock, analog input amplitude = –1 dBFS, AVDD5 = 5 V, AVDD3 = 3.3 V, and DVDD3 = 3.3 V, unless otherwise noted.

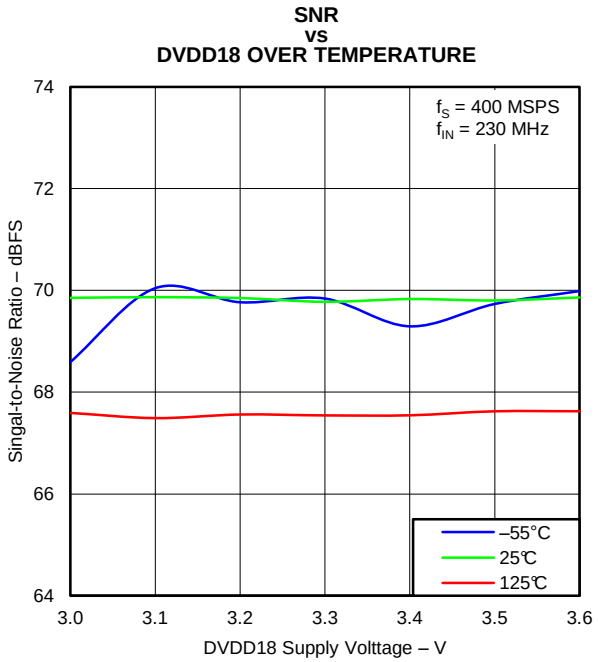


Figure 27.

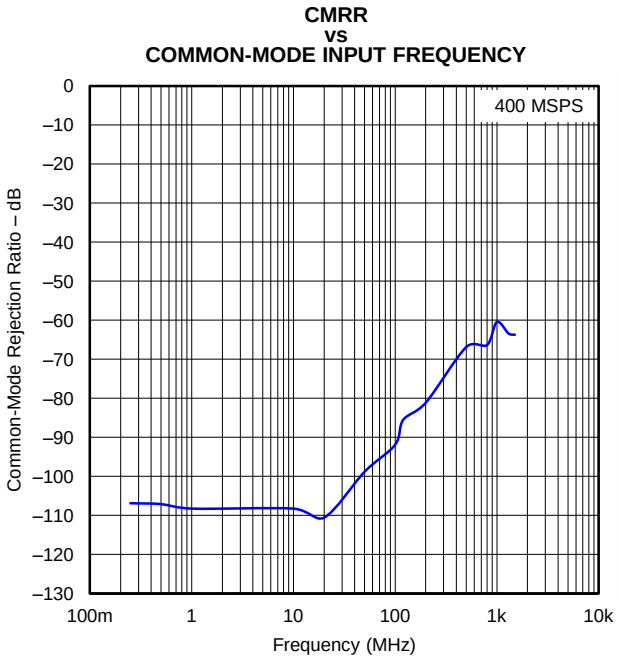


Figure 28.

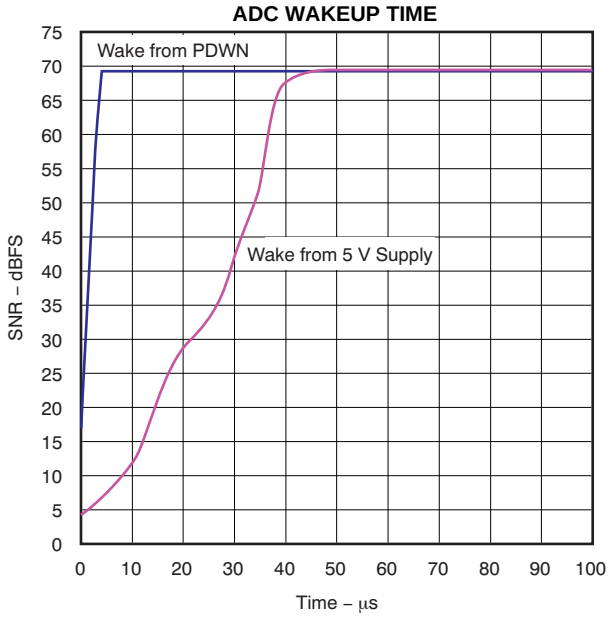


Figure 29.

APPLICATIONS INFORMATION

Theory of Operation

The ADS5474 is a 14-bit, 400-MSPS, monolithic pipeline ADC. Its bipolar analog core operates from 5-V and 3.3-V supplies, while the output uses a 3.3-V supply to provide LVDS-compatible outputs. The conversion process is initiated by the rising edge of the external input clock. At that instant, the differential input signal is captured by the input track-and-hold (T&H), and the input sample is converted sequentially by a series of lower resolution stages, with the outputs combined in a digital correction logic block. Both the rising and the falling clock edges are used to propagate the sample through the pipeline every half clock cycle. This process results in a data latency of 3.5 clock cycles, after which the output data are available as a 14-bit parallel word, coded in offset binary format.

Input Configuration

The analog input for the ADS5474 consists of an analog pseudo-differential buffer followed by a bipolar transistor T&H. The analog buffer isolates the source driving the input of the ADC from any internal switching and presents a high impedance that is easy to drive at high input frequencies, compared to an ADC without a buffered input. The input common-mode is set internally through a 500-Ω resistor connected from 3.1 V to each of the inputs (common-mode is ~2.4V on 12- and 13-bit members of this family). This configuration results in a differential input impedance of 1 kΩ.

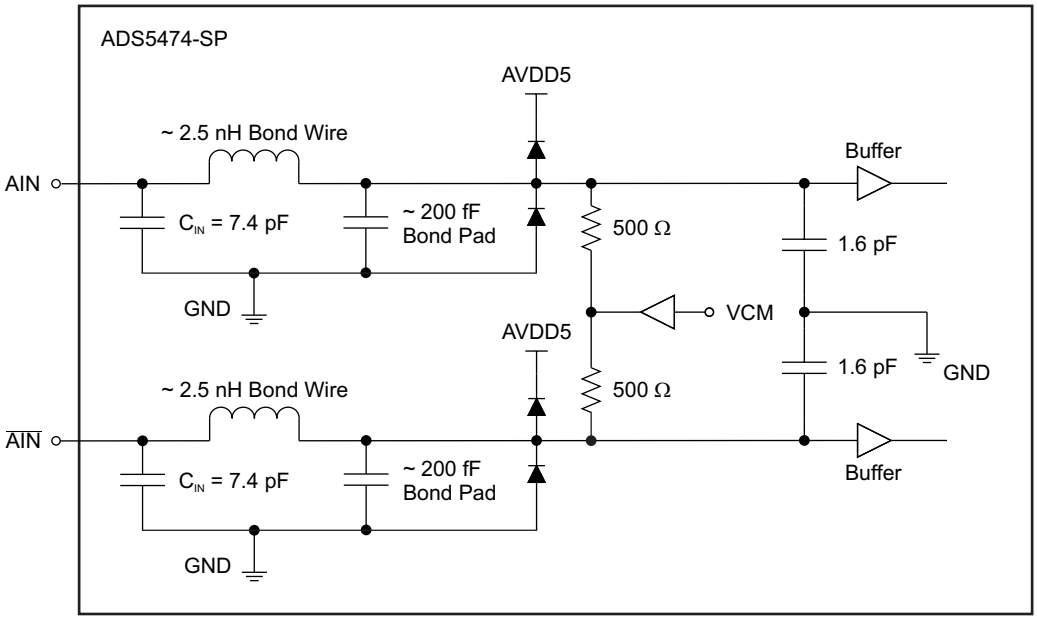


Figure 30. Analog Input Equivalent Circuit

For a full-scale differential input, each of the differential lines of the input signal (pins 16 and 17) swings symmetrically between (3.1 V + 0.55 V) and (3.1 V – 0.55 V). This range means that each input has a maximum signal swing of 1.1 V_{PP} for a total differential input signal swing of 2.2 V_{PP}. Operation below 2.2 V_{PP} is allowable, with the characteristics of performance versus input amplitude demonstrated in Figure 19 and Figure 20. For instance, for performance at 1.1 V_{PP} rather than 2.2 V_{PP}, refer to the SNR and SFDR at –6 dBFS (0 dBFS = 2.2 V_{PP}). The maximum swing is determined by the internal reference voltage generator, eliminating the need for any external circuitry for this purpose.

The ADS5474 performs optimally when the analog inputs are driven differentially. The circuit in Figure 31 shows one possible configuration using an RF transformer with termination either on the primary or on the secondary of the transformer. In addition, the evaluation module is configured with two back-to-back transformers, also demonstrating good performance. If voltage gain is required, a step-up transformer can be used.

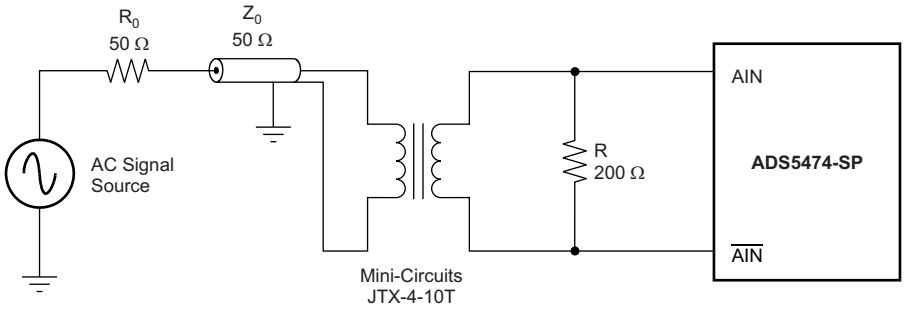


Figure 31. Converting a Single-Ended Input to a Differential Signal Using an RF Transformer

In addition to the transformer configurations, Texas Instruments offers a wide selection of single-ended operational amplifiers that can be selected depending on the application. An RF gain-block amplifier, such as Texas Instruments' THS9001, can also be used for high-input-frequency applications. For large voltage gains at intermediate-frequencies in the 50 MHz to 400 MHz range, the configuration shown in Figure 32 can be used. The component values can be tuned for different intermediate frequencies. The example shown in Figure 32 is located on the evaluation module and is tuned for an IF of 170 MHz. More information regarding this configuration can be found in the *ADS5474 EVM User Guide* (SLAU194) and the *THS9001 50-MHz to 350-MHz Cascadeable Amplifier* data sheet (SLOS426), both available for download at www.ti.com.

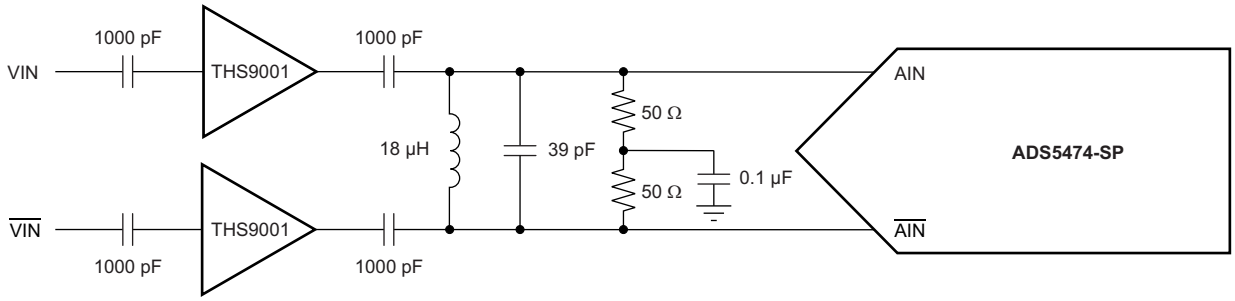


Figure 32. Using the THS9001 IF Amplifier With the ADS5474

For applications requiring dc-coupling with the signal source, a differential input/differential output amplifier such as the THS4509 (shown in Figure 33) provides good harmonic performance and low noise over a wide range of frequencies.

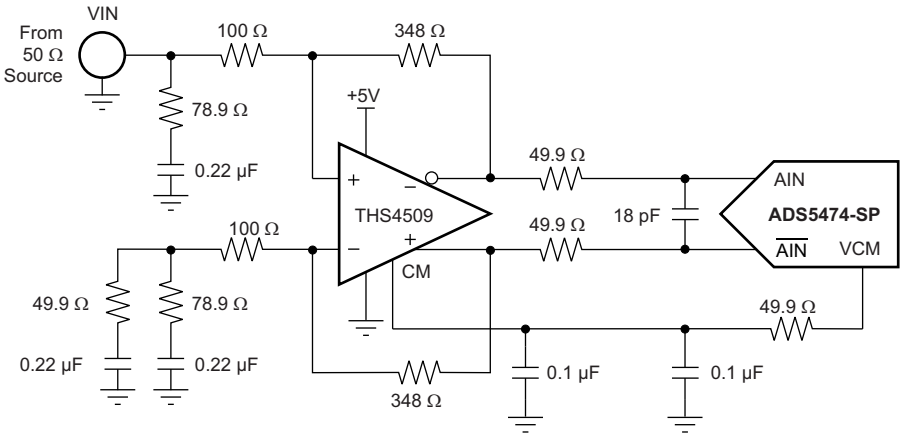


Figure 33. Using the THS4509 or THS4520 With the ADS5474

In this configuration, the THS4509 amplifier circuit provides 10 dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5474 by utilizing the VCM output pin of the ADC. The 50-Ω resistors and 18-pF capacitor between the THS4509 outputs and ADS5474 inputs (along with the input capacitance of the ADC) limit the bandwidth of the signal to about 70 MHz (–3 dB). Input termination is accomplished via the 78.9-Ω resistor and 0.22-µF capacitor to ground, in conjunction with the input impedance of the amplifier circuit. A 0.22-µF capacitor and 49.9-Ω resistor are inserted to ground across the 78.9-Ω resistor and 0.22-µF capacitor on the alternate input to balance the circuit. Gain is a function of the source impedance, termination, and 348-Ω feedback resistor. See the THS4509 data sheet for further component values to set proper 50-Ω termination for other common gains. Because the ADS5474 recommended input common-mode voltage is 3.1 V, the THS4509 operates from a single power-supply input with V_{S+} = 5 V and $V_{S–}$ = 0 V (ground). This configuration has the potential to slightly exceed the recommended output voltage from the THS4509 of 3.6V due to the ADC input common-mode of 3.1V and the +0.55V full-scale signal. This will not harm the THS4509 but may result in a degradation in the harmonic performance of the THS4509. An amplifier with a wider recommended output voltage range is the THS4520, which is optimized for low noise and low distortion in the range of frequencies up to ~20 MHz. Applications that are not sensitive to harmonic distortion could consider either device at higher frequencies.

Clock Inputs

The ADS5474 clock input can be driven with either a differential clock signal or a single-ended clock input. The characterization of the ADS5474 is typically performed with a 3-V_{PP} differential clock, but the ADC performs well with a differential clock amplitude down to ~0.5 V_{PP}, as shown in . The clock amplitude becomes more of a factor in performance as the analog input frequency increases. In low-input-frequency applications, where jitter may not be a big concern, the use of a single-ended clock could save cost and board space without much performance tradeoff. When clocked with this configuration, it is best to connect $\overline{CLK}$ to ground with a 0.01-µF capacitor, while CLK is ac-coupled with a 0.01-µF capacitor to the clock source, as shown in Figure 35.

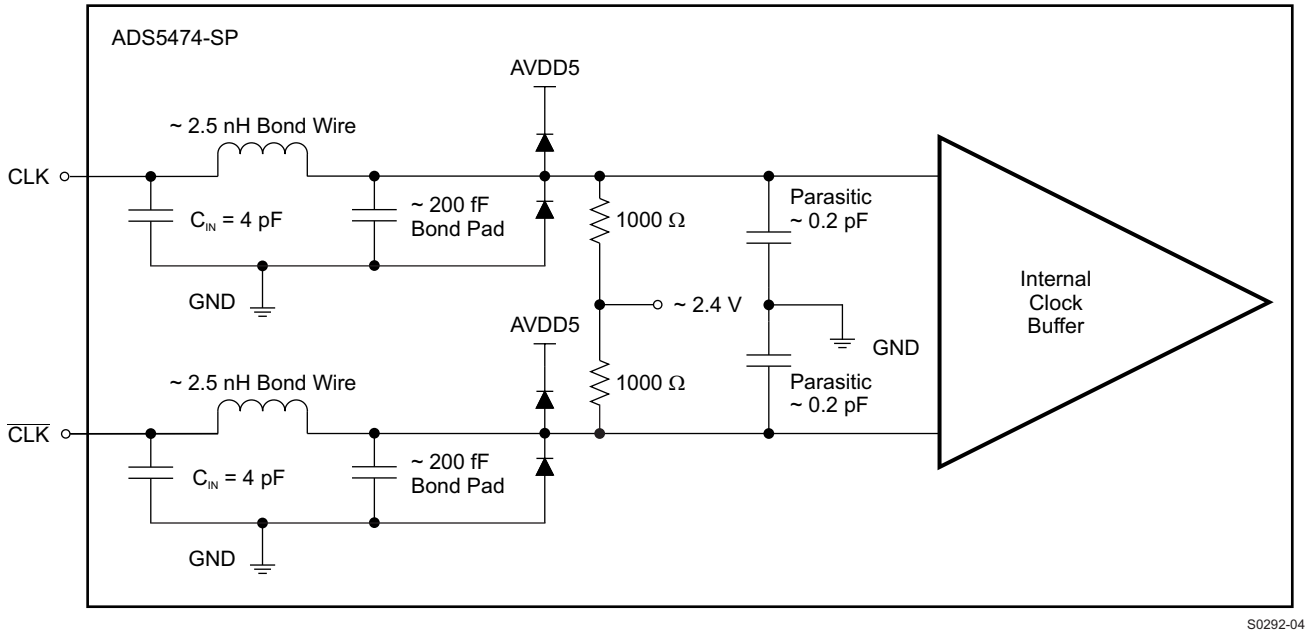


Figure 34. Clock Input Circuit

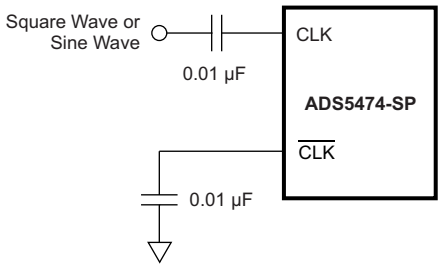


Figure 35. Single-Ended Clock

For jitter-sensitive applications, the use of a differential clock has some advantages at the system level. The differential clock allows for common-mode noise rejection at the printed circuit board (PCB) level. With a differential clock, the signal-to-noise ratio of the ADC is better for jitter-sensitive, high-frequency applications because the board level clock jitter is superior.

Larger clock amplitude levels are recommended for high analog input frequencies or slow clock frequencies. In the case of a sinusoidal clock, larger amplitudes result in higher clock slew rates and reduces the impact of clock noise on jitter. At high analog input frequencies, the sampling process is sensitive to jitter. And at slow clock frequencies, a small amplitude sinusoidal clock has a lower slew rate and can create jitter-related SNR degradation. Figure 36 demonstrates a recommended method for converting a single-ended clock source into a differential clock; it is similar to the configuration found on the evaluation board and was used for much of the characterization. See also *Clocking High Speed Data Converters* (SLYT075) for more details.

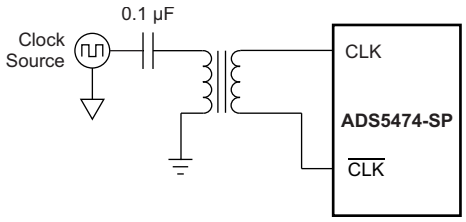


Figure 36. Differential Clock

The common-mode voltage of the clock inputs is set internally to 2.4 V using internal 1-kΩ resistors. It is recommended to use ac coupling, but if this scheme is not possible, the ADS5474 features good tolerance to clock common-mode variation. Additionally, the internal ADC core uses both edges of the clock for the conversion process. Ideally, a 50% duty-cycle clock signal should be provided.

The ADS5474 is capable of achieving 69.2 dBFS SNR at 350 MHz of analog input frequency. In order to achieve the SNR at 350 MHz the clock source rms jitter must be at least 144 fsec in order for the total rms jitter to be 177 fsec. A summary of maximum recommended rms clock jitter as a function of analog input frequency is provided in Table 2. The equations used to create the table are also presented.

Table 2. Recommended RMS Clock Jitter

INPUT FREQUENCY (MHz)	MEASURED SNR (dBc)	TOTAL JITTER (fsec rms)	MAXIMUM CLOCK JITTER (fsec rms)
30	69.3	1818	1816
70	69.1	798	791
130	69.1	429	417
230	68.8	251	229
350	68.2	177	144
450	67.4	151	110
750	65.6	111	42
1000	63.7	104	14

Equation 1 and Equation 2 are used to estimate the required clock source jitter.

$$SNR\ (dBc) = -20 \times LOG10\ (2 \times \pi \times f_{IN} \times j_{TOTAL}) \quad (1)$$

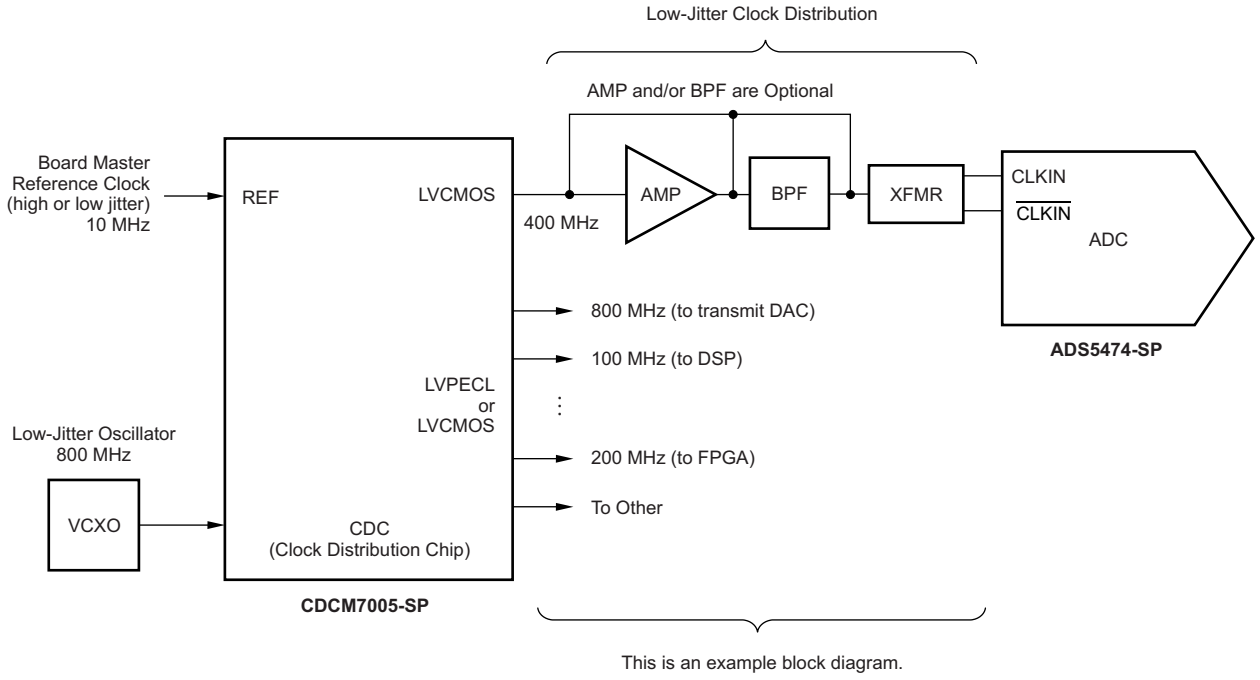
$$j_{TOTAL} = (j_{ADC}^{2} + j_{CLOCK}^{2})^{1/2} \quad (2)$$

where:

j_{TOTAL} = the rms summation of the clock and ADC aperture jitter;
j_{ADC} = the ADC internal aperture jitter which is located in the data sheet;
j_{CLOCK} = the rms jitter of the clock at the clock input pins to the ADC; and
f_{IN} = the analog input frequency.

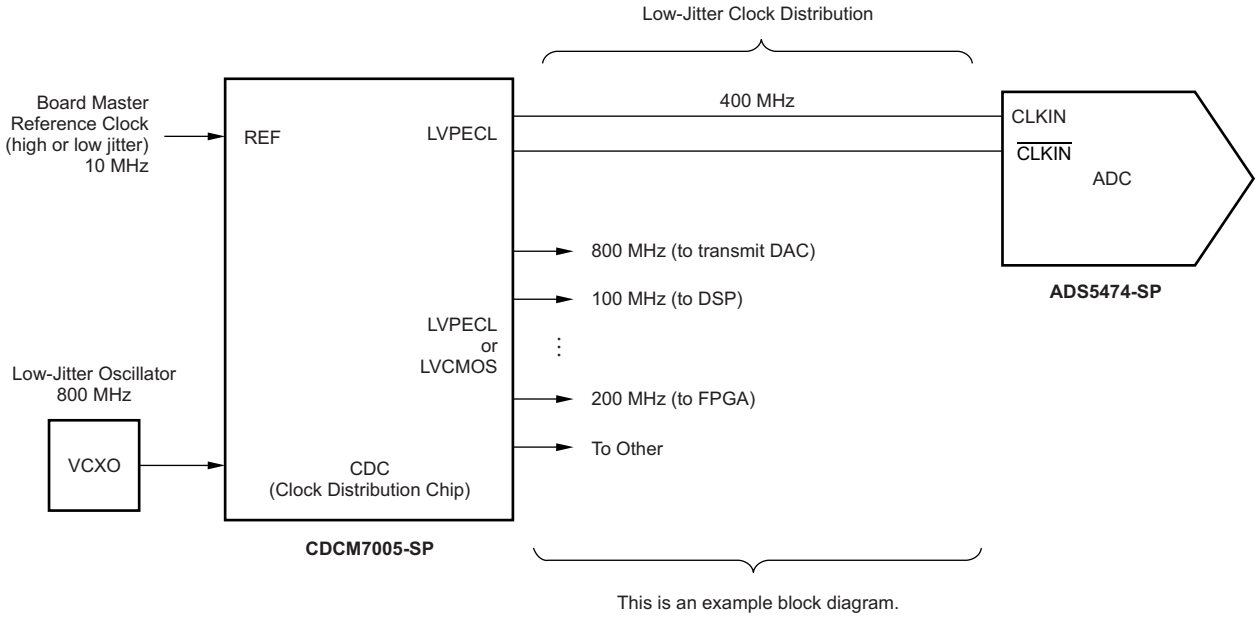
Notice that the SNR is a strong function of the analog input frequency, not the clock frequency. The slope of the clock source edges can have a mild impact on SNR as well and is not taken into account for these estimates. For this reason, maximizing clock source amplitudes at the ADC clock inputs is recommended, though not required (faster slope is desirable for jitter-related SNR). For more information on clocking high-speed ADCs, see Application Note SLWA034, *Implementing a CDC7005 Low Jitter Clock Solution For High-Speed, High-IF ADC Devices*, on the Texas Instruments web site. Recommended clock distribution chips (CDCs) are the TI CDC7005, the CDCM7005-SP and CDCE72010. Depending on the jitter requirements, a band pass filter (BPF) is sometimes required between the CDC and the ADC. If the insertion loss of the BPF causes the clock amplitude to be too low for the ADC, or the clock source amplitude is too low to begin with, an inexpensive amplifier can be placed between the CDC and the BPF.

Figure 37 represents a scenario where an LVCMOS single-ended clock output is used from a TI CDCM7005-SP with the clock signal path optimized for maximum amplitude and minimum jitter. This type of conditioning might generally be well-suited for use with greater than 150 MHz of input frequency. The jitter of this setup is difficult to estimate and requires a careful phase noise analysis of the clock path. The BPF (and possibly a low-cost amplifier because of insertion loss in the BPF) can improve the jitter between the CDC and ADC when the jitter provided by the CDC is still not adequate. The total jitter at the CDCM7005-SP output depends largely on the phase noise of the VCXO selected, as well as the CDCM7005-SP, and typically has 50–100 fs of rms jitter. If it is determined that the jitter from the CDCM7005-SP with a VCXO is sufficient without further conditioning, it is possible to clock the ADS5474 directly from the CDCM7005-SP using differential LVPECL outputs, as illustrated in Figure 38 (see the CDCM7005-SP data sheet for the exact schematic). This scenario may be more suitable for less than 150 MHz of input frequency where jitter is not as critical. A careful analysis of the required jitter is recommended before determining the proper approach.



Consult the CDCM7005 data sheet for proper schematic and specifications regarding allowable input and output frequency and amplitude ranges.

Figure 37. Optimum Jitter Clock Circuit



Consult the CDCM7005 data sheet for proper schematic and specifications regarding allowable input and output frequency and amplitude ranges.

Figure 38. Acceptable Jitter Clock Circuit

Digital Outputs

The ADC provides 14 LVDS-compatible, offset binary data outputs (D13 to D0; D13 is the MSB and D0 is the LSB), a data-ready signal (DRY), and an over-range indicator (OVR). It is recommended to use the DRY signal to capture the output data of the ADS5474. DRY is source-synchronous to the DATA/OVR outputs and operates at the same frequency, creating a half-rate DDR interface that updates data on both the rising and falling edges of DRY. It is recommended that the capacitive loading on the digital outputs be minimized. Higher capacitance shortens the data-valid timing window. The values given for timing (see Figure 2) were obtained with a measured 10-pF parasitic board capacitance to ground on each LVDS line (or 5-pF differential parasitic capacitance). When setting the time relationship between DRY and DATA at the receiving device, it is generally recommended that setup time be maximized, but this partially depends on the setup and hold times of the device receiving the digital data (like an FPGA or Field Programmable Field Array). Since DRY and DATA are coincident, it will likely be necessary to delay either DRY or DATA such that setup time is maximized.

Referencing Figure 2, the polarity of DRY with respect to the sample N data output transition is undetermined because of the unknown startup logic level of the clock divider that generates the DRY signal (DRY is a frequency divide-by-two of CLK). Either the rising or the falling edge of DRY will be coincident with sample N and the polarity of DRY could invert when power is cycled off/on or when the power-down pin is cycled. Data capture from the transition and not the polarity of DRY is recommended, but not required. If the synchronization of multiple ADS5474 devices is required, it might be necessary to use a form of the CLKIN signal rather than DRY to capture the data.

The DRY frequency is identical on the ADS5474 and ADS5463 (where DRY equals ½ the CLK frequency), but different than it is on the pin-similar ADS5444 (where DRY equals the CLK frequency). The LVDS outputs all require an external 100-Ω load between each output pair in order to meet the expected LVDS voltage levels. For long trace lengths, it may be necessary to place a 100-Ω load on each digital output as close to the ADS5474 as possible and another 100-Ω differential load at the end of the LVDS transmission line to provide matched impedance and avoid signal reflections. The effective load in this case reduces the LVDS voltage levels by half.

The OVR output equals a logic high when the 14-bit output word attempts to exceed either all 0s or all 1s. This flag is provided as an indicator that the analog input signal exceeded the full-scale input limit of approximately 2.2 V_{PP} (± gain error). The OVR indicator is provided for systems that use gain control to keep the analog input signal within acceptable limits.

Power Supplies

The ADS5474 uses three power supplies. For the analog portion of the design, a 5-V and 3.3-V supply (AVDD5 and AVDD3) are used, while the digital portion uses a 3.3-V supply (DVDD3). The use of low-noise power supplies with adequate decoupling is recommended. Linear supplies are preferred to switched supplies; switched supplies tend to generate more noise components that can be coupled to the ADS5474. The user may be able to supply power to the device with a less-than-ideal supply and still achieve good performance. It is not possible to make a single recommendation for every type of supply and level of decoupling for all systems. The power consumption of the ADS5474 does not change substantially over clock rate or input frequency as a result of the architecture and process.

Because there are two diodes connected in reverse between AVDD3 and DVDD3 internally, a power-up sequence is recommended. When there is a delay in power up between these two supplies, the one that lags could have current sinking through an internal diode before it powers up. The sink current can be large or small depending on the impedance of the external supply and could damage the device or affect the supply source.

The best power up sequence is one of the following options (regardless of when AVDD5 powers up):

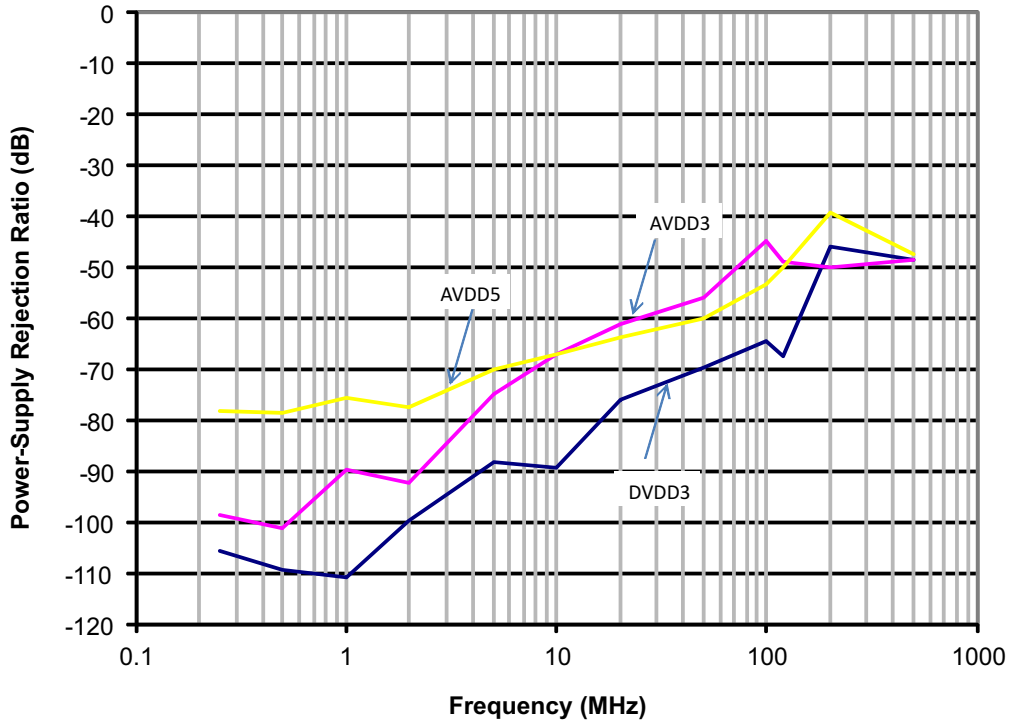
1) Power up both AVDD3 and DVDD3 at the same time (best scenario), OR

2) Keep the voltage difference less than 0.8V between AVDD3 and DVDD3 during the power up (0.8V is not a hard specification - a smaller delta between supplies is safer).

If the above sequences are not practical then the sink current from the supply needs to be controlled or protection added externally. The max transient current (on the order of µsec) for DVDD3 or AVDD3 pin is 500mA to avoid potential damage to the device or reduce its lifetime.

Values for analog and clock input given in the Absolute Maximum Ratings are valid when the supplies are on. When the power supplies are off and the clock or analog inputs are still alive, the input voltage and current needs to be limited to avoid device damage. If the ADC supplies are off, the max/min continuous DC voltage is +/- 0.95 V and max DC current is 20 mA for each input pin (clock or analog), relative to ground.

Figure 39. PSRR vs Supply Injected Frequency



DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

Aperture Delay

The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Clock Pulse Duration/Duty Cycle

The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse duration) to the period of the clock signal, expressed as a percentage.

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. DNL is the deviation of any single step from this ideal value, measured in units of LSB.

Common-Mode Rejection Ratio (CMRR)

CMRR measures the ability to reject signals that are presented to both analog inputs simultaneously. The injected common-mode frequency level is translated into dBFS, the spur in the output FFT is measured in dBFS, and the difference is the CMRR in dB.

Effective Number of Bits (ENOB)

ENOB is a measure in units of bits of converter performance as compared to the theoretical limit based on quantization noise:

$$ENOB = (SINAD - 1.76)/6.02 \quad (3)$$

Gain Error

Gain error is the deviation of the ADC actual input full-scale range from its ideal value, given as a percentage of the ideal input full-scale range.

Integral Nonlinearity (INL)

INL is the deviation of the ADC transfer function from a best-fit line determined by a least-squares curve fit of that transfer function. The INL at each analog input value is the difference between the actual transfer function and this best-fit line, measured in units of LSB.

Offset Error

Offset error is the deviation of output code from mid-code when both inputs are tied to common-mode.

Power-Supply Rejection Ratio (PSRR)

PSRR is a measure of the ability to reject frequencies present on the power supply.

The injected frequency level is translated into dBFS, the spur in the output FFT is measured in dBFS, and the difference is the PSRR in dB. The measurement calibrates out the benefit of the board supply decoupling capacitors.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and in the first five harmonics.

$$SNR = 10\log_{10}\frac{P_S}{P_N} \quad (4)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10\log_{10}\frac{P_S}{P_N + P_D} \quad (5)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Temperature Drift

Temperature drift (with respect to gain error and offset error) specifies the change from the value at the nominal temperature to the value at T_{MIN} or T_{MAX}. It is computed as the maximum variation the parameters over the whole temperature range divided by $T_{MIN} - T_{MAX}$.

Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental (P_S) to the power of the first five harmonics (P_D).

$$THD = 10\log_{10}\frac{P_S}{P_D} \quad (6)$$

THD is typically given in units of dBc (dB to carrier).

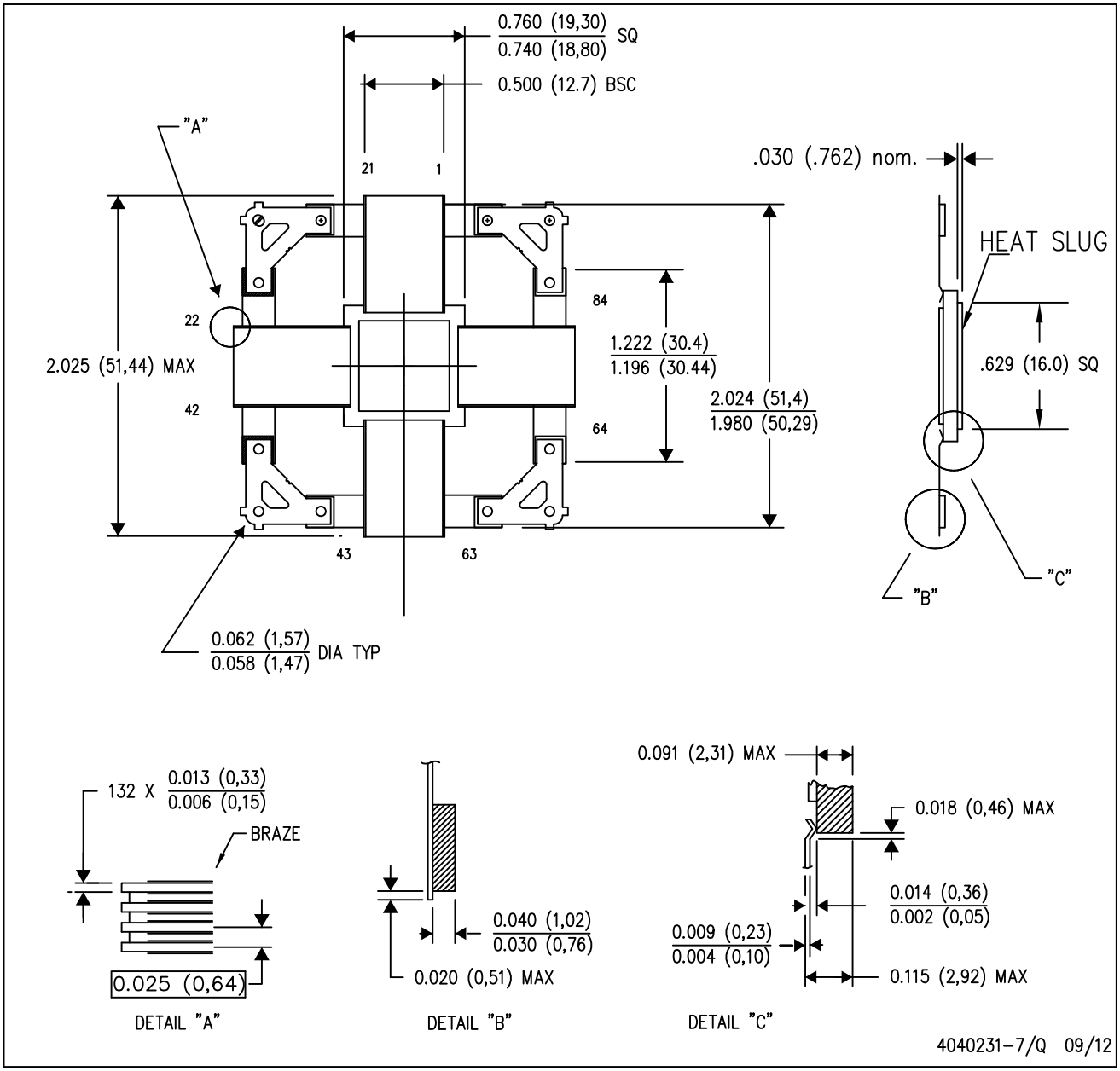
Two-Tone Intermodulation Distortion (IMD3)

IMD3 is the ratio of the power of the fundamental (at frequencies f_1, f_2) to the power of the worst spectral component at either frequency $2f_1 - f_2$ or $2f_2 - f_1$). IMD3 is given in units of either dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

REVISION HISTORY

Changes from Original (September 2013) to Revision A	Page
• Added /EM bullet to FEATURES section	1

HFG (S–CQFP–F84) CERAMIC QUAD FLATPACK WITH NCTB



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to non–conductive tie bar carrier.
D. This package is hermetically sealed with a metal lid.
E. The leads are gold plated and can be solderdipped.
F. Leads not shown for clarity purposes.

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