2.5MHz, Synchronous Boost Regulator

General Description

The RT4803A allows systems to take advantage of new battery chemistries that can supply significant energy when the battery voltage is lower than the required voltage for system power ICs. By combining built-in power transistors, synchronous rectification, and low supply current; this IC provides a compact solution for systems using advanced Li-Ion battery chemistries.

The RT4803A is a boost regulator designed to provide a minimum output voltage from a single-cell Li-Ion battery, even when the battery voltage is below system minimum. In boost mode, output voltage regulation is guaranteed to a maximum load current of 2000mA. Quiescent current in shutdown mode is less than 1μA, which maximizes battery life. The regulator transitions smoothly between bypass and normal boost mode. The device can be forced into bypass mode to reduce quiescent current.

The RT4803A is available in the WL-CSP-16B 1.67x1.67 (BSC) package.

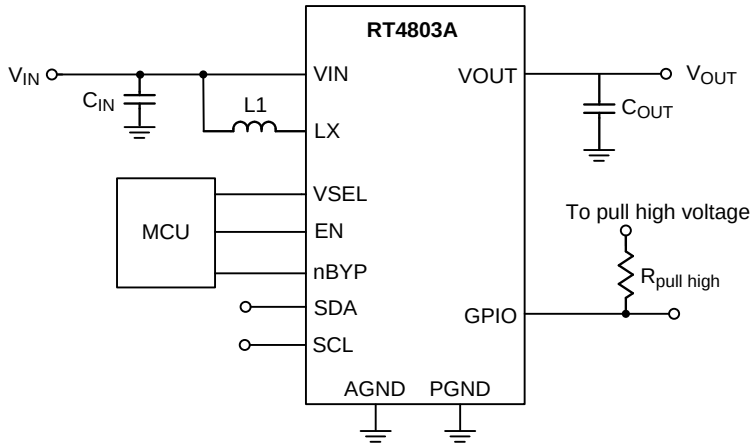
Applications

- Single-Cell Li-Ion, LiFePO4 Smart-Phones or Tablet
- 2.5G/3G/4G Mini-Module Data Cards

Features

- **Input Voltage Range : 1.8V to 5V**
- **Programmable Output Voltage from 2.85V to 4.4V with 50mV/Step**
- **Default Boost Output Voltage Setting :**
  - **V_{OUT} = 3.4V at VSEL = H**
  - **V_{OUT} = 3.15V at VSEL = L**
- **Maximum Continuous Load Current : 2A at V_{IN} > 2.65V Boosting V_{OUT} to 3.35V**
- **Up to 95% Efficiency**
- **nBYP (L) : Forced Bypass Mode**
- **nBYP (H) : Auto Bypass Operation when V_{IN} > Target V_{OUT}**
- **Internal Synchronous Rectifier**
- **Over-Current Protection**
- **Under-Voltage Protection**
- **Over-Voltage Protection**
- **Over-Temperature Protection**
- **Ultra Low Operating Quiescent Current**
- **Discharge Function Trigger at GPIO Manual Pull Low**
- **Available in a WL-CSP-16B 1.67x1.67 (BSC) Package**

Simplified Application Circuit



Ordering Information

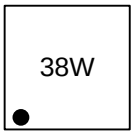
RT4803A □
└Package Type
WSC : WL-CSP-16B 1.67x1.67 (BSC)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

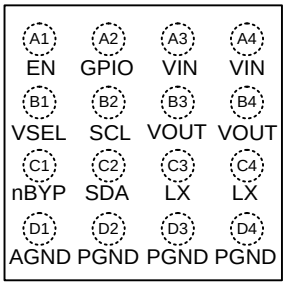
Marking Information



38 : Product Code
W : Date Code

Pin Configuration

(TOP VIEW)

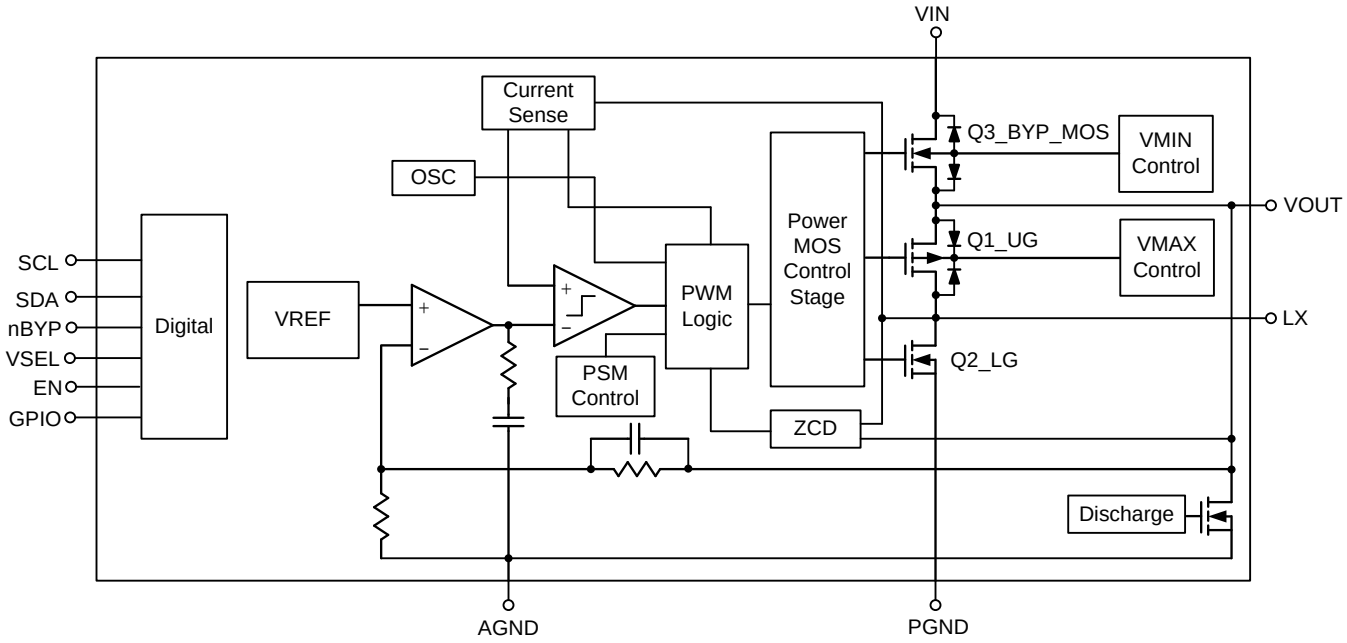


WL-CSP-16B 1.67x1.67 (BSC)

Functional Pin Description

Pin No.	Pin Name	I/O	Pin Function
A1	EN	I	Chip enable input pin. High level voltage enables the device while low level voltage turns the device off. This pin must be terminated.
A2	GPIO	I/O	General purpose input/output. (Detail illustrate as operation section)
A3, A4	VIN	I	Power supply input.
B1	VSEL	I	Output voltage selection pin. Default boost output voltage setting V_{OUT} = 3.4V at VSEL = H and V_{OUT} = 3.15V at VSEL = L. This pin must be terminated.
B2	SCL	I	Serial interface clock. (Pull down if I^2C is non-used).
B3, B4	VOUT	O	Boost output voltage pin. PCB trace length from BSTVOUT to the output filter capacitor should be as short and wide as possible.
C1	nBYP	I	This pin can be used to activate forced bypass mode. When this pin is LOW, the bypass switches are turned on into forced bypass mode. Detail mode define as Table 1 discussion.
C2	SDA	I/O	Serial interface date line. (Pull down if I^2C is non-used)
C3, C4	LX	I/O	This pin is the connection between two build-in switches in the chip, which should be connected to the external inductor. The inductor should be connected to this pin with the shortest path.
D1	AGND	--	Analog ground. This is the signal ground reference for the IC.
D2, D3, D4	PGND	--	Power ground should be connected to this pin with the shortest path for power transmission to reduce parasitic component effect.

Functional Block Diagram



Operation

The RT4803A combined built-in power transistors, synchronous rectification, and low supply current, it provides a compact solution for system using advanced Li-Ion battery chemistries.

In boost mode, output voltage regulation is guaranteed to maximum load current of 2000mA. Quiescent current in Shutdown mode is less than 1μA, which maximizes battery life.

Under-Voltage Lockout

The under-voltage lockout circuit prevents the device from operating incorrectly at low input voltages. It prevents the converter from turning on the power switches under undefined conditions. V_{IN} voltage must be greater than UVLO rising threshold to enable the converter. During operation, if V_{IN} voltage drops below UVLO falling threshold, the converter is disabled until the supply exceeds the UVLO rising threshold. The RT4803A automatically restarts if the input voltage recovers to the input voltage UVLO high level.

EN and nBYP

It is used to select mode. As the Table 1 shown, there are four device states. When both EN and nBYP pull low. It enters forced bypass mode with low quiescent mode (4μA). When the EN pull low and nBYP pull high, it is shutdown mode and quiescent current is less than 1uA. It works in forced bypass without low quiescent mode, if the EN pulled high and nBYP pulled low. When EN and nBYP both pull high, the RT4803A is boost and auto bypass mode. There should be a delay time (> 60μs) from EN pull high to nBYP pull high to guarantee normal operation.

Table 1

EN Input	nBYP Input	Mode Define	Device State
0	0	Forced bypass with low quiescent mode	The device in forced bypass with low quiescent mode featuring a low quiescent current down to about 4μA (typ.).
0	1	Shutdown mode	The device is shutdown. The device shutdown current is approximately about 1μA (max).
1	0	Forced bypass without low quiescent mode	The device is active in forced bypass without low quiescent mode. The device supply current is approximately about 15μA (typ.).
1	1	Boost and auto bypass mode	The device includes boost and auto bypass mode depend on V_{IN} larger than V_{OUT} or not. The device supply current is approximately about 35μA (typ.) with auto bypass mode / 55μA (typ.) with boost mode.

Enable (nBYP = High Status)

The device can be enabled or disabled by the EN pin. When the EN pin is higher than the threshold of logic-high, the device starts operating follow Figure 2 operation diagram and Table 2 condition. In shutdown mode, the converter stops switching, internal control circuitry is turned off. The output voltage reduce by component consumption (Cap ESR...) that state have not discharge function. Discharge function only trigger with GPIO pull low status (Reg.0x01[3] setting 0).

Soft-Start State

During soft-start state, if V_{OUT} reach to 95% V_{OUT_Target}. The RT4803A will into boost operation. Otherwise count over 512μs then the RT4803A will into fault state.

Boost / Auto Bypass Mode

nBYP = H There are two normal operation modes, one is the boost mode, and the other one is auto bypass mode. In the boost mode, it provides the power to load by internal synchronous switches after the soft-start state. In the auto bypass mode, input voltage will pass through it to the output terminal directly. That can provide max current capacity with RT4803A. Detail description as below :

- **Boost Mode (Auto PFM/PWM Control Method)**

  In order to save power and improve efficiency at low loads, the Boost operate in PFM (Pulse Frequency Modulation) as the inductor drops into DCM (Discontinuous Current Mode). The switching frequency is proportional to loading to reach output voltage regulation. When load increases and inductor current becomes continuous again, the Boost automatically goes back to PWM (Pulse Width Modulation) fixed frequency mode.

- **Auto Bypass Mode**

  That control loop will auto transfer to auto bypass mode, if VIN increase higher than V_{OUT}. MOSFET Q3 will turn on and MOSFET Q1 and Q2 turn off synchronous. If the RT4803A into auto bypass mode MOSFET Q3 current limit is 4000mA (typ.) as shown in Figure 1.

Forced Bypass Mode

nBYP = L MOSFET Q3, turn on MOSFET Q1 and Q2 turn off input voltage will pass through it to the output terminal directly. If the RT4803A into forced bypass mode MOSFET Q3 current limit is 4000mA (typ.) as shown in Figure 1.

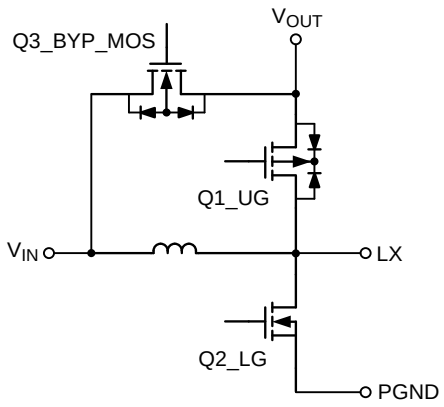


Figure 1. Boost Converter with Bypass Mode

LIN State

When V_{IN} > UVLO and EN low to High, output capacitor begins to be charged with linear startup until V_{IN} - V_{OUT} smaller than 300mV (typ.). Linear startup include LIN1 and LIN2 states. LIN1 pre-charge current is 1000mA (typ.) with 800μs duration and IC goes into LIN2 pre-charge with 2000mA (typ.) keeping 1600μs duration if V_{IN} - V_{OUT} is still larger than 300mV (typ.).

If V_{IN} - V_{OUT} smaller than 300mV, the RT4803A will into soft start operation after Linear startup (LIN1/2) states. Otherwise the RT4803A will into fault operation.

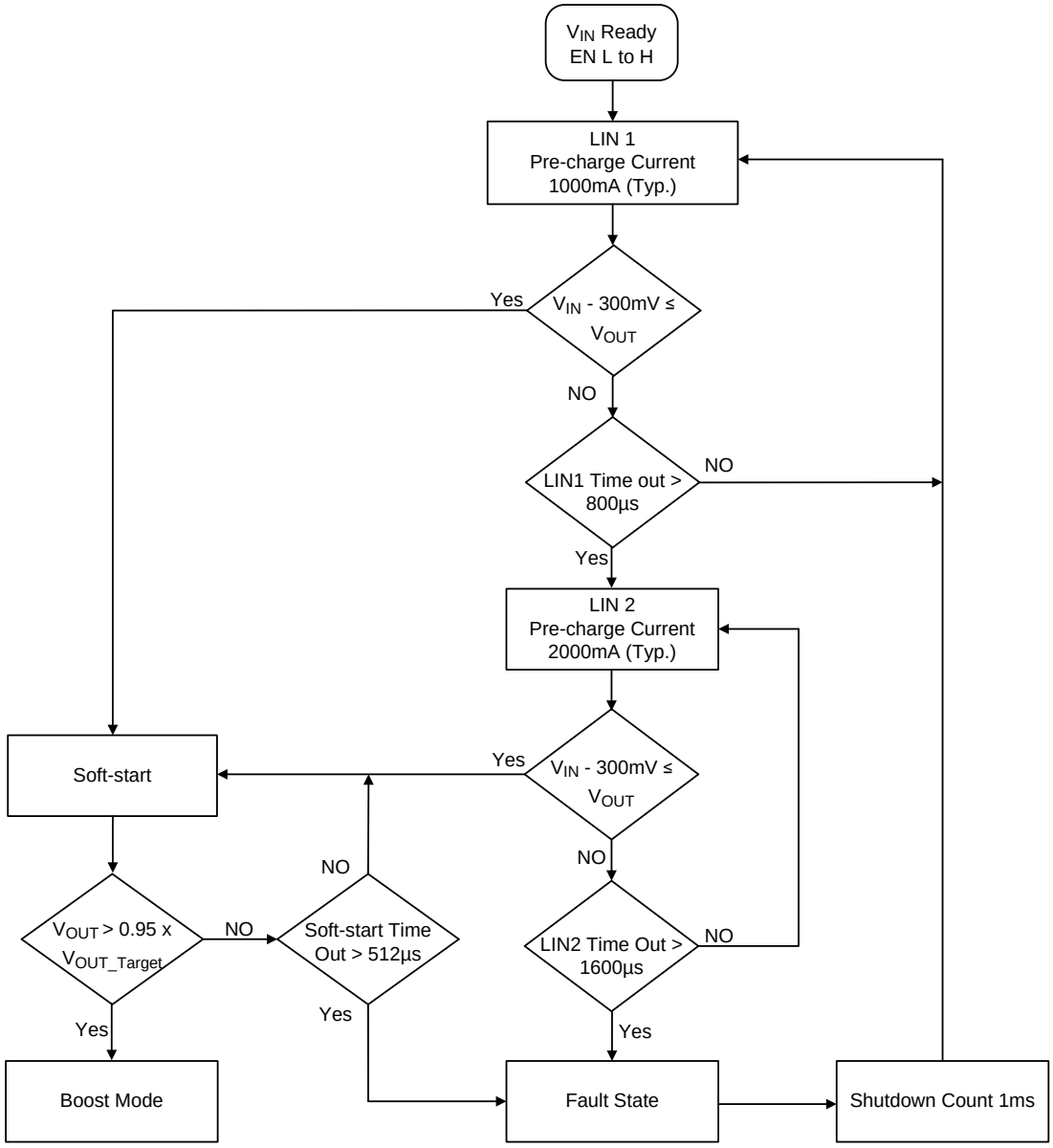


Figure 2. The RT4803A State Chart

Table 2

Mode	Description	Condition
LIN (Include LIN1/LIN2 states)	Linear startup 1	V_{IN} - 300mV ≥ V_{OUT}
	Linear startup 2	
Soft-Start	Boost soft-start	0.95 x V_{OUT_Target} > V_{OUT} ≥ V_{IN} - 300mV
Boost	Boost mode	V_{OUT_Target} ≥ 0.95 x V_{OUT_Target}
If V_{IN} increase higher than V_{OUT}		
Auto Bypass	Auto bypass mode	V_{IN} ≥ V_{OUT} Control loop auto transfer between auto bypass mode and boost mode.

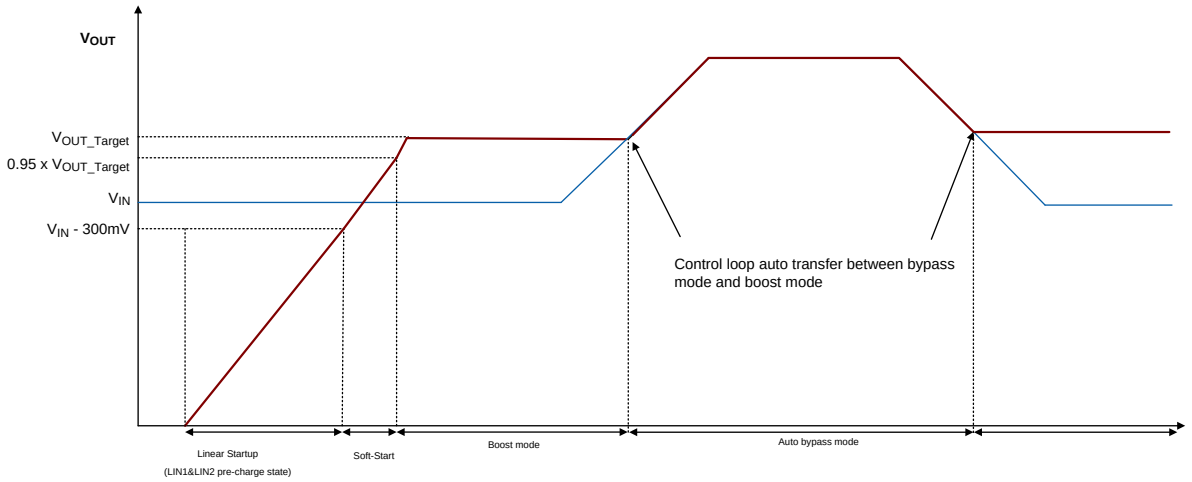


Figure 3. V_{OUT} Mode Transition Diagram with EN L to H and V_{IN} Variation (nBYP = H; I_O = 0A)

VSEL

In order to maintain a target minimum output voltage under worse application condition (ex : full load transient), the output voltage set point can be dynamically increased by asserting the VSEL input. The functionality also helps to mitigate undershoot during line transient of worse case.

The RT4803A VSEL = L output voltage default setting is 3.15V that can be programmed by Reg.0x02[4:0]. VSEL = H output voltage default setting is 3.4V that can be programmed by Reg.0x03[4:0].

GPIO

GPIO is arranged to be either a mode selection or nRST/nFAULT function. It be controlled by Reg.0x01[3]. GPIO port configuration bit.

- **Reg.0x01[3] setting 0 :**

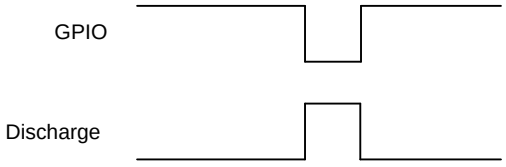
  GPIO supports manual reset input (nRST) and interrupt generation output (nFAULT).

  Fault output (open drain interrupt) : GPIO will pull low if the fault occurred

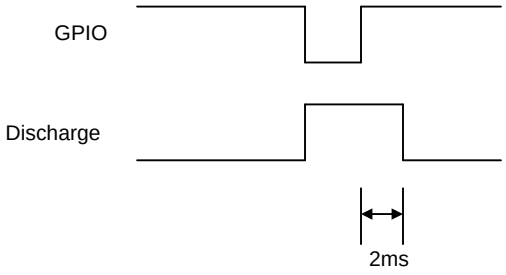
  Manual reset input : If GPIO manual toggle the RT4803A will restart as Figure 3 state chart.

  As the following figures shown, the RT4803A features the discharge function depends on Reg.0x01[3] setting 0. The function is released when GPIO goes high 2ms later in every modes but shut down mode.

  In shut down mode, it is released right away when GPIO goes high.



(a). In Shut down Mode (EN = 0, nBYP = 1)



(b). In Other Modes

Figure 4. Discharge Function Diagram

- **Reg.0x01[3] setting 1 :**

  It is an input of device mode selection.

  MODE_CTRL[1:0] in Register 0x01[1:0] set 2'b00, and GPIOCFG in Register 0x01[3] set 1'b1. GPIO pin must be configured as the mode selection input.

  GPIO pin set Low : Auto PFM/PWM operation

  GPIO pin set High : Forced PWM control operation

Current Limit

The RT4803A employs a valley-current limit detection scheme to sense inductor current during the off-time. When the loading current is increased such that the loading is above the valley current limit threshold, the off-time is increased until the current is decreased to valley-current threshold. Next on-time begins after current is decreased to valley-current threshold. On-time is decided by (V_{OUT} - V_{IN}) / V_{OUT} ratio. The output voltage decreases when further loading current increase. As the following figure shown, the current limit function is implemented by the scheme.

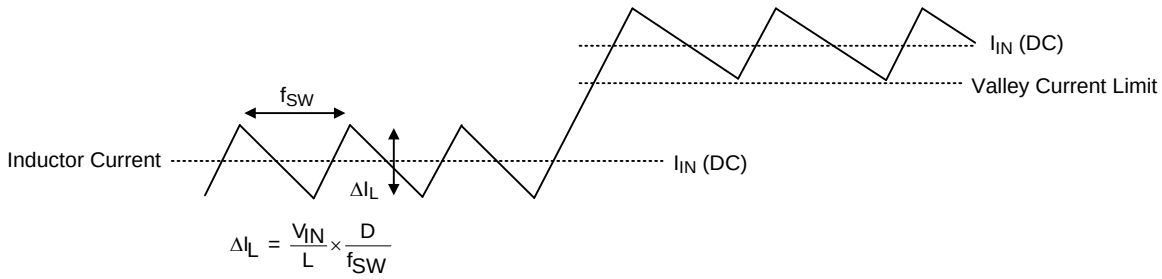


Figure 5. Inductor Currents in Current Limit Operation

OTP

The converter has an over-temperature protection. When the junction temperature is higher than the thermal shutdown rising threshold, the system will be latched and the output voltage will no longer be regulated until the junction temperature drops under the falling threshold.

OVP

The device does not operate with V_{IN} over the over-voltage protection (OVP) level (5.7V). There is a typical 100mV hysteresis implemented to avoid unstable on/off behavior. Input voltage increase higher than 5.7V, IC will shut down until voltage level reduce smaller than 5.6V, that device will recovery normal operation. OVP protection can avoid IC operate at abnormal input power and prevent to damage device.

UVP

Avoid large power dissipation to damage IC at abnormal operation or state. UVP protection has been employed to prevent this state. If V_{OUT} abnormal drop smaller than 80% V_{OUT}, IC goes into shutdown at fault signal trigger. After fault state count 1ms, IC will recovery operation until abnormal state remove.

Fault State

Fault state will trigger as below conditions :

1. Linear startup fail
2. Soft-start fail
3. UVP
4. OTP

If fault state occur, IC will goes into shut down with 1ms. After 1ms count complete, IC will restart. The state chart of the RT4803A is shown in Figure 2.

Protection

The RT4803A features some protections, such as OCP, OVP, UVLO, OTP and UVP. As the table shown, it is described the protection actions.

Protection Type	Threshold Refer to Electrical Spec.	Protection Method	Shut Down Delay Time	Reset Method
OCP	I_L > 4A	Turn on UG	Without shutdown behavior	I_L < 4A
OVP	V_{IN} > 5.7V	Turn off UG, LG, BYP_MOS	No delay	V_{IN} < 5.6V
UVLO	V_{IN} < 1.6V (max)	Turn off UG, LG, BYP_MOS	No delay	V_{IN} > 1.8V (max)
OTP	TEMP > 160°C	Turn off UG, LG, BYP_MOS	No delay	OTP Hysteresis = 20°C
UVP	V_{OUT} < 0.8 x V_{OUT_Target}	Turn off UG,LG, BYP_MOS	2ms	V_{OUT} > 0.8 x V_{OUT_Target}

Absolute Maximum Ratings (Note 1)

- EN, GPIO, VIN, VSEL, SCL, VOUT, nBYP, SDA, LX ---------- –0.2V to 6V
- LX (<200ns) ---------- –3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  WL-CSP-16B 1.67x1.67 (BSC) ---------- 2.09W
- Package Thermal Resistance (Note 2)

  WL-CSP-16B 1.67x1.67 (BSC), θ_{JA} ---------- 47.7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Input Voltage Range ---------- 1.8V to 5V
- Output Voltage Range ---------- 2.85V to 4.4V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 3V, V_{OUT} = 3.4V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN Operation Range	V_{IN}		1.8	--	5	V
Quiescent Current	I_Q	Auto Bypass Mode, V_{IN} = 3.8V	--	35	70	μA
		Boost mode, I_{LOAD} = 0mA, Switching, V_{IN} = 3V	--	55	100	
		Forced bypass with LIQ, V_{IN} = 3.6V	--	4	8	
		Forced bypass without LIQ, V_{IN} = 3.6V	--	15	25	
VIN Shutdown Current	I_{SHDN}	EN = 0V, nBYP = H, V_{IN} = 3.6V	--	--	1	μA
VOUT to VIN Reverse Leakage (Note 5)	I_{LK}	V_{OUT} = 5V, EN = nBYP = H, V_{IN} < V_{OUT}	--	0.2	1	μA
VOUT Leakage Current	I_{LK_OUT}	V_{OUT} = 0V, EN = 0V, V_{IN} = 4.2V	--	0.1	1	μA
VOUT Discharge Impedance	R_DIS_OUT		--	80	--	Ω
Under Voltage Lock Out	V_{UVLO}	V_{IN} Rising	--	1.6	1.8	V
Under Voltage Lock Out Hysteresis	V_{UVLO_HYS}		--	200	--	mV
GPIO Low	V_{GPIO}	I_{GPIO} = 5mA	--	--	0.4	V
GPIO Leakage Current	I_{GPIO_LK}	V_{GPIO} = 5V	--	--	1	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Logic Level High EN, VSEL, nBYP, GPIO	V_{IH}		1.2	--	--	V
Logic Level Low EN, VSEL, nBYP, GPIO	V_{IL}		--	--	0.4	V
Output Voltage Accuracy	$V_{OUT\_ACCURACY}$	$V_{OUT} - V_{IN}$ > 100mV, PWM	–2	--	2	%
Minimum On Time	T_{ON}	V_{IN} = 3V, V_{OUT} = 3.5V, I_{LOAD} > 1000mA	--	80	--	ns
Maximum Duty Cycle	D_{MAX}		40	--	--	%
Switching Frequency	f_{SW}	V_{IN} = 2.65V, V_{OUT} = 3.5V, I_{LOAD} = 1000mA	2	2.5	3	MHz
Boost Valley Current Limit	I_{CL}	V_{IN} = 2.9V	3.5	4	4.5	A
LIN1 Pre-Charge Current	I_{LIN1}		700	1000	1300	mA
LIN2 Pre-Charge Current	I_{LIN2}		1400	2000	2600	mA
Auto/Forced Bypass Current Limit	I_{BPCL}	V_{IN} = 3.2V	3	4	10	A
N-Channel Boost Switch $R_{DS(ON)}$ (UG)	R_{DSN}	V_{IN} = 3.2V, V_{OUT} = 3.5V	--	60	95	mΩ
P-Channel Boost Switch $R_{DS(ON)}$ (LG)	R_{DSP}	V_{IN} = 3.2V, V_{OUT} = 3.5V	--	40	80	mΩ
N-Channel Bypass Switch $R_{DS(ON)}$ (BYP_MOS)	R_{DSP_BYP}	V_{IN} = 3.2V, V_{OUT} = 3.5V	--	40	60	mΩ
Hot Die Trigger Threshold	T_{HD}	Boost mode	--	100	--	°C
Hot Die Release Threshold	T_{HDR}	Boost mode	--	90	--	°C
Over-Temperature Protection	T_{OTP}		--	160	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	20	--	°C
FAULT Restart Time	T_{RST}		--	1	--	ms

I^2C Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCL, SDA High-Level Input Threshold Voltage	V_{IH_I2C}		1.2	--	--	V
SCL, SDA Low-Level Input Threshold Voltage	V_{IL_I2C}		--	--	0.4	V
SDA Digital Output Low	V_{OL_I2C}		--	--	0.4	V
SCL Clock Frequency	f_{CLK}	Standard-mode	--	--	100	kHz
		Fast-mode	--	--	400	
		Fast-mode Plus	--	--	1000	
		High-speed mode Cb = 400pF	--	--	1.7	MHz
		High-speed mode Cb = 100pF	--	--	3.4	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Bus Free Time between Stop and Start Condition	t_{BUF}	Standard-mode	4.7	--	--	µs
		Fast-mode	1.3	--	--	
		Fast-mode Plus	0.5	--	--	
(Repeated) Start Hold Time	$t_{HD;STA}$	Standard-mode	4	--	--	µs
		Fast-mode	0.6	--	--	
		Fast-mode Plus	0.26	--	--	
		High-speed mode Cb = 400pF	160	--	--	
		High-speed mode Cb = 100pF	160	--	--	
(Repeated) Start Setup Time	$t_{SU;STA}$	Standard-mode	4.7	--	--	µs
		Fast-mode	0.6	--	--	
		Fast-mode Plus	0.26	--	--	
		High-speed mode Cb = 400 pF	160	--	--	ns
		High-speed mode Cb = 100 pF	160	--	--	
STOP Condition Setup Time	$t_{SU;STO}$	Standard-mode	4	--	--	µs
		Fast-mode	0.6	--	--	
		Fast-mode Plus	0.26	--	--	
		High-speed mode Cb = 400pF	160	--	--	ns
		High-speed mode Cb = 100pF	160	--	--	
SDA Data Hold Time	$t_{HD;DAT}$	Standard-mode	0.1	--	--	ns
		Fast-mode	0.1	--	--	
		Fast-mode Plus	0.1	--	--	
		High-speed mode Cb = 400pF	0.1	--	150	
		High-speed mode Cb = 100pF	0.1	--	70	
SDA Valid Acknowledge Time	$t_{VD;ACK}$	Standard-mode	--	--	3.45	µs
		Fast-mode	--	--	0.9	
		Fast-mode Plus	--	--	0.45	
SDA Setup Time	$t_{SU;DAT}$	Standard-mode	250	--	--	ns
		Fast-mode	100	--	--	
		Fast-mode Plus	50	--	--	
		High-speed mode Cb = 400pF	10	--	--	
		High-speed mode Cb = 100pF	10	--	--	
SCL Clock Low Time	t_{LOW}	Standard-mode	4.7	--	--	µs
		Fast-mode	1.3	--	--	
		Fast-mode Plus	0.5	--	--	
		High-speed mode Cb = 400pF	320	--	--	ns
		High-speed mode Cb = 100pF	160	--	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCL Clock High Time	t_{HIGH}	Standard-mode	4	--	--	µs
		Fast-mode	0.6	--	--	
		Fast-mode Plus	0.26	--	--	
		High-speed mode Cb = 400pF	120	--	--	ns
		High-speed mode Cb = 100pF	60	--	--	

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

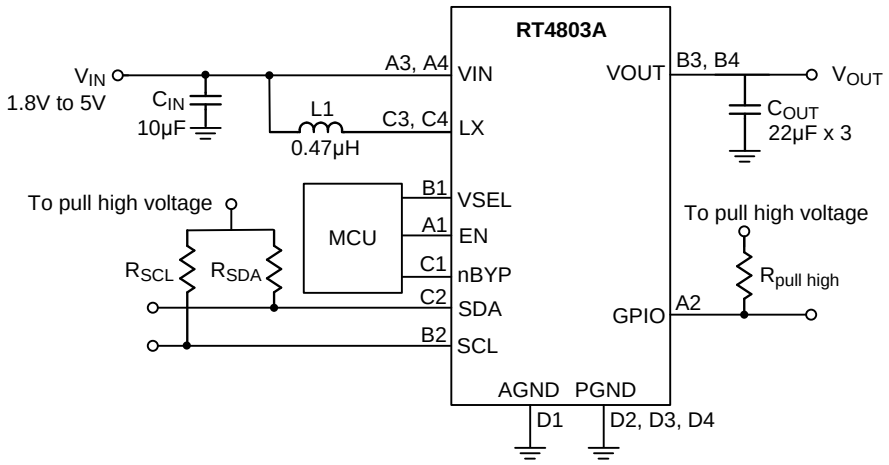
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. V_{OUT} can not connect external power source at any operation state.

Typical Application Circuit

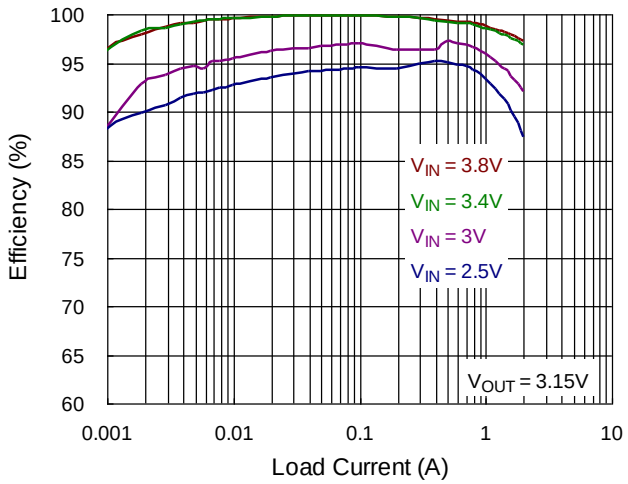


BOM of Test Board

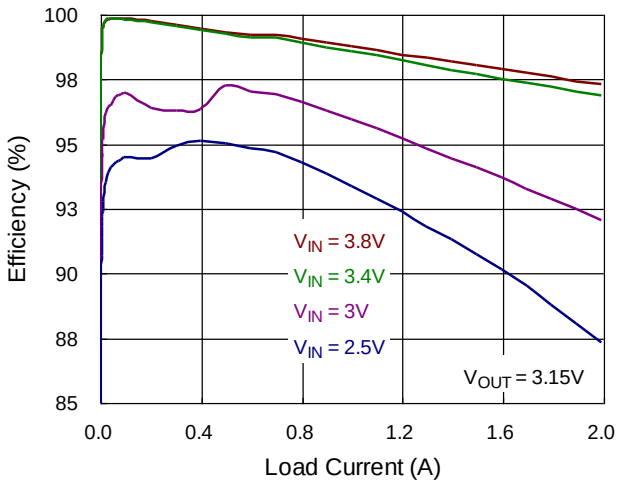
Reference	Part Number	Description	Package	Manufacturer
C_{IN}	GRM188R61A106KE69	10µF/10V/X5R	0603	Murata
C_{OUT}	GRM188R61A226ME15D	22µF/10V/X5R	0603	Murata
L1	DFE252012F-R47M=P2	0.47µH	2520	Murata

Typical Operating Characteristics

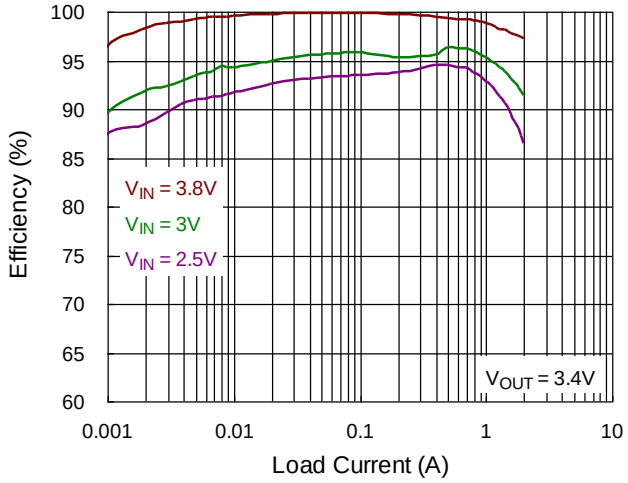
Efficiency vs. Load Current



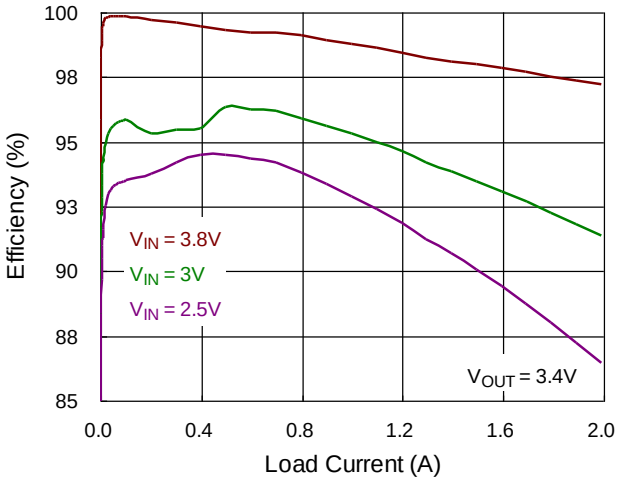
Efficiency vs. Load Current



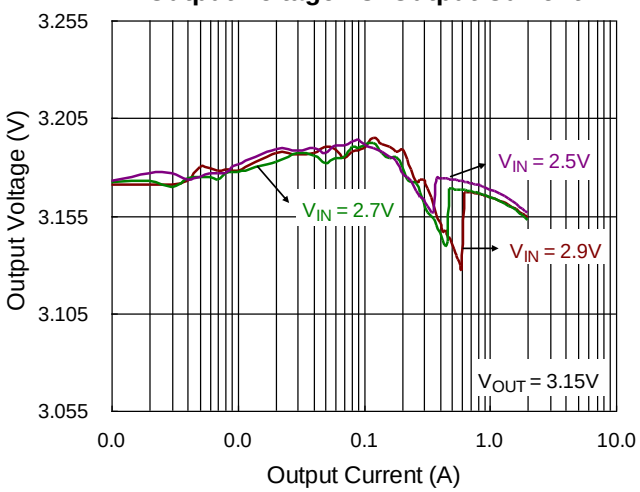
Efficiency vs. Load Current



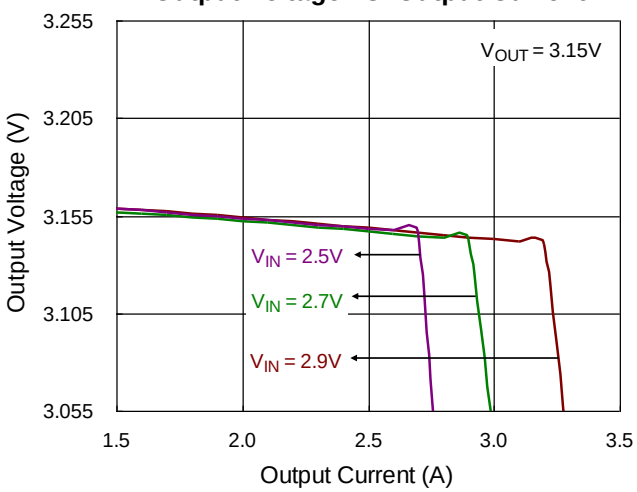
Efficiency vs. Load Current



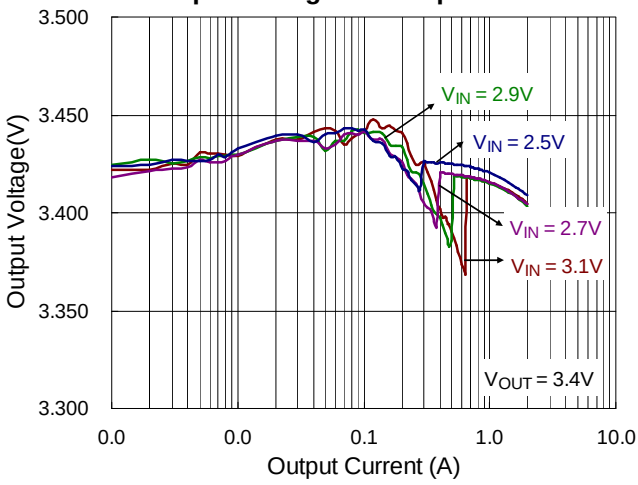
Output Voltage vs. Output Current



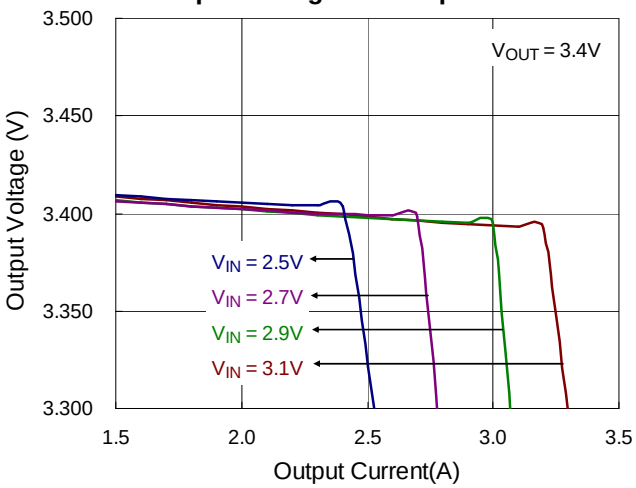
Output Voltage vs. Output Current



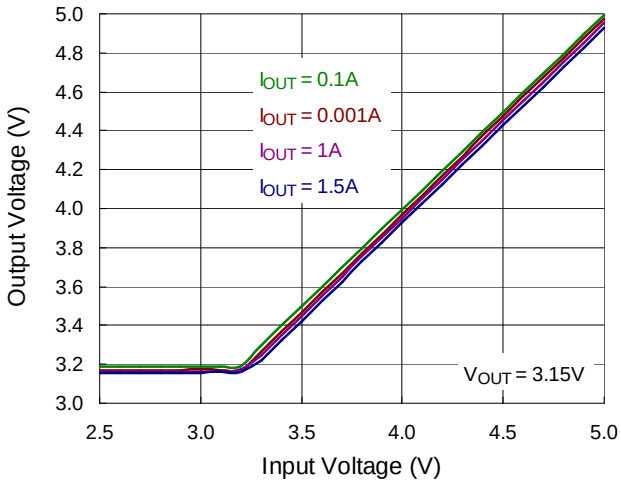
Output Voltage vs. Output Current



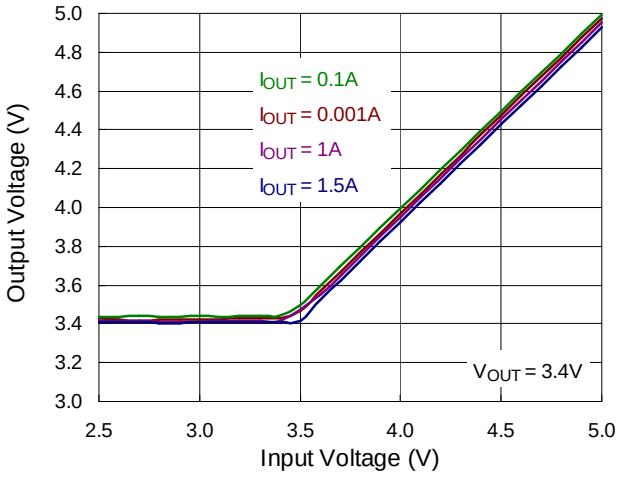
Output Voltage vs. Output Current



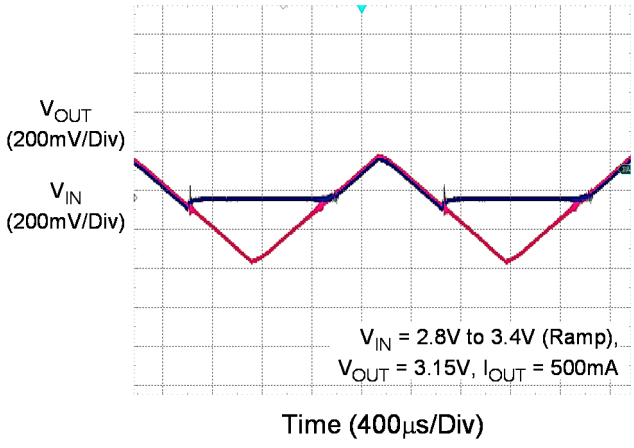
Output Voltage vs. Input Voltage



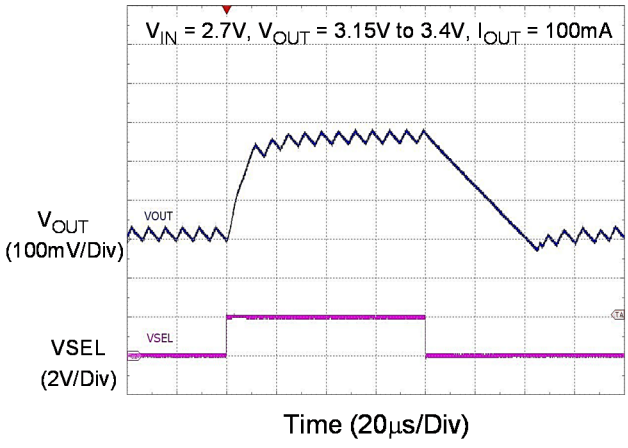
Output Voltage vs. Input Voltage



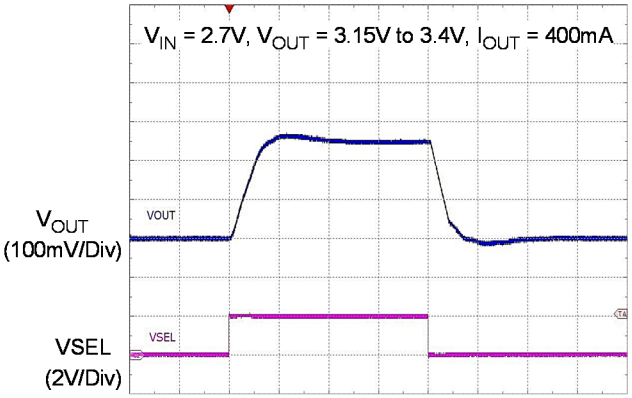
Boost to Bypass Mode Exit / Entry



VSEL Load Current

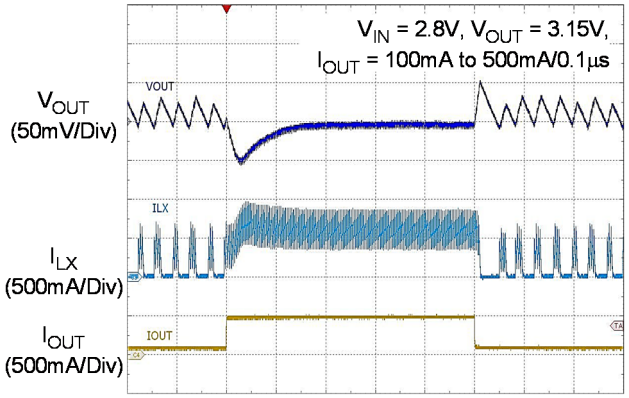


VSEL Load Current



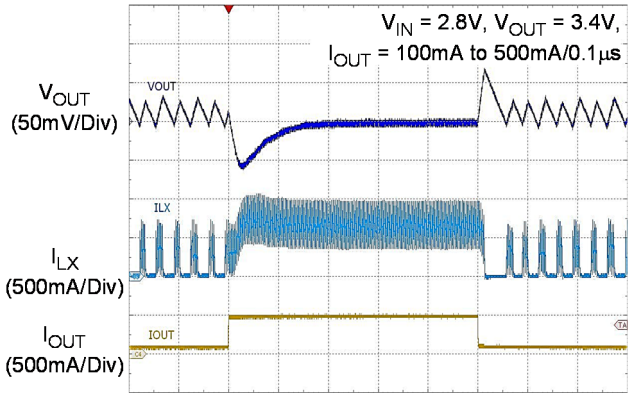
Time (20μs/Div)

Load Transient V_{OUT} = 3.15V



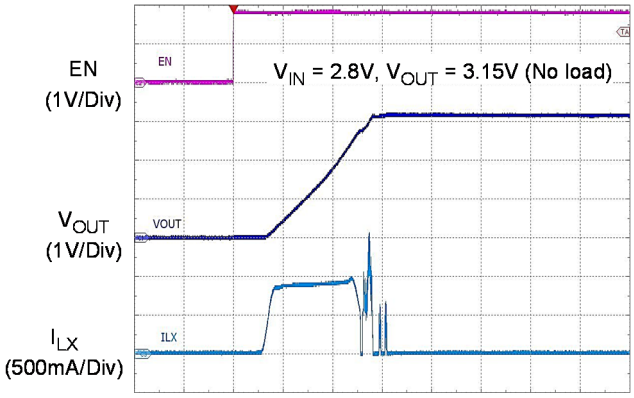
Time (20μs/Div)

Load Transient V_{OUT} = 3.4V



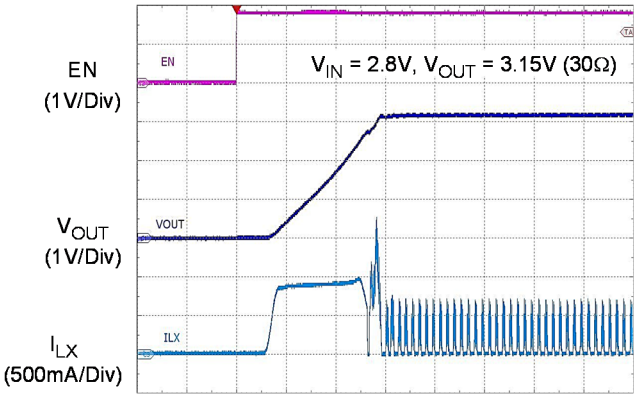
Time (20μs/Div)

Power On V_{OUT} = 3.15V (No Load)



Time (50μs/Div)

Power On V_{OUT} = 3.15V (30Ω)



Time (50μs/Div)

Application Information

Boost Output Current Capacity

The RT4803A device features a valley inductor current limit and max duty cycle limit scheme. In boost mode, the current limit threshold can be set via an I^2C register. The RT4803A devices have a default fixed current limit threshold. See the register table for detailed information. Although current limit can be programmable, but output current capacity also limited by max duty cycle design. So the maximum continuous output current (I_{OUTMAX}), as below choose step :

First application duty cycle must smaller than max duty cycle.

$$1 - \frac{V_{IN}}{V_{OUT}} = \text{Duty} < 40\% \ (\text{max duty cycle limit})$$

If application condition duty cycle smaller than max duty cycle limit, that max output capacity can be calculate as below equation :

$$I_{OUT_{MAX}} = \frac{V_{IN}}{V_{OUT}} \times \eta \times I_{IN_{MAX}}$$

($I_{IN_{MAX}}$ about equal $I_{L_{valley\ current\ limit\ level}}$)

Inductor Selection

Inductor value choose will effect transient, ripple and other performance. The RT4803A recommended nominal inductance value is 0.47μH to achieve advantage performance.

The inductor peak current varies as a function of the load. It is advisable to select an inductor with a saturation current rating higher than peak current of application flowing through the power switches.

It is suggested to select an inductor with the low DCR to obtain good performance and efficiency for application. The inductor saturation current must be chosen carefully considering the current limit (4500mA max default level).

The peak current of application can be estimated using as below equation :

$$I_{LPEAK_{MAX}} = \frac{V_{IN} \times D}{2 \times L \times f_{SW}} + \frac{I_{OUT_{MAX}} \times V_{OUT}}{V_{IN} \times \eta}$$

Input Capacitor Selection

Steady state and transient response operation performance also depend on input voltage stability or not. The RT4803A at least a 10μF input capacitor is recommended to prevent input voltage instability with application operation. And that suggest placed as close as possible to the V_{IN} and GND pins of the IC is recommended.

Output Capacitor Selection

The ripple voltage is an important index for choosing output capacitor. This portion consists of two parts. One is the product of ripple current with the ESR of the output capacitor, while the other part is formed by the charging and discharging process of the output capacitor.

Output capacitor is selected according to output ripple which is calculated as below equation.

$$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_{OUT_{CAP}}$$

$$\Delta V_{ESR} = I_{C_{RMS}} \times R_{C_{ESR}}$$

$$\Delta V_{OUT_{CAP}} = \frac{I_{OUT} \times \text{Duty}}{f_{SW} \times C_{MIN}}$$

User can use equation choose capacitor to meeting systems ripple specification. And at least 22μF x 3 capacitors is recommended to matching application with V_{OUT} ripple request and stability performance.

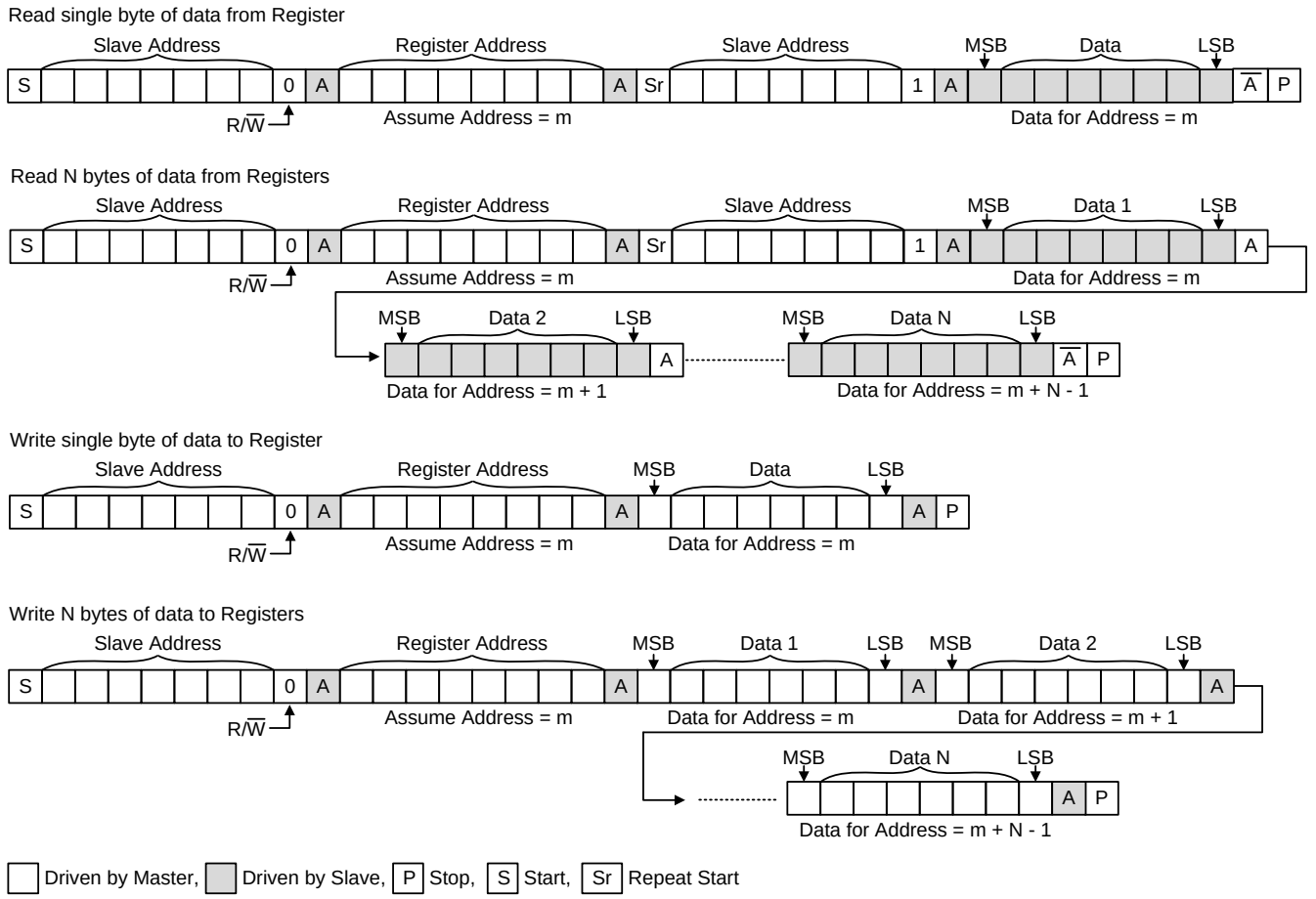
Register Table Lists [Slave address = 1110101 (0x75)]

Name	Address	Description
CONFIG	0x01	MODE control and spread modulation control
VOUTFLOOR	0x02	VSEL = L output voltage programmable register address
VOUTROOF	0x03	VSEL = H output voltage programmable register address
ILIMSET	0x04	Set current limit and soft-start current limit
STATUS	0x05	Read IC status

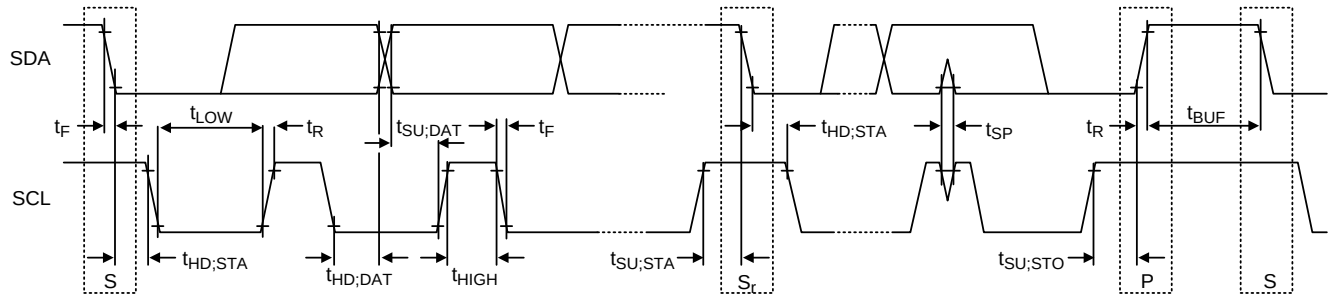
I²C Interface

The RT4803A I²C slave address is 1110101 (7bits). The I²C interface supports fast mode (bit rate up to 400kb/s).

The write or read bit stream (N ≥ 1) is shown below :



I²C Waveform Information



Address 0x01		CONFIG						
Bits	7	6	5	4	3	2	1	0
Name	RESET	ENABLE[1:0]		Reserved	GPIOCFG	SSFM	MODE_CTRL[1 : 0]	
Reset	0	0	0	0	0	0	0	1
Type	RW	RW	RW	RW	RW	RW	RW	RW
Address 0x02		**VOUTFLOOR**						
Bits	7	6	5	4	3	2	1	0
Name	Reserved			VOUT[4:0]				
Reset	0	0	0	0	0	1	1	0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Address 0x03		**VOUTROOF**						
Bits	7	6	5	4	3	2	1	0
Name	Reserved			VOUT[4:0]				
Reset	0	0	0	0	1	0	1	1
Type	RW	RW	RW	RW	RW	RW	RW	RW
Address 0x04		**ILIMSET**						
Bits	7	6	5	4	3	2	1	0
Name	Reserved		ILIM_OFF	SOFT_START	ILIM[3:0]			
Reset	0	0	0	1	1	1	0	1
Type	RW	RW	RW	RW	RW	RW	RW	RW
Address 0x05		**STATUS**						
Bits	7	6	5	4	3	2	1	0
Name	TSD	HOTDIE	DCDCMODE	OPMODE	ILIMPT	ILIMBST	FAULT	PGOOD
Reset	0	0	0	0	0	0	0	0
Type	R	R	R	R	R	R	R	R

Addr	Reg Name	Bit	Bit Name	Default	Type	Description
0x01	CONFIG	7	RESET	0	R/W	0 : Normal operation (default) 1 : All registers are reset to default value.
		6:5	ENABLE[1:0]	00	R/W	00 : Device operation follows hardware control signal. (Refer to Table 1) (default) 01 : Device operation in auto transition mode (boost/auto pass) regardless of the nBYP control signal. (EN = 1) 10 : Device is forced in bypass mode regardless of the nBYP control signal. (EN = 1) 11 : Device is in shutdown mode. Regardless of the nBYP control signal. (EN = 1)
		4	Reserved	0	R/W	Reserved
		3	GPIOCFG	0	R/W	0 : GPIO port is configured to support manual reset input (nRST) and interrupt generation output (nFAULT). (default) 1 : GPIO port is configured as a device mode selection input.
		2	SSFM	0	R/W	0 : Spread spectrum modulation is disabled. (default) 1 : Spread spectrum modulation is enabled in PWM mode.
		1:0	MODE_CTRL[1:0]	01	R/W	00 : Device operation follows hardware control signal (GPIO must be configured as mode select input). 01 : PFM with automatic transition into PWM operation. (default) 10 : Forced PWM operation. 11 : PFM with automatic transition into PWM operation (VSEL = L), forced PWM operation. (VSEL = H).

Addr	Reg Name	Bit	Bit Name	Default	Type	Description
0x02	VOUTFLOOR	7:5	Reserved	000	R/W	Reserved
		4:0	VOUT[4:0]	00110	R/W	00000 : V_{OUT} = 2.85V 00001 : V_{OUT} = 2.9V 00010 : V_{OUT} = 2.95V 00011 : V_{OUT} = 3V 00100 : V_{OUT} = 3.05V … 00110 : V_{OUT} = 3.15V (default) … 11111 : V_{OUT} = 4.4V
0x03	VOUTROOF	7:5	Reserved	000	R/W	Reserved
		4:0	VOUT[4:0]	01011	R/W	00000 : V_{OUT} = 2.85V 00001 : V_{OUT} = 2.9V 00010 : V_{OUT} = 2.95V 00011 : V_{OUT} = 3V 00100 : V_{OUT} = 3.05V … 01011 : V_{OUT} = 3.4V (default) … 11111 : V_{OUT} = 4.4V
0x04	ILIMSET	7:6	Reserved	00	R/W	Reserved
		5	ILIM_OFF	0	R/W	0 : Current limit enabled (default) 1 : Current limit disabled
		4	SOFT_START	1	R/W	0 : Boost soft-start current is limited per ILIM bit settings. (EN L to H with V_{IN} ready state) 1 : Boost soft-start current is limited to ca. 1250mA inductor valley current. (default) (EN L to H with V_{IN} ready state)
		3:0	ILIM[3:0]	1101	R/W	1000 : 1500mA 1001 : 2000mA 1010 : 2500mA 1011 : 3000mA 1100 : 3500mA 1101 : 4000mA (default) 1110 : 4500mA 1111 : 5000mA

Addr	Reg Name	Bit	Bit Name	Default	Type	Description
0x05	STATUS	7	TSD	0	R	0 : Normal operation. 1 : Thermal shutdown tripped. The flag is reset after readout.
		6	HOTDIE	0	R	0 : T_J < 90°C (Typ.) 1 : T_J > 100°C (Typ.)
		5	DCDCMODE	0	R	0 : Device operates in PFM mode. 1 : Device operates in PWM mode.
		4	OPMODE	0	R	0 : Device operates in forced bypass mode. 1 : Device operates in DC-DC mode.
		3	ILIMPT	0	R	0 : Normal operation. 1 : Indicates that the bypass FET current limit has triggered. This flag is reset after readout.
		2	ILIMBST	0	R	0 : Normal operation. 1 : Indicates that the valley input current limit has triggered. This flag is reset after readout.
		1	FAULT	0	R	0 : Normal operation. 1 : Indicates that a fault condition has occurred. This flag is reset after readout.
		0	PGOOD	0	R	0 : Indicates the output voltage is out of regulation. 1 : Indicates the output voltage is within its nominal range. This bit is set if the converter is forced in pass-through.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WL-CSP-16B 1.67x1.67 (BSC) package, the thermal resistance, θ_{JA}, is 47.7°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (47.7°C/W) = 2.09W for WL-CSP-16B 1.67x1.67 (BSC) package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

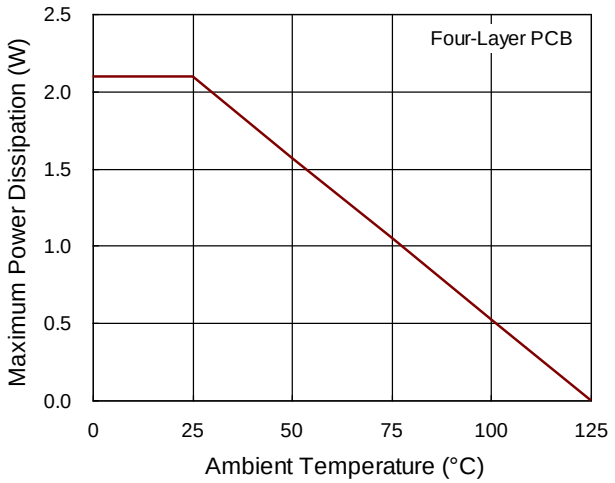


Figure 6. Derating Curve of Maximum Power Dissipation

Layout Considerations

The PCB layout is an important step to maintain the high performance of the RT4803A.

Both the high current and the fast switching nodes demand full attention to the PCB layout to save the robustness of the RT4803A through the PCB layout. Improper layout might show the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. For the best performance of the RT4803A, the following PCB layout guidelines must be strictly followed.

- Place the input and output capacitors as close as possible to the input and output pins respectively for good filtering.
- For thermal consider, it needed to maximize the pure area for the power stage area besides the LX.

Top View

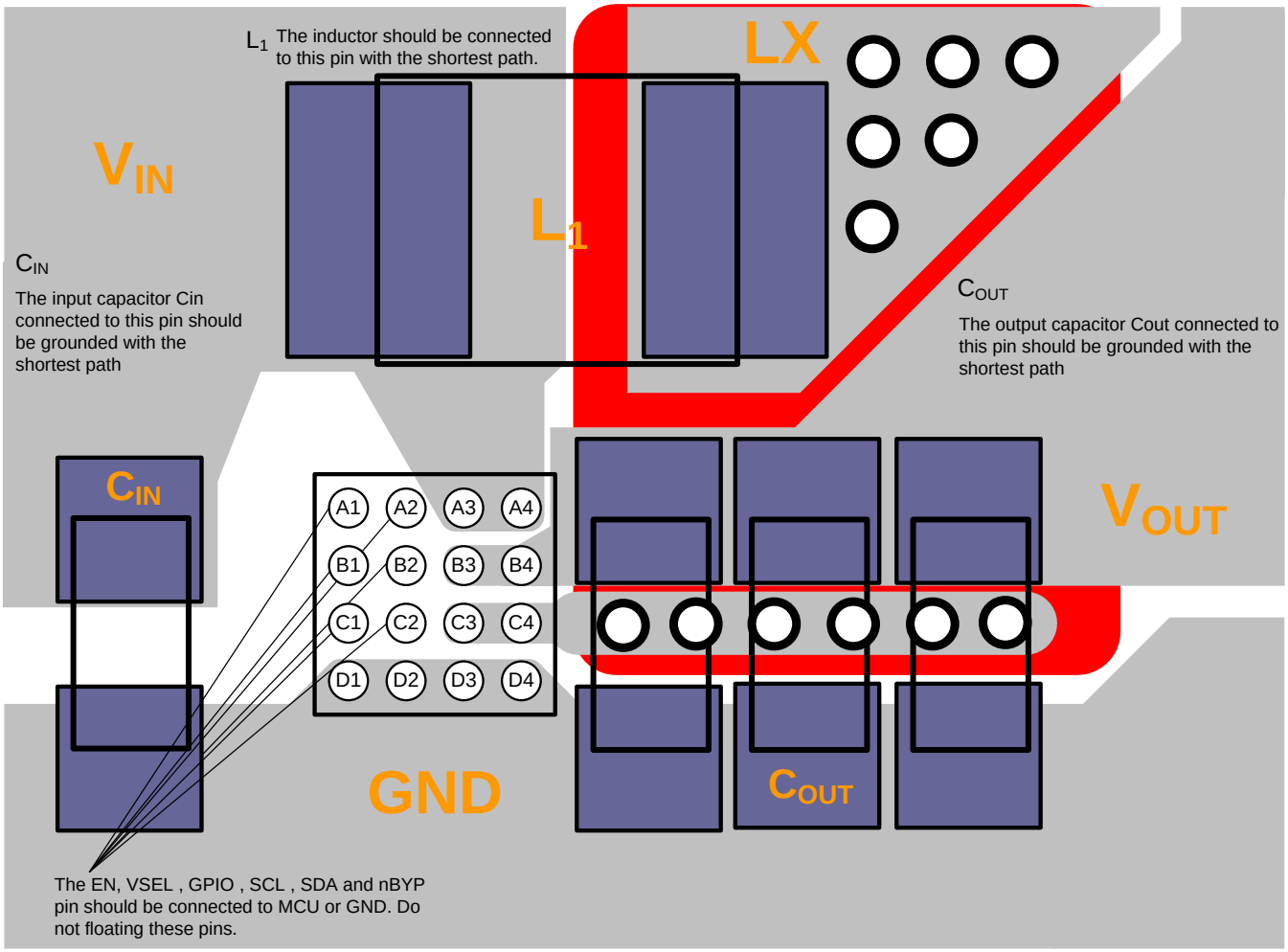
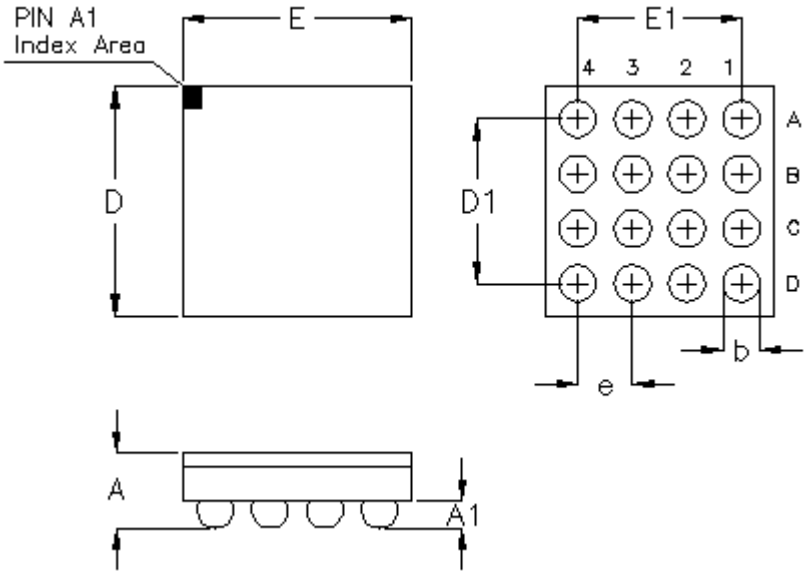


Figure 7. PCB Layout Guide

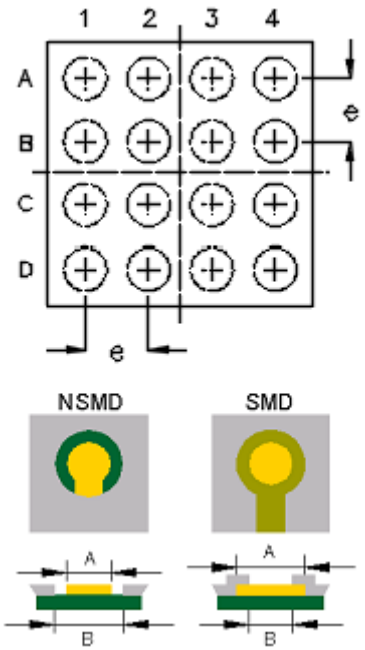
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.620	1.720	0.064	0.068
D1	1.200		0.047	
E	1.620	1.720	0.064	0.068
E1	1.200		0.047	
e	0.400		0.016	

WL-CSP-16B 1.67x1.67 (BSC)

Footprint Information



Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP1.67*1.67-16(BSC)	16	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

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