A system optimized alternative to FPGAs, the 66AK2L06 SoC

Texas Instruments

Scalable, high-performance data acquisition and transmission processing enables breakthrough products

Applications that are based on high-speed data acquisition and transmission are typically found in avionics and defense markets, medical imaging, test and measurement and other industrial applications. Specific equipment examples include radar technology, ultrasound equipment, wireless network testers, and LIDAR. At the core of each of these products are a signal chain that consists of data acquisition and/or transmission which requires an analog front end capturing and transmitting data, and a digital end converting the data to digital format for further real-time processing. These systems typically include a processor or processors, and custom or semi-custom circuit to support the digital front end and JESD204B interface. The single 66AK2L06 SoC, pre-integrated in a TI design with the ADC12J4000 and DAC38J84 as shown in Figure 1, enables the game-changing shift from current core solutions, affording a new wave of product innovations with time to market of up to three times faster than previous technology. Visit **66AK2L06** to learn more

Highly integrated SoC with JESD204B attach enables game changes in power, cost and size

Based on TI's high-performance KeyStone™ II architecture, the 66AK2L06 system-on-chip (SoC) is a

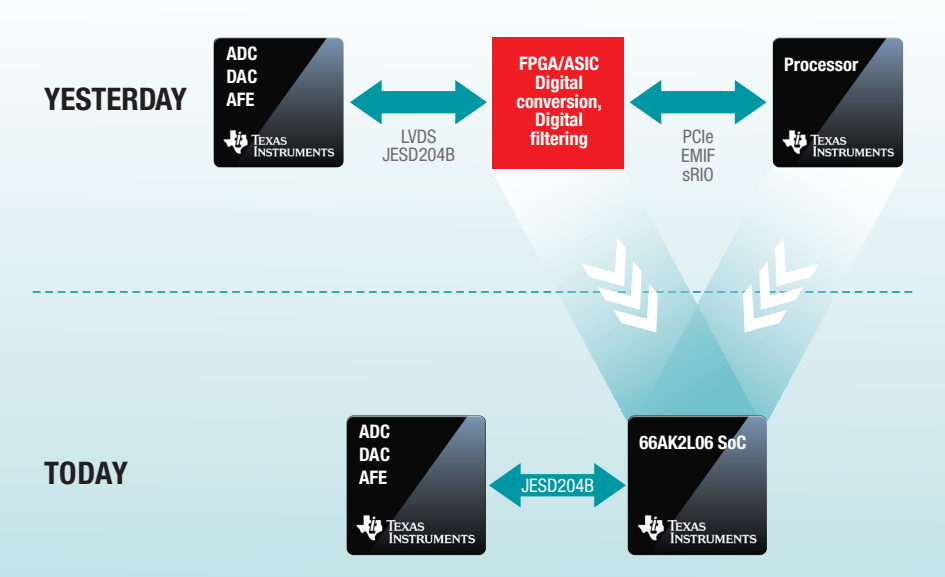

Figure 1: Game-changing SoC and front-end integration provide step-function reductions

Key features

- 66AK2L06 SoC
  - Highly efficient and scalable high-speed data acquisition and transmission single-chip solution
  - Enables significant solution cSWaP enhancements
    - Solution power reductions by up to 50 percent
    - Solution weight and board area reductions by up to 66 percent
  - High-speed JESD204B chip-to-chip interface
    - 4 × 7.36Gbps SerDes line rate
  - Fully integrated, software programmable digital front end accelerators for digital up and down conversion and digital filtering
    - For wideband sample rate conversion up to 48 channels
    - 368 MSPS, 300-MHz BW, 4 × 7.36Gbps JESD, 8192-pt FFT, FIR filters
  - Fast Fourier transform coprocessor (FFTC) improving latency for FFT/inverse FFT (iFFT) execution up to 8K-points with better performance that a fixed-point DSP core implementation
  - KeyStone™ II architecture with full performance entitlement
- ADC12J4000
  - Wideband sampling and digital tuning
  - 12 bit, 4 GSPS
  - JESD204B
- DAC38J84
  - Low power, 4-channel
  - 16 bit, 2.5-GSPS per channel
  - JESD204B

scalable, low-power high-speed data acquisition solution that is JESD204B interface enabled with an integrated digital front end (DFE), digital down converter, digital up converter, ARM® and DSP cores and Fast Fourier Transform (FFT) acceleration. It significantly improves the cost, size, weight and power (cSWaP) parameters over current solutions, eliminating the need for additional custom devices such as field programmable gate arrays (FGPAs) or application specific integrated circuits (ASICs). The SoC's dual-ARM, quad-DSP cores, along with the DFE, are fully software programmable, enabling optimal performance, as well as end product scalability and quick time to market. The TI pre-integration and validation of the 66AK2L06 SoC with the 16-bit, 4-GSPS, RF-sampling ADC12J400 analog-to-digital converter (ADC); 16-bit, 2.5-GSPS DAC38J84 digital-to-analog converter (DAC); and required control software enables customers to get products to market more rapidly. The ADC12J4000 and DAC38J84 are both JESD204B-enabled, affording reduced power consumption and board space and providing the performance needed for high-speed data acquisition applications.

Achieving cSWaP product transformation through KeyStone II architecture

Simplifying the interface via JESD204B

JESD204B is a serial communications link interface which conforms to the JESD204B standard from JEDEC and provides for a high-throughput, low-in-count serial link between analog-to-digital (ADC) and digital-to-analog (DAC) converters, and is integrated into the 66AK2L06 SoC. JESD204B is a flexible and scalable serial link interface that can accommodate a wide range of data transfer speeds and configurations, such as multiple ADCs or DACs on one JESD differential pair. By embedding the clock in the data stream and including algorithms to optimize the sampling of data bits, JESD204B is able to simplify routing between devices because significantly fewer lanes are needed on the board. The 66AK2L06 SoC is unique in that it supports a direct JESD204B interface between the ADC/DAC/AFE to the processor itself; no intermediate circuitry required.

Integrated yet software-programmable Digital Front End

To date, high-speed data acquisition solutions have required FGPA or ASIC solutions to execute the critical functions of the DFE. Each implementation has been honed to the specific application configuration, ultimately committing the gates in the FPGA or ASIC. By integrating the DFE, the 66AK2L06 SoC combines all the high-throughput digital processing into one optimized processing unit and as a result, the SoC is able to perform a variety of functions on-chip, from fundamental signal processing including channelization/decimation and re-sampling, to exponential complex multiplications, filtering and FFT/iFFT. The on-chip integration of this essential function reduces overall cost, size and weight by eliminating additional hardware and associated interfaces while providing the added bonus of ease of use in quickly re-programming for field adjustments or new product variations.

Mandatory **DFE channelization and data converter interface** functions – these are signal processing functions to be performed with most types of applications:

- Carrier filtering to comply with standardized spectral emission masks
- Tuning and channel aggregation and distribution
- JESD204B SerDes interfaces to TI high-speed ADCs and DACs
- The baseband block (BB) provides:
  - Programmable complex gain per channel for transmit data
  - Programmable circular clipper for transmit data
  - Programmable back-end automatic gain control (BeAGC) for receive data
  - Programmable power measurement options for both transmit (TX) and receive (RX) channels
  - Supports up to 24 RX channels and 24 TX channels
  - Provides loopback functionality
- The digital down/up conversion (DDUC) provides:
  - Multi-channel up/down conversion
  - Flexible input/output sample rates
  - Programmable resampling options
  - Programmable FIR to meet spectral mask requirements
  - Gain, phase and fractional delay adjustment per channel

On-chip DSP and FFT accelerator for algorithm software programmability

The FFTC coprocessors are accessible across all four C66x cores on the 66AK2L06 SoC. This module can be used to accelerate the FFT and iFFT computations that are required in various applications, hence freeing up DSP core cycles for other processing. The FFTC provides the following features:

- iFFT and FFT processing for the following sizes:
  - $2^a \times 3^b$ for 2 <= a <=13, 0 <= b <=1 – maximum size 8192
  - $12 \times 2^a \times 3^b \times 5^c$ for sizes between 12 and 1296
- 16 bits I / 16 bits Q input and output
- Throughput varies slightly depending on the FFT size. For example an FFT of 4096 points, can be processed by a single FFTC at a throughput of 525 Msps for a 1.2-GHz device.
- SNR ranging from 84 to 100 dB depending of the FFT size
- Dynamic and programmable scaling modes
- Dynamic scaling mode returns block exponent
- Support for "FFT shift" (switch left/right halves)
- Support for cyclic prefix (addition and removal)
- Ping/Pong input, output buffers
- Input data scaling with shift
- Output data scaling
- Zero padding

Enabling low-power solutions

The architectural aspects of the 66AK2L06 SoC not only make it a low-power device, but its unique capabilities such as the integrated DFE reduce the overall power consumption

of the entire system. Similar to the KeyStone devices before it, the 66AK2L06 SoC has achieved its exceedingly low power consumption through a combination of process technologies, TI's low-power SmartReflex™ technology and innovative power management techniques, such as dynamic voltage, frequency scaling, memory retention until access, power and clock gating, and others.

Performance entitlement through highly scalable, software programmable KeyStone II-based architecture

The 66AK2L06 SoC is based on TI's KeyStone II architecture, which provides considerable scalability and flexibility within the device itself, affording manufacturers the ability to base an array of multiple products from the same common hardware/software SoC platform. This increases customers' productivity and profitability.

The KeyStone II architecture provides more than enough throughput and on-chip resources to enable the processing cores to reach their optimum processing performance without constraints, such as intra-bus blocking. Referred to as multicore "entitlement", this empowerment is ensured by the architecture's ability to provide non-blocking access to all processing cores, peripherals, co-processors and I/O channels. Some of the key elements of the KeyStone architecture are its Multicore Navigator, TeraNet and Multicore Share Memory Controller, per Figure 2.

The **Multicore Navigator** controls and abstracts the connections among the various subsystems that make up the KeyStone architecture and SoC. This innovative packet-based manager has a unified interface for communications, data transfers and job management. While delivering higher system performance, it ensures fewer interrupts and reduces the complexity of software because of its "fire-and-forget" action model.

TeraNet – a hierarchal switch fabric – delivers more than two terabits of none-blocking data bandwidth within the 66AK2L06 SoC. This virtually guarantees that the cores and coprocessors are never idle because of data communication latencies or contention. As a result, each processing element is able to operate at its optimum rate. Since the TeraNet switch fabric is hierarchical instead of a flat crossbar, overall power consumption is much lower in idle states and systems latency is minimized. Low latency is an important key that could be traded for extra processing power.

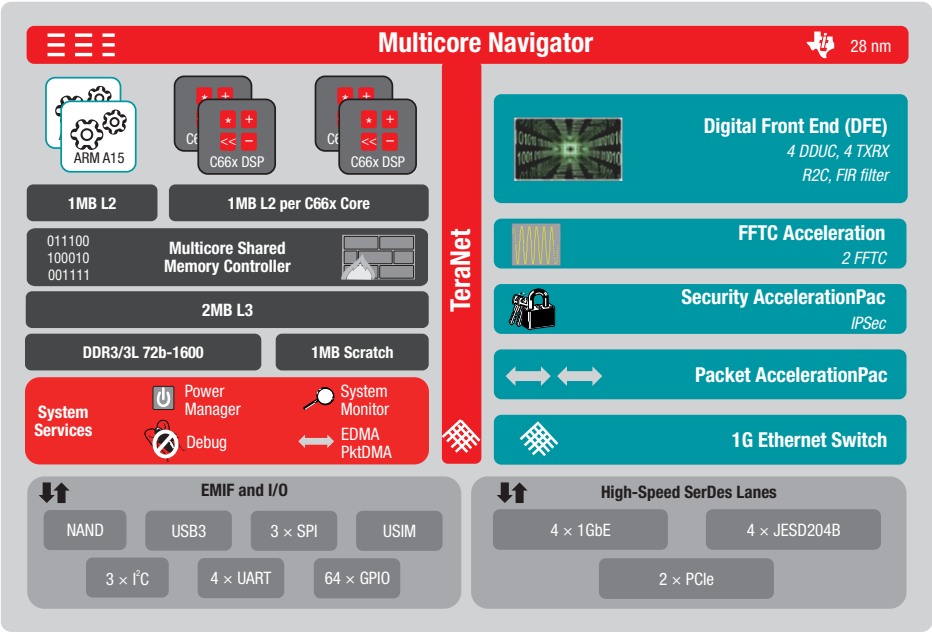

Figure 2: The 66AK2L06 SoC leverages the KeyStone II architecture for full performance entitlement.

The **DDR3 external memory interface (EMIF)** on the 66AK2L06 SoC is made up of one 1,600-MHz, 72-bit bus supporting as much as 8 GB of addressable memory space. With its direct connection to the MSMC, the DDR3 EMIF is able to reduce any latency associated with external memory fetches and provide the speed needed for large data transfers, which is essential for advanced applications with heavy data storage needs.

Powerful core performance – The KeyStone II architecture leverages advanced 28-nm technology for improved cost efficiency through the integration of multiple RISC and DSP cores at lower power consumption. The two ARM Cortex®-A15 cores provide high-performance RISC processing at ultra-low power consumption levels. The four TMS320C66x DSP cores integrated into the 66AK2L06 SoC enable programmable performance of signal processing and compute intensive math, supported by an FFT coprocessor. The C-programmable C66xx DSP core is the world's fastest integrated floating-point DSP delivering over 20 GFLOPS at 1.25 GHz while also supporting deterministic real-time performance.

Software programmability and system pre-integration provide 3× faster time to market

Introducing the software programmable Digital Front End

To date, the digital front end functions such as up and down conversion, FIR filtering, etc. of high-speed data acquisition products have been implemented in FPGA or ASICS. They are most often programmed using VHSIC hardware design language (VHDL) which in turn gets implemented as hard-coded IP blocks within the device. The 66AK2L06 SoC integrated, software programmable DFE allows for natural C, C++ floating-point algorithms to be quickly compiled, analyzed and adjusted as necessary, up front, and once the product is fielded, greatly improving the R&D time and costs. In addition, similar products can be created using

that common C, C++ software as a starting point, enabling OEM product scalability.

The 66AK2L06 SoC leverages the software ease of use achieved by previous KeyStone-based SoCs

An important aspect of the scalability of the 66AK2L06 SoC is the consistent and continuous software track that is essential to all of TI's processors. In addition to the hardware compatibilities of the KeyStone II architecture, software developed for any KeyStone-based device is scalable upward to future SoCs. The KeyStone II multicore software development kit (MCSDK) is pre-integrated and testing with the mainline Linux™ operating system for the ARM cores and TI-RTOS real-time operating system for the DSPs, affording the optimal balance of performance and ease of use for SoC software developers. The ARM and, unlike most existing implementations, the DSP cores, along with radio front end, are fully software programmable for a straightforward, efficient path to initial product algorithm implementation, as well as ease in subsequent code permutations for product variances and deployed enhancements.

TI ADCs, DACs, AFEs: Additional boost for developer time to market

While the 66AK2L06 SoC JESD204B interface enables seamless connection to the robust family of TI ADCs/DACs/AFEs, TI has pre-integrated and validated the real-time processing engine with a pair of commonly used TI data converters, the ADC12J400 and DAC38J84, offering yet even more simplification and ease of implementation for developers in this portion of the market. This is offered as a TI reference design, enabling manufacturers to spend less time and resources on board-level design, bring-up, integration and test.

Complete tools and support

TI has developed a range of tools and support capabilities that save equipment manufacturers time, resources and development budget so that these resources can be allocated to developing differentiating product features. The MCSDK provides highly-optimized bundles of foundational, platform-specific drivers to enable development on selected TI ARM and DSP devices. It gives developers the ability to evaluate hardware and software capabilities of the evaluation platform and to rapidly develop applications. The Radio Frequency Software Development Kit (RFSDK) provides APIs to initialize and configure digital front end (DFE) and JESD. The RFSDK will work with a set of configurations for the pre-validated system solutions based on the 66AK2L06 SoC and high-speed data converters (ADCs/DACs) or analog front end (AFE). Additionally the RFSDK provides reconfiguration capability through a graphical user interface (GUI) to control and manage DFE/JESD features such as frequency, filters and gains. The RFSDK enables developers to accelerate time to market, leveraging the programmability of DFE and JESD to create a scalable system solution for the high-speed data generation and acquisition market.

Other development tools include TI's well known Code Composer Studio™ (CCStudio) integrated development environment (IDE), and a full suite of best-in-class Eclipse-based development and debugging tools. CCStudio IDE features a C compiler for both ARM and DSP and a Windows® debugger for visibility into source code execution and performance. The compiler generates high-performance code that is first-pass efficient, reducing the need for cycles of code optimization. The debugging tools help designers get products to market faster, saving development resources by visualizing problems and finding solutions quickly. In addition, an evaluation module (EVM) and TI reference design (TI Designs) are available to facilitate rapid application software development platforms and product prototypes.

For more information

Visit **66AK2L06** to learn more.

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