DS25MB100-EVK

Signal Conditioning Mux-Buffer

Demo Board User Guide

Introduction

The DS25MB100 is a signal conditioning 2:1 multiplexer and 1:2 buffer designed to support port redundancy. Advanced signal conditioning features utilizing input equalization and output driver de-emphasis enable data communication over FR4 backplane or cable at 0.25 - 2.5Gb/s.

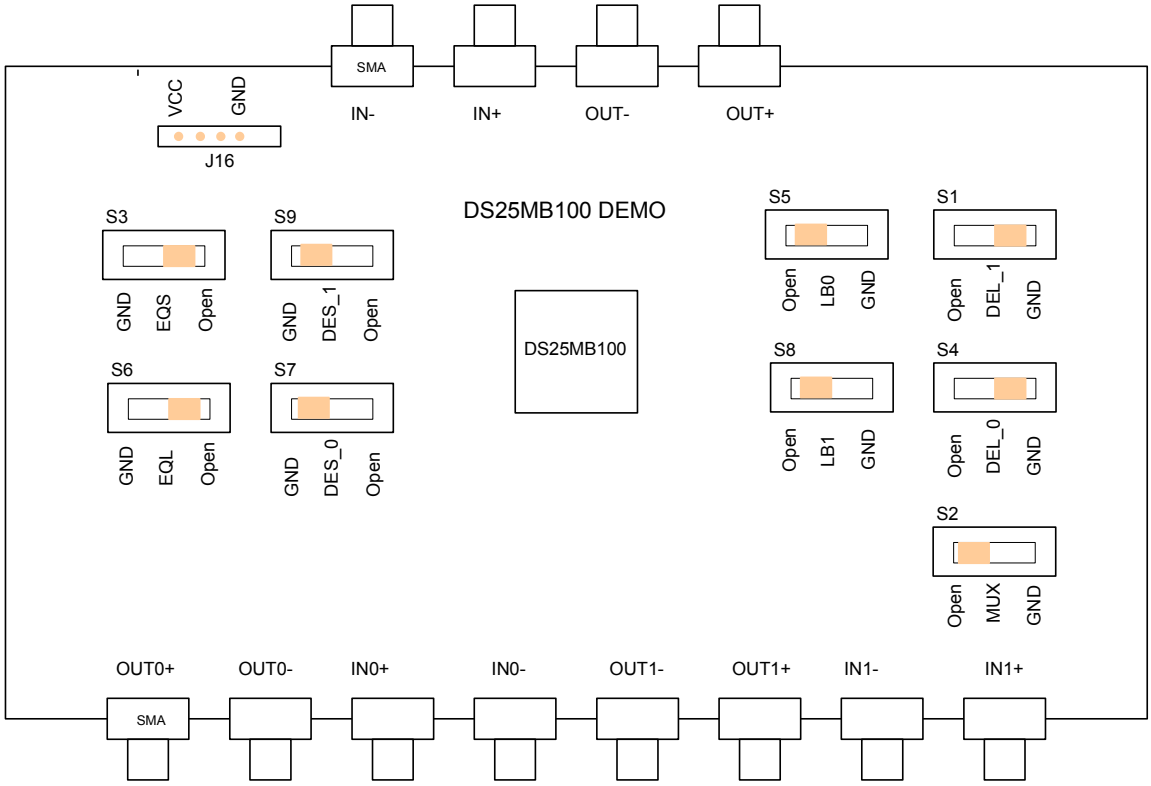
The DS25MB100 demo board is designed to assist customers to evaluate the functionality and performance. All input and output ports of the DS25MB100 are brought out to SMA connectors for accessibility to instrumentation.

Evaluation Kit Content

This evaluation kit consists of the following components:

(1) DS25MB100 demo board
(2) Demo Board User Guide (this document)
(3) Demo board schematic

DS25MB100 Demo Board



Connection Diagram

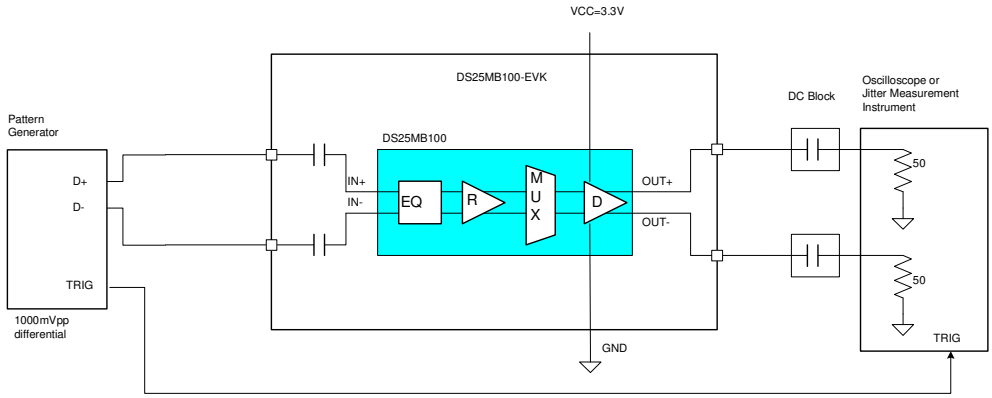


Figure 1. Typical connection for evaluation of the DS25MB100

Power		
VCC	JP17 J16.3/4	3.3V ± 5%
GND	JP20 J16.1/2	0V

EQ controls		
EQL	S6 J21	EQL enables or disables Equalizer at the line-side (IN±). EQS enables or disables Equalizers at the switch-side (IN0± and IN1±).
EQS	S3 J3	When EQL or EQS is open, it is logic 1 (equalizer bypassed). When EQL or EQS is strapped to GND, it is logic 0.

De-emphasis controls		
DEL_0	S4 J4	Set de-emphasis level for all outputs at the line side (OUT±). When DEL_1 or DEL_0 is opened, it is logic 1.
DEL_1	S1 J1	When DEL_1 or DEL_0 is strapped to GND, it is logic 0.
DES_0	S7 J22	Set de-emphasis level for all outputs at the switch side (OUT0±, and OUT1±).
DES_1	S9 J25	When DES_1 or DES_0 is opened, it is logic 1. When DES_1 or DES_0 is strapped to GND, it is logic 0.

Mux controls		
MUX	S2 J2	Set the multiplexer position to select IN0± or IN1±. When MUX is opened, it is logic 1 (selects IN0±). When MUX is strapped to GND, it is logic 0 (IN1±).

Loopback controls		
LB1	S8 J24	Enable or disable loopback. When LB0 or LB1 is opened, it is logic 1 (No loopback).
LB0	S5 J5	When LB0 or LB1 is strapped to GND, it is logic 0 (normal mode).

RSV control		
RSV	JP8.2	Reserved for factory testing purposes. JP8.2 is permanently tied to GND.

Switch S and jumper J are connected in parallel for each logic control pin. When switch is being used, jumper should be kept open. When jumper is used, the corresponding switch should be kept at OFF position.

Logic control for data paths

Following tables list the logic states of the control pins used to configure the data paths of the DS25MB100. More detailed information about pin functions and pin descriptions can be found in the DS25MB100 datasheet.

Table 1. Logic table for multiplex controls

MUX	*Mux Function*
0	MUX select switch input, IN1±.
1 (default)	MUX select switch input, IN0±.

Table 2. Logic table for loopback controls

LB0	*Loopback Function*
0	Enable loopback from IN0± to OUT0±.
1 (default)	Normal mode. Loopback disabled.

LB1	*Loopback Function*
0	Enable loopback from IN1± to OUT1±.
1 (default)	Normal mode. Loopback disabled.

Table 3. Line-side de-emphasis controls

DEL_[1:0]	*De-emphasis level in mVpp (VODB)*	*De-emphasis level in mVpp (VODPE)*	*De-emphasis in dB (VODPE/VODB)*	*Typical FR4 board trace*
0 0	1300	1300	0	10 inches
0 1	1300	920	-3	20 inches
1 0	1300	650	-6	30 inches
1 1 (Default)	1300	461	-9	40 inches

Table 4. Switch-side de-emphasis controls

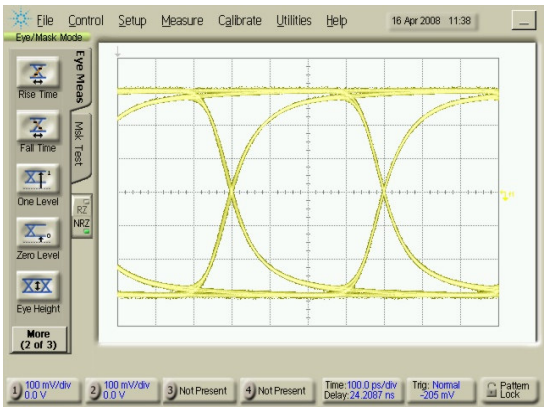
DES_[1:0]	*De-emphasis level in mVpp (VODB)*	*De-emphasis level in mVpp (VODPE)*	*De-emphasis in dB (VODPE/VODB)*	*Typical FR4 board trace*
0 0	1300	1300	0	10 inches
0 1	1300	920	-3	20 inches
1 0	1300	650	-6	30 inches
1 1 (Default)	1300	461	-9	40 inches

Table 5. EQ controls for line or switch side

EQL or EQS	*Equalizer Function*
0	Enable equalization
1 (default)	Equalization disabled.

Typical output waveforms

The followings are typical eye diagrams of the DS25MB100 using demo board connected as shown in Figure 1.



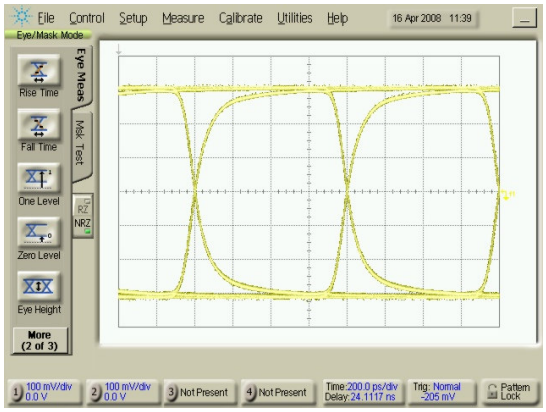
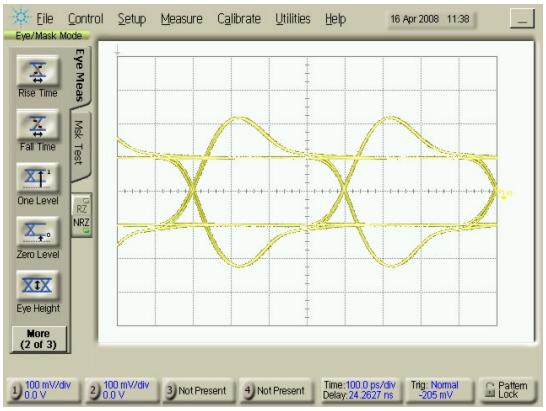


Figure 2a-b. Eye diagrams at 2.5 and 1.25 Gb/s, PRBS7 pattern, Pre-emphasis=0dB



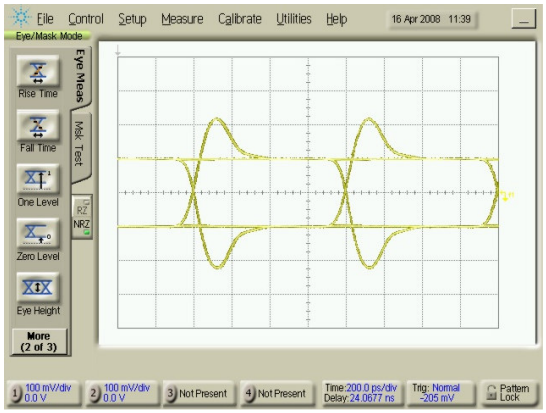
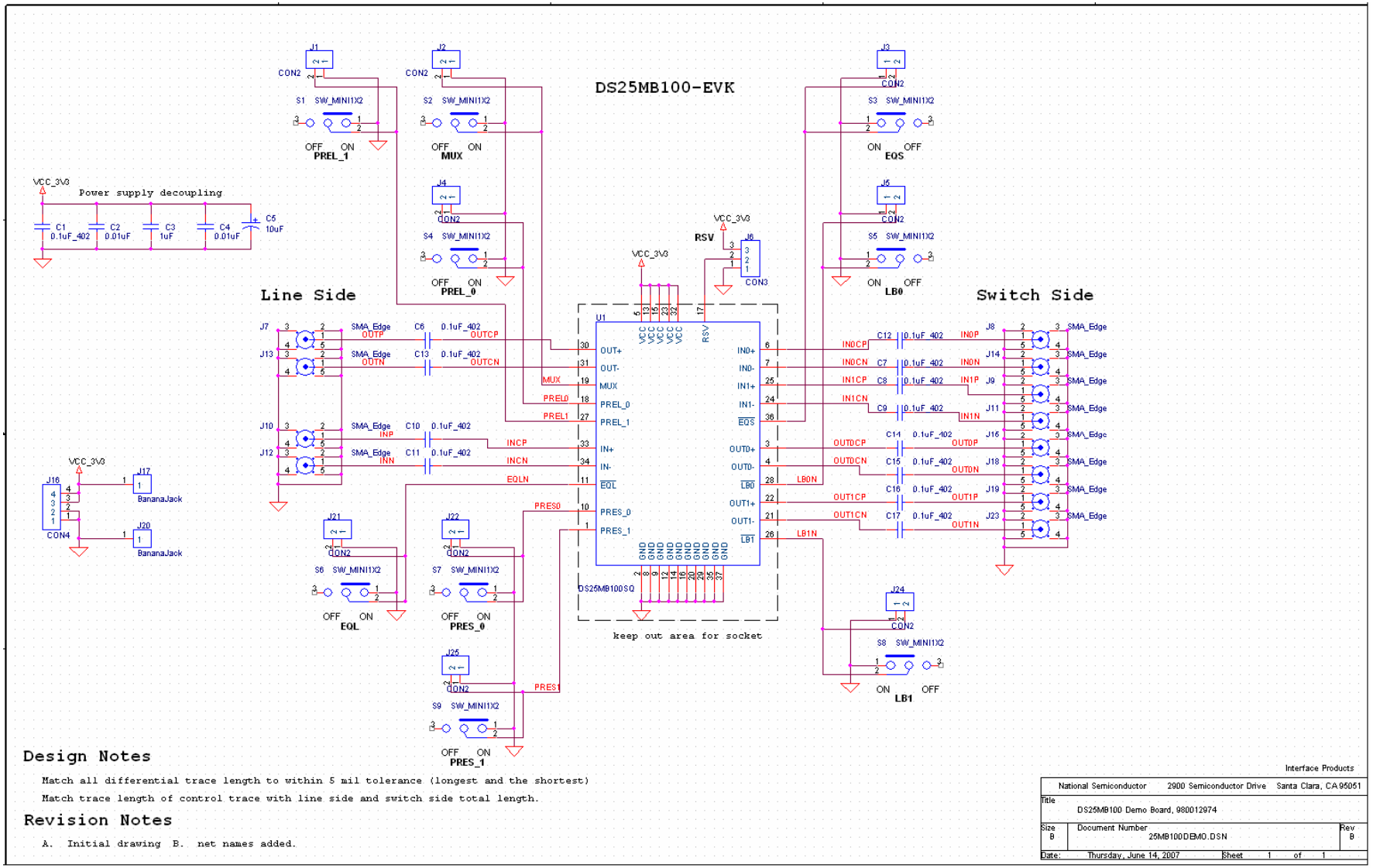


Figure 3a-b. Eye diagrams at 2.5 and 1.25 Gb/s, PRBS7 pattern, De-emphasis=9dB

Reference Material

DS25MB100 datasheet
National web site http://www.national.com/appinfo/lvds/

DS25MB100-EVK board schematic



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