



Integrated Device Technology, Inc.

# 128K x 64 FLOW THRU ZBT SRAM 128K x 64 PIPELINE ZBT SRAM

**ADVANCE  
INFORMATION  
IDT7MBV4153  
IDT7MBV4154**

### FEATURES:

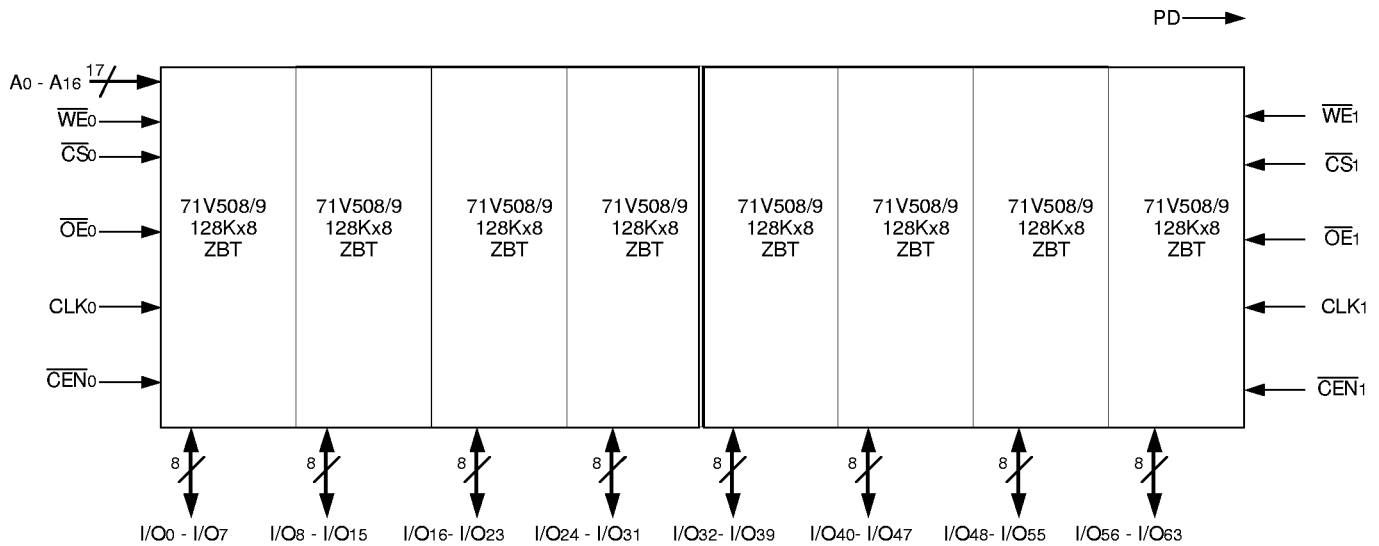
- Low profile 160-lead AMP Free Height Surface Mount Board-to-Board Connector family (5mm-8mm plug options)
- High speed – 50 MHz flow thru, 100 MHz pipeline
- ZBT advantage – no dead cycles between Write and Read Cycles
- Low power deselect mode
- Single 3.3V power supply ( $\pm 5\%$ )

### DESCRIPTION:

The IDT7MBV4153/54 are ZBT SRAM 3.3V synchronous SRAM modules constructed on an epoxy laminate (FR-4) substrate using 8 static RAMs in plastic ZBT packages and a 160-lead board-to-board connector receptacle. The ZBT SRAM is designed to eliminate dead cycles when turning the bus around between reads and writes, or writes and reads. Thus, it has been given the name ZBT™, or Zero Bus Turn-around.

The 160-lead AMP Free Height Surface Mount Board-to-Board Connector configuration allows 160 leads to be mated to a plug on the board which is 2.80 inches long and 1.50 inches wide. The maximum height (with an 8mm plug) from the base board to the top of the module is 0.535 inches.

## FUNCTIONAL BLOCK DIAGRAM



4261 dwg 01

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**COMMERCIAL TEMPERATURE RANGE**

**OCTOBER 1997**

## MODULE PINOUT

Vcc	81	1	I/O0
I/O1	82	2	I/O2
I/O3	83	3	GND
I/O5	84	4	I/O4
Vcc	85	5	I/O6
I/O7	86	6	NC
I/O9	87	7	GND
I/O11	88	8	I/O8
Vcc	89	9	I/O10
I/O13	90	10	I/O12
I/O15	91	11	GND
NC	92	12	I/O14
Vcc	93	13	I/O16
I/O17	94	14	I/O18
I/O19	95	15	GND
I/O21	96	16	I/O20
Vcc	97	17	I/O22
I/O23	98	18	NC
I/O25	99	19	GND
I/O27	99	20	I/O24
Vcc	101	21	I/O26
I/O29	102	22	I/O28
I/O31	103	23	GND
NC	104	24	I/O30
Vcc	105	25	WE0
NC	106	26	WE1
NC	107	27	GND
CEN0	108	28	PD0
Vcc	109	29	PD1
CEN1	110	30	PD2
A0	111	31	GND
A2	112	32	A1
Vcc	113	33	A3
A4	114	34	A5
A6	115	35	GND
Vcc	116	36	A7
A8	117	37	A9
A10	118	38	A11
GND	119	39	GND
CLK0	120	40	CLK1
GND	121	41	GND
A12	122	42	A13
A14	123	43	GND
Vcc	124	44	A15
A16	125	45	A17 <sup>(1)</sup>
<sup>(1)</sup> A18	126	46	GND
<sup>(1)</sup> A20	127	47	A19 <sup>(1)</sup>
Vcc	128	48	A21 <sup>(1)</sup>
<sup>(1)</sup> A22	129	49	CS1
CS0	130	50	GND
OE0	131	51	OE1
Vcc	132	52	RES <sup>(1)</sup>
<sup>(1)</sup> RES	133	53	RES <sup>(1)</sup>
NC	134	54	GND
NC	135	55	NC
Vcc	136	56	NC
I/O33	137	57	I/O32
I/O35	138	58	GND
I/O37	139	59	I/O34
Vcc	140	60	I/O36
I/O39	141	61	I/O38
NC	142	62	GND
I/O41	143	63	I/O40
Vcc	144	64	I/O42
I/O43	145	65	I/O44
I/O45	146	66	GND
I/O47	147	67	I/O46
Vcc	148	68	NC
I/O49	149	69	I/O48
I/O51	150	70	GND
I/O53	151	71	I/O50
Vcc	152	72	I/O52
I/O55	153	73	I/O54
NC	154	74	GND
I/O57	155	75	I/O56
Vcc	156	76	I/O58
I/O59	157	77	I/O60
I/O61	158	78	GND
I/O63	159	79	I/O62
Vcc	160	80	NC

4261 dwg 02

### TOP VIEW

#### NOTES:

1. These pins are No Connects; they are reserved for future modules.

## PIN NAMES

A0 – A22	Address Inputs
I/O0 – I/O63	Data Inputs/Outputs
CS0, CS1	Chip Select Inputs
OE0, OE1	Data Output Enable Inputs
WE0, WE1	Write Enable Inputs
CLK0, CLK1	Clock Inputs
CEN0, CEN1	Clock Enable Inputs
PD0-PD2	Presence Detect Pins
RES	Reserved Pins
NC	No Connect
GND	Ground
Vcc	3.3 Volt Power Supply

4261 tbl 01

## PRESENCE DETECT TABLE

PD0	PD1	PD2	
NC	NC	NC	No Module Present
GND	NC	Vcc	128Kx64 FT ZBT
GND	NC	GND	128Kx64 PIPE ZBT

4261 tbl 02

## ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
VTERM for Vcc	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-10 to +85	°C
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	50	mA

#### NOTE:

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

4261 tbl 03

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V -5%/+5%

4261 tbl 04

## RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	3.15	3.3	3.45	V
GND	Supply Voltage	0	0	0.0	V
V <sub>IH</sub>	Input High Voltage	2.0	—	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

**NOTE:**

1. V<sub>IL</sub> = -1.0V for pulse width less than t<sub>CYC</sub>/2, once per cycle.

4261 tbl 05

## DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V<sub>DD</sub> = 3.3V ±5%)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I <sub>LI</sub>	Input Leakage Current-Address	V <sub>DD</sub> = Max., V <sub>IN</sub> = 0V to V <sub>DD</sub>	—	40	μA
I <sub>LI</sub>	Input Leakage Current-Clock, Control	V <sub>DD</sub> = Max., V <sub>IN</sub> = 0V to V <sub>DD</sub>	—	20	μA
I <sub>LI</sub>	Input Leakage Current-Data	V <sub>DD</sub> = Max., V <sub>IN</sub> = 0V to V <sub>DD</sub>	—	5	μA
I <sub>LO</sub>	Output Leakage Current	$\overline{OE} \geq V_{IH}$ , V <sub>OUT</sub> = 0V to V <sub>DD</sub> , V <sub>DD</sub> = Max.	—	5	μA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 5 mA, V <sub>DD</sub> = Min.	—	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -5 mA, V <sub>DD</sub> = Min.	2.4	—	V

4261 tbl 06

## DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE<sup>(1)</sup> (V<sub>DD</sub> = 3.3V ±5%, V<sub>HD</sub> = V<sub>DD</sub> - 0.2V, V<sub>LD</sub> = 0.2V)

Symbol	Parameter	Test Condition	7MBV4153	7MBV4154	Unit
I <sub>DD</sub>	Operating Power Supply Current	$\overline{CS} \leq V_{IL}$ , Outputs Open, V <sub>DD</sub> = Max., V <sub>IN</sub> ≥ V <sub>IH</sub> or ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> <sup>(2)</sup>	960	1760	mA
I <sub>SB</sub>	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$ , Outputs Open, V <sub>DD</sub> = Max., V <sub>IN</sub> ≥ V <sub>IH</sub> or ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> <sup>(2)</sup>	360	640	mA
I <sub>SB1</sub>	Full Standby Power Supply Current	$\overline{CS} \geq V_{HD}$ , Outputs Open, V <sub>DD</sub> = Max., V <sub>IN</sub> ≥ V <sub>HD</sub> or ≤ V <sub>LD</sub> , f = 0 <sup>(2)</sup>	160	160	mA

**NOTES:**

4261 tbl 07

- All values are maximum guaranteed values.
- At f = f<sub>MAX</sub>, address inputs are switching at 1/t<sub>CYC</sub> and CLK is cycling at 1/t<sub>CYC</sub>; at f=0, no input signals are changing.

## CAPACITANCE

(T<sub>A</sub> = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>IN1</sub>	Input Capacitance-Address	V <sub>IN</sub> = 3dV	60	pF
C <sub>IN2</sub>	Input Capacitance-Control, Clock	V <sub>in</sub> = 3dV	30	pF
C <sub>I/O</sub>	I/O Capacitance	V <sub>OUT</sub> = 3dV	10	pF

**NOTE:**

4261 tbl 08

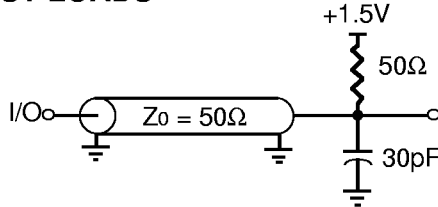
- This parameter is guaranteed by design, but not production tested.

## AC TEST CONDITIONS

Input Pulse Levels	0 to 3V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

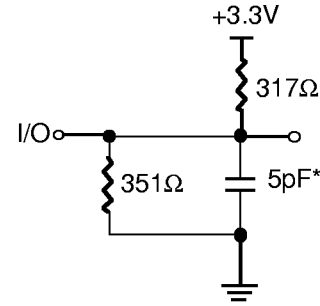
4261 tbl 09

## AC TEST LOADS



4261 dwg 03

Figure 1. AC Test Load



4261 dwg 04

Figure 2. AC Test Load  
(for toHZ, tCHZ, toLZ, and tbc1)

\* Including scope and jig

## AC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

(V<sub>DD</sub> = 3.3V ±5%, T<sub>A</sub> = 0 to 70°C)

Symbol	Parameter	7MBV4154S100		7MBV4154S80		Unit
		Min	Max	Min	Max	
<b>Clock Times</b>						
f <sub>MAX</sub>	Clock Frequency	—	100	—	80	MHz
t <sub>CYC</sub>	Clock Cycle Time	10	—	12.5	—	ns
t <sub>CH</sub>	Clock High Pulse Width	4	—	4	—	ns
t <sub>CL</sub>	Clock Low Pulse Width	4	—	4	—	ns
<b>Output Times</b>						
t <sub>CD</sub>	Clock High to Valid Data	—	5	—	7	ns
t <sub>CDC</sub>	Clock High to Data Change	2	—	2	—	ns
t <sub>CLZ</sub>	Clock High to Output Active	2	—	2	—	ns
t <sub>CHZ</sub>	Clock High to Data High-Z	2	—	2	—	ns
t <sub>OE</sub>	Output Enable Access Time	—	5	—	6	ns
t <sub>OLZ</sub>	Output Enable Low to Data Active	0	—	0	—	ns
t <sub>OHZ</sub>	Output Enable High to Data High-Z	—	5	—	6	ns
<b>Set Up Times</b>						
t <sub>SE</sub>	Clock Enable Setup Time	1.5	—	2	—	ns
t <sub>SA</sub>	Address Setup Time	1.5	—	2	—	ns
t <sub>SD</sub>	Data In Setup Time	1.5	—	2	—	ns
t <sub>SW</sub>	Write Enable Setup Time	1.5	—	2	—	ns
t <sub>SC</sub>	Chip Select Setup Time	1.5	—	2	—	ns
<b>Hold Times</b>						
t <sub>HE</sub>	Clock Enable Hold Time	1	—	1	—	ns
t <sub>HA</sub>	Address Hold Time	2.5	—	2.5	—	ns
t <sub>HD</sub>	Data In Hold Time	1	—	1	—	ns
t <sub>HW</sub>	Write Enable Hold Time	1	—	1	—	ns
t <sub>HC</sub>	Chip Select Hold Time	1	—	1	—	ns

### NOTES:

1. Parameters shown reflect component specifications, and they do not necessarily reflect module tester limits.

4261 tbl 09

## AC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

(VDD = 3.3V ±5%, TA = 0 to 70°C)

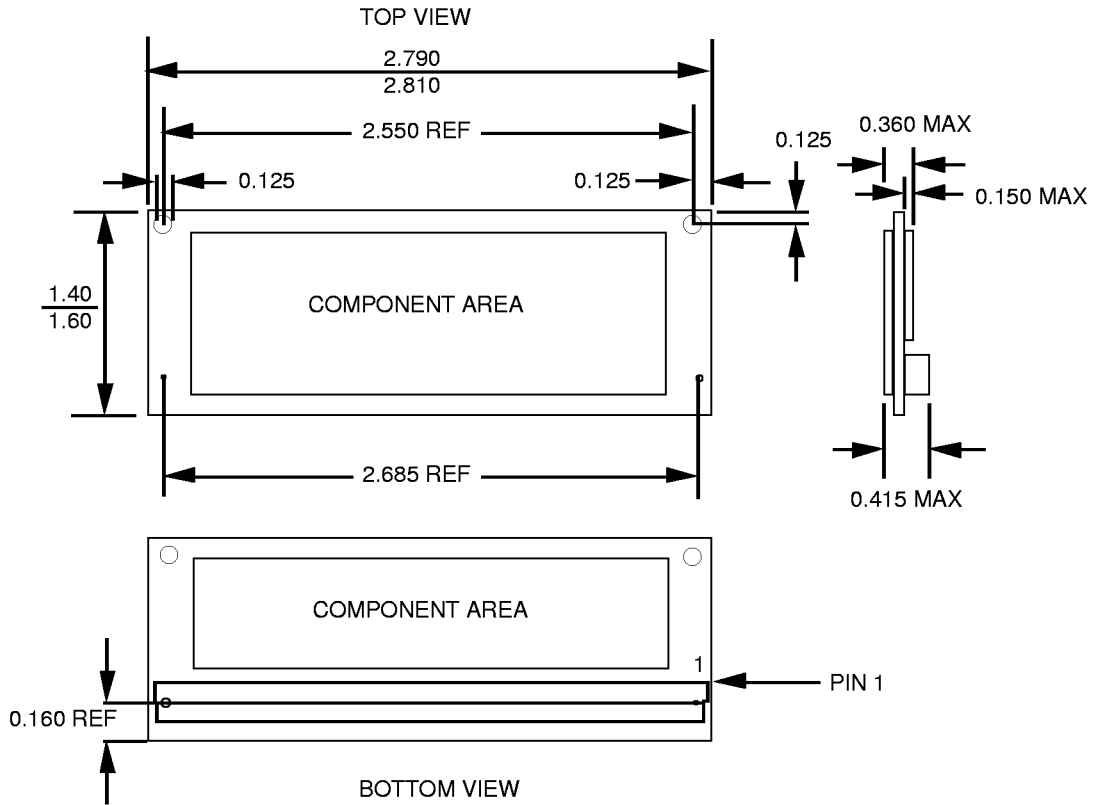
Symbol	Parameter	IDT7MBV4153S50		
		Min.	Max.	Unit
<b>Clock Times</b>				
fMAX	Clock Frequency	—	50	MHz
tcYC	Clock Cycle Time	20	—	ns
tCH	Clock High Pulse Width	6	—	ns
tCL	Clock Low Pulse Width	6	—	ns
<b>Output Times</b>				
tCD	Clock High to Valid Data	—	10	ns
tCDC	Clock High to Data Change	2	—	ns
tCLZ	Clock High to Output Active	2	—	ns
tCHZ	Clock High to Data High-Z	2	6	ns
toE	Output Enable Access Time	—	7	ns
toLZ	Output Enable Low to Data Active	0	—	ns
toHZ	Output Enable High to Data High-Z	—	6	ns
<b>Set Up Times</b>				
tSE	Clock Enable Setup Time	2.5	—	ns
tSA	Address Setup Time	2.5	—	ns
tSD	Data In Setup Time	2.5	—	ns
tSW	Write Enable Setup Time	2.5	—	ns
tSC	Chip Select Setup Time	2.5	—	ns
<b>Hold Times</b>				
tHE	Clock Enable Hold Time	1	—	ns
tHA	Address Hold Time	2.5	—	ns
tHD	Data In Hold Time	1	—	ns
tHW	Write Enable Hold Time	1	—	ns
tHC	Chip Select Hold Time	1	—	ns

**NOTES:**

- Parameters shown reflect component specifications, and they do not necessarily reflect module tester limits.

4261 tbl 10

**PACKAGE DRAWING**



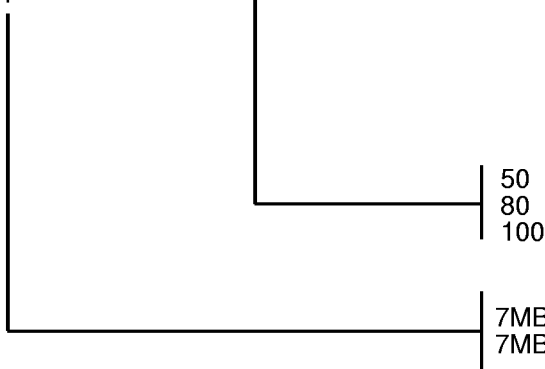
**NOTES:**

1. Specified dimension are in inches.
2. The receptacle used on the module is AMP part number 177983-8..

4261 dwg 05

**ORDERING INFORMATION**

IDT	<u>XXXXX</u>	<u>S</u>	<u>X</u>
	Device Type	Power	Speed



Clock Frequency in Megahertz  
(Speed of the SRAMs used on the Module)  
(Flowthru Only)  
(Pipeline Only)  
(Pipeline Only)

7MBV4153 128K x 64 Flow-Thru ZBT SRAM Module  
7MBV4154 128K x 64 Pipeline ZBT SRAM Module

4261 dwg 06

Integrated Device Technology, Inc. reserves the right to make changes to the specifications in this data sheet in order to improve design or performance and to supply the best possible product.

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