Stratix IV E FPGA Development Board

Reference Manual

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Contents

1. Overview

Introduction

This document describes the hardware features of the Altera® Stratix® IV E FPGA development board, including the detailed pin-out and component reference information required to create custom FPGA designs that interface with all components of the board.

General Description

The Stratix IV E FPGA development board provides a hardware platform for developing and prototyping high-performance and logic-intensive designs based on Altera Stratix IV E devices. The board provides a wide range of peripherals and memory interfaces to facilitate the development of the Stratix IV E FPGA designs.

Two high-speed mezzanine card (HSMC) connectors are available to add additional functionality via a variety of HSMCs available from Altera and various partners.

To see a list of the latest HSMCs available or to download a copy of the HSMC specification, refer to the Development Board Daughtercards page of the Altera website.

Stratix IV E devices provide a solution for applications that do not require high-speed CDR-based transceivers, but are logic, user I/O, or memory intensive.

For more information on the following topics, refer to the respective documents:

- Stratix IV device family, refer to the *Stratix IV Device Handbook*.
- Stratix IV E FPGA Development Kit, refer to the *Stratix IV E FPGA Development Kit User Guide*.
- HSMC Specification, refer to the *High Speed Mezzanine Card (HSMC) Specification*.

Board Component Blocks

The board features the following major component blocks:

- Stratix IV E EP4SE530H35C2N FPGA in the 1152-pin hybrid FineLine BGA (FBGA) package
  - 531,200 LEs
  - 212,480 adaptive logic modules (ALMs)
  - 8 phase locked loops (PLLs)
  - 1024 18-bit x 18-bit multipliers
  - 0.9-V core power

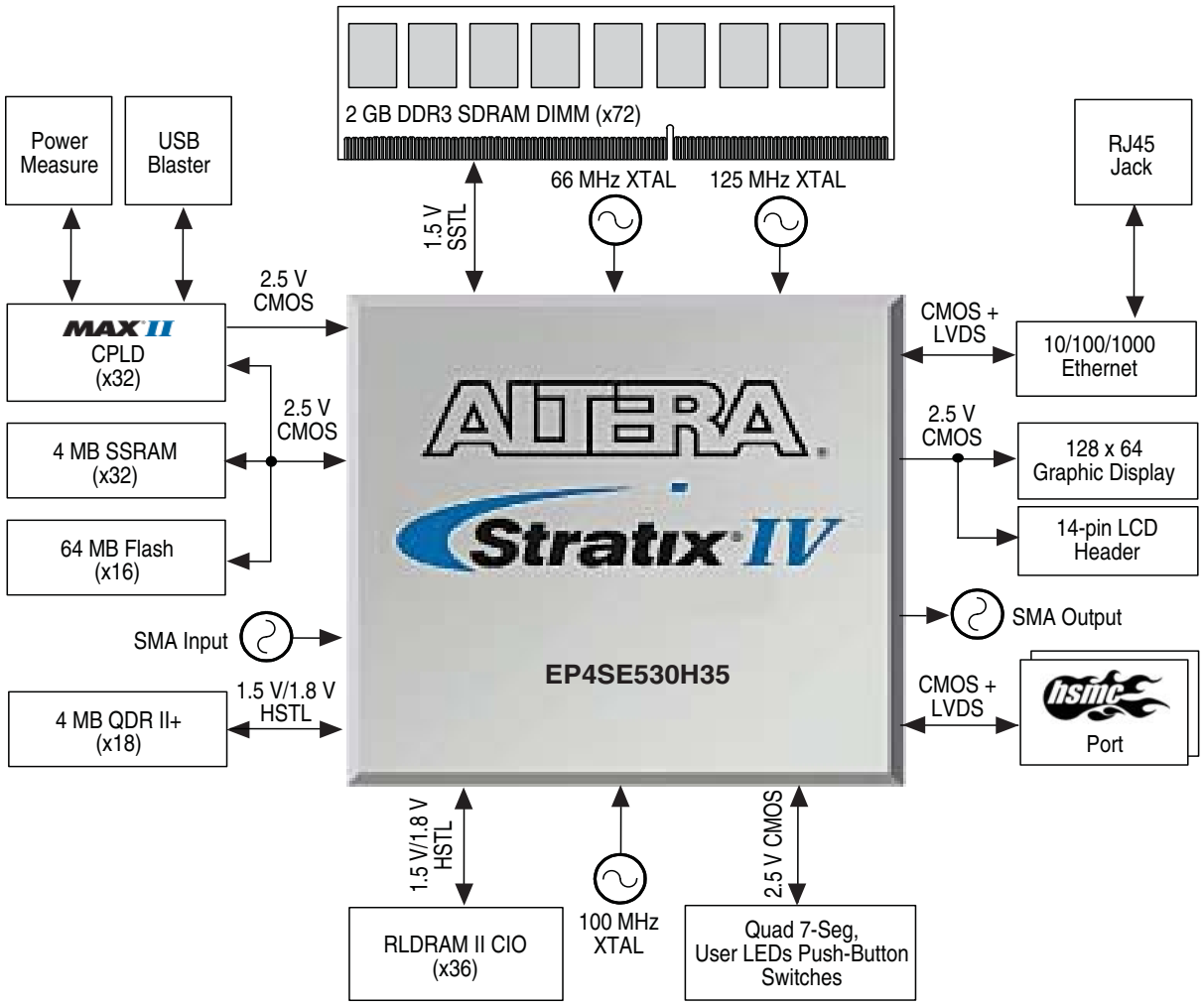
- MAX® II EPM2210F256C3N CPLD in the 256-pin FBGA package
  - 2.5-V core power
- FPGA configuration circuitry
  - MAX II CPLD EPM2210 System Controller and Flash fast passive parallel (FPP) configuration
  - On-board USB-Blaster™ for use with the Quartus® II Programmer
- On-Board ports
  - USB 2.0 – FTDI 12-Mbps PHY
  - One Gigabit Ethernet port
  - Two HSMC expansion ports
- On-Board memory
  - 2-gigabytes (GB) DDR3 SDRAM DIMM with a 72-bit data bus
  - 72-megabits (Mb) QDR II+ SRAM with a 18-bit data bus
  - 576-Mb RLDRAM II combined input/output (CIO) with a 36-bit data bus
  - 18-Mb Synchronous Static Random Access Memory (SSRAM) with a 36-bit data bus
  - 512-Mb Flash with a 16-bit data bus
- On-Board clocking circuitry
  - Five on-board oscillators
    - 50-MHz oscillator (one single-ended input to the FPGA and Max II CPLD)
    - 66-MHz oscillator (two differential inputs to the FPGA)
    - 100-MHz oscillator (one differential inputs to the FPGA)
    - 100-MHz oscillator (one single-ended input to the Max II CPLD)
    - 125-MHz oscillator (two differential inputs to the FPGA)
  - SMA connectors for external clock input
  - SMA connector for clock output
  - HSMC input and output ports

- General user I/O
  - LEDs and displays
    - Eight user LEDs
    - One power on LED
    - One configuration done LED
    - Three HSMC LEDs per interface — one transmit (TX), one receive (RX) and one presence detect (PSNTn)
    - Factory LEDs (LOAD, FACTORY, ERROR, USER_1, and USER_2)
    - Single quad seven-segment display
    - 128 x 64 graphics display
    - 16-character x 2-line LCD display
  - Push-Button switches
    - One CPU reset push-button switch
    - One system reset push-button switch
    - One user reset push-button switch
    - One factory configuration push-button switch
    - One reset configuration push-button switch
    - Four general user push-button switches
  - One 16-position rotary switch
  - DIP switches
    - One eight-position user DIP switch
    - One eight-position MAX II CPLD EPM2210 System Controller specific DIP switch
    - One four-position clock enable DIP switch
- Power supply
  - 14-V – 20-V DC input
  - On-board power measurement circuitry
  - 20-W per HSMC interface
- Mechanical
  - 8.25″ x 7″ board
  - Bench-top operation

Development Board Block Diagram

Figure 1–1 shows the block diagram of the Stratix IV E FPGA development board.

Figure 1–1. Stratix IV E FPGA Development Board Block Diagram



Handling the Board

When handling the board, it is important to observe the following static discharge precaution:

CAUTION

Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board. The Stratix IV E FPGA development board must be stored in a temperature of between –40° C and 100° C. The recommended operating temperature is between 0° C and 55° C.

2. Board Components

Introduction

This chapter introduces the major components on the Stratix IV E FPGA development board. Figure 2–1 illustrates major component locations and Table 2–1 provides a brief description of all component features of the board.

A complete set of schematics, a physical layout database, and GERBER files for the development board reside in the Stratix IV E FPGA development kit documents directory.

For information about powering up the board and installing the demonstration software, refer to the *Stratix IV E FPGA Development Kit User Guide*.

This chapter consists of the following sections:

Board Overview

This section provides an overview of the Stratix IV E FPGA development board, including an annotated board image and component descriptions. Figure 2–1 provides an overview of the development board features.

Figure 2–1. Overview of the Stratix IV E FPGA Development Board Features

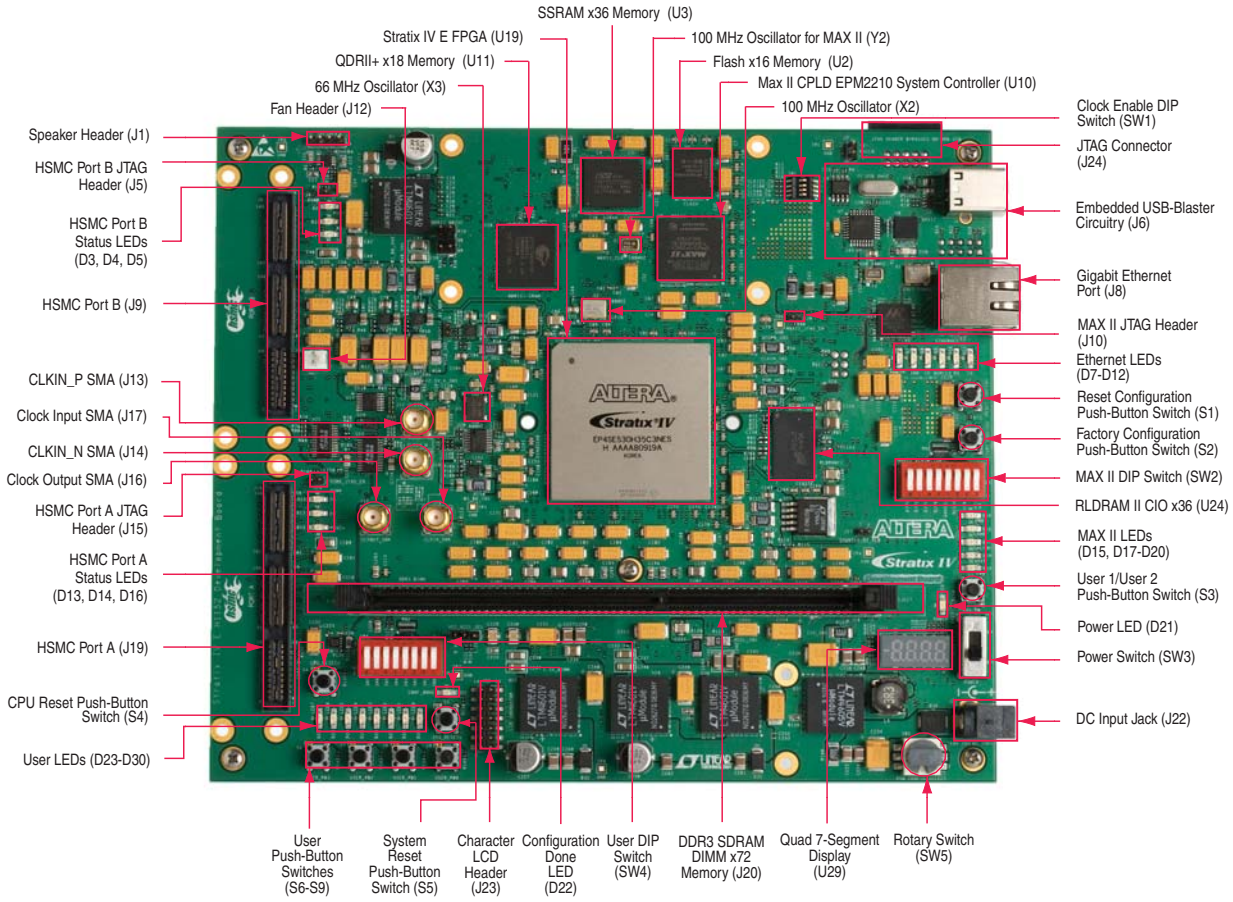


Table 2–1 describes the components and lists their corresponding board references.

Table 2–1. Stratix IV E FPGA Development Board Components (Part 1 of 4)

Board Reference	Type	Description
Featured Devices		
U19	FPGA	EP4SE530H35, 1152-pin FBGA.
U10	CPLD	EPM2210F256, 256-pin FBGA.
Configuration, Status, and Setup Elements		
J6	USB type-B connector	USB interface for programming the FPGA through embedded USB-Blaster JTAG via a type-B USB cable.
J24	JTAG connector (bottom side)	Disables embedded blaster (for use with external USB-Blasters).

Table 2–1. Stratix IV E FPGA Development Board Components (Part 2 of 4)

Board Reference	Type	Description
J15	HSMC Port A JTAG header	Place a shunt on this header to include the HSMC port A in the JTAG chain.
J5	HSMC Port B JTAG header	Place a shunt on this header to include the HSMC port B in the JTAG chain.
J10	MAX II JTAG header	Place a shunt on this header to include the MAX II CPLD EPM2210 System Controller in the JTAG chain.
SW1	Clock enable DIP switch	Enables the oscillators when the switch is ON (positioned on the left side of the switch).
SW2	MAX II DIP switch	MAX II user DIP switches.
	66 MHz oscillator select	Selects the on board oscillator when driven low and selects the differential SMA inputs when driven high.
SW5	Rotary switch	Selects factory or user FPGA image to load on power up. After power up, this switch selects the power rail monitored from among a total of 12 rails.
D7-D12	Ethernet LEDs	Illuminates to show the connection speed as well as transmit or receive activity.
D15, D17-D20	MAX II LEDs	Illuminates when the MAX II CPLD EPM2210 System Controller is actively configuring the FPGA. The LED types include MAX_EMB (labeled as USER_1 on the board), MAX_LOAD, MAX_FACTORY, MAX_PB (labeled as USER_2 on the board), and MAX_ERROR.
D21	Power LED	Illuminates when power is present.
D22	Configuration done LED	Illuminates when the FPGA is configured.
D13, D14	HSMC port A status LEDs	You can configure these LEDs to indicate transmit or receive activity.
D16	HSMC port A present LED	Illuminates when a daughtercard is plugged into the HSMC port A.
D3, D4	HSMC port B status LEDs	You can configure these LEDs to indicate transmit or receive activity.
D5	HSMC port B present LED	Illuminates when a daughtercard is plugged into the HSMC port B.
Clock Circuitry		
X2	100 MHz oscillator	100.0 MHz crystal oscillator to the FPGA.
X3	66 MHz oscillator	66.6 MHz crystal oscillator with a single-ended input to the LVDS clock buffer (U22). This oscillator is also MUXed with the differential SMA clock inputs (J13 and J14) based on the CLK66_SEL input. The CLK66_SEL signal needs to be set to '0' on SW2 to enable the oscillator clock source. Two LVDS clocks are output from the clock buffer to the FPGA.
X4	125 MHz oscillator	125.000 MHz crystal oscillator to the LVDS clock buffer. Two LVDS clocks are output from the clock buffer to the FPGA.
X5	50 MHz oscillator	50 MHz single-ended oscillator to the FPGA and MAX II CPLD EPM2210 System Controller.
Y2	100 MHz oscillator (for MAX II CPLD)	100 MHz single-ended dedicated clock oscillator to the MAX II CPLD EPM2210 System Controller.
J17	Clock input SMAs	Drives LVPECL-compatible clock inputs into the FPGA.
J16	Clock output SMA	Drives out 2.5-V CMOS clock output from the FPGA.

Table 2–1. Stratix IV E FPGA Development Board Components (Part 3 of 4)

Board Reference	Type	Description
J13	CLKIN_P SMA (positive)	Drives LVPECL-compatible differential clock inputs into the LVDS clock buffer (U22).The CLK66_SEL signal needs to be set to '1' on SW2 to enable the SMA clock source. Two LVDS clocks are output from the clock buffer to the FPGA.
J14	CLKIN_N SMA (negative)	
General User Input/Output		
SW4	User DIP switch	Connects directly to the FPGA. When the switch is ON, a logic 0 is selected.
S1	Reset configuration push-button switch	Press to reconfigure the FPGA from flash memory.
S2	Factory configuration push-button switch	Press to reconfigure the FPGA to the factory default design.
S3	User 1 /User 2 push-button switch	User-defined push-button switch. Driven to the MAX II CPLD EPM2210 System Controller.
S4	CPU reset push-button switch	Press to reset the FPGA logic.
S5	System reset push-button switch	Press to reset the MAX II CPLD EPM2210 System Controller and FPGA logic.
S6-S9	User push-button switches	Four user push-button switches. Driven low when pressed.
D23-D30	User LEDs	Illuminates when driven low.
Display Ports		
J23	Character LCD header	Header which interfaces to the provided 16 character × 2 line LCD module along with two standoffs.
U29	Seven-segment LED	Quad digit seven-segment LED display. The display is controlled by the Stratix IV E FPGA device. Each segment of the display can be illuminated by driving a logic 0 to the connected device's I/O pin.
J27	Graphics LCD connector (bottom side)	Connector to plug in the flex cable from the 128 × 64 graphics display. Lift the connector latch to plug in the flex cable, and then close the latch.
Components and Interfaces		
J19	HSMC port A	Provides 17 LVDS channels per the HSMC specification.
J9	HSMC port B	Provides 17 LVDS channels per the HSMC specification.
J8	Gigabit Ethernet	RJ-45 connector providing a 10/100/1000 Ethernet connection via a Marvell 88E1111 PHY and interfaces to the FPGA-based Altera Triple Speed Ethernet MegaCore function in SGMII mode.
J12	Fan header	Header to plug in the fan.
J1	Speaker header	Optional speaker header for user design.
Memory Devices		
J20	DDR3 SDRAM DIMM x72 memory	DDR3 SDRAM DIMM (256 M x 72) 240-pin connector, populated with a dual rank 2-GB memory module, and interfaces with a 72-bit data width on the Vertical I/O (VIO) banks.
U24	RLDRAM II CIO x36 memory	533-MHz RLDRAM II CIO device in a 16 M x 36 configuration.
U11	QDR II+ x18 memory	QDR II+ SRAM device in a 4 M x 18 configuration for high-speed, low-latency memory access.

Table 2–1. Stratix IV E FPGA Development Board Components (Part 4 of 4)

Board Reference	Type	Description
U3	SSRAM x36 memory	A single 250-MHz 18-Mb (2 M x 36) SSRAM device with a 165-BGA package footprint. This footprint allows for both Flow-Through and Pipelined devices (single or dual cycle deselect).
U2	Flash x16 memory	Embedded memory device which provides a 16-bit 64-MB non-volatile memory port.
Power Supply		
J22	DC input jack	Accepts a 14-V – 20-V DC power supply.
SW3	Power switch	Switch to power on or off the board when power is supplied from the DC input jack.

Featured Device: Stratix IV E Device

The Stratix IV E FPGA development board features the Stratix IV E EP4SE530H35 device (U19) in a 1152-pin FBGA package.

For more information about the Stratix IV device family, refer to the *Stratix IV Device Handbook*.

Table 2–2 describes the features of the Stratix IV E EP4SE530H35 device.

Table 2–2. Stratix IV E EP4SE530H35 Device Features

ALMs	Equivalent LEs	M9K RAM Blocks	M144K RAM Blocks	Total RAM bits	18-bit × 18-bit Multipliers	Maximum User I/O Pins	PLLs	Package Type
212,480	531,200	1,280	64	27,376	1,024	736	8	1152-pin FBGA

Table 2–3 lists the Stratix IV E EP4SE530H35 component reference and manufacturing information.

Table 2–3. Stratix IV E EP4SE530H35 Device Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U19	FPGA, Stratix IV E F1152, leadfree	Altera Corporation	EP4SE530H35C2N	www.altera.com

I/O Resources

Figure 2–2 illustrates the bank organization and I/O count for the EP4SE530 device in the 1152-pin FBGA package.

Figure 2–2. EP4SE530 Device I/O Bank Diagram

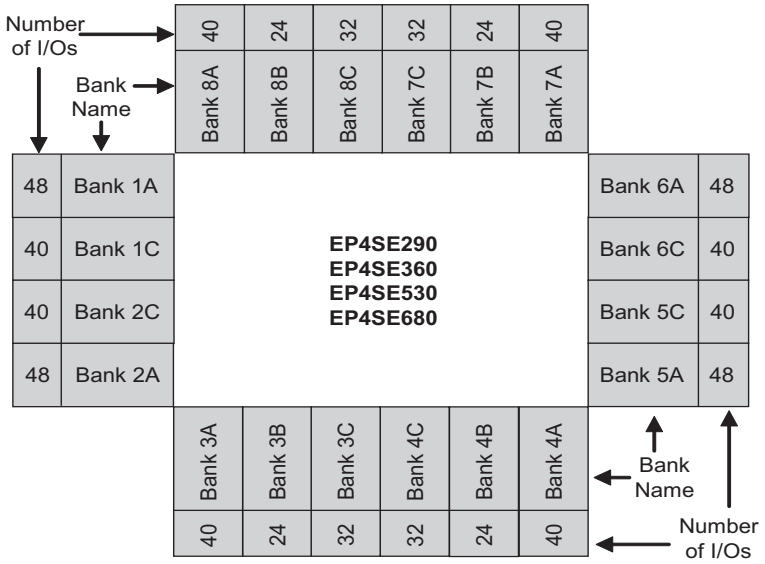


Table 2–4 lists the Stratix IV E device pin count and usage by function on the development board.

Table 2–4. Stratix IV E Device Pin Count and Usage

Function	I/O Standard	I/O Count	Special Pins
OSC/SMAs	1.5-V/2.5-V CMOS	13	12 Clock Inputs, 1 Output
DDR3 DIMM	1.5-V SSTL	153	18 DQS pins
QDR II+	1.5-V HSTL	69	2 CQ pins
RLDRAM II CIO	1.5-V HSTL	77	—
HSMC Port A	2.5-V CMOS + LVDS	86	3 Clock Inputs
HSMC Port B	2.5-V CMOS + LVDS	86	3 Clock Inputs
Flash, SSRAM, MAX	2.5-V CMOS	91	—
Gigabit Ethernet	2.5-V CMOS	36	—
User I/O (LEDs, DIP Switch, Push-Buttons)	1.5-V/2.5-V CMOS	21	—
14-pin LCD Header	2.5-V CMOS	11	—
Graphic Display	2.5-V CMOS	15	—
Seven-Segment Display	2.5-V CMOS	13	—
EEPROM	2.5-V CMOS	4	—
MAX II Control, Speaker	2.5-V CMOS	6	—
Device I/O Total:		681	

MAX II CPLD EPM2210 System Controller

The board utilizes the EPM2210 System Controller, an Altera MAX II CPLD, for the following purposes:

- FPGA configuration from flash memory
- Power consumption monitoring
- Temperature monitoring
- Fan control
- Virtual JTAG interface for PC-based power and temperature GUI
- Control registers for clocks
- Control registers for remote system update

Figure 2–3 illustrates the MAX II CPLD EPM2210 System Controller's functionality and external circuit connections as a block diagram.

Figure 2–3. MAX II CPLD EPM2210 System Controller Block Diagram

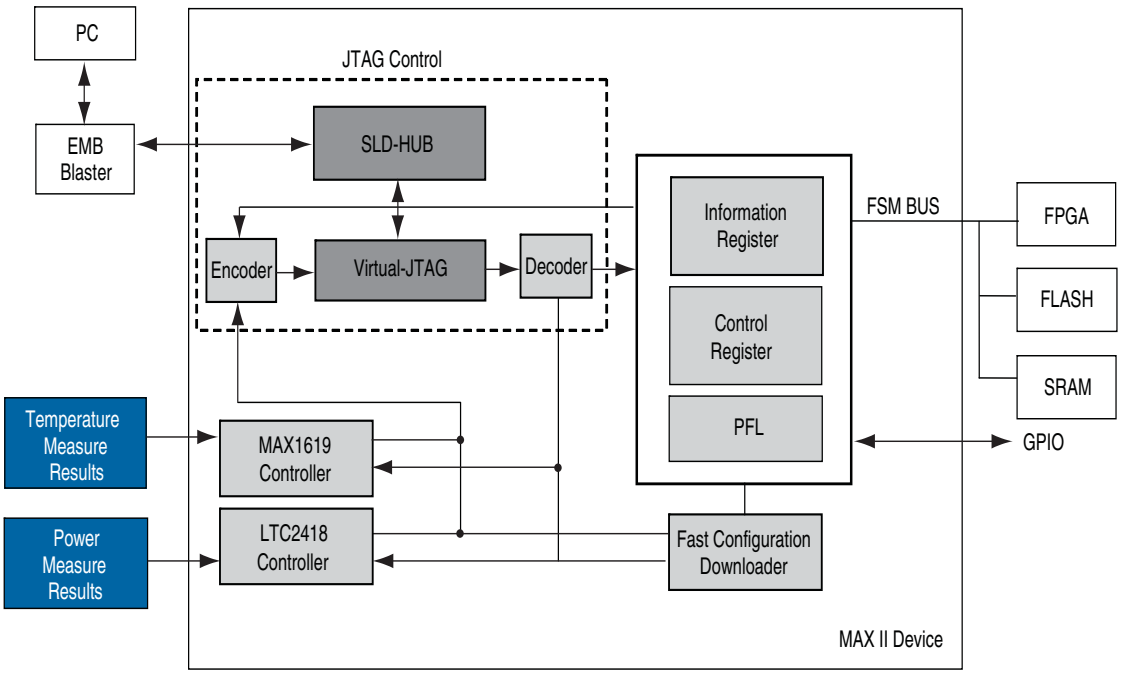


Table 2–5 lists the I/O signals present on the MAX II CPLD EPM2210 System Controller. The signal names and functions are relative to the MAX II device (U10).

Table 2–5. MAX II CPLD EPM2210 System Controller Device (U10) Pin-Out (Part 1 of 5)

Schematic Signal Name	I/O Standard	EPM2210 Pin Number	Stratix IV E Device Pin Number	Other Connections	Description
2.5V_FPGA_PG	2.5-V	E9	—	U41.7	FPGA 2.5-V power good monitor
2.5V_HSMC_PG	2.5-V	A7	—	U26.7	HSMC 2.5-V power good monitor

Table 2–5. MAX II CPLD EPM2210 System Controller Device (U10) Pin-Out (Part 2 of 5)

Schematic Signal Name	I/O Standard	EPM2210 Pin Number	Stratix IV E Device Pin Number	Other Connections	Description
3.3V_PG	2.5-V	E8	—	U9.G12	3.3-V power good monitor
CLK100_EN	2.5-V	J1	—	SW1.3, X2.1	100 MHz oscillator enable
CLK125_EN	2.5-V	J2	—	SW1.4, X4.1	125 MHz oscillator enable
CLK50_EN	2.5-V	H3	—	SW1.1, X5.1	50 MHz oscillator enable
CLK66_EN	2.5-V	H4	—	SW1.2, X3.1	66 MHz oscillator enable
CLK66_SEL	2.5-V	L14	—	SW2.8, U22.3	DIP-clock select SMA or oscillator
CLKIN_50	2.5-V	J12	J12	X5.3	50 MHz clock input
CLKIN_MAX_100	2.5-V	H12	—	Y2.3	100 MHz oscillator to the MAX II CPLD EPM2210 System Controller
FACTORY_CONFIGn	2.5-V	A10	—	S2.2	Load factory or user design at power-up
FLASH_ADVn	2.5-V	L13	D20	U2.F6	FSM bus flash memory address valid
FLASH_CEn	2.5-V	K14	K25	U2.B4	FSM bus flash memory chip enable
FLASH_CLK	2.5-V	L15	K24	U2.E6	FSM bus flash memory clock
FLASH_OEn	2.5-V	M16	K23	U2.F8	FSM bus flash memory output enable
FLASH_RDYBSYn	2.5-V	L11	C20	U2.F7	FSM bus flash memory ready
FLASH_RESETn	2.5-V	M15	G21	U2.D4	FSM bus flash memory reset
FLASH_WEn	2.5-V	L12	L22	U2.G8	FSM bus flash memory write enable
FPGA_CONF_DONE	2.5-V	E3	AH29	—	FPGA configuration done
FPGA_CONFIGn	2.5-V	E4	AE25	—	FPGA configuration active
FPGA_DATA0	2.5-V	D3	T28	—	FPGA configuration data
FPGA_DATA1	2.5-V	L1	T27	—	FPGA configuration data
FPGA_DATA2	2.5-V	K5	R34	—	FPGA configuration data
FPGA_DATA3	2.5-V	L2	R33	—	FPGA configuration data
FPGA_DATA4	2.5-V	K4	T25	—	FPGA configuration data
FPGA_DATA5	2.5-V	M1	T24	—	FPGA configuration data
FPGA_DATA6	2.5-V	K3	T32	—	FPGA configuration data
FPGA_DATA7	2.5-V	M2	R31	—	FPGA configuration data
FPGA_DCLK	2.5-V	C2	AL3	—	FPGA configuration clock
FPGA_STATUSn	2.5-V	C3	AH28	—	FPGA configuration ready
FSM_A0	2.5-V	N9	F22	—	FSM bus address
FSM_A1	2.5-V	T8	H23	U2.A1	FSM bus address
FSM_A2	2.5-V	T9	G23	U3.R6, U2.B1	FSM bus address
FSM_A3	2.5-V	R9	F23	U3.P6, U2.C1	FSM bus address
FSM_A4	2.5-V	P9	D27	U3.A2, U2.D1	FSM bus address
FSM_A5	2.5-V	T10	D28	U3.A10, U2.D2	FSM bus address
FSM_A6	2.5-V	P13	F25	U3.B2, U2.A2	FSM bus address

Table 2–5. MAX II CPLD EPM2210 System Controller Device (U10) Pin-Out (Part 3 of 5)

Schematic Signal Name	I/O Standard	EPM2210 Pin Number	Stratix IV E Device Pin Number	Other Connections	Description
FSM_A7	2.5-V	R10	F26	U3.B10, U2.C2	FSM bus address
FSM_A8	2.5-V	M10	G24	U3.N6, U2.A3	FSM bus address
FSM_A9	2.5-V	T11	F24	U3.P3, U2.B3	FSM bus address
FSM_A10	2.5-V	N10	E26	U3.P4, U2.C3	FSM bus address
FSM_A11	2.5-V	R11	D26	U3.P8, U2.D3	FSM bus address
FSM_A12	2.5-V	P10	A30	U3.P9, U2.C4	FSM bus address
FSM_A13	2.5-V	T12	A33	U3.P10, U2.A5	FSM bus address
FSM_A14	2.5-V	M11	B31	U3.P11, U2.B5	FSM bus address
FSM_A15	2.5-V	R12	A31	U3.R3, U2.C5	FSM bus address
FSM_A16	2.5-V	N11	B32	U3.R4, U2.D7	FSM bus address
FSM_A17	2.5-V	T13	A32	U3.R8, U2.D8	FSM bus address
FSM_A18	2.5-V	P11	M23	U3.R9, U2.A7	FSM bus address
FSM_A19	2.5-V	R13	L23	U3.R10, U2.B7	FSM bus address
FSM_A20	2.5-V	M12	B29	U3.R11, U2.C7	FSM bus address
FSM_A21	2.5-V	R14	C29	U3.B1, U2.C8	FSM bus address
FSM_A22	2.5-V	N12	C31	U3.A1, U2.A8	FSM bus address
FSM_A23	2.5-V	T15	D31	U3.B11, U2.G1	FSM bus address
FSM_A24	2.5-V	P12	F27	U3.C10, U2.H8	FSM bus address
FSM_A25	2.5-V	E13	D18	U3.P2, U2.B6	FSM bus address
FSM_A26	2.5-V	J16	W10	U2.B8	FSM bus address
FSM_D0	2.5-V	P4	G27	U3.J10, U2.F2	FSM bus data
FSM_D1	2.5-V	R1	F28	U3.J11, U2.E2	FSM bus data
FSM_D2	2.5-V	P5	E28	U3.K10, U2.G3	FSM bus data
FSM_D3	2.5-V	T2	D30	U3.K11, U2.E4	FSM bus data
FSM_D4	2.5-V	N5	C30	U3.L10, U2.E5	FSM bus data
FSM_D5	2.5-V	R3	F29	U3.L11, U2.G5	FSM bus data
FSM_D6	2.5-V	P6	E29	U3.M10, U2.G6	FSM bus data
FSM_D7	2.5-V	R4	J24	U3.M11, U2.H7	FSM bus data
FSM_D8	2.5-V	N6	J25	U3.D10, U2.E1	FSM bus data
FSM_D9	2.5-V	T4	A24	U3.D11, U2.E3	FSM bus data
FSM_D10	2.5-V	M6	A26	U3.E10, U2.F3	FSM bus data
FSM_D11	2.5-V	R5	B25	U3.E11, U2.F4	FSM bus data
FSM_D12	2.5-V	P7	A25	U3.F10, U2.F5	FSM bus data
FSM_D13	2.5-V	T5	J20	U3.F11, U2.H5	FSM bus data
FSM_D14	2.5-V	N7	K20	U3.G10, U2.G7	FSM bus data
FSM_D15	2.5-V	R6	K21	U3.G11, U2.E7	FSM bus data
FSM_D16	2.5-V	M7	K22	U3.D1	FSM bus data
FSM_D17	2.5-V	T6	C26	U3.D2	FSM bus data

Table 2–5. MAX II CPLD EPM2210 System Controller Device (U10) Pin-Out (Part 4 of 5)

Schematic Signal Name	I/O Standard	EPM2210 Pin Number	Stratix IV E Device Pin Number	Other Connections	Description
FSM_D18	2.5-V	P14	B26	U3.E1	FSM bus data
FSM_D19	2.5-V	R7	J22	U3.E2	FSM bus data
FSM_D20	2.5-V	P8	J21	U3.F1	FSM bus data
FSM_D21	2.5-V	T7	C24	U3.F2	FSM bus data
FSM_D22	2.5-V	N8	E25	U3.G1	FSM bus data
FSM_D23	2.5-V	R8	D25	U3.G2	FSM bus data
FSM_D24	2.5-V	F12	D24	U3.J1	FSM bus data
FSM_D25	2.5-V	D16	A27	U3.J2	FSM bus data
FSM_D26	2.5-V	F13	A29	U3.K1	FSM bus data
FSM_D27	2.5-V	D15	C27	U3.K2	FSM bus data
FSM_D28	2.5-V	F14	C28	U3.L1	FSM bus data
FSM_D29	2.5-V	D14	E23	U3.L2	FSM bus data
FSM_D30	2.5-V	E12	D23	U3.M1	FSM bus data
FSM_D31	2.5-V	C15	B28	U3.M2	FSM bus data
HSMA_PSNTn	2.5-V	F16	—	J19.160, R189	HSMC port A present
HSMB_PSNTn	2.5-V	G13	—	J9.160, R189	HSMC port B present
JTAG_EPM2210_TDO	2.5-V	M5	—	U35.5	JTAG data output for MAX II
JTAG_FPGA_TDO	2.5-V	L6	G29	U35.2	JTAG data output for FPGA
JTAG_TCK	2.5-V	P3	F30	J24.1, U8.L9, J9.35, J19.35	JTAG clock signal
JTAG_TMS	2.5-V	N4	H28	J24.5, U8.J11, J9.36, J19.36	JTAG mode select signal
MAX_CLK	2.5-V	H5	N3	—	FSM bus MAX II clock
MAX_CSn	2.5-V	L16	N29	—	FSM bus MAX II chip select
MAX_DIP0	2.5-V	E14	—	SW2.1	DIP - reserved
MAX_DIP1	2.5-V	D13	—	SW2.2	DIP - reserved
MAX_DIP2	2.5-V	K16	—	SW2.3	DIP - reserved
MAX_DIP3	2.5-V	N2	—	SW2.4	DIP - reserved
MAX_DIP4	2.5-V	N14	—	SW2.5	DIP - reserved
MAX_DIP5	2.5-V	M13	—	SW2.6	DIP - reserved
MAX_DIP6	2.5-V	N15	—	SW2.7	DIP - reserved
MAX_EMB	2.5-V	E15	—	D15	User-defined push-button switch (labeled as USER_1 on the board)
MAX_ERROR	2.5-V	H15	—	D20	FPGA configuration error LED
MAX_FACTORY	2.5-V	G16	—	D18	FPGA factory configuration LED
MAX_LOAD	2.5-V	H14	—	D17	FPGA configuration active LED
MAX_OEn	2.5-V	K13	K27	—	FSM bus MAX II output enable
MAX_PB	2.5-V	D4	—	S3	User-defined push-button switch (labeled as USER_2 on the board)

Table 2–5. MAX II CPLD EPM2210 System Controller Device (U10) Pin-Out (Part 5 of 5)

Schematic Signal Name	I/O Standard	EPM2210 Pin Number	Stratix IV E Device Pin Number	Other Connections	Description
MAX_PHASE_CLK0	2.5-V	J4	—	U30.A8	Power regulator 0 degrees phase control
MAX_PHASE_CLK180	2.5-V	K1	—	U33.B9	Power regulator 180 degrees phase control
MAX_TO_STRATIX4	2.5-V	H1	K1	—	Optional pin for user function
MAX_USER	2.5-V	G12	—	D19	User-defined LED (labeled as USER_1/USER_2 on the board)
MAX_WEn	2.5-V	K15	K28	—	FSM bus MAX II write enable
OVERTEMP	2.5-V	M4	—	Q1	Fan speed control
OVERTEMPn	2.5-V	E7	—	U18.9	Temperature monitor over-temperature indicator
PGM0	2.5-V	N13	—	SW5.1	Rotary switch input
PGM1	2.5-V	P15	—	SW5.2	Rotary switch input
PGM2	2.5-V	M14	—	SW5.4	Rotary switch input
PGM3	2.5-V	N16	—	SW5.8	Rotary switch input
PHASE0	2.5-V	C13	—	U49.4	Power clock 0 degrees
PHASE90	2.5-V	B16	—	U49.5, U36.A8	Power clock 90 degrees
PHASE180	2.5-V	C12	—	U49.6, U29.A8	Power clock 180 degrees
PHASE270	2.5-V	A15	—	U49.7, U6.A8	Power clock 270 degrees
RESET_CONFIGn	2.5-V	R16	—	S1	Force FPGA configuration push-button switch
SENSE_ADC_F0	2.5-V	E2	—	U44.2	Power monitor frequency
SENSE_CS0n	2.5-V	F5	—	U43.3	Power monitor 0 chip select
SENSE_CS1n	2.5-V	F2	—	U43.2	Power monitor 1 chip select
SENSE_SCK	2.5-V	E1	—	U44.5	Power monitor SPI clock
SENSE_SDI	2.5-V	F4	—	U44.4	Power monitor SPI data in
SENSE_SDO	2.5-V	F3	—	U44.3	Power monitor SPI data out
SSRAM_GWn	2.5-V	E11	—	U3.B7	FSM bus SSRAM global write enable
SSRAM_MODE	2.5-V	D11	—	U3.R1	FSM bus SSRAM burst sequence selection
SSRAM_ZZ	2.5-V	A13	—	U3.H11	FSM bus SSRAM power sleep mode
SYS_RESETn	2.5-V	M9	U31	S5	User-defined reset
TSENSE_ALERTN	2.5-V	J5	—	U18.11	Temperature monitor alert
TSENSE_SMB_CLK	2.5-V	L3	—	U18.14, U21.6	Temperature monitor SMB clock
TSENSE_SMB_DATA	2.5-V	N1	—	U18.12, U21.7	Temperature monitor SMB data
VDDQ_QDRII_PG	2.5-V	A9	—	U16.7	I/O supply

Table 2–6 lists the MAX II CPLD EPM2210 System Controller component reference and manufacturing information.

Table 2–6. MAX II CPLD EPM2210 System Controller Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U10	IC - MAX II CPLD EPM2210 256FBGA -3 LF 2.5V VCCINT	Altera Corporation	EPM2210F256C3N	www.altera.com

Configuration, Status, and Setup Elements

This section describes the board's configuration, status, and setup elements.

Configuration

This section describes the FPGA, flash memory, and MAX II CPLD EPM2210 System Controller device programming methods supported by the Stratix IV E FPGA development board. The Stratix IV E FPGA development board supports the following three configuration methods:

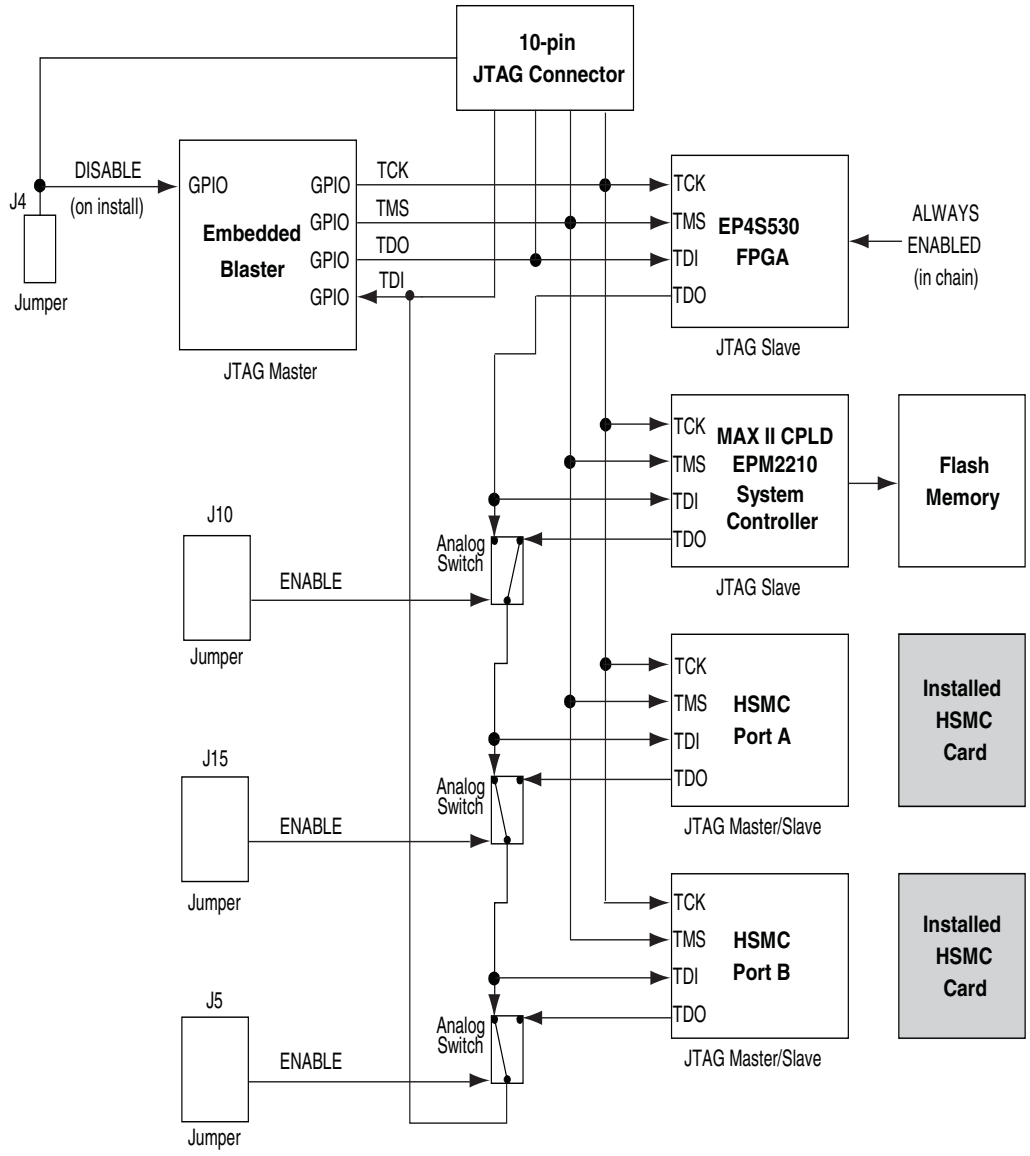
- Embedded USB-Blaster is the default method for configuring the FPGA at any time using the Quartus II Programmer in JTAG mode with the supplied USB cable.
- Flash memory programming using the Board Update Portal factory design.
- FPGA Programming from Flash memory for configuring the FPGA using stored images from the flash memory on either power-up or pressing the reset configuration push-button switch (S1).

FPGA Programming over Embedded USB-Blaster

The USB-Blaster is implemented using a USB Type-B connector (J6), a FTDI USB 2.0 PHY device (U7), and an Altera MAX II CPLD (U10). This allows the configuration of the FPGA using a USB cable directly connected between the USB port on the board (J6) and a USB port of a PC running the Quartus II software. The JTAG chain is normally mastered by the embedded USB-Blaster found in the MAX II CPLD EPM2210 System Controller.

The embedded USB-Blaster is automatically disabled when an external USB-Blaster is connected to the JTAG chain. Figure 2–4 illustrates the JTAG chain.

Figure 2–4. JTAG Chain



Each jumper shown in Figure 2–4 is located near its corresponding interface. To connect a device or interface in the chain, the corresponding shunt must be installed to the jumper. The FPGA, by default, is always in the chain.

A board must be plugged into the HSMC port in order for the chain to be contiguous. If there is a shunt on the jumper without a board plugged in to the corresponding HSMC port, the chain is broken and configuration cannot be performed.

The MAX II CPLD EPM2210 System Controller must be in the chain to use some of the GUI interfaces. For this setting, place a jumper shunt on the MAX II JTAG header (J10).

Flash Memory Programming

Flash memory programming is possible through a variety of methods using the Stratix IV E device.

The default method is to use the factory design called the Board Update Portal. This design is an embedded webserver, which serves the Board Update Portal web page. The web page allows you to select new FPGA designs including hardware, software, or both in an industry-standard S-Record File (**.flash**) and write the design to the user hardware page (page 1) of the flash memory over the network.

The secondary method is to use the pre-built parallel flash loader (PFL) design included in the development kit. The development board implements the Altera PFL megafunction for flash memory programming. The PFL megafunction is a block of logic that is programmed into an Altera programmable logic device (FPGA or CPLD). The PFL functions as a utility for writing to a compatible flash memory device. This pre-built design contains the PFL megafunction that allows you to write either page 0, page 1, or other areas of flash memory over the USB interface using the Quartus II software. This method is used to restore the development board to its factory default settings.

Other methods to program the flash memory can be used as well, including the Nios® II processor.

For more information on the Nios II processor, refer to the Nios II Processor page of the Altera website.

FPGA Programming from Flash Memory

On either power-up or by pressing the reset configuration push-button switch (S1), the MAX II CPLD EPM2210 System Controller's PFL configures the FPGA from the flash memory. The PFL megafunction reads 16-bit data from the flash memory and converts it to fast passive parallel (FPP) format. This 8-bit data is then written to the FPGA's dedicated configuration pins during configuration. The bit stream loaded into the FPGA is selected by the PGM rotary switch (SW5) connected to the MAX II CPLD EPM2210 System Controller.

Figure 2–5 illustrates the connection for FPGA programming from flash memory.

Figure 2–5. FPGA Programming from Flash Memory

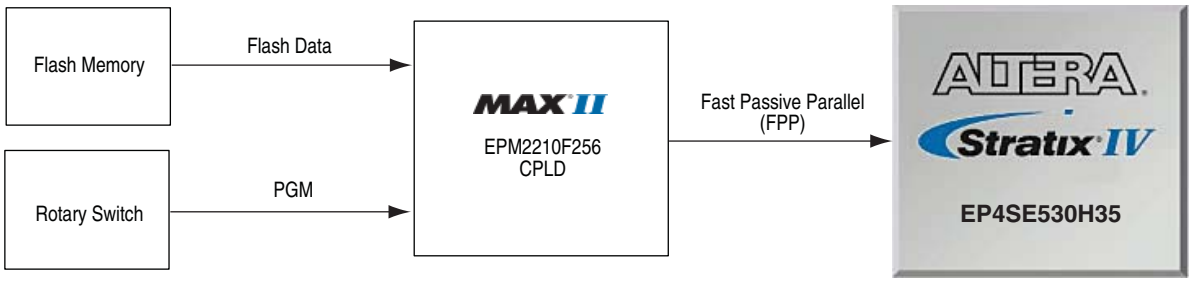


Table 2–7 shows the flash memory map storage.

Table 2–7. Flash Memory Map

Block Description	Size	Address Range
Unused	32 KB	0x03FF8000 - 0x03FFFFFF
Unused	32 KB	0x03FF0000 - 0x03FF7FFF
Unused	32 KB	0x03FE8000 - 0x03FEFFFF
Unused	32 KB	0x03FE0000 - 0x03FE7FFF
User software	11,669 KB	0x034C0000 - 0x03FDFFFF
User hardware	21,627 KB	0x02020000 - 0x034BFFFF
Reserved	128 KB	0x02000000 - 0x0201FFFF
zipfs (html, web content)	5,898 KB	0x01A60000 - 0x01FFFFFF
Factory software	5,898 KB	0x014C0000 - 0x01A5FFFF
Factory hardware	21,627 KB	0x00020000 - 0x014BFFFF
PFL option bits	32 KB	0x00018000 - 0x0001FFFF
Reserved	32 KB	0x00010000 - 0x00017FFF
Ethernet option bits	32 KB	0x00008000 - 0x0000FFFF
User design reset vector	32 KB	0x00000000 - 0x00007FFF

There are two pages reserved for the FPGA configuration data. The factory hardware page is considered page 0 and is loaded upon power-up if the rotary switch is set to '0'. Otherwise, the user hardware page 1 is loaded.

For more information on the following topics, refer to the respective documents:

- Board Update Portal, refer to the *Stratix IV E FPGA Development Kit User Guide*.
- PFL design, refer to the *Stratix IV E FPGA Development Kit User Guide*.
- PFL megafunction, refer to *AN 386: Using the Parallel Flash Loader with the Quartus II Software.*

Status Elements

The development board includes general user, board specific, and status LEDs. This section describes the status elements.

Table 2–8 lists the LED board references, names, and functional descriptions.

Table 2–8. Board-Specific LEDs (Part 1 of 2)

Board Reference	Schematic Signal Name	Description	I/O Standard	Stratix IV E Device Pin Number	Other Connections
D11	ENET_LED_TX	Green LED. Illuminates to indicate Ethernet PHY transmit activity. Driven by the Marvell 88E1111 PHY.	2.5-V	—	—
D12	ENET_LED_RX	Green LED. Illuminates to indicate Ethernet PHY receive activity. Driven by the Marvell 88E1111 PHY.		—	—
D7	ENET_LED_LINK10	Green LED. Illuminates to indicate Ethernet linked at 10 Mbps connection speed. Driven by the Marvell 88E1111 PHY.		—	—
D8	ENET_LED_LINK100	Green LED. Illuminates to indicate Ethernet linked at 100 Mbps connection speed. Driven by the Marvell 88E1111 PHY.		—	—
D9	ENET_LED_LINK1000	Green LED. Illuminates to indicate Ethernet linked at 1000 Mbps connection speed. Driven by the Marvell 88E1111 PHY.		N32	—
D10	ENET_LED_DUPLEX	Green LED. Illuminates to indicate Ethernet PHY is operating in Duplex mode. Driven by the Marvell 88E1111 PHY.		—	—
D15	MAX_EMB (labeled USER_1 on the board)	Green LED. Illuminates to indicate which configuration page is loaded.		—	U10.E15
D17	MAX_LOAD	Green LED. Illuminates when the MAX II CPLD EPM2210 System Controller is actively configuring the FPGA. Driven by the MAX II CPLD EPM2210 System Controller.		—	U10.H14
D18	MAX_FACTORY	Green LED. Illuminates when FPGA is configured with the default factory design.		—	U10.G16
D19	MAX_USER (labeled USER_2 on the board)	Green LED. Illuminates to indicate which configuration page is loaded.		—	U10.G12
D20	MAX_ERROR	Red LED. Illuminates when the MAX II CPLD EPM2210 System Controller fails to configure the FPGA. Driven by the MAX II CPLD EPM2210 System Controller.		—	U10.H15
D22	FPGA_CONF_DONE	Green LED. Illuminates when the FPGA is successfully configured. Driven by the MAX II CPLD EPM2210 System Controller.		AH29	U10.E3
D21	12V	Blue LED. Illuminates when 12-V power rail is active.	—	—	—

Table 2–8. Board-Specific LEDs (Part 2 of 2)

Board Reference	Schematic Signal Name	Description	I/O Standard	Stratix IV E Device Pin Number	Other Connections
D16	HSMA_PSNTn	Green LEDs. Illuminates when HSMC port A has a board or cable plugged-in such that pin 160 becomes grounded. Driven by the add-in card.	2.5-V	—	—
D5	HSMB_PSNTn	Green LEDs. Illuminates when HSMC port B has a board or cable plugged-in such that pin 160 becomes grounded. Driven by the add-in card.		—	—

Table 2–9 lists the board-specific LEDs component references and manufacturing information.

Table 2–9. Board-Specific LEDs Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
D5, D7-D19, D22-D30	Green LEDs	Lumex Inc.	SML-LX1206GC-TR	www.lumex.com
D20	Red LED	Lumex Inc.	SML-LX1206IC-TR	www.lumex.com
D21	Blue LED	Lumex Inc.	SML-LX1206USBC-TR	www.lumex.com

Setup Elements

The development board includes several different kinds of setup elements. This section describes the following setup elements:

- MAX II DIP switch
- User DIP switch
- Clock enable DIP switch
- JTAG chain jumpers
- On-Board memory headers
- Reset configuration push-button switch
- Rotary switch

MAX II DIP Switch

The MAX II DIP switch (SW2) provides user-specific control settings for the MAX II CPLD EPM2210 System Controller logic design. There is a 66-MHz clock select switch which is used to select between the on-board oscillator or the user-defined external clock source supplied on the SMA inputs. Table 2–10 shows the switch controls and descriptions.

Table 2–10. MAX II DIP Switch Controls

Board Reference	Schematic Signal Name	Description	I/O Standard	Stratix IV E Device Pin Number	Other Connections	Default
SW2.1	DIP0	MAX II user-defined DIP switch. When the switch is in the OPEN or OFF position, a logic 1 is selected. When the switch is in the CLOSED or ON position, a logic 0 is selected.	2.5-V	—	U10.E14	ON
SW2.2	DIP1			—	U10.D13	ON
SW2.3	DIP2			—	U10.K16	ON
SW2.4	DIP3			—	U10.N2	ON
SW2.5	DIP4			—	U10.N14	ON
SW2.6	DIP5			—	U10.M13	ON
SW2.7	DIP6			—	U10.N15	ON
SW2.8	CLK66_SEL	Selects either the on-board oscillator or the SMA inputs. ON : SMA input clock select OFF : 66 MHz clock select		—	U10.L14	ON

Table 2–11 lists the MAX II DIP switch component reference and manufacturing information.

Table 2–11. MAX II DIP Switch Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
SW2	Eight-Position slide DIP switch	Grayhill	76SB08ST	www.grayhill.com

User DIP Switch

Board reference SW4 is a 8-pin DIP switch. The switches in SW4 are user-defined and provided for additional FPGA input control. There is no board-specific function for these switches. Table 2–12 shows the user DIP switch controls and descriptions.

Table 2–12. User DIP Switch Controls

Board Reference	Schematic Signal Name	Description	I/O Standard	Stratix IV E Device Pin Number	Other Connections	Default
SW4.1	USER_DIPSW0	User-Defined DIP switch connected to the FPGA device. When the switch is in the OFF position, a logic 1 is selected. When the switch is in the ON position, a logic 0 is selected.	2.5-V	A28	—	ON
SW4.2	USER_DIPSW1			A19	—	ON
SW4.3	USER_DIPSW2			C18	—	ON
SW4.4	USER_DIPSW3			A20	—	ON
SW4.5	USER_DIPSW4			K19	—	ON
SW4.6	USER_DIPSW5			J19	—	ON
SW4.7	USER_DIPSW6			L19	—	ON
SW4.8	USER_DIPSW7			L20	—	ON

Table 2–13 lists the user DIP switch component reference and manufacturing information.

Table 2–13. User DIP Switch Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
SW4	Eight-Position slide DIP switch	Grayhill	76SB08ST	www.grayhill.com

Clock Enable DIP Switch

The clock enable DIP switch (SW1) enables or disables the on-board oscillators. Table 2–14 shows the switch controls and descriptions.

Table 2–14. Clock Enable DIP Switch Controls

Board Reference	Schematic Signal Name	Description	I/O Standard	Stratix IV E Device Pin Number	Other Connections	Default
1	CLK50_EN	Clock enable DIP switch. When the switch is in the OPEN or ENABLE position, a logic 1 is selected. When the switch is in the CLOSED or DISABLE position, a logic 0 is selected.	2.5-V	—	U10.H3	ENABLE
2	CLK66_EN			—	U10.H4	ENABLE
3	CLK100_EN			—	U10.J1	ENABLE
4	CLK125_EN			—	U10.J2	ENABLE

Table 2–15 lists the clock enable DIP switch component reference and manufacturing information.

Table 2–15. Clock Enable DIP Switch Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
SW1	Four-Position slide DIP switch	C & K Components/ TTI Inc.	TDA04H0SB1	www.ck-components.com www.ttiinc.com

JTAG Chain Jumpers

The JTAG chain jumpers are provided to either remove or include devices in the active JTAG chain. However, the Stratix IV E FPGA device is always in the JTAG chain. Table 2–16 shows the jumper controls and its descriptions.

Table 2–16. JTAG Chain Jumper Controls

Board Reference	Schematic Signal Name	Description	Default
J4	USB_DISABLEn	ON : Embedded USB-Blaster disable OFF : Embedded USB-Blaster enable	OFF
J10	MAXII_JTAG_EN	ON : MAX II CPLD EPM2210 System Controller in-chain OFF : Bypass MAX II CPLD EPM2210 System Controller	ON
J15	HSMA_JTAG_EN	ON : HSMA in-chain OFF : Bypass HSMA	OFF
J5	HSMB_JTAG_EN	ON : HSMB in-chain OFF : Bypass HSMB	OFF
J21	VCC_VCCL_SEL	ON (Pins 1 and 2) : VCC and VCCL = 0.9 V (if R126 is installed) ON (Pins 2 and 3) : VCC and VCCL = 1.1 V (do not place the shunt on these pins) OFF : VCC and VCCL = 0.6 V (do not leave the shunt off)	ON (Pins 1 and 2)
J2	MSEL0	ON : Logic 0 is selected for MSEL OFF : Logic 1 is selected for MSEL	ON

Table 2–17 lists the JTAG chain jumper component references and manufacturing information.

Table 2–17. JTAG Chain Jumper Component References and Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
J2, J21	2×1 pin, 100 mil header	Samtec	TSW-103-08-G-S	www.samtec.com
J4, J5, J10, J15	2×1 pin, 2 mm header	Samtec	TMM-102-01-S-S	www.samtec.com

On-Board Memory Headers

The on-board memory headers are provided to set the output impedance and I/O voltage level for the QDR II+ and RLDRAM II memories. Table 2–16 shows the header settings and its descriptions.

Table 2–18. On-Board Memory Header Settings

Board Reference	Schematic Signal Name	Description	Default
J7	QDRII_ZQ	Shunt on pins 1-2: Min output impedance Shunt on pins 3-4: 50-Ω output impedance Shunt on pins 5-6: 60-Ω output impedance	Shunt on pins 3-4
J11	–	Shunt ON: QDR II VDDQ at 1.8 V Shunt OFF: QDR II VDDQ at 1.5 V	Shunt OFF
J18	–	Shunt ON: RLDRAMII VDDQ at 1.8 V Shunt OFF: RLDRAMII VDDQ at 1.5 V	Shunt OFF
J28	RLDC_ZQ	Shunt on pins 1-2: Max output impedance Shunt on pins 3-4: 60-Ω output impedance Shunt on pins 5-6: 50-Ω output impedance	Shunt OFF
J29	DDR3_DIMM_TEST[5:1]	User-defined test pins for the DDR3 (optional).	Shunt OFF

Table 2–19 lists the on-board memory header component references and manufacturing information.

Table 2–19. On-Board Memory Header Component References and Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
J7, J28	3×2 vertical header	Samtec	TSW-103-07-L-D	www.samtec.com
J11, J18	2×1 2 mm pitch vertical header	Samtec	TMM-102-01-S-S	www.samtec.com
J29	2×5 100 mil pitch vertical header	Samtec	TSM-105-01-T-DV-TR	www.samtec.com

Reset Configuration Push-button Switch

The reset configuration push-button switch (S1), is an input to the MAX II CPLD EPM2210 System Controller. The push-button switch forces a reconfiguration of the FPGA from flash memory. The location in the flash memory is based on the rotary switch setting when the configuration push-button is released. Valid settings include 0 and 1 on the two pages in flash memory reserved for FPGA designs.

Table 2–20 lists the reset configuration push-button switches component reference and manufacturing information.

Table 2–20. Reset Configuration Push-Button Switches Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
S1	Push-Button switch	Panasonic	EVQPAC07K	www.panasonic.com/industrial/components/components.html

Rotary Switch

The 16-position rotary switch (SW5) is wired to the MAX II CPLD EPM2210 System Controller. This rotary switch serves the following purposes:

- At power-up or when the reset configuration push-button switch (S1) is pressed, this switch selects either the factory (page 0) or the user (page 1) design to load into the FPGA. The FPGA reconfiguration can also be done by writing a logic 1 to the `srst` register over the FSM bus in the MAX II CPLD EPM2210 System Controller.
- After power-up, the rotary switch selects the power rail monitored from among a total of 12 rails. The power information is displayed in the Power GUI on a host PC with a USB connection to the board.
- User applications can obtain the switch value by reading the `rsr` register over the FSM bus in the MAX II CPLD EPM2210 System Controller.

Refer to Table 2–53 on page 2–59 for the specific power rails that are measured based on the rotary switch position.

Table 2–21 lists the rotary switch component reference and manufacturing information.

Table 2–21. Rotary Switch Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
SW5	16-position rotary switch	Grayhill	94HCB16WT	www.grayhill.com

Clock Circuitry

This section describes the board's clocking circuitry.

Stratix IV E FPGA Clocks

The development board has several on-board oscillators.

Figure 2–6 shows the Stratix IV E FPGA development board clocking diagram.

Figure 2–6. Stratix IV E FPGA Development Board Clocking Diagram

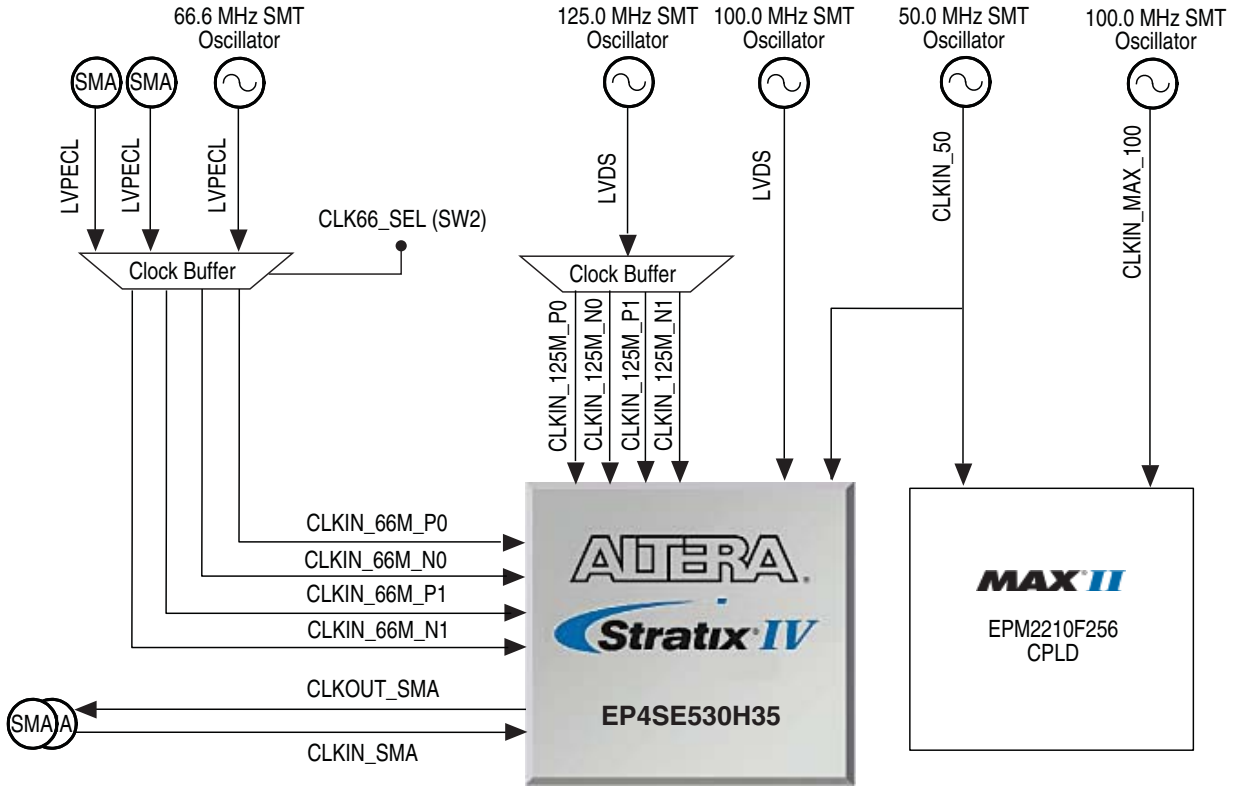


Table 2–22 shows the clock distribution for the Stratix IV E FPGA development board.

Table 2–22. Stratix IV E FPGA Development Board Clock Distribution (Part 1 of 2)

Frequency	Schematic Signal Name	Signal Originates From	Signal Propagates To
66.6 MHz	CLKIN_66M_P0	X3.3	U19.W33 U19.W34 U19.AN16 U19.AP16 (From clock buffer, IDT ICS8543, U22)
	CLKIN_66M_N0		
	CLKIN_66M_P1		
	CLKIN_66M_N1		
User Input	CLKIN_SMA_P	J13	
	CLKIN_SMA_N	J14	
125.00 MHz	CLKIN_125M_P0	X4.4	U19.T33 U19.B16 (From clock buffer NB6L11SMNG, U40)
	CLKIN_125M_P1		
	CLKIN_125M_N0	X4.5	U19.T34 U19.A16 (From clock buffer NB6L11SMNG, U40)
	CLKIN_125M_N1		
100.00 MHz	CLKIN_100M_P0	X2.4	U19.B17
	CLKIN_100M_N0	X2.5	U19.A17

Table 2–22. Stratix IV E FPGA Development Board Clock Distribution (Part 2 of 2)

Frequency	Schematic Signal Name	Signal Originates From	Signal Propagates To
50 MHz	CLKIN_50	X5.3	U19.V33 and U10.J12
6.000 MHz	USB_XTAL	Y1	U7.27 and U7.28 (USB PHY, FT245BL)
24 MHz	CLKIN_24MHZ	Y3	U8.E1 (Embedded USB-Blaster, EPM240M100)
100.00 MHz	CLKIN_MAX_100	Y2.3	U10.H12 (MAX II CPLD EPM2210 System Controller)
25 MHz	ENET_XTAL_25MHZ	X1	U15.55 (Ethernet PHY, Marvell 88E1111 PHY)

Table 2–23 lists the crystal oscillators component references and manufacturing information.

Table 2–23. Crystal Oscillator Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
Y1	6 MHz Crystal Oscillator	Abracon Corporation	ABL-6.000MHZ-B2	www.abracon.com
X1	25 MHz Crystal Oscillator, LVCMOS/LVTTL	ECS, Inc.	ECS-3953C-250-B	www.ecsxtal.com
X5	50 MHz Oscillator, 2.5 V, clock oscillator, SMD	ECS, Inc.	ECS-3525-500-B-xx	www.ecsxtal.com
Y2	100 MHz Oscillator, 1.8 V, CMOS clock oscillator, SMD	Pletronics	SM5545TEX-100.00M	www.pletronics.com
X4	125 MHz Crystal Oscillator, 2.5 V, LVDS	Epson	EG-2121CA 125.0000M-LGPNL3	www.eea.epson.com
Y3	24 MHz Oscillator, 3.3 V, CMOS clock oscillator, SMD	Pletronics	SM5545TEV-24.0M	www.pletronics.com
X2	100 MHz Crystal Oscillator, 2.5 V, LVDS	Epson	EG-2121CA 100.0000M-LHPNL3	www.eea.epson.com
X3	66 MHz Crystal Oscillator	ECS, Inc.	ECS-3953C-666-X	www.ecsxtal.com

General User Input/Output

This section describes the user I/O interface to the FPGA, including the push-buttons, DIP switches, and LCD displays.

User-Defined Push-Button Switches

The development board includes four user-defined push-button switches. For information on the board specific push-button switches, refer to "Setup Elements" on page 2–17.

Board references S6 to S9 are push-button switches that allow you to interact with the Stratix IV E device. When the switch is pressed and held down, the device pin is set to logic 0; when the switch is released, the device pin is set to logic 1. There is no board-specific function for these general user push-button switches.

The board reference S4 is the CPU reset push-button switch, CPU_RESETn, which is an input to the Stratix IV E FPGA device. The CPU_RESETn is intended to be the master reset signal for the FPGA design loaded into the Stratix IV E device. The CPU_RESETn signal must be enabled within the Quartus II software for this reset function to work. Otherwise, the CPU_RESETn acts as a regular I/O pin. When enabled in the Quartus II software, and then pulled high on the board, this switch resets every register within the FPGA.

Table 2–24 lists the user-defined push-button switch schematic signal names and their corresponding Stratix IV E FPGA device pin numbers.

Table 2–24. User-Defined Push-Button Switch Schematic Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number	Other Connections
S1	Reset configuration push-button switch. Driven to the MAX II CPLD System Controller to reconfigure the FPGA from flash memory.	RESET_CONFIGn	2.5-V	—	U10.R16
S2	Factory configuration push-button switch. Driven to the MAX II CPLD System Controller to reconfigure the FPGA to the default factory design.	FACTORY_CONFIGn		—	U10.A10
S3	User-defined push-button switch. Driven to the MAX II CPLD System Controller.	MAX_PB (Labeled as USER_1/USER_2 on the board)		—	U10.D4
S4	CPU reset push-button switch. Driven to the Stratix IV E device to reset the FPGA.	CPU_RESETn		Y4	—
S5	User-defined reset push-button switch. Driven to MAX II CPLD and Stratix IV E device for logic reset.	SYS_RESETn		U31	U10.M9
S6	User-defined push-button switch. Driven to the Stratix IV E device.	USER_PB0		L17	—
S7		USER_PB1		F16	—
S8		USER_PB2		E16	—
S9		USER_PB3		K17	—

Table 2–25 lists the user-defined push-button switch component reference and the manufacturing information.

Table 2–25. User-Defined Push-button Switch Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
S1-S9	Push-Button Switch	Panasonic	EVQPAC07K	www.panasonic.com/industrial/components/components.html

User-Defined LEDs

The development board includes general and HSMC user-defined LEDs. This section describes all user-defined LEDs. For information on board specific or status LEDs, refer to "Status Elements" on page 2–15.

General User-Defined LEDs

Board references D23 through D30 are eight user-defined LEDs which allow status and debugging signals to be driven to the LEDs from the designs loaded into the Stratix IV E FPGA device. The LEDs illuminate when a logic 0 is driven, and turns off when a logic 1 is driven. There is no board-specific function for these LEDs.

Table 2–26 lists the user-defined LED schematic signal names and their corresponding Stratix IV E FPGA pin numbers.

Table 2–26. User-Defined LED Schematic Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number
D30	User-defined LEDs. Driving a logic 0 on the I/O pin turns the LED ON. Driving a logic 1 on the I/O pin turns the LED OFF.	USER_LED0	2.5-V	F21
D29		USER_LED1		C23
D28		USER_LED2		B23
D27		USER_LED3		A23
D26		USER_LED4		D19
D25		USER_LED5		C19
D24		USER_LED6		F19
D23		USER_LED7		E19

Table 2–27 lists the user-defined LED component reference and the manufacturing information.

Table 2–27. User-Defined LED Component Reference and Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
D23-D30	Green LEDs	Lumex Inc.	SML-LX1206GC-TR	www.lumex.com

HSMC User-Defined LEDs

The HSMC port A and B have three LEDs located nearby. The LEDs are labeled TX, RX, and PSNTn. The PSNTn LED illuminates when a daughtercard is plugged into the respective HSMC port. There are no board-specific functions for the TX and RX LEDs but they are intended to display data flow to and from the connected daughtercards and are driven by the Stratix IV E FPGA device.

Table 2–28 lists the HSMC user-defined LED schematic signal names and their corresponding Stratix IV E FPGA pin numbers.

Table 2–28. HSMC User-Defined LED Schematic Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number
D13	User-defined green LEDs. Illuminates when data is being transmitted by the FPGA.	HSMA_TX_LED	2.5-V	G30
D14	User-defined green LEDs. Illuminates when data is being received by the FPGA.	HSMA_RX_LED		AK12
D3	User-defined green LEDs. Illuminates when data is being transmitted by the FPGA.	HSMB_TX_LED		N4
D4	User-defined green LEDs. Illuminates when data is being received by the FPGA.	HSMB_RX_LED		P23

Table 2–29 lists the HSMC user-defined LED component reference and the manufacturing information.

Table 2–29. HSMC User-Defined LED Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
D3, D4, D13, D14	Green LEDs	Lumex Inc.	SML-LX1206GC-TR	www.lumex.com

Seven-Segment LED Display

The development board includes one quad digit seven-segment LED display. The display is controlled by the Stratix IV E FPGA device. Each segment of the display can be illuminated by driving a logic 0 to the connected device's I/O pin.

Table 2–30 summarizes the display segments and pin assignments for the seven-segment LED display.

Table 2–30. Seven-Segment LED Display Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number
U29.12	A	SEVEN_SEG_A	2.5-V	F33
U29.11	B	SEVEN_SEG_B		N30
U29.3	C	SEVEN_SEG_C		L32
U29.8	D	SEVEN_SEG_D		R26
U29.2	E	SEVEN_SEG_E		L31
U29.9	F	SEVEN_SEG_F		M27

Table 2–30. Seven-Segment LED Display Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number
U29.7	G	SEVEN_SEG_G	2.5-V	K29
U29.5	DP	SEVEN_SEG_DP		L29
U29.1	DIG_SEL1	SEVEN_SEG_SEL1		M26
U29.10	DIG_SEL2	SEVEN_SEG_SEL2		R28
U29.4	DIG_SEL3	SEVEN_SEG_SEL3		J29
U29.6	DIG_SEL4	SEVEN_SEG_SEL4		R27
U29.13	DIG_MINUS	SEVEN_SEG_MINUS		K30

Table 2–29 lists the seven-segment LED display component reference and the manufacturing information.

Table 2–31. Seven-Segment LED Display Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
U29	Quad digit seven-segment LED	Lumex Inc.	LDQ-M2212RI	www.lumex.com

Character LCD

The development board contains a single 14-pin 0.1" pitch dual-row header that interfaces to a 16 character × 2 line Lumex character LCD display. The LCD has a 14-pin receptacle that mounts directly to the board's 14-pin character LCD header (J23), so it can be easily removed for access to components under the display. You can also use the character LCD header for debugging or other purposes.

Table 2–32 summarizes the character LCD pin assignments. The signal names are relative to the Stratix IV E FPGA.

Table 2–32. Character LCD Header Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number
J23.1	Power	5.0V	—	—
J23.2	Ground	GND	—	—
J23.3	Ground	GND	—	—
J23.4	LCD data or command select	LCD_D_Cn	2.5-V	AF13
J23.5	LCD write enable	LCD_WEn		AF14
J23.6	LCD chip select	LCD_CSn		AM9
J23.7	LCD data bus	LCD_DATA0		AP9
J23.8	LCD data bus	LCD_DATA1		AP11
J23.9	LCD data bus	LCD_DATA2		AN10
J23.10	LCD data bus	LCD_DATA3		AP10
J23.11	LCD data bus	LCD_DATA4		AE13
J23.12	LCD data bus	LCD_DATA5		AE14

Table 2–32. Character LCD Header Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number
J23.13	LCD data bus	LCD_DATA6	2.5-V	AE15
J23.14	LCD data bus	LCD_DATA7		AF15

Table 2–33 shows the character LCD pin definitions, and is an excerpt from the Lumex data sheet.

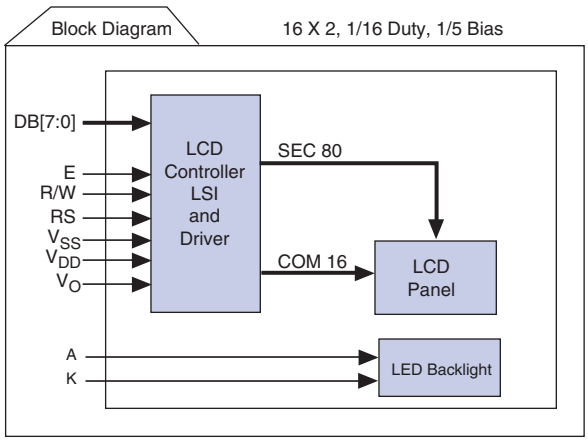
For more information such as timing, character maps, interface guidelines, and other related documentation, visit www.lumex.com.

Table 2–33. Character LCD Pin Definitions and Functions

Pin Number	Symbol	Level	Function	
1	V_{DD}	—	Power supply	5 V
2	V_{SS}	—		GND (0 V)
3	V_0	—		For LCD drive
4	RS	H/L	Register select signal H: Data input L: Instruction input	
5	R/W	H/L	H: Data read (module to MPU) L: Data write (MPU to module)	
6	E	H, H to L	Enable	
7–14	DB0–DB7	H/L	Data bus, software selectable 4-bit or 8-bit mode	

Figure 2–7 shows the functional block diagram of the Lumex LCD display.

Figure 2–7. Character LCD Display Block Diagram



The particular model used does not have a backlight.

Table 2–34 lists the LCD component references and the manufacturing information.

Table 2–34. LCD Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
J23	2×7 pin, 100 mil, vertical header	Samtec	TSM-107-01-G-DV	www.samtec.com
	2×16 character LCD display, 5×8 dot matrix	Lumex Inc.	LCM-S01602DSR/C	www.lumex.com

Graphics LCD

The development board contains a single 30-pin 0.5 mm pitch connector that interfaces to a 128 × 64 graphics LCD display.

Table 2–35 summarizes the graphics LCD pin assignments. The signal names are relative to the Stratix IV E FPGA.

Table 2–35. Graphics LCD Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number
J27.1	LCD chip select	LCD1_CSn	2.5-V	N25
J27.2	LCD reset	LCD1_RSTn		AL12
J27.3	LCD data or command select	LCD1_D_Cn		N26
J27.4	LCD write enable	LCD1_WEn		N31
J27.5	LCD	LCD1_E_RDn		H31
J27.6	LCD data bus	LCD1_DATA0		F31
J27.7	LCD data bus	LCD1_DATA1		H32
J27.8	LCD data bus	LCD1_DATA2		J30
J27.9	LCD data bus	LCD1_DATA3		E34
J27.10	LCD data bus	LCD1_DATA4		J33
J27.11	LCD data bus	LCD1_DATA5	2.5-V	R24
J27.12	LCD data bus	LCD1_DATA6		P25
J27.13	LCD data bus	LCD1_DATA7		M30
J27.28	LCD interface mode select	LCD1_BS1		N24
J27.29	LCD parallel or serial data select	LCD1_SERn		R29

Table 2–36 lists the graphics LCD component references and the manufacturing information.

Table 2–36. Graphics LCD Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
J27	FPC/FFC 30POS, 0.5 mm pitch Horz SMD bottom contact, flick lock	Hirose Electronic Co.	FH12S-30S-0.5SH(55)	www.hirose-connectors.com
	128 × 64 graphics LCD display	Optrex America, Inc.	F-55472GNFQJ-LB-AEN	www.optrex.com

Components and Interfaces

This section describes the development board's communication ports and interface cards relative to the Stratix IV E FPGA device. The development board supports the following communication ports:

- 10/100/1000 Ethernet
- Embedded USB-Blaster
- HSMC

10/100/1000 Ethernet

The development board incorporates a triple speed 10/100/1000 BASE-T Ethernet port. This implementation uses a discrete Ethernet PHY (Marvell 88E1111) device and RJ45 connector with integrated magnetics connected to the FPGA. The Marvell 88E1111 PHY device is an auto-negotiating Ethernet PHY with a GMII, RGMII, or SGMII interface to the FPGA. The MAC function must be provided in the FPGA for typical networking applications. The device uses 2.5-V and 1.1-V power rails and requires a 25-MHz reference clock driven from a dedicated oscillator.

Table 2–37 lists the SGMII and RGMII interface pin assignments to the FPGA for the Ethernet PHY device.

Table 2–37. Ethernet PHY Pin Assignments, Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number	Other Connections
U15.8	RGMII transmit clock	ENET_GTX_CLK	2.5-V	M33	—
U15.23	Management bus interrupt	ENET_INTn		F32	—
U15.70	Duplex/Collision LED	ENET_LED_DUPLEX		—	—
U15.76	10 Mb Link LED	ENET_LED_LINK10		—	U15.64, U15.59
U15.74	100 Mb Link LED	ENET_LED_LINK100		—	—
U15.73	1000 Mb Link LED	ENET_LED_LINK1000			—
U15.69	RX Data Active LED	ENET_LED_RX		—	U15.65
U15.68	TX Data Active LED	ENET_LED_TX		—	U15.61
U15.25	Management bus data clock	ENET_MDC		K34	—
U15.24	Management bus data	ENET_MDIO		N27	—
U15.28	Device reset	ENET_RESETn		M31	—
U15.30	Reset	ENET_RSET		—	—
U15.2	RSGMII receive clock	ENET_RX_CLK		K32	—
U15.83	GMII collision	ENET_RX_COL		J31	—
U15.84	GMII carrier sense	ENET_RX_CRS		K33	—
U15.95	RSGMII receive data bus	ENET_RX_D0		M24	—
U15.92	RSGMII receive data bus	ENET_RX_D1		P34	—
U15.93	RSGMII receive data bus	ENET_RX_D2		J34	—

Table 2–37. Ethernet PHY Pin Assignments, Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number	Other Connections
U15.91	RSGMII receive data bus	ENET_RX_D3	2.5-V	M34	—
U15.90	RSGMII receive data bus	ENET_RX_D4		C34	—
U15.89	RSGMII receive data bus	ENET_RX_D5		P29	—
U15.87	RSGMII receive data bus	ENET_RX_D6		H34	—
U15.86	RSGMII receive data bus	ENET_RX_D7		J32	—
U15.94	RSGMII receive control	ENET_RX_DV		P32	—
U15.3	GMII receive error	ENET_RX_ER		K31	—
U15.75	SGMII receive data	ENET_RX_N	LVDS	D34	—
U15.77	SGMII receive data	ENET_RX_P		D33	—
U15.80	SGMII 625 MHz Clock	ENET_S_CLKN		V32	—
U15.79	SGMII 625 MHz Clock	ENET_S_CLKP		V31	—
U15.4	25 MHz MII Transmit Clock	ENET_TX_CLK	2.5-V	R32	—
U15.11	RGMII transmit data bus	ENET_TX_D0		P28	—
U15.12	RGMII transmit data bus	ENET_TX_D1		F34	—
U15.14	RGMII transmit data bus	ENET_TX_D2		N34	—
U15.16	RGMII transmit data bus	ENET_TX_D3		L28	—
U15.17	RGMII transmit data bus	ENET_TX_D4		G33	—
U15.18	RGMII transmit data bus	ENET_TX_D5		C33	—
U15.19	RGMII transmit data bus	ENET_TX_D6	2.5-V	N33	—
U15.20	RGMII transmit data bus	ENET_TX_D7		G31	—
U15.9	RGMII transmit control	ENET_TX_EN		L34	—
U15.7	GMII transmit error	ENET_TX_ER		M29	—
U15.81	SGMII data input	ENET_TX_N	LVDS	T30	—
U15.82	SGMII data input	ENET_TX_P		T29	—
U15.55	25 MHz crystal	ENET_XTAL_25MHZ	2.5-V	—	X1.4
U15.31	Media dependent interface	MDI_N0		—	J8.2
U15.34	Media dependent interface	MDI_N1		—	J8.6
U15.41	Media dependent interface	MDI_N2		—	J8.5
U15.43	Media dependent interface	MDI_N3		—	J8.8
U15.29	Media dependent interface	MDI_P0		—	J8.1
U15.33	Media dependent interface	MDI_P1		—	J8.3
U15.39	Media dependent interface	MDI_P2		—	J8.4
U15.42	Media dependent interface	MDI_P3		—	J8.7

Table 2–38 lists the Ethernet PHY device component references and manufacturing information.

Table 2–38. Ethernet PHY Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U15	10/100/1000 Base-T Ethernet PHY	Marvell Semiconductor	88E1111-B2-CAAIC000	www.marvell.com
J8	RJ45 single port with magnetics	Halo Electronics, Inc.	HFJ11-1G02ERL	www.haloelectronics.com

Embedded USB-Blaster

The development board incorporates the FTDI USB 2.0 PHY chip which interfaces to the USB type-B connector (J6). The maximum speed of the interface is 12 Mbps. The typical application speed is 1.5 Mbps; however, the actual system speed may vary.

The primary usage for the USB device is to provide JTAG programming for on-board devices such as the FPGA and flash memory. The interface is also the default means through which the FPGA connects to Altera PC applications such as SignalTap® II, DSP Builder, and the Nios II JTAG UART. You can build user applications using the Virtual JTAG or System Console libraries found in the Quartus II software.

For more information about the data sheet and related documentation, contact FTDI at www.ftdichip.com.

Table 2–39 lists the USB 2.0 component reference and manufacturing information.

Table 2–39. USB 2.0 Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U7	FTDI USB FIFO	FTDI Ltd.	FT245BL	www.ftdichip.com

High-Speed Mezzanine Cards

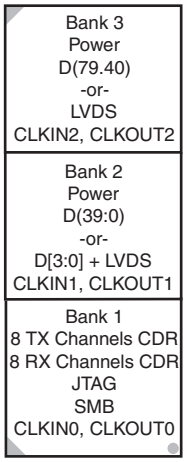
The development board contains two HSMC interfaces called port A and port B. The HSMC interfaces support both single-ended and differential signaling. The interface also allows JTAG, SMB, clock outputs and inputs, as well as power for compatible HSMC cards. The HSMC is an Altera-developed open specification, which allows you to expand the functionality of the development board through the addition of mezzanine cards.

For more information about the HSMC specification such as signaling standards, signal integrity, compatible connectors, and mechanical information, refer to the *High Speed Mezzanine Card (HSMC) Specification* manual.

The HSMC connector has a total of 172 pins, including 120 signal pins, 39 power pins, and 13 ground pins. The ground pins are located between the two rows of signal and power pins, acting both as a shield and a reference. The HSMC host connector is based on the 0.5 mm-pitch QSH/QTH family of high-speed, board-to-board connectors from Samtec. There are three banks in this connector. Bank 1 has every third pin removed as done in the QSH-DP/QTH-DP series. Bank 2 and bank 3 have all the pins populated as done in the QSH/QTH series.

Figure 2–8 shows the bank arrangement of signals with respect to the Samtec connector's three banks.

Figure 2–8. HSMC Signal and Bank Diagram



The HSMC interface has programmable bi-directional I/O pins that can be used as 2.5-V LVCMOS, which is 3.3-V LVTTL-compatible. These pins can also be used as various differential I/O standards including, but not limited to, LVDS, mini-LVDS, and RSDS with up to 17 full-duplex channels.

As noted in the *High Speed Mezzanine Card (HSMC) Specification* manual, LVDS and single-ended I/O standards are only guaranteed to function when mixed according to either the generic single-ended pin-out or generic differential pin-out.

Table 2–40 lists the HSMC port A interface pin assignments, signal names, and functions.

Table 2–40. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 5)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number	Other Connections
J19.1	Transceiver TX bit 7	NC	1.4-V PCML	—	—
J19.2	Transceiver RX bit 7			—	—
J19.3	Transceiver TX bit 7n			—	—
J19.4	Transceiver RX bit 7n			—	—
J19.5	Transceiver TX bit 6			—	—
J19.6	Transceiver RX bit 6			—	—

Table 2–40. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 5)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number	Other Connections
J19.7	Transceiver TX bit 6n	NC	1.4-V PCML	—	—
J19.8	Transceiver RX bit 6n			—	—
J19.9	Transceiver TX bit 5			—	—
J19.10	Transceiver RX bit 5			—	—
J19.11	Transceiver TX bit 5n			—	—
J19.12	Transceiver RX bit 5n			—	—
J19.13	Transceiver TX bit 4			—	—
J19.14	Transceiver RX bit 4			—	—
J19.15	Transceiver TX bit 4n			—	—
J19.16	Transceiver RX bit 4n			—	—
J19.17	Transceiver TX bit 3			—	—
J19.18	Transceiver RX bit 3			—	—
J19.19	Transceiver TX bit 3n			—	—
J19.20	Transceiver RX bit 3n			—	—
J19.21	Transceiver TX bit 2			—	—
J19.22	Transceiver RX bit 2			—	—
J19.23	Transceiver TX bit 2n			—	—
J19.24	Transceiver RX bit 2n			—	—
J19.25	Transceiver TX bit 1			—	—
J19.26	Transceiver RX bit 1			—	—
J19.27	Transceiver TX bit 1n			—	—
J19.28	Transceiver RX bit 1n			—	—
J19.29	Transceiver TX bit 0			—	—
J19.30	Transceiver RX bit 0			—	—
J19.31	Transceiver TX bit 0n			—	—
J19.32	Transceiver RX bit 0n			—	—
J19.33	Management serial data	HSMA_SDA	2.5-V	V3	—
J19.34	Management serial clock	HSMA_SCL		Y2	—
J19.35	JTAG clock signal	JTAG_TCK		—	—
J19.36	JTAG mode select signal	JTAG_TMS		—	—
J19.37	JTAG data output	HSMA_JTAG_TDO		—	—
J19.38	JTAG data input	HSMA_JTAG_TDI		—	—
J19.39	Dedicated CMOS clock out	HSMA_CLK_OUT0		W11	—
J19.40	Dedicated CMOS clock in	HSMA_CLK_IN0		B20	—
J19.41	Dedicated CMOS I/O bit 0	HSMA_D0		AL10	—
J19.42	Dedicated CMOS I/O bit 1	HSMA_D1		AL11	—
J19.43	Dedicated CMOS I/O bit 2	HSMA_D2		AN7	—
J19.44	Dedicated CMOS I/O bit 3	HSMA_D3		AP7	—

Table 2–40. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 5)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number	Other Connections
J19.47	LVDS TX bit 0 or CMOS bit 4	HSMA_TX_D_P0	LVDS or 2.5-V	AC11	—
J19.48	LVDS RX bit 0 or CMOS bit 5	HSMA_RX_D_P0		AJ4	—
J19.49	LVDS TX bit 0n or CMOS bit 6	HSMA_TX_D_N0		AB10	—
J19.50	LVDS RX bit 0n or CMOS bit 7	HSMA_RX_D_N0		AJ3	—
J19.53	LVDS TX bit 1 or CMOS bit 8	HSMA_TX_D_P1		AC9	—
J19.54	LVDS RX bit 1 or CMOS bit 9	HSMA_RX_D_P1		AG4	—
J19.55	LVDS TX bit 1n or CMOS bit 10	HSMA_TX_D_N1		AC8	—
J19.56	LVDS RX bit 1n or CMOS bit 11	HSMA_RX_D_N1		AG3	—
J19.59	LVDS TX bit 2 or CMOS bit 12	HSMA_TX_D_P2		AH5	—
J19.60	LVDS RX bit 2 or CMOS bit 13	HSMA_RX_D_P2		AM2	—
J19.61	LVDS TX bit 2n or CMOS bit 14	HSMA_TX_D_N2		AH4	—
J19.62	LVDS RX bit 2n or CMOS bit 15	HSMA_RX_D_N2		AM1	—
J19.65	LVDS TX bit 3 or CMOS bit 16	HSMA_TX_D_P3		AE8	—
J19.66	LVDS RX bit 3 or CMOS bit 17	HSMA_RX_D_P3		AL2	—
J19.67	LVDS TX bit 3n or CMOS bit 18	HSMA_TX_D_N3		AE7	—
J19.68	LVDS RX bit 3n or CMOS bit 19	HSMA_RX_D_N3		AL1	—
J19.71	LVDS TX bit 4 or CMOS bit 20	HSMA_TX_D_P4		AF6	—
J19.72	LVDS RX bit 4 or CMOS bit 21	HSMA_RX_D_P4		AJ2	—
J19.73	LVDS TX bit 4n or CMOS bit 22	HSMA_TX_D_N4		AF5	—
J19.74	LVDS RX bit 4n or CMOS bit 23	HSMA_RX_D_N4		AK1	—
J19.77	LVDS TX bit 5 or CMOS bit 24	HSMA_TX_D_P5		AD7	—
J19.78	LVDS RX bit 5 or CMOS bit 25	HSMA_RX_D_P5		AH2	—
J19.79	LVDS TX bit 5n or CMOS bit 26	HSMA_TX_D_N5		AD6	—
J19.80	LVDS RX bit 5n or CMOS bit 27	HSMA_RX_D_N5		AJ1	—
J19.83	LVDS TX bit 6 or CMOS bit 28	HSMA_TX_D_P6		AE6	—
J19.84	LVDS RX bit 6 or CMOS bit 29	HSMA_RX_D_P6		AF4	—
J19.85	LVDS TX bit 6n or CMOS bit 30	HSMA_TX_D_N6		AE5	—
J19.86	LVDS RX bit 6n or CMOS bit 31	HSMA_RX_D_N6		AF3	—
J19.89	LVDS TX bit 7 or CMOS bit 32	HSMA_TX_D_P7		AD4	—
J19.90	LVDS RX bit 7 or CMOS bit 33	HSMA_RX_D_P7		AG1	—
J19.91	LVDS TX bit 7n or CMOS bit 34	HSMA_TX_D_N7		AD3	—
J19.92	LVDS RX bit 7n or CMOS bit 35	HSMA_RX_D_N7		AH1	—
J19.95	LVDS or CMOS clock out 1 or CMOS bit 36	HSMA_CLK_OUT_P1		V10	—
J19.96	LVDS or CMOS clock in 1 or CMOS bit 37	HSMA_CLK_IN_P1		W2	—
J19.97	LVDS or CMOS clock out 1 or CMOS bit 38	HSMA_CLK_OUT_N1		W9	—

Table 2–40. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 5)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number	Other Connections
J19.98	LVDS or CMOS clock in 1 or CMOS bit 39	HSMA_CLK_IN_N1	LVDS or 2.5-V	W1	—
J19.101	LVDS TX bit 8 or CMOS bit 40	HSMA_TX_D_P8		AC6	—
J19.102	LVDS RX bit 8 or CMOS bit 41	HSMA_RX_D_P8		AF2	—
J19.103	LVDS TX bit 8n or CMOS bit 42	HSMA_TX_D_N8		AC5	—
J19.104	LVDS RX bit 8n or CMOS bit 43	HSMA_RX_D_N8		AF1	—
J19.107	LVDS TX bit 9 or CMOS bit 44	HSMA_TX_D_P9		AB6	—
J19.108	LVDS RX bit 9 or CMOS bit 45	HSMA_RX_D_P9		AE2	—
J19.109	LVDS TX bit 9n or CMOS bit 46	HSMA_TX_D_N9		AB5	—
J19.110	LVDS RX bit 9n or CMOS bit 47	HSMA_RX_D_N9		AE1	—
J19.113	LVDS TX bit 10 or CMOS bit 48	HSMA_TX_D_P10		AB8	—
J19.114	LVDS RX bit 10 or CMOS bit 49	HSMA_RX_D_P10		AE4	—
J19.115	LVDS TX bit 10n or CMOS bit 50	HSMA_TX_D_N10		AC7	—
J19.116	LVDS RX bit 10n or CMOS bit 51	HSMA_RX_D_N10		AE3	—
J19.119	LVDS TX bit 11 or CMOS bit 52	HSMA_TX_D_P11		Y6	—
J19.120	LVDS RX bit 11 or CMOS bit 53	HSMA_RX_D_P11		AC2	—
J19.121	LVDS TX bit 11n or CMOS bit 54	HSMA_TX_D_N11		Y5	—
J19.122	LVDS RX bit 11n or CMOS bit 55	HSMA_RX_D_N11		AD1	—
J19.125	LVDS TX bit 12 or CMOS bit 56	HSMA_TX_D_P12		AA7	—
J19.126	LVDS RX bit 12 or CMOS bit 57	HSMA_RX_D_P12		AB2	—
J19.127	LVDS TX bit 12n or CMOS bit 58	HSMA_TX_D_N12		AA6	—
J19.128	LVDS RX bit 12n or CMOS bit 59	HSMA_RX_D_N12		AC1	—
J19.131	LVDS TX bit 13 or CMOS bit 60	HSMA_TX_D_P13		Y8	—
J19.132	LVDS RX bit 13 or CMOS bit 61	HSMA_RX_D_P13		AA1	—
J19.133	LVDS TX bit 13n or CMOS bit 62	HSMA_TX_D_N13		Y7	—
J19.134	LVDS RX bit 13n or CMOS bit 63	HSMA_RX_D_N13		AB1	—
J19.137	LVDS TX bit 14 or CMOS bit 64	HSMA_TX_D_P14		Y10	—
J19.138	LVDS RX bit 14 or CMOS bit 65	HSMA_RX_D_P14		AC4	—
J19.139	LVDS TX bit 14n or CMOS bit 66	HSMA_TX_D_N14		Y9	—
J19.140	LVDS RX bit 14n or CMOS bit 67	HSMA_RX_D_N14		AB3	—
J19.143	LVDS TX bit 15 or CMOS bit 68	HSMA_TX_D_P15		W12	—
J19.144	LVDS RX bit 15 or CMOS bit 69	HSMA_RX_D_P15		AB4	—
J19.145	LVDS TX bit 15n or CMOS bit 70	HSMA_TX_D_N15		Y11	—
J19.146	LVDS RX bit 15n or CMOS bit 71	HSMA_RX_D_N15		AA3	—
J19.149	LVDS TX bit 16 or CMOS bit 72	HSMA_TX_D_P16		AA12	—
J19.150	LVDS RX bit 16 or CMOS bit 73	HSMA_RX_D_P16		AA4	—
J19.151	LVDS TX bit 16n or CMOS bit 74	HSMA_TX_D_N16		AB11	—
J19.152	LVDS RX bit 16n or CMOS bit 75	HSMA_RX_D_N16		Y3	—

Table 2–40. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 5 of 5)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number	Other Connections
J19.155	LVDS or CMOS clock out 2 or CMOS bit 76	HSMA_CLK_OUT_P2	LVDS or 2.5-V	R12	—
J19.156	LVDS or CMOS clock in 2 or CMOS bit 77	HSMA_CLK_IN_P2		U4	—
J19.157	LVDS or CMOS clock out 2 or CMOS bit 78	HSMA_CLK_OUT_N2		T11	—
J19.158	LVDS or CMOS clock in 2 or CMOS bit 79	HSMA_CLK_IN_N2		U3	—
J19.160	HSMC port A presence detect	HSMA_PSNTn	2.5-V	—	U10.F16
D4	User LED to show RX data activity on HSMC port A	HSMA_RX_LED		AK12	—
D3	User LED to show TX data activity on HSMC port A	HSMA_TX_LED		G30	—

Table 2–41 lists the HSMC port B interface pin assignments, signal names, and functions.

Table 2–41. HSMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 4)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number	Other Connections
J9.1	Transceiver TX bit 7	NC	1.4-V PCML	—	—
J9.2	Transceiver RX bit 7			—	—
J9.3	Transceiver TX bit 7n			—	—
J9.4	Transceiver RX bit 7n			—	—
J9.5	Transceiver TX bit 6			—	—
J9.6	Transceiver RX bit 6			—	—
J9.7	Transceiver TX bit 6n			—	—
J9.8	Transceiver RX bit 6n			—	—
J9.9	Transceiver TX bit 5			—	—
J9.10	Transceiver RX bit 5			—	—
J9.11	Transceiver TX bit 5n			—	—
J9.12	Transceiver RX bit 5n			—	—
J9.13	Transceiver TX bit 4			—	—
J9.14	Transceiver RX bit 4			—	—
J9.15	Transceiver TX bit 4n			—	—
J9.16	Transceiver RX bit 4n			—	—
J9.17	Transceiver TX bit 3			—	—
J9.18	Transceiver RX bit 3			—	—
J9.19	Transceiver TX bit 3n			—	—
J9.20	Transceiver RX bit 3n			—	—

Table 2–41. HSMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 4)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number	Other Connections
J9.21	Transceiver TX bit 2	NC	1.4-V PCML	—	—
J9.22	Transceiver RX bit 2			—	—
J9.23	Transceiver TX bit 2n			—	—
J9.24	Transceiver RX bit 2n			—	—
J9.25	Transceiver TX bit 1			—	—
J9.26	Transceiver RX bit 1			—	—
J9.27	Transceiver TX bit 1n			—	—
J9.28	Transceiver RX bit 1n			—	—
J9.29	Transceiver TX bit 0			—	—
J9.30	Transceiver RX bit 0			—	—
J9.31	Transceiver TX bit 0n			—	—
J9.32	Transceiver RX bit 0n			—	—
J9.33	Management serial data	HSMB_SDA	2.5-V	U10	—
J9.34	Management serial clock	HSMB_SCL		M28	—
J9.35	JTAG clock signal	JTAG_TCK		—	—
J9.36	JTAG mode select signal	JTAG_TMS		—	—
J9.37	JTAG data output	HSMB_JTAG_TDO		—	—
J9.38	JTAG data input	HSMB_JTAG_TDI		—	—
J9.39	Dedicated CMOS clock out	HSMB_CLK_OUT0		N6	—
J9.40	Dedicated CMOS clock in	HSMB_CLK_IN0		B19	—
J9.41	Dedicated CMOS I/O bit 0	HSMB_D0		P7	—
J9.42	Dedicated CMOS I/O bit 1	HSMB_D1		W5	—
J9.43	Dedicated CMOS I/O bit 2	HSMB_D2		N5	—
J9.44	Dedicated CMOS I/O bit 3	HSMB_D3		P8	—
J9.47	LVDS TX bit 0 or CMOS bit 4	HSMB_TX_D_P0	LVDS or 2.5-V	P11	—
J9.48	LVDS RX bit 0 or CMOS bit 5	HSMB_RX_D_P0		R4	—
J9.49	LVDS TX bit 0n or CMOS bit 6	HSMB_TX_D_N0		P10	—
J9.50	LVDS RX bit 0n or CMOS bit 7	HSMB_RX_D_N0		R3	—
J9.53	LVDS TX bit 1 or CMOS bit 8	HSMB_TX_D_P1		T9	—
J9.54	LVDS RX bit 1 or CMOS bit 9	HSMB_RX_D_P1		P4	—
J9.55	LVDS TX bit 1n or CMOS bit 10	HSMB_TX_D_N1		T8	—
J9.56	LVDS RX bit 1n or CMOS bit 11	HSMB_RX_D_N1		P3	—
J9.59	LVDS TX bit 2 or CMOS bit 12	HSMB_TX_D_P2		T7	—
J9.60	LVDS RX bit 2 or CMOS bit 13	HSMB_RX_D_P2		P2	—
J9.61	LVDS TX bit 2n or CMOS bit 14	HSMB_TX_D_N2		U6	—
J9.62	LVDS RX bit 2n or CMOS bit 15	HSMB_RX_D_N2		R1	—
J9.65	LVDS TX bit 3 or CMOS bit 16	HSMB_TX_D_P3		T5	—
J9.66	LVDS RX bit 3 or CMOS bit 17	HSMB_RX_D_P3		N2	—

Table 2–41. HSMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 4)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number	Other Connections
J9.67	LVDS TX bit 3n or CMOS bit 18	HSMB_TX_D_N3	LVDS or 2.5-V	T4	—
J9.68	LVDS RX bit 3n or CMOS bit 19	HSMB_RX_D_N3		P1	—
J9.71	LVDS TX bit 4 or CMOS bit 20	HSMB_TX_D_P4		R10	—
J9.72	LVDS RX bit 4 or CMOS bit 21	HSMB_RX_D_P4		M1	—
J9.73	LVDS TX bit 4n or CMOS bit 22	HSMB_TX_D_N4		R9	—
J9.74	LVDS RX bit 4n or CMOS bit 23	HSMB_RX_D_N4		N1	—
J9.77	LVDS TX bit 5 or CMOS bit 24	HSMB_TX_D_P5		R7	—
J9.78	LVDS RX bit 5 or CMOS bit 25	HSMB_RX_D_P5		L2	—
J9.79	LVDS TX bit 5n or CMOS bit 26	HSMB_TX_D_N5		R6	—
J9.80	LVDS RX bit 5n or CMOS bit 27	HSMB_RX_D_N5		L1	—
J9.83	LVDS TX bit 6 or CMOS bit 28	HSMB_TX_D_P6		N9	—
J9.84	LVDS RX bit 6 or CMOS bit 29	HSMB_RX_D_P6		K4	—
J9.85	LVDS TX bit 6n or CMOS bit 30	HSMB_TX_D_N6		N8	—
J9.86	LVDS RX bit 6n or CMOS bit 31	HSMB_RX_D_N6		K3	—
J9.89	LVDS TX bit 7 or CMOS bit 32	HSMB_TX_D_P7		M7	—
J9.90	LVDS RX bit 7 or CMOS bit 33	HSMB_RX_D_P7		J4	—
J9.91	LVDS TX bit 7n or CMOS bit 34	HSMB_TX_D_N7		M6	—
J9.92	LVDS RX bit 7n or CMOS bit 35	HSMB_RX_D_N7		J3	—
J9.95	LVDS or CMOS clock out 1 or CMOS bit 36	HSMB_CLK_OUT_P1		P6	—
J9.96	LVDS or CMOS clock in 1 or CMOS bit 37	HSMB_CLK_IN_P1		U2	—
J9.97	LVDS or CMOS clock out 1 or CMOS bit 38	HSMB_CLK_OUT_N1		P5	—
J9.98	LVDS or CMOS clock in 1 or CMOS bit 39	HSMB_CLK_IN_N1		U1	—
J9.101	LVDS TX bit 8 or CMOS bit 40	HSMB_TX_D_P8		L7	—
J9.102	LVDS RX bit 8 or CMOS bit 41	HSMB_RX_D_P8		H2	—
J9.103	LVDS TX bit 8n or CMOS bit 42	HSMB_TX_D_N8		L6	—
J9.104	LVDS RX bit 8n or CMOS bit 43	HSMB_RX_D_N8		J1	—
J9.107	LVDS TX bit 9 or CMOS bit 44	HSMB_TX_D_P9		L5	—
J9.108	LVDS RX bit 9 or CMOS bit 45	HSMB_RX_D_P9		G2	—
J9.109	LVDS TX bit 9n or CMOS bit 46	HSMB_TX_D_N9		L4	—
J9.110	LVDS RX bit 9n or CMOS bit 47	HSMB_RX_D_N9		H1	—
J9.113	LVDS TX bit 10 or CMOS bit 48	HSMB_TX_D_P10		K6	—
J9.114	LVDS RX bit 10 or CMOS bit 49	HSMB_RX_D_P10		F1	—
J9.115	LVDS TX bit 10n or CMOS bit 50	HSMB_TX_D_N10		K5	—
J9.116	LVDS RX bit 10n or CMOS bit 51	HSMB_RX_D_N10		G1	—
J9.119	LVDS TX bit 11 or CMOS bit 52	HSMB_TX_D_P11		J7	—

Table 2–41. HSMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 4)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number	Other Connections
J9.120	LVDS RX bit 11 or CMOS bit 53	HSMB_RX_D_P11	LVDS or 2.5-V	H4	—
J9.121	LVDS TX bit 11n or CMOS bit 54	HSMB_TX_D_N11		J6	—
J9.122	LVDS RX bit 11n or CMOS bit 55	HSMB_RX_D_N11		H3	—
J9.125	LVDS TX bit 12 or CMOS bit 56	HSMB_TX_D_P12		W8	—
J9.126	LVDS RX bit 12 or CMOS bit 57	HSMB_RX_D_P12		E2	—
J9.127	LVDS TX bit 12n or CMOS bit 58	HSMB_TX_D_N12		W7	—
J9.128	LVDS RX bit 12n or CMOS bit 59	HSMB_RX_D_N12		E1	—
J9.131	LVDS TX bit 13 or CMOS bit 60	HSMB_TX_D_P13		K8	—
J9.132	LVDS RX bit 13 or CMOS bit 61	HSMB_RX_D_P13		C1	—
J9.133	LVDS TX bit 13n or CMOS bit 62	HSMB_TX_D_N13		K7	—
J9.134	LVDS RX bit 13n or CMOS bit 63	HSMB_RX_D_N13		D1	—
J9.137	LVDS TX bit 14 or CMOS bit 64	HSMB_TX_D_P14		L9	—
J9.138	LVDS RX bit 14 or CMOS bit 65	HSMB_RX_D_P14		D3	—
J9.139	LVDS TX bit 14n or CMOS bit 66	HSMB_TX_D_N14		L8	—
J9.140	LVDS RX bit 14n or CMOS bit 67	HSMB_RX_D_N14		D2	—
J9.143	LVDS TX bit 15 or CMOS bit 68	HSMB_TX_D_P15		M10	—
J9.144	LVDS RX bit 15 or CMOS bit 69	HSMB_RX_D_P15		G5	—
J9.145	LVDS TX bit 15n or CMOS bit 70	HSMB_TX_D_N15		M9	—
J9.146	LVDS RX bit 15n or CMOS bit 71	HSMB_RX_D_N15		G4	—
J9.149	LVDS TX bit 16 or CMOS bit 72	HSMB_TX_D_P16		N11	—
J9.150	LVDS RX bit 16 or CMOS bit 73	HSMB_RX_D_P16		F4	—
J9.151	LVDS TX bit 16n or CMOS bit 74	HSMB_TX_D_N16		N10	—
J9.152	LVDS RX bit 16n or CMOS bit 75	HSMB_RX_D_N16		F3	—
J9.155	LVDS or CMOS clock out 2 or CMOS bit 76	HSMB_CLK_OUT_P2		H6	—
J9.156	LVDS or CMOS clock in 2 or CMOS bit 77	HSMB_CLK_IN_P2		T2	—
J9.157	LVDS or CMOS clock out 2 or CMOS bit 78	HSMB_CLK_OUT_N2		H5	—
J9.158	LVDS or CMOS clock in 2 or CMOS bit 79	HSMB_CLK_IN_N2		T1	—
J9.160	HSMC port B presence detect	HSMB_PSNTn	2.5-V	—	U10.G13
D4	User LED to show RX data activity on HSMC port B	HSMB_RX_LED		P23	—
D3	User LED to show TX data activity on HSMC port B	HSMB_TX_LED		N4	—

Table 2–42 lists the HSMC connector component reference and manufacturing information.

Table 2–42. HSMC Connector Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
J9 and J19	HSMC, custom version of QSH-DP family high-speed socket.	Samtec	ASP-122953-01	www.samtec.com

Memory

This section describes the board's memory interface support, signal names, types, and connectivity relative to the Stratix IV E FPGA device. The board has the following memory interfaces:

- DDR3
- QDR II+
- RLDRAM II CIO
- SSRAM
- Flash

For more information about the memory interfaces, refer to the External Memory Interfaces Handbook.

DDR3

There is a single DDR3 SDRAM DIMM on the board, providing a dual rank 2-GB interface with a 72-bit data bus width on the vertical I/O banks. This memory interface is designed to run at a maximum frequency of 533 MHz.

Table 2–43 lists the DDR3 pin assignments, signal names, and functions.

Table 2–43. DDR3 Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 5)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number
J20.188	Address bus	DDR3_DIMM_A0	1.5-V SSTL Class I	AL17
J20.181	Address bus	DDR3_DIMM_A1		AM17
J20.61	Address bus	DDR3_DIMM_A2		AL18
J20.180	Address bus	DDR3_DIMM_A3		AM18
J20.59	Address bus	DDR3_DIMM_A4		AN18
J20.58	Address bus	DDR3_DIMM_A5		AP18
J20.178	Address bus	DDR3_DIMM_A6		AL19
J20.56	Address bus	DDR3_DIMM_A7		AM19

Table 2–43. DDR3 Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 5)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number
J20.177	Address bus	DDR3_DIMM_A8	1.5-V SSTL Class I	AP19
J20.175	Address bus	DDR3_DIMM_A9		AK18
J20.70	Address bus	DDR3_DIMM_A10		AP15
J20.55	Address bus	DDR3_DIMM_A11		AL20
J20.174	Address bus	DDR3_DIMM_A12		AK19
J20.196	Address bus	DDR3_DIMM_A13		AF16
J20.172	Address bus	DDR3_DIMM_A14		AE18
J20.171	Address bus	DDR3_DIMM_A15		AD19
J20.71	Bank address bus	DDR3_DIMM_BA0		AM15
J20.190	Bank address bus	DDR3_DIMM_BA1		AM16
J20.52	Bank address bus	DDR3_DIMM_BA2		AK16
J20.74	Column address strobe	DDR3_DIMM_CASn		AK13
J20.50	Clock enable 0	DDR3_DIMM_CKE0		AJ16
J20.169	Clock enable 1	DDR3_DIMM_CKE1		AD18
J20.185	Differential output clock 0 complement	DDR3_DIMM_CLK_N0	Differential 1.5-V SSTL Class I	AJ8
J20.64	Differential output clock 1 complement	DDR3_DIMM_CLK_N1		AK7
J20.184	Differential output clock 0	DDR3_DIMM_CLK_P0		AH8
J20.63	Differential output clock 1	DDR3_DIMM_CLK_P1		AJ7
J20.193	Chip select	DDR3_DIMM_CSn0	1.5-V SSTL Class I	AL16
J20.76	Chip select	DDR3_DIMM_CSn1		AE16
J20.79	Chip select	DDR3_DIMM_CSn2		AD15
J20.198	Chip select	DDR3_DIMM_CSn3		AD16
J20.125	Data write mask bit 0 (byte enables)	DDR3_DIMM_DM0		AJ28
J20.134	Data write mask bit 1 (byte enables)	DDR3_DIMM_DM1		AG24
J20.143	Data write mask bit 2 (byte enables)	DDR3_DIMM_DM2		AL26
J20.152	Data write mask bit 3 (byte enables)	DDR3_DIMM_DM3		AH22
J20.203	Data write mask bit 4 (byte enables)	DDR3_DIMM_DM4		AK21
J20.212	Data write mask bit 5 (byte enables)	DDR3_DIMM_DM5		AN12
J20.221	Data write mask bit 6 (byte enables)	DDR3_DIMM_DM6		AK9
J20.230	Data write mask bit 7 (byte enables)	DDR3_DIMM_DM7		AL5
J20.161	Data write mask bit 8 (byte enables)	DDR3_DIMM_DM8		AF21
J20.3	Data bus	DDR3_DIMM_DQ0		AL29
J20.4	Data bus	DDR3_DIMM_DQ1		AM29
J20.9	Data bus	DDR3_DIMM_DQ2		AN30
J20.10	Data bus	DDR3_DIMM_DQ3		AM30
J20.122	Data bus	DDR3_DIMM_DQ4		AJ29

Table 2–43. DDR3 Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 5)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number
J20.123	Data bus	DDR3_DIMM_DQ5	1.5-V SSTL Class I	AJ27
J20.128	Data bus	DDR3_DIMM_DQ6		AH27
J20.129	Data bus	DDR3_DIMM_DQ7		AJ26
J20.12	Data bus	DDR3_DIMM_DQ8		AP32
J20.13	Data bus	DDR3_DIMM_DQ9		AP30
J20.18	Data bus	DDR3_DIMM_DQ10		AP31
J20.19	Data bus	DDR3_DIMM_DQ11		AN31
J20.131	Data bus	DDR3_DIMM_DQ12		AH26
J20.132	Data bus	DDR3_DIMM_DQ13		AF24
J20.137	Data bus	DDR3_DIMM_DQ14		AH25
J20.138	Data bus	DDR3_DIMM_DQ15		AF23
J20.21	Data bus	DDR3_DIMM_DQ16		AM28
J20.22	Data bus	DDR3_DIMM_DQ17		AP29
J20.27	Data bus	DDR3_DIMM_DQ18		AP27
J20.28	Data bus	DDR3_DIMM_DQ19		AN27
J20.140	Data bus	DDR3_DIMM_DQ20		AK27
J20.141	Data bus	DDR3_DIMM_DQ21		AL28
J20.146	Data bus	DDR3_DIMM_DQ22		AK25
J20.147	Data bus	DDR3_DIMM_DQ23		AM26
J20.30	Data bus	DDR3_DIMM_DQ24		AK24
J20.31	Data bus	DDR3_DIMM_DQ25		AL25
J20.36	Data bus	DDR3_DIMM_DQ26		AM23
J20.37	Data bus	DDR3_DIMM_DQ27		AL23
J20.149	Data bus	DDR3_DIMM_DQ28		AH23
J20.150	Data bus	DDR3_DIMM_DQ29		AJ24
J20.155	Data bus	DDR3_DIMM_DQ30		AJ23
J20.156	Data bus	DDR3_DIMM_DQ31		AK22
J20.81	Data bus	DDR3_DIMM_DQ32		AM21
J20.82	Data bus	DDR3_DIMM_DQ33		AP20
J20.87	Data bus	DDR3_DIMM_DQ34		AP21
J20.88	Data bus	DDR3_DIMM_DQ35		AN21
J20.200	Data bus	DDR3_DIMM_DQ36		AL22
J20.201	Data bus	DDR3_DIMM_DQ37		AM22
J20.206	Data bus	DDR3_DIMM_DQ38		AJ20
J20.207	Data bus	DDR3_DIMM_DQ39		AJ21
J20.90	Data bus	DDR3_DIMM_DQ40		AH15
J20.91	Data bus	DDR3_DIMM_DQ41		AJ15
J20.96	Data bus	DDR3_DIMM_DQ42		AG15

Table 2–43. DDR3 Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 5)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number
J20.97	Data bus	DDR3_DIMM_DQ43	1.5-V SSTL Class I	AK15
J20.209	Data bus	DDR3_DIMM_DQ44		AP13
J20.210	Data bus	DDR3_DIMM_DQ45		AM12
J20.215	Data bus	DDR3_DIMM_DQ46		AN13
J20.216	Data bus	DDR3_DIMM_DQ47		AP14
J20.99	Data bus	DDR3_DIMM_DQ48		AH12
J20.100	Data bus	DDR3_DIMM_DQ49		AJ12
J20.105	Data bus	DDR3_DIMM_DQ50		AG12
J20.106	Data bus	DDR3_DIMM_DQ51		AJ13
J20.218	Data bus	DDR3_DIMM_DQ52		AJ10
J20.219	Data bus	DDR3_DIMM_DQ53		AL8
J20.224	Data bus	DDR3_DIMM_DQ54		AL7
J20.225	Data bus	DDR3_DIMM_DQ55		AJ9
J20.108	Data bus	DDR3_DIMM_DQ56		AN4
J20.109	Data bus	DDR3_DIMM_DQ57		AP4
J20.114	Data bus	DDR3_DIMM_DQ58		AP2
J20.115	Data bus	DDR3_DIMM_DQ59		AP5
J20.227	Data bus	DDR3_DIMM_DQ60		AM6
J20.228	Data bus	DDR3_DIMM_DQ61		AN6
J20.233	Data bus	DDR3_DIMM_DQ62		AL4
J20.234	Data bus	DDR3_DIMM_DQ63		AM4
J20.39	Data bus	DDR3_DIMM_DQ64		AP26
J20.40	Data bus	DDR3_DIMM_DQ65		AP23
J20.45	Data bus	DDR3_DIMM_DQ66		AP24
J20.46	Data bus	DDR3_DIMM_DQ67		AN24
J20.158	Data bus	DDR3_DIMM_DQ68		AE22
J20.159	Data bus	DDR3_DIMM_DQ69		AE21
J20.164	Data bus	DDR3_DIMM_DQ70		AD21
J20.165	Data bus	DDR3_DIMM_DQ71		AE20
J20.6	Data strobe bit N0	DDR3_DIMM_DQS_N0		AM32
J20.15	Data strobe bit N1	DDR3_DIMM_DQS_N1		AP33
J20.24	Data strobe bit N2	DDR3_DIMM_DQS_N2		AP28
J20.33	Data strobe bit N3	DDR3_DIMM_DQS_N3		AM24
J20.84	Data strobe bit N4	DDR3_DIMM_DQS_N4		AP22
J20.93	Data strobe bit N5	DDR3_DIMM_DQS_N5		AJ14
J20.102	Data strobe bit N6	DDR3_DIMM_DQS_N6		AJ11
J20.111	Data strobe bit N7	DDR3_DIMM_DQS_N7		AP3
J20.42	Data strobe bit N8	DDR3_DIMM_DQS_N8		AP25

Table 2–43. DDR3 Pin Assignments, Schematic Signal Names, and Functions (Part 5 of 5)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number
J20.126	Data strobe bit N9	DDR3_DIMM_DQS_N9	1.5-V SSTL Class I	AK28
J20.135	Data strobe bit N10	DDR3_DIMM_DQS_N10		AH24
J20.144	Data strobe bit N11	DDR3_DIMM_DQS_N11		AL27
J20.153	Data strobe bit N12	DDR3_DIMM_DQS_N12		AJ22
J20.204	Data strobe bit N13	DDR3_DIMM_DQS_N13		AL21
J20.213	Data strobe bit N14	DDR3_DIMM_DQS_N14		AP12
J20.222	Data strobe bit N15	DDR3_DIMM_DQS_N15		AL9
J20.231	Data strobe bit N16	DDR3_DIMM_DQS_N16		AM5
J20.162	Data strobe bit N17	DDR3_DIMM_DQS_N17		AG21
J20.7	Data strobe bit P0	DDR3_DIMM_DQS_P0		AM31
J20.16	Data strobe bit P1	DDR3_DIMM_DQS_P1		AN33
J20.25	Data strobe bit P2	DDR3_DIMM_DQS_P2		AN28
J20.34	Data strobe bit P3	DDR3_DIMM_DQS_P3		AL24
J20.85	Data strobe bit P4	DDR3_DIMM_DQS_P4		AN22
J20.94	Data strobe bit P5	DDR3_DIMM_DQS_P5		AH14
J20.103	Data strobe bit P6	DDR3_DIMM_DQS_P6		AH11
J20.112	Data strobe bit P7	DDR3_DIMM_DQS_P7		AN3
J20.43	Data strobe bit P8	DDR3_DIMM_DQS_P8		AN25
J20.53	DIMM error output	DDR3_DIMM_ERR_OUTn		AG19
J20.187	DIMM event	DDR3_DIMM_EVENTn		AE11
J20.195	On-die termination control pin 0	DDR3_DIMM_ODT0		AL14
J20.77	On-die termination control pin 1	DDR3_DIMM_ODT1		AL13
J20.68	DIMM parity input	DDR3_DIMM_PAR_IN		AH19
J20.192	Row address strobe	DDR3_DIMM_RASn		AL15
J20.168	Reset	DDR3_DIMM_RESETn		AJ19
J20.118	Presence detect clock input	DDR3_DIMM_SCL		AF20
J20.238	Presence detect data	DDR3_DIMM_SDA		AN19
—	Test pin	DDR3_DIMM_TEST1		AC22
—	Test pin	DDR3_DIMM_TEST2		AE24
—	Test pin	DDR3_DIMM_TEST3		AF19
—	Test pin	DDR3_DIMM_TEST4		AF11
—	Test pin	DDR3_DIMM_TEST5		AC12
J20.73	Write enable	DDR3_DIMM_WEn		AM14

Table 2–44 lists the DDR3 component references and manufacturing information.

Table 2–44. DDR3 Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
B2	533-MHz 2-GB DDR3 SDRAM UDIMM 256M x72	Micron	MT18JSF25672AY-1G1	www.micron.com
J20	DDR3 240-pin DIMM Socket	AMP/Tyco	1932000-6	www.tycoelectronics.com

QDR II+ SRAM

The 72-Mb QDR II+ consists of a single QDR II+ burst-of-4 SRAM, providing 4-MB memory interface with an 18-bit read data bus and an 18-bit write data bus. The default I/O voltage for the QDR II+ SRAM and the Stratix IV E FPGA is 1.5 V. Placing a shunt on jumper J11 provides 1.8 V for VDDQ.

This memory interface is designed to run between 120 MHz, the minimum frequency for this device, and at a maximum frequency of 400 MHz. The internal bus in the FPGA is typically 2 or 4 times the width at full rate or half rate respectively. For example, a 400-MHz 18-bit interface becomes a 200-MHz 72-bit bus.

Table 2–45 lists the QDR II+ SRAM pin assignments, signal names, and functions.

Table 2–45. QDR II+ SRAM Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 3)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number
U11.A9	Address bus	QDRII_A0	1.5-V HSTL Class I	D14
U11.B4	Address bus	QDRII_A1		E14
U11.B8	Address bus	QDRII_A2		A15
U11.C5	Address bus	QDRII_A3		A14
U11.C7	Address bus	QDRII_A4		C14
U11.N5	Address bus	QDRII_A5		C7
U11.N6	Address bus	QDRII_A6		A6
U11.N7	Address bus	QDRII_A7		F14
U11.P4	Address bus	QDRII_A8		D7
U11.P5	Address bus	QDRII_A9		B8
U11.P7	Address bus	QDRII_A10		D9
U11.P8	Address bus	QDRII_A11		E10
U11.R3	Address bus	QDRII_A12		E8
U11.R4	Address bus	QDRII_A13		D8
U11.R5	Address bus	QDRII_A14		B7
U11.R7	Address bus	QDRII_A15		A8
U11.R8	Address bus	QDRII_A16		C9
U11.R9	Address bus	QDRII_A17		F15
U11.A3	Address bus	QDRII_A18		B13
U11.A10	Address bus	QDRII_A19		D15

Table 2–45. QDR II+ SRAM Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 3)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number
U11.A2	Address bus	QDRII_A20	1.5-V HSTL Class I	E13
U11.C6	Address bus	QDRII_A21		B14
U11.B7	Write byte select 0	QDRII_BWSN0		C11
U11.A5	Write byte select 1	QDRII_BWSN1		D11
U11.A1	Read clock N	QDRII_CQ_N	Differential 1.5-V HSTL Class I	C4
U11.A11	Read clock P	QDRII_CQ_P		H11
U11.P10	Write data bit	QDRII_D0	1.5-V HSTL Class I	A9
U11.N11	Write data bit	QDRII_D1		B10
U11.M11	Write data bit	QDRII_D2		B11
U11.K10	Write data bit	QDRII_D3		A11
U11.J11	Write data bit	QDRII_D4		E11
U11.G11	Write data bit	QDRII_D5		A12
U11.E10	Write data bit	QDRII_D6		C12
U11.D11	Write data bit	QDRII_D7		D12
U11.C11	Write data bit	QDRII_D8		D13
U11.B3	Write data bit	QDRII_D9		L14
U11.C3	Write data bit	QDRII_D10		K15
U11.D2	Write data bit	QDRII_D11		K13
U11.F3	Write data bit	QDRII_D12		K14
U11.G2	Write data bit	QDRII_D13		G13
U11.J3	Write data bit	QDRII_D14		D10
U11.L3	Write data bit	QDRII_D15		F11
U11.M3	Write data bit	QDRII_D16		F13
U11.N2	Write data bit	QDRII_D17		G12
U11.H1	DLL enable	QDRII_DOFFn		K12
U11.A6	Write clock N	QDRII_K_N	Differential 1.5-V HSTL Class I	H14
U11.B6	Write clock P	QDRII_K_P		J14
U11.R6	On-die termination	QDRII_ODT	1.5-V HSTL Class I	C3
U11.P11	Read data bit	QDRII_Q0		A3
U11.M10	Read data bit	QDRII_Q1		B4
U11.L11	Read data bit	QDRII_Q2		A4
U11.K11	Read data bit	QDRII_Q3		A5
U11.J10	Read data bit	QDRII_Q4		C6
U11.F11	Read data bit	QDRII_Q5		F8
U11.E11	Read data bit	QDRII_Q6		G9
U11.C10	Read data bit	QDRII_Q7		F9
U11.B11	Read data bit	QDRII_Q8		G10
U11.B2	Read data bit	QDRII_Q9		J12
U11.D3	Read data bit	QDRII_Q10		J11

Table 2–45. QDR II+ SRAM Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 3)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number
U11.E3	Read data bit	QDRII_Q11	1.5-V HSTL Class I	G8
U11.F2	Read data bit	QDRII_Q12		G11
U11.G3	Read data bit	QDRII_Q13		B2
U11.K3	Read data bit	QDRII_Q14		B5
U11.L2	Read data bit	QDRII_Q15		F6
U11.N3	Read data bit	QDRII_Q16		C5
U11.P3	Read data bit	QDRII_Q17		D6
U11.P6	Read data valid	QDRII_QVLD		A2
U11.A8	Read port select	QDRII_RPSn		K16
U11.A4	Write port select	QDRII_WPSn		D17

Table 2–46 lists the QDR II+ SRAM component reference and manufacturing information.

Table 2–46. QDR II+ SRAM Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U11	QDR II+ 4M x18, 400 MHz, BGA-165	Cypress Semiconductor	CY7C15632V18-400BZXC	www.cypress.com
			CY7C15632V18-450BZXC	
		NEC	UPD44647186AF5-E25-FQ1-SSA	www.nec.com
			UPD44647186AF5-E22-FQ1-SSA	

RLDRAM II CIO

The RLDRAM II CIO is a 576-Mb RLDRAM II memory interface with a 36-bit data bus width. This memory interface is designed to run at a maximum frequency of 400 MHz. The default I/O voltage for the RLDRAM II CIO device and the Stratix IV E FPGA is 1.5 V. Placing a shunt on jumper J11 provides 1.8 V for VDDQ.

Table 2–47 lists the RLDRAM II CIO pin assignments, signal names, and functions.

Table 2–47. RLDRAM II CIO Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 3)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number
U24.G12	Address bus	RLDC_A0	1.5-V HSTL Class I	V25
U24.G11	Address bus	RLDC_A1		V24
U24.G10	Address bus	RLDC_A2		AB25
U24.H12	Address bus	RLDC_A3		AB24
U24.H11	Address bus	RLDC_A4		W26
U24.F1	Address bus	RLDC_A5		AB26
U24.G2	Address bus	RLDC_A6		AA33
U24.G3	Address bus	RLDC_A7		AA25
U24.G1	Address bus	RLDC_A8		AA34
U24.H2	Address bus	RLDC_A9	1.5-V HSTL Class I	AB27
U24.M12	Address bus	RLDC_A10		AH30
U24.M11	Address bus	RLDC_A11		AG30
U24.M10	Address bus	RLDC_A12		AH34
U24.L12	Address bus	RLDC_A13		AG33
U24.L11	Address bus	RLDC_A14		AH33
U24.P1	Address bus	RLDC_A15		AG34
U24.M2	Address bus	RLDC_A16		AD30
U24.M3	Address bus	RLDC_A17		AE31
U24.N1	Address bus	RLDC_A18		AF34
U24.N12	Address bus	RLDC_A19		AG29
U24.E12	Address bus	RLDC_A20		AA24
U24.E1	Address bus	RLDC_A21		W30
U24.D1	Address bus	RLDC_A22		W27
U24.J11	Bank address	RLDC_BA0		AC31
U24.K11	Bank address	RLDC_BA1		AC28
U24.H1	Bank address	RLDC_BA2		AB33
U24.K12	Input clock N	RLDC_CK_N	Differential 1.5-V HSTL Class I	AF32
U24.J12	Input clock P	RLDC_CK_P		AF31
U24.L2	Chip select	RLDC_CSn	1.5-V HSTL Class I	AC29
U24.J2	Input data clock	RLDC_DK_N0	Differential 1.5-V HSTL Class I	AB34
U24.K2	Input data clock	RLDC_DK_N1		AK34
U24.J1	Input data clock	RLDC_DK_P0		AC34
U24.K1	Input data clock	RLDC_DK_P1		AK33

Table 2–47. RLDRAM II CIO Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 3)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number
U24.P12	Input data mask	RLDC_DM	1.5-V HSTL Class I	AH31
U24.B11	Data bit	RLDC_DQ0		AA29
U24.B10	Data bit	RLDC_DQ1		AA30
U24.C11	Data bit	RLDC_DQ2		AB29
U24.C10	Data bit	RLDC_DQ3		AB30
U24.E11	Data bit	RLDC_DQ4		AD33
U24.E10	Data bit	RLDC_DQ5		AD34
U24.F11	Data bit	RLDC_DQ6		AE34
U24.F10	Data bit	RLDC_DQ7		Y25
U24.B2	Data bit	RLDC_DQ8		Y26
U24.B3	Data bit	RLDC_DQ9		AE33
U24.C2	Data bit	RLDC_DQ10		AA31
U24.C3	Data bit	RLDC_DQ11	Differential 1.5-V HSTL Class I	AA32
U24.D2	Data bit	RLDC_DQ12		W24
U24.D3	Data bit	RLDC_DQ13	1.5-V HSTL Class I	Y23
U24.E2	Data bit	RLDC_DQ14		Y28
U24.E3	Data bit	RLDC_DQ15		Y29
U24.F2	Data bit	RLDC_DQ16		AA27
U24.F3	Data bit	RLDC_DQ17		AA28
U24.U2	Data bit	RLDC_DQ18		AD28
U24.U3	Data bit	RLDC_DQ19		AD29
U24.T2	Data bit	RLDC_DQ20		AE29
U24.T3	Data bit	RLDC_DQ21		AE30
U24.P2	Data bit	RLDC_DQ22		AF28
U24.P3	Data bit	RLDC_DQ23		AF29
U24.N2	Data bit	RLDC_DQ24		AG31
U24.N3	Data bit	RLDC_DQ25		AG32
U24.U11	Data bit	RLDC_DQ26		AC25
U24.U10	Data bit	RLDC_DQ27		AC26
U24.T11	Data bit	RLDC_DQ28		AD26
U24.T10	Data bit	RLDC_DQ29		AD27
U24.R11	Data bit	RLDC_DQ30		AE27
U24.R10	Data bit	RLDC_DQ31		AE28
U24.P11	Data bit	RLDC_DQ32		AL33
U24.P10	Data bit	RLDC_DQ33		AL34
U24.N11	Data bit	RLDC_DQ34		AM34
U24.N10	Data bit	RLDC_DQ35		AL32

Table 2–47. RLDRAM II CIO Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 3)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number
U24.D10	Output data clock N	RLDC_QK_N0	Differential 1.5-V HSTL Class I	AB32
U24.R3	Output data clock N	RLDC_QK_N1		AJ32
U24.D11	Output data clock P	RLDC_QK_P0		AB31
U24.R2	Output data clock P	RLDC_QK_P1		AJ31
U24.F12	Data valid	RLDC_QVLD	1.5-V HSTL Class I	AC32
U24.L1	Input reference voltage	RLDC_REFn		AD31
U24.M1	Write enable	RLDC_WEn		AE32

Table 2–48 lists the RLDRAM II CIO component reference and manufacturing information.

Table 2–48. RLDRAM II CIO Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U24	533 MHz RLDRAM II CIO 16M x36, BGA-144	Micron	MT49H16M36HT-18	www.micron.com

SSRAM

The SSRAM device consists of a single standard synchronous SRAM, providing 2-MB memory interface with a 36-bit data bus. This device is part of the shared FSM bus which connects to the flash memory, SSRAM, and MAX II CPLD EPM2210 System Controller. The device speed is 250-MHz single-data-rate.

Table 2–49 lists the SSRAM pin assignments, signal names, and functions.

Table 2–49. SSRAM Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 3)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number	Other Connections
U3.R6	Address bus	FSM_A2	2.5-V	G23	U10.T9, U2.B1
U3.P6	Address bus	FSM_A3		F23	U10.R9, U2.C1
U3.A2	Address bus	FSM_A4		D27	U10.P9, U2.D1
U3.A10	Address bus	FSM_A5		D28	U10.T10, U2.D2
U3.B2	Address bus	FSM_A6		F25	U10.P13, U2.A2
U3.B10	Address bus	FSM_A7		F26	U10.R10, U2.C2
U3.N6	Address bus	FSM_A8		G24	U10.M10, U2.A3
U3.P3	Address bus	FSM_A9		F24	U10.T11, U2.B3
U3.P4	Address bus	FSM_A10		E26	U10.N10, U2.C3
U3.P8	Address bus	FSM_A11		D26	U10.R11, U2.D3
U3.P9	Address bus	FSM_A12		A30	U10.P10, U2.C4
U3.P10	Address bus	FSM_A13		A33	U10.T12, U2.A5
U3.P11	Address bus	FSM_A14		B31	U10.M11, U2.B5
U3.R3	Address bus	FSM_A15		A31	U10.R12, U2.C5
U3.R4	Address bus	FSM_A16		B32	U10.N11, U2.D7
U3.R8	Address bus	FSM_A17		A32	U10.T13, U2.D8
U3.R9	Address bus	FSM_A18		M23	U10.P11, U2.A7
U3.R10	Address bus	FSM_A19		L23	U10.R13, U2.B7
U3.R11	Address bus	FSM_A20		B29	U10.M12, U2.C7
U3.B1	Address bus	FSM_A21		C29	U10.R14, U2.C8
U3.A1	Address bus	FSM_A22		C31	U10.N12, U2.A8
U3.B11	Address bus	FSM_A23		D31	U10.T15, U2.G1
U3.C10	Address bus	FSM_A24		F27	U10.P12, U2.H8
U3.P2	Address bus	FSM_A25		D18	U10.E13, U2.B6
U3.J10	Data bus	FSM_D0		G27	U10.P4, U2.F2
U3.J11	Data bus	FSM_D1		F28	U10.R1, U2.E2
U3.K10	Data bus	FSM_D2		E28	U10.P5, U2.G3
U3.K11	Data bus	FSM_D3		D30	U10.T2, U2.E4
U3.L10	Data bus	FSM_D4		C30	U10.N5, U2.E5
U3.L11	Data bus	FSM_D5		F29	U10.R3, U2.G5
U3.M10	Data bus	FSM_D6		E29	U10.P6, U2.G6

Table 2–49. SSRAM Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 3)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number	Other Connections
U3.M11	Data bus	FSM_D7	2.5-V	J24	U10.R4, U2.H7
U3.D10	Data bus	FSM_D8		J25	U10.N6, U2.E1
U3.D11	Data bus	FSM_D9		A24	U10.T4, U2.E3
U3.E10	Data bus	FSM_D10		A26	U10.M6, U2.F3
U3.E11	Data bus	FSM_D11		B25	U10.R5, U2.F4
U3.F10	Data bus	FSM_D12		A25	U10.P7, U2.F5
U3.F11	Data bus	FSM_D13		J20	U10.T5, U2.H5
U3.G10	Data bus	FSM_D14		K20	U10.N7, U2.G7
U3.G11	Data bus	FSM_D15		K21	U10.R6, U2.E7
U3.D1	Data bus	FSM_D16		K22	U10.M7
U3.D2	Data bus	FSM_D17		C26	U10.T6
U3.E1	Data bus	FSM_D18		B26	U10.P14
U3.E2	Data bus	FSM_D19		J22	U10.R7
U3.F1	Data bus	FSM_D20		J21	U10.P8
U3.F2	Data bus	FSM_D21		C24	U10.T7
U3.G1	Data bus	FSM_D22		E25	U10.N8
U3.G2	Data bus	FSM_D23		D25	U10.R8
U3.J1	Data bus	FSM_D24		D24	U10.F12
U3.J2	Data bus	FSM_D25		A27	U10.D16
U3.K1	Data bus	FSM_D26		A29	U10.F13
U3.K2	Data bus	FSM_D27		C27	U10.D15
U3.L1	Data bus	FSM_D28		C28	U10.F14
U3.L2	Data bus	FSM_D29		E23	U10.D14
U3.M1	Data bus	FSM_D30		D23	U10.E12
U3.M2	Data bus	FSM_D31		B28	U10.C15
U3.A8	Address status controller	SSRAM_ADSCn		G20	—
U3.B9	Address status processor	SSRAM_ADSPn		F20	—
U3.A9	Address valid	SSRAM_ADVn		D21	—
U3.A7	Byte write enable	SSRAM_BWEn		B22	—
U3.B5	Byte lane 0 write enable	SSRAM_BWn0		D22	—
U3.A5	Byte lane 1 write enable	SSRAM_BWn1		E22	—
U3.A4	Byte lane 2 write enable	SSRAM_BWn2		E20	—
U3.B4	Byte lane 3 write enable	SSRAM_BWn3		H20	—
U3.B3	Chip enable 2	SSRAM_CE2		—	—
U3.A3	Chip enable 1	SSRAM_CE1n		A21	—
U3.A6	Chip enable 3	SSRAM_CE3n		—	—
U3.B6	Clock	SSRAM_CLK		C21	—
U3.N11	Data bus parity lane 0	SSRAM_DQP0		—	—

Table 2–49. SSRAM Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 3)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number	Other Connections
U3.C11	Data bus parity lane 1	SSRAM_DQP1	2.5-V	—	—
U3.C1	Data bus parity lane 2	SSRAM_DQP2		—	—
U3.N1	Data bus parity lane 3	SSRAM_DQP3		—	—
U3.B7	Global write enable	SSRAM_GWn		—	U10.E11
U3.R1	Mode	SSRAM_MODE		—	U10.D11
U3.B8	Output enable	SSRAM_OEn		A22	—
U3.H11	Sleep	SSRAM_ZZ		—	U10.A13

Table 2–50 lists the SSRAM component reference and manufacturing information.

Table 2–50. SSRAM Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U3	250 MHz standard synchronous pipelined SCD static RAM, 512K × 36, BGA-165	ISSI Inc.	IS61VPS51236A-250B3	www.issi.com

Flash

The flash interface consists of a single Numonyx StrataFlash embedded memory device, providing 64-MB memory interface with a 16-bit data bus. This device is part of the shared FSM bus which connects to the flash memory, SSRAM, and MAX II CPLD EPM2210 System Controller.

The parameter blocks of this device are located at the bottom of the address space. The parameter blocks are 32 K and main blocks are 128 K.

This 16-bit data memory interface can sustain burst read operations at up to 52 MHz for a throughput of 832 Mbps. The write performance is 125 µs for a single word and 440 µs for a 32-word buffer. The erase time is 400 ms for a 32 K parameter block and 1200 ms for a 128 K main block.

Table 2–51 lists the flash pin assignments, signal names, and functions.

Table 2–51. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number	Other Connections
U2.F6	Address valid	FLASH_ADVn	2.5-V	D20	U10.L13
U2.B4	Chip enable	FLASH_CEn		K25	U10.K14
U2.E6	Clock	FLASH_CLK		K24	U10.L15
U2.F8	Output enable	FLASH_OEn		K23	U10.M16
U2.F7	Ready	FLASH_RDYBSYn		C20	U10.L11
U2.D4	Reset	FLASH_RESETn		G21	U10.M15
U2.G8	Write enable	FLASH_WEn		L22	U10.L12
U2.C6	Write protect	FLASH_WPn		—	—
U2.A1	Address bus	FSM_A1		H23	U10.T8
U2.B1	Address bus	FSM_A2		G23	U10.T9, U3.R6
U2.C1	Address bus	FSM_A3		F23	U10.R9, U3.P6
U2.D1	Address bus	FSM_A4		D27	U10.P9, U3.A2
U2.D2	Address bus	FSM_A5		D28	U10.T10, U3.A10
U2.A2	Address bus	FSM_A6		F25	U10.P13, U3.B2
U2.C2	Address bus	FSM_A7		F26	U10.R10, U3.B10
U2.A3	Address bus	FSM_A8		G24	U10.M10, U3.N6
U2.B3	Address bus	FSM_A9		F24	U10.T11, U3.P3
U2.C3	Address bus	FSM_A10		E26	U10.N10, U3.P4
U2.D3	Address bus	FSM_A11		D26	U10.R11, U3.P8
U2.C4	Address bus	FSM_A12		A30	U10.P10, U3.P9
U2.A5	Address bus	FSM_A13		A33	U10.T12, U3.P10
U2.B5	Address bus	FSM_A14		B31	U10.M11, U3.P11
U2.C5	Address bus	FSM_A15		A31	U10.R12, U3.R3
U2.D7	Address bus	FSM_A16		B32	U10.N11, U3.R4
U2.D8	Address bus	FSM_A17		A32	U10.T13, U3.R8
U2.A7	Address bus	FSM_A18		M23	U10.P11, U3.R9
U2.B7	Address bus	FSM_A19		L23	U10.R13, U3.R10
U2.C7	Address bus	FSM_A20		B29	U10.M12, U3.R11
U2.C8	Address bus	FSM_A21		C29	U10.R14, U3.B1
U2.A8	Address bus	FSM_A22		C31	U10.N12, U3.A1
U2.G1	Address bus	FSM_A23		D31	U10.T15, U3.B11
U2.H8	Address bus	FSM_A24		F27	U10.P12, U3.C10
U2.B6	Address bus	FSM_A25		D18	U10.E13, U3.P2
U2.B8	Address bus	FSM_A26		W10	U10.J16
U2.F2	Data bus	FSM_D0		G27	U10.P4, U3.J10

Table 2–51. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Stratix IV E Device Pin Number	Other Connections
U2.E2	Data bus	FSM_D1	2.5-V	F28	U10.R1, U3.J11
U2.G3	Data bus	FSM_D2		E28	U10.P5, U3.K10
U2.E4	Data bus	FSM_D3		D30	U10.T2, U3.K11
U2.E5	Data bus	FSM_D4		C30	U10.N5, U3.L10
U2.G5	Data bus	FSM_D5		F29	U10.R3, U3.L11
U2.G6	Data bus	FSM_D6		E29	U10.P6, U3.M10
U2.H7	Data bus	FSM_D7		J24	U10.R4, U3.M11
U2.E1	Data bus	FSM_D8		J25	U10.N6, U3.D10
U2.E3	Data bus	FSM_D9		A24	U10.T4, U3.D11
U2.F3	Data bus	FSM_D10		A26	U10.M6, U3.E10
U2.F4	Data bus	FSM_D11		B25	U10.R5, U3.E11
U2.F5	Data bus	FSM_D12		A25	U10.P7, U3.F10
U2.H5	Data bus	FSM_D13		J20	U10.T5, U3.F11
U2.G7	Data bus	FSM_D14		K20	U10.N7, U3.G10
U2.E7	Data bus	FSM_D15		K21	U10.R6, U3.G11

Table 2–52 lists the flash component reference and manufacturing information.

Table 2–52. Flash Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U2	512-Mbyte synchronous flash	Numonyx	PC28F512P30BF	www.numonyx.com

Power Supply

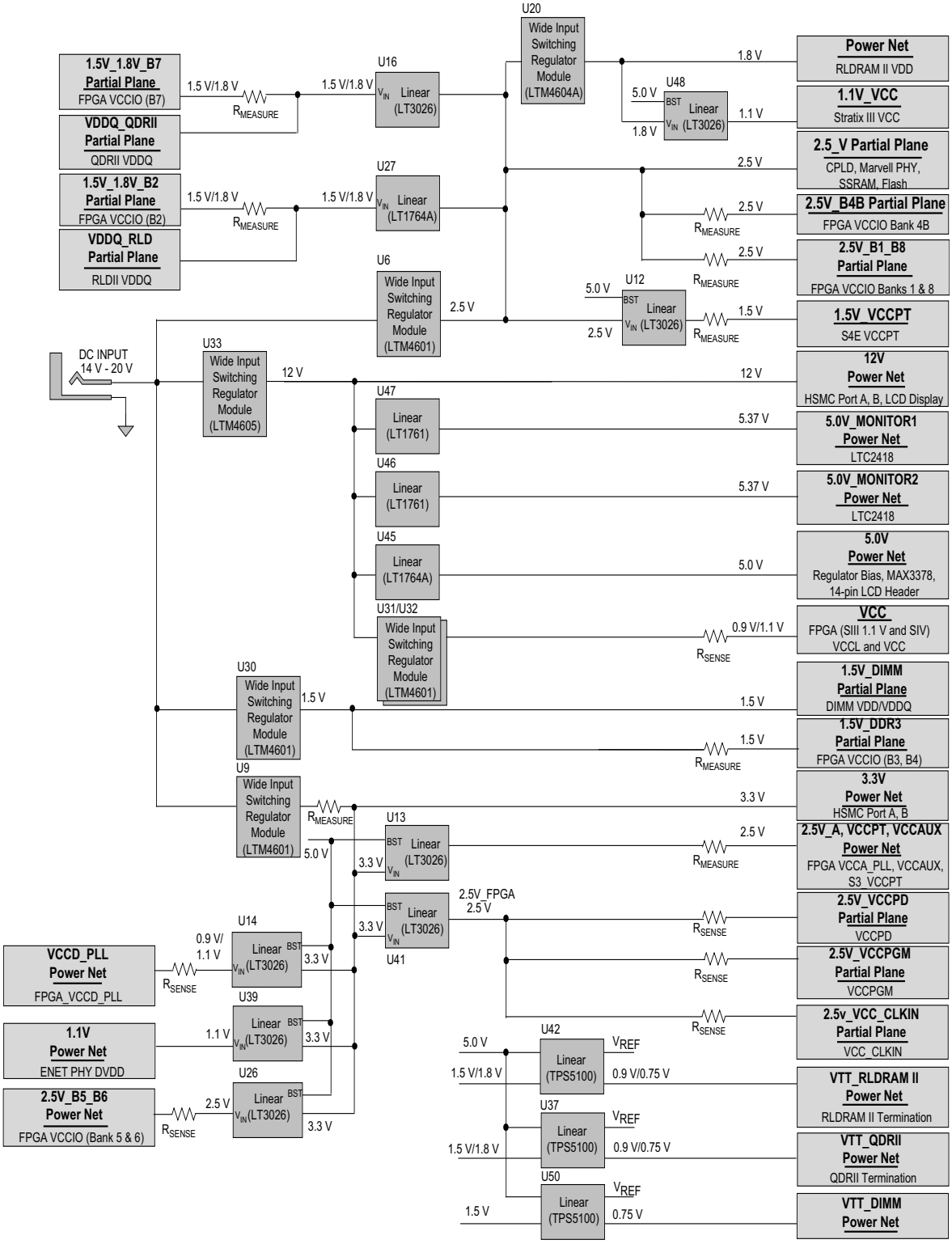
The development board's power is provided through a laptop style DC power input. The input voltage must be in the range of 14 V to 20 V. The DC voltage is then stepped down to various power rails used by the components on the board.

An on-board multi-channel analog-to-digital converter (ADC) is used to measure both the voltage and current for several specific board rails. The power utilization is displayed in a GUI that graphs power consumption versus time.

Power Distribution System

Figure 2–9 shows the power distribution system on the development board.

Figure 2–9. Power Distribution System



Power Measurement

There are 12 power supply rails which have on-board voltage and current sense capabilities. These 8-channel differential 24-bit ADC devices and rails are split from the primary supply plane by a low-value sense resistor for the ADC to measure voltage and current. A SPI bus connects these ADC devices to the MAX II CPLD EPM2210 System Controller.

Figure 2–10 shows the block diagram for the power measurement circuitry.

Figure 2–10. Power Measurement Circuit

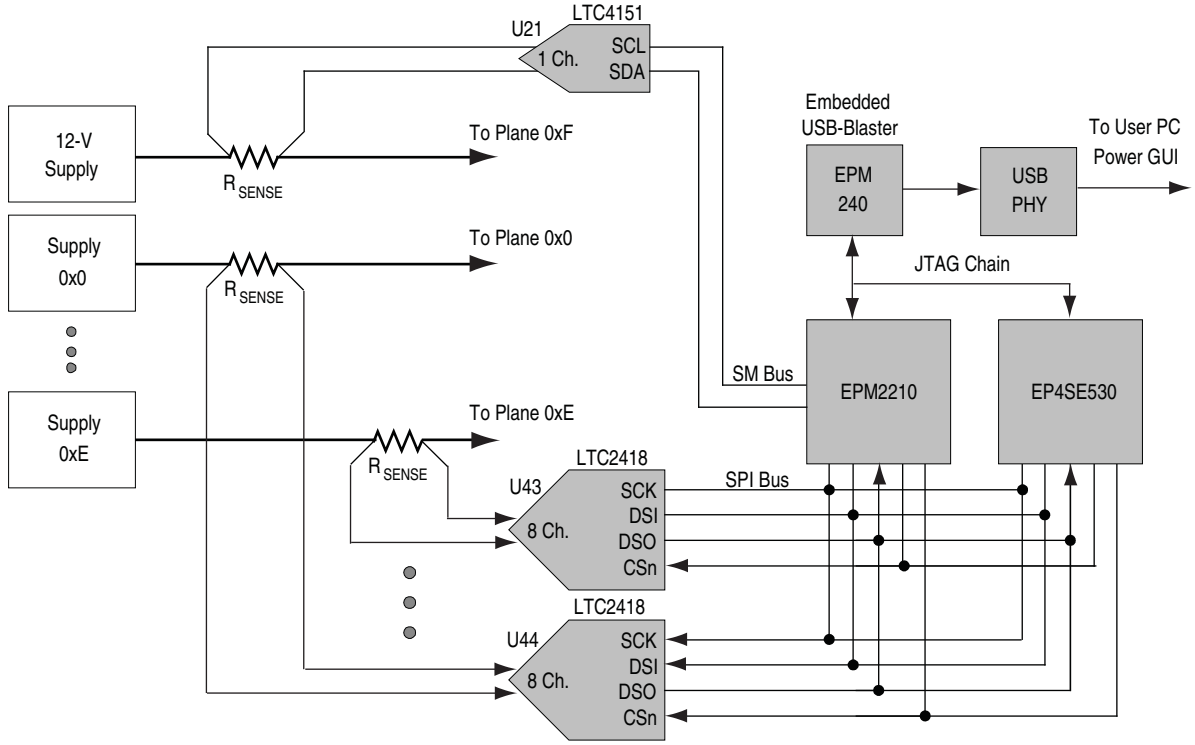


Table 2–53 lists the targeted rails. The schematic signal name column specifies the name of the rail being measured and the device pin column specifies the devices attached to the rail. If no subnet is named, the power is the total output power for that voltage.

Table 2–53. Power Rail Measurements Based on the Rotary Switch Position (Part 1 of 2)

Switch	Schematic Signal Name	Voltage (V)	Device Pin	Description
0	1.5V_1.8V_B7	1.5	VCCIO_B7	Bank 7 I/O power (QDRII)
1	2.5V_B5_B6	2.5	VCCIO_B5	Bank 5 I/O power (HSMC port A)
			VCCIO_B6	Bank 6 I/O power (HSMC port B)
2	1.5V_DDR3	1.5	VCCIO_B3	Bank 3 I/O power (DDR3 memory)
			VCCIO_B4A	Bank 4A I/O power (DDR3 memory)
			VCCIO_B4C	Bank 4C I/O power (DDR3 memory)

Table 2–53. Power Rail Measurements Based on the Rotary Switch Position (Part 2 of 2)

Switch	Schematic Signal Name	Voltage (V)	Device Pin	Description
3	2.5V_B4B	2.5	VCCIO_B4B	Bank 4B I/O power (Character LCD, HSMA)
4	1.5V_1.8V_B2	1.5	VCCIO_B2	Bank 2 I/O power (RLDRAM II CIO)
5	2.5V_VCCPD		VCCPD	I/O pre-drivers power
6	VCCL	0.9	VCC	FPGA core and periphery power
7	VCCPT	1.5	VCCPT	Programmable power technology
8	VCCD_PLL	0.9	VCCD_PLL	Digital PLL power
9	2.5V_A_SENSE	2.5	VCCA_PLL	Analog PLL power
10	2.5V_VCCPGM	2.5	VCCPGM	Configuration pins power
11	2.5V_VCC_CLKIN	2.5	VCC_CLKIN	Differential clock power for top and bottom I/O banks
12	2.5V_B1_B8	2.5	VCCIO_B1	Bank 1 I/O power (Graphics LCD, Ethernet, and seven-segment display)
			VCCIO_B8	Bank 8 I/O power (FSM bus and user LEDs)

Table 2–54 lists the power measurement ADC component reference and manufacturing information

Table 2–54. Power Measurement ADC Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U23, U25	8-channel differential 24-bit ADC	Linear Technology	LTC2418CGN#PBF	www.linear.com

Statement of China-RoHS Compliance

Table 2–55 lists hazardous substances included with the kit.

Table 2–55. Table of Hazardous Substances' Name and Concentration ***Notes (1), (2)***

Part Name	Lead (Pb)	Cadmium (Cd)	Hexavalent Chromium (Cr6+)	Mercury (Hg)	Polybrominated biphenyls (PBB)	Polybrominated diphenyl Ethers (PBDE)
Stratix IV E FPGA development board	X*	0	0	0	0	0
12 V power supply	0	0	0	0	0	0
Type A-B USB cable	0	0	0	0	0	0
User guide	0	0	0	0	0	0

Notes to Table 2–55:

(1) 0 indicates that the concentration of the hazardous substance in all homogeneous materials in the parts is below the relevant threshold of the SJ/T11363-2006 standard.

(2) X* indicates that the concentration of the hazardous substance of at least one of all homogeneous materials in the parts is above the relevant threshold of the SJ/T11363-2006 standard, but it is exempted by EU RoHS.

A. Board Revision History

This appendix catalogs revisions to the Stratix IV E FPGA development board.

Table A–1 lists the versions of all releases of the Stratix IV E FPGA development board.

Table A–1. Stratix IV E FPGA Development Board Revision History

Version	Release Date	Description
Graphics LCD	May 2011	The Optrex 128x64 graphics LCD part number F-51852GNFQJ-LB-AIN was replaced with Optrex part number F-55472GNFQJ-LB-AEN.
Single-die flash	June 2010	The Intel dual-die 512-Mb flash part number PC48F4400P0VB00 was replaced with Numonyx single-die flash part number PC28F512P30BF.
Production silicon	November 2009	Initial release.

Graphics LCD Version Differences

The original graphics LCD part number F-51852GNFQJ-LB-AIN which uses negative bias voltages connected to nets V1, V2, V3, V4, and V5 has become obsolete. The replacement module uses positive bias voltages connected to these same nets. This requires a modification to the power supply on the circuit board.

You should not use the original graphics LCD on a newer, positive bias voltage circuit board, and conversely, not use the newer graphics LCD on an earlier, negative bias voltage circuit board.

To determine which graphics LCD model your board is using, refer to the back of the module itself (J27) for the printed part number. This may require un-snapping the module from the board.

To determine which type of power supply your board is using, check if your board has inductors L5 and L6 installed. These inductors are located on the bottom of the board underneath the graphics LCD.

Single-Die Flash Version Differences

The single-die flash version of the Stratix IV E FPGA development board is created to replace the obsolete dual-die flash device with a single-die flash device. The two flash devices are considered equivalent except for some software routines used to access them because the single-die device has only one CFI table whereas the duel-die device has two CFI tables.

To determine which flash your board is using, refer to the device part number installed at U2. The single-die package is smaller than the dual-die version.

For more information about the flash change and its application, refer to the *Stratix IV E FPGA Development Kit User Guide*.

This chapter provides additional information about the document and Altera.

Document Revision History

The following table shows the revision history for this document.

Date	Version	Changes
May 2011	1.2	■ Updated the manufacturing part number of the flash device in Table 2–52 to indicate the replacement of dual-die flash with a single-die flash. ■ Updated the manufacturing part number of the graphics LCD in Table 2–36 to indicate the replacement of a new graphics LCD version. ■ Added an appendix to document the board revision changes. ■ Converted the document to new frame template and made textual and style changes.
February 2010	1.1	■ Updated development board block diagram in Figure 1–1. ■ Adjusted flash memory map in Table 2–7. ■ Updated QDR II+ SRAM manufacturing information in Table 2–46.
November 2009	1.0	Initial release.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact *(1)*	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Non-technical support (General)	Email	nacomp@altera.com
(Software Licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.
italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>***.pof** file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections within a document and titles of Quartus II Help topics. For example, "Typographic Conventions."
`Courier type`	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. The suffix `n` denotes an active-low signal. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
↵	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	A question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.