Evaluation Board for AD9510

AD9510/PCB

FEATURES

Full-featured evaluation board for the AD9510
PC evaluation software for control and exercise of the AD9510
USB interface

APPLICATIONS

AD9510 performance evaluation
GUI control panel for learning AD9510 programming

EVALUATION BOARD DESCRIPTION

This user guide describes the AD9510 evaluation board hardware and software. The software provides a graphical user interface (GUI) for easy interface with the various on-chip functions of the AD9510. This allows for a thorough exploration and evaluation of the AD9510's operation, performance, and capabilities. **Note that the AD9510 evaluation board software should be installed before connecting the AD9510 evaluation board to the PC.**

The AD9510 is a highly sophisticated, performance clock distribution part with numerous user programmable functions. To use the evaluation board properly, see the current data sheet for the AD9510 on the Analog Devices website. You can download the data sheet from www.analog.com/AD9510.

Note that this user guide includes instructions for both the AD9510/PCB and AD9510-VCO/PCB, which includes a 245.76 MHz VCXO and loop filter.

AD9510 DEVICE DESCRIPTION

The AD9510 provides a multi-output clock distribution function along with an on-chip phase-locked loop (PLL) core. The design emphasizes low jitter and phase noise to maximize data converter performance. Other applications with demanding phase noise and jitter requirements also benefit from this part.

The PLL section consists of a programmable reference divider (R), a low noise phase frequency detector (PFD), a precision charge pump (CP), and a programmable feedback divider (N). By connecting an external VCXO or VCO to the CLK2/CLK2B pins, frequencies up to 1.6 GHz may be synchronized to the input reference.

There are eight independent clock outputs: four are LVPECL (1.2 GHz), and four are selectable as either LVDS (800 MHz) or CMOS (250 MHz).

Each output has a programmable divider can be bypassed or set to divide by any integer up to 32. The phase of one clock output relative to another clock output can be varied by means of a divider phase select function that serves as a coarse timing adjustment. Two of the LVDS/CMOS outputs feature programmable delay elements with full-scale ranges up to 10 ns of delay. This fine tuning delay block has 5-bit resolution, giving 32 possible delays from which to choose for each full-scale setting.

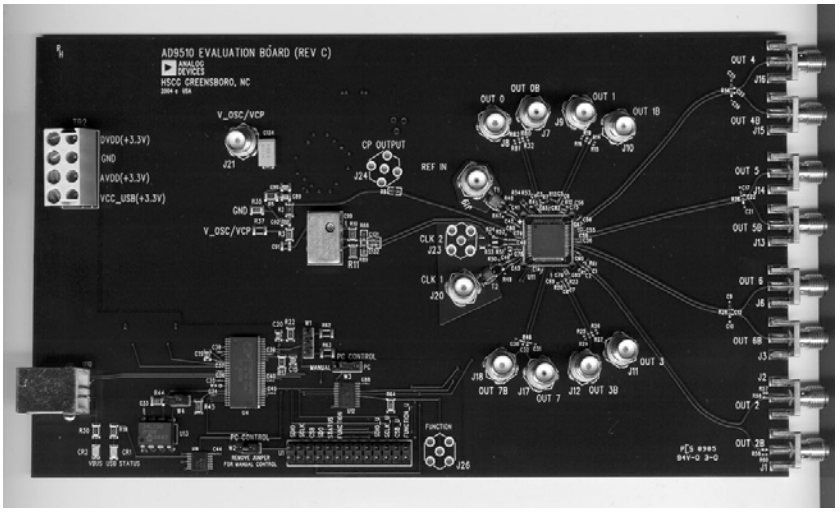

Figure 1. AD9510 Evaluation Board

Rev. 0
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TABLE OF CONTENTS

REVISION HISTORY

10/05—Revision 0: Initial Version

EVALUATION BOARD REQUIREMENTS

SYSTEM FEATURES

In order to run the evaluation software, the following system features are needed:

Operating System

Microsoft® Windows® 98, Windows® ME, Windows® 2000, or Windows® XP.

Display

Designed for XGA with 1024 × 768 display resolution, 800 × 600 minimum recommended display resolution.

PC

A Pentium® II-class or higher recommended.

Disk Space

6 MB or more.

I/O Port

USB port.

HARDWARE NEEDS

Before using the AD9510 evaluation board, take a moment to verify that you have the following hardware:

Power Supplies

The AD9510/PCB requires at least two independent power supplies, one for V_OSC/VCP (3.3 V to 5 V) and one for AVDD/DVDD/VCC_USB (3.3 V ± 5% on the board).

Function Generators

A signal source (crystal oscillator, function generator) is required to clock the AD9510.

Measurement

An appropriate measurement device such as a spectrum analyzer or a high bandwidth oscilloscope is needed.

SETTING UP THE EVALUATION BOARD

POWER SUPPLIES

The AD9510 evaluation board has four distinct power domains: AVDD, DVDD, VCC_USB, and V_OSC/VCP. Shown in Table 1, these domains provide power to the analog and digital portion of the AD9510, the charge pump in the PLL and VCO/VCXO, as well as USB communication circuitry. These four domains do not require four distinct power supplies however, as the analog, digital, and USB domains always run at 3.3 V. The VCO/VCXO and charge pump domain can run at 3.3 V to 5.0 V, depending on the requirements of the VCO/VCXO.

Table 1. Power Supply Domain Descriptions

Name	Voltage	Description
AVDD	3.3 V	Provides power to the analog portion of the AD9510.
DVDD	3.3 V	Provides power to the digital portion of the AD9510.
VCC_USB	3.3 V	Provides power to the USB circuitry on the evaluation board.
V_OSC/VCP	3.3 V/5 V	Provides power to the charge pump in the on-chip PLL and the external oscillator.

Connect the power supplies to the AD9510 evaluation board using the 4-pin connector (TB2) on the upper left-hand side of the board. This connector has pins for AVDD, DVDD, VCC_USB and GND.

The V_OSC/VCP power supply connection is through an SMA connector, J21.

USB AND PC VS. MANUAL CONTROL

The AD9510 evaluation board has two options available to program the part. The first is a PC-controlled USB connection using the evaluation software provided with the evaluation board. The second is using the I/O header pins to program the part manually.

Configuring the Evaluation Board for PC Control (Default Setup)

To use the evaluation software and USB connection, the evaluation board must be configured for PC control. This is accomplished by connecting two jumpers. First, W29, located next to the I/O header, must have a jumper. Next, W3 must have a jumper on the PC side (right) of the connector. With those two jumpers in place, the board is configured for PC control through the USB connection. This is the default configuration for the AD9510 evaluation board.

Configuring the Evaluation Board for Manual Control

To program the part manually through the I/O header, the evaluation board must be configured for manual control. This is accomplished by connecting two jumpers. First, W29, located next to the I/O header must be empty (no jumper). Next, W3 must have a jumper on the manual side (left) of the connector. With this configuration, the board is ready for manual control through the I/O header.

CLOCK INPUTS

Table 2 shows the three clock inputs on the evaluation board: REFIN, CLK1, and CLK2. REFIN is the reference clock for the PLL, CLK1 is a clock distribution input, and CLK2 is the oscillator input for an external VCO or VCXO. If the on-chip PLL frequency synthesizer and external VCO/VCXO is not used, CLK2 can be used as an additional clock distribution input. Each of the three AD9510 clock inputs is differential. However, the AD9510 evaluation board is configured for single-ended inputs.

Table 2. Clock Inputs and Functions

Clock Input	Function
REFIN	Reference Frequency for PLL
CLK1	Clock Distribution Input 1
CLK2	Clock Distribution Input 2; External Oscillator Input for PLL

Single-Ended Input Configuration

The REFIN, CLK1, and CLK2 inputs are connected via single-ended SMA connectors. However, each of these inputs is converted from single-ended to differential by means of a balun before driving the AD9510 inputs differentially.

Driving CLK2 with an External VCO/VCXO

It is important to remember that when a VCXO is being used, the CLK2 SMA connection must be electrically disconnected from the part. In that case, the VCXO output is used as the CLK2/CLK2B input to the AD9510.

When a VCO is used, the CLK2 input must be connected to the VCO output by soldering a 0 Ω resistor at R9. It is also important to remember that while you can view the VCO output through the CLK2 SMA, driving a signal into the CLK2 SMA while the VCO is running is not recommended.

PHASE-LOCKED LOOP (PLL)

The on-chip PLL frequency synthesizer requires an external oscillator and charge pump filter to operate. The AD9510 evaluation board has three options to provide an external oscillator: an on-board VCXO, an on-board VCO, or an off-board oscillator. All three options require an appropriate charge pump filter. For the on-board configurations, pads are provided for the charge pump filter. If the off-board configuration is desired, an SMA allows the user to take the charge pump current to another board.

Configuration Options

There are three primary configurations for the AD9510 evaluation board when using the PLL. A VCXO, a VCO, or an off-board oscillator and charge pump filter can be used. If the PLL is not used, but the CLK2 input is still desired, the board should be configured as if an off-board oscillator was being used. A summary of configuration components is presented in Table 3.

Using the VCXO (Default Setup on AD9510-VCO/PCB)

To configure the AD9510 evaluation board for use with a VCXO, the first step is to populate the board with the VCXO and an appropriate charge pump filter. These components should be placed on the top of the board. Next, the CLK2 SMA must be electrically disconnected from the part by the removal of Balun T3.

In addition, the signal traces from the VCXO that is to be shorted to the part input traces through 0 Ω resistors at R33 and R34. The charge pump trace should be shorted to the VCXO charge pump filter through a 0 Ω resistor at R8. There should be no resistors at R38 or R6 for the VCXO configuration. Finally, a 0 Ω resistor is placed at R35 [R37] to reference the charge pump filter to GND [V_OSC/VCP].

Using the VCO

To configure the AD9510 evaluation board for use with an on-board VCO, the first step is to populate the VCO and VCO charge pump filter on the bottom of the board. Just as with the charge pump filter for the VCXO, the VCO charge pump filter needs to be referenced to V_OSC/VCP or GND. This can be accomplished by placing a 0 Ω resistor at R29 or R31, respectively. Next, the charge pump current trace from the part must be connected to the charge pump filter. This is accomplished by placing a 0 Ω resistor at R38 and R6. In addition, there should be no resistor at R8. Next, the VCO output needs to be connected to the CLK2 input trace. This is accomplished placing a 0 Ω resistor at R9. Finally, the CLK2 input must be configured for single-ended input. Any resistors at R33 and R34 should be removed and then Balun T3 should be replaced. (See the Single-Ended Input Configuration section.)

Using an Off-Board Oscillator and Charge Pump Filter

To configure the AD9510 evaluation board for use with an off-board oscillator and charge pump filter, the charge pump output SMA and CLK2 SMA input (through Balun T3) must be connected. The charge pump SMA is connected by removing any resistors at R8 or R6, and placing a 0 Ω resistor at R38. The CLK2 input can be configured by first removing any resistors at R9, R33, R34, and then placing a balun at T3.

Default PLL Configuration

Depending on the evaluation board part number, the AD9510/PCB can come with or without a 245.76 MHz VCXO.

Table 3. PLL Configuration Components

PLL Configuration	VCXO	VCO	T3	R33	R34	R8	R38	R6
Not in Use			Required	Open	Open	Open	Open	Open
VCXO	Required		Open	0 Ω	0 Ω	0 Ω	Open	Open
VCO		Required	Required	Open	Open	Open	0 Ω	0 Ω
Off-Board Oscillator			Required	Open	Open	Open	0 Ω	Open

Table 4. AD9510 Evaluation Board Configurations

Part Number	PLL Configuration (Default)	Oscillator Frequency (Default)	Charge Pump Filter (Default)
AD9510/PCB	No VCO/VCXO	N/A	Not Present
AD9510-VCO/PCB	VCXO	245.76 MHz	Present

CLOCK OUTPUTS

There are eight clock outputs on the AD9510. Four are LVPECL and four are LVDS/CMOS. Each output has a variety of possibilities for output termination.

Output Termination Options

LVPECL Clock Outputs

Each LVPECL output has several output termination options (see Table 5). There are pads for ac coupling capacitors, which can be shorted with 0 Ω resistors if necessary. Additionally, there are two trace-to-GND resistor pads, one before and one after the ac coupling cap. Finally, there is a trace-to-VDD resistor pad. These pads can be used in any combination to provide a wide range of termination possibilities.

LVDS/CMOS Clock Outputs

Each LVDS output has several output termination options. First and foremost, a trace-to-trace resistor is used to control the differential impedance termination. Another trace-to-trace pad can be used for an additional resistor or a trace-to-trace capacitive load. Finally, there are two capacitors to GND that can be used for capacitive loading, or with resistors as resistor-to-ground terminations.

Default Configuration

LVPECL Default Configuration

The default output termination for the LVPECL outputs is 50 Ω to VDD − 2 V. This is accomplished by connecting each output trace, both the true and the complementary, to VDD through a 127 Ω resistor and to GND through an 83 Ω resistor. Additionally, the trace is not ac-coupled, so that there is a 0 Ω resistor in series with each trace where the ac-coupled capacitor would be located.

LVDS/CMOS Default Configuration

The default output termination for the LVDS outputs is a 100 Ω resistor between the two traces. This provides the 100 Ω differential impedance for the LVDS signal. None of the capacitive loading pads is populated.

Changing the Configuration

Changing the termination configuration is as simple as removing or adding resistors and capacitors. Because there are so many different options for termination configurations, refer to Table 5 and Table 6, as well as the Schematic section and text found on the evaluation board to help determine the appropriate termination scheme.

Table 5. LVPECL Output Termination Components

Output Channel	Pre-AC Coupling Resistor to GND	AC Coupling Capacitor	Post-AC Coupling Resistor to GND	Post-AC Coupling Resistor to VDD
OUT0	R4	C4	R82	R81
OUT0B	R7	C3	R80	R32
OUT1	R13	C5	R19	R16
OUT1B	R12	C6	R14	R15
OUT2	R61	C1	R57	R58
OUT2B	R1	C2	R60	R59
OUT3	R23	C7	R27	R26
OUT3B	R20	C8	R25	R24

Table 6. LVDS Output Termination Components

Output Channel	Termination Resistor	Loading Capacitor to GND	Loading Capacitor to Other Trace
OUT4	R56	C25	C27
OUT4B	R56	C26	C27
OUT5	R36	C17	C22
OUT5B	R36	C21	C22
OUT6	R28	C9	C12
OUT6B	R28	C10	C12
OUT7	R46	C30	C32
OUT7B	R46	C31	C32

EVALUATION BOARD SOFTWARE INSTALLATION

As mentioned in the Evaluation Board Requirements section, the following system requirements must be met before installing the evaluation board software:

- **Operating System:** Windows 98, Windows Me, Windows 2000, or Windows XP.
- **Display:** Designed for XGA with 1024 × 768 display resolution, 800 × 600 minimum recommended display resolution.
- **PC:** A Pentium II-class or higher recommended.
- **Disk Space:** 6 MB or more.
- **I/O Port:** USB port.

Follow the instructions below to install the AD9510 evaluation board software. (Note: Do not connect the evaluation board to the computer until *after* the software installation has been completed.)

1. **Log on** with administrative privileges.
2. **Uninstall** any previous version of the AD9510 evaluation software.
3. **Insert** the **AD9510 Evaluation Software CD-ROM** into your computer and run the **setup.exe** from the software folder.

Follow the installation software's instructions on screen.

CONNECTING THE USB

Windows 98, Windows ME, and Windows 2000

1. Power up the evaluation board.
2. Connect the evaluation board to the computer using a USB cable.
3. When the USB cable is connected, a pop-up window (Figure 2) appears and then disappears.

Figure 2.

4. Next, another pop-up window (Figure 3) should appear and disappear.

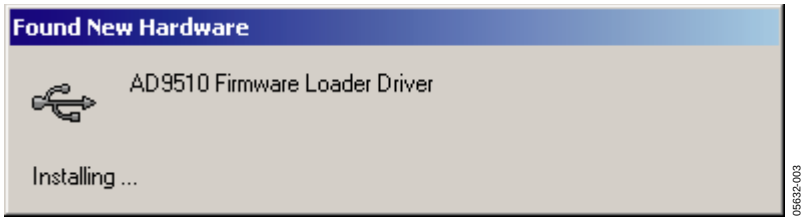

Figure 3.

5. If you are using Windows 2000 and you see the window shown in Figure 4, click **Finish**.

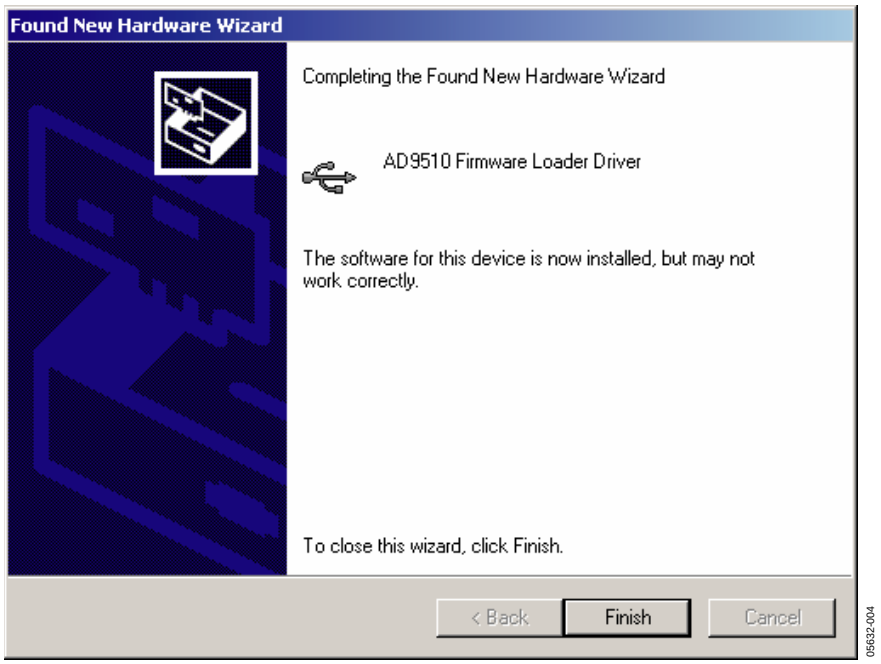

Figure 4.

6. The pop-up window in Figure 5 appears next.

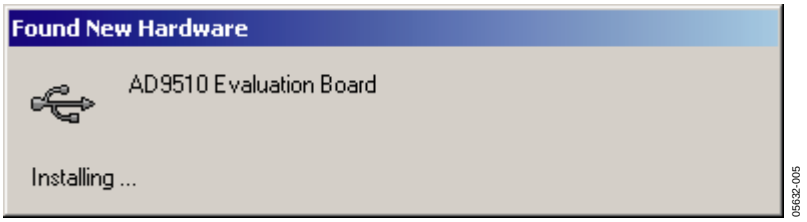

Figure 5.

After the pop-up window in Figure 5 has disappeared, you should notice that the USB Status LED on the evaluation board is flashing. This indicates that the evaluation board is now connected properly.

Windows XP

1. Power up the evaluation board.
2. Connect the evaluation board to the computer using a USB cable.
3. When the USB cable is connected, the window in Figure 6 appears. Click **Next** to continue.

Figure 6.

4. When the window in Figure 7 appears, click **Continue Anyway**.

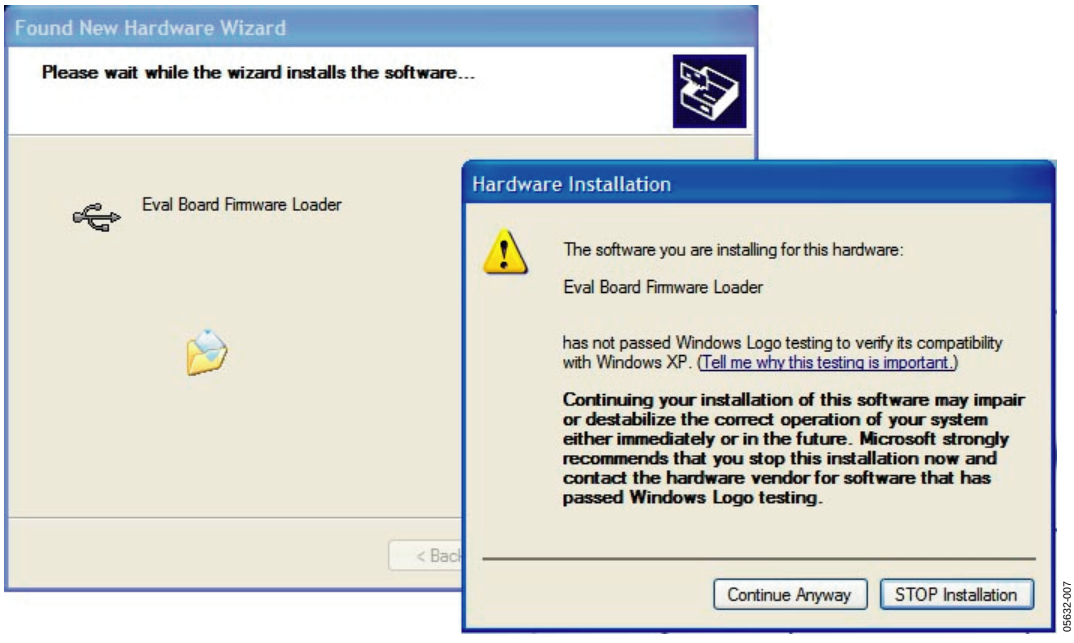

Figure 7.

5. Click **Finish** when the window in Figure 8 appears.

Figure 8.

6. Click **Next** when the window in Figure 9 appears.

Figure 9.

7. When the window in Figure 10 appears, click **Continue Anyway**.

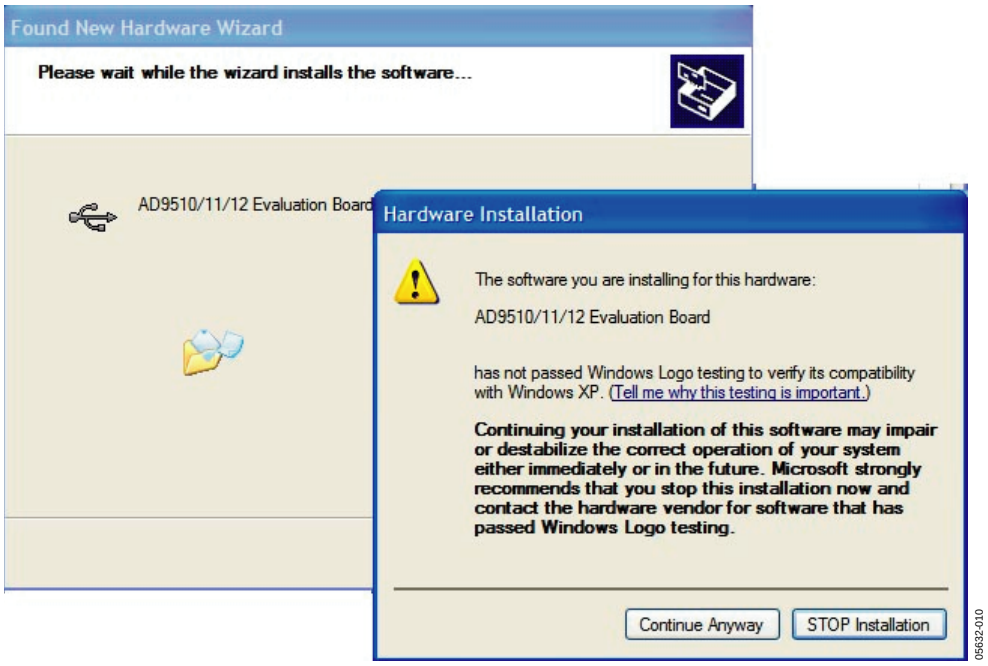

Figure 10.

8. Click **Finish** when the window in Figure 11 appears.

Figure 11.

After the screen in Figure 11 disappears, you should notice that the USB Status LED on the evaluation board is flashing. This indicates that the evaluation board is properly connected.

USING THE EVALUATION BOARD SOFTWARE

GETTING STARTED

Note: Before starting the AD9510 evaluation software, make sure that the AD9510 evaluation board is powered up, connected to the computer, and that the red status LED is flashing. Then, follow these instructions:

1. Click on the **Start** button and select **Programs**.
2. Select **AD9510 Eval Software**, and then **AD9510 Eval Software** (see Figure 12).

Figure 12.

If everything is connected and working properly, then the evaluation software should resemble Figure 13.

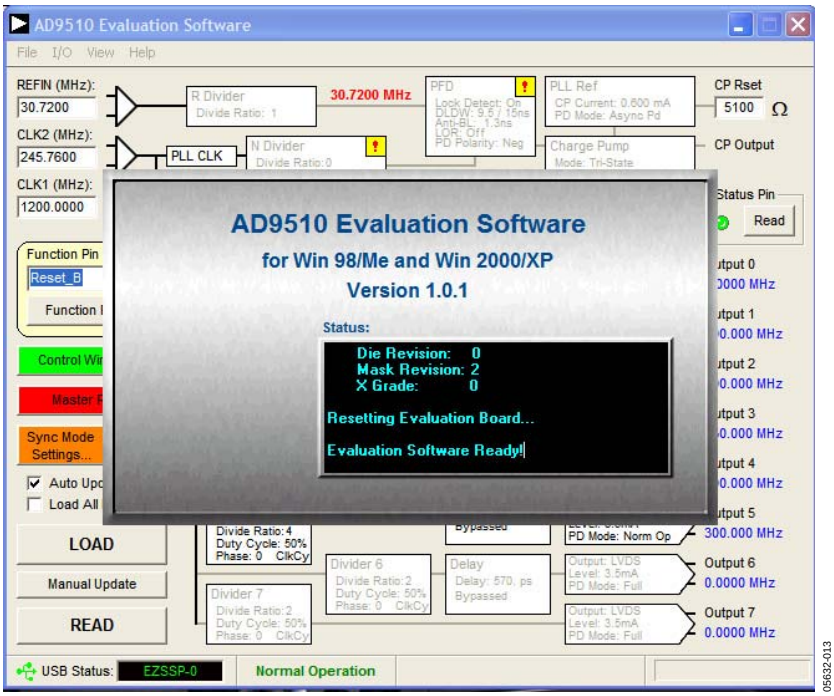

Figure 13.

CONFIGURING THE EVALUATION BOARD

Saving and Loading User Settings

The AD9510 evaluation software allows you to save and load AD9510 configurations. This is accomplished through the **File Menu** and the **Save** or **Load Setup** commands.

1. Select **File > Save Setup**.
2. Select the **directory** and **file name** where you want to save the current user configuration. The default file name is **Settings.stp.** All settings are saved together.
3. To reload these settings at any time, select **File > Load Setup**. A window appears and opens to the default directory, **C:\Program Files\ADI\AD9510 Eval Software.** From here, you may choose the desired setup.

The AD9510 is shipped with a setup/configuration file to configure the AD9510 to run with the default VCXO and PLL configuration. This configuration file assumes a REFCLK frequency of 61.44 MHz and a VCXO of 245.76 MHz. The divider values are R = 4, N = 16 (A = 2, B = 7, P = 2/3). This yields a PFD frequency of 15.36 MHz. The REFCLK frequency can be changed as long as the R divider is altered so that 15.36 MHz is still the input frequency to the PFD.

Serial Control Port Options

The serial control port on the AD9510 has several configuration options. These can be controlled by selecting the **Configure Serial Port** option under the **I/O menu**, which opens the **Serial Port Config** window. (see Figure 14 below).

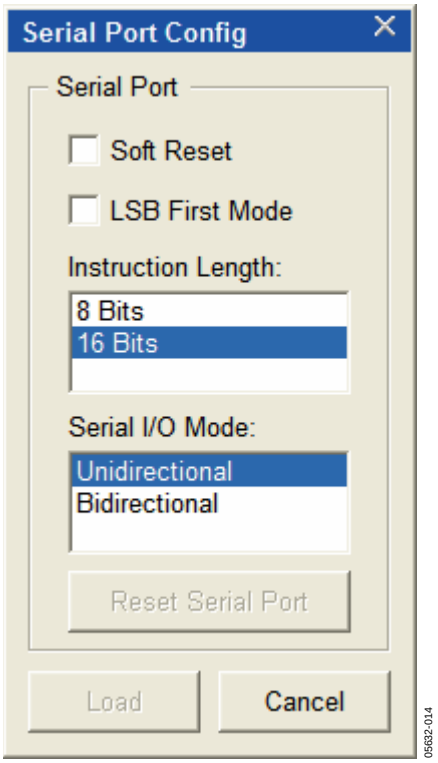

Figure 14. SPI Port Configuration

MAIN INTERFACE WINDOW

The main interface window resembles the block diagram depicted in Figure 15. There are four major sections to the main window: Clock Inputs, PLL, Clock Distribution, and Control Functions.

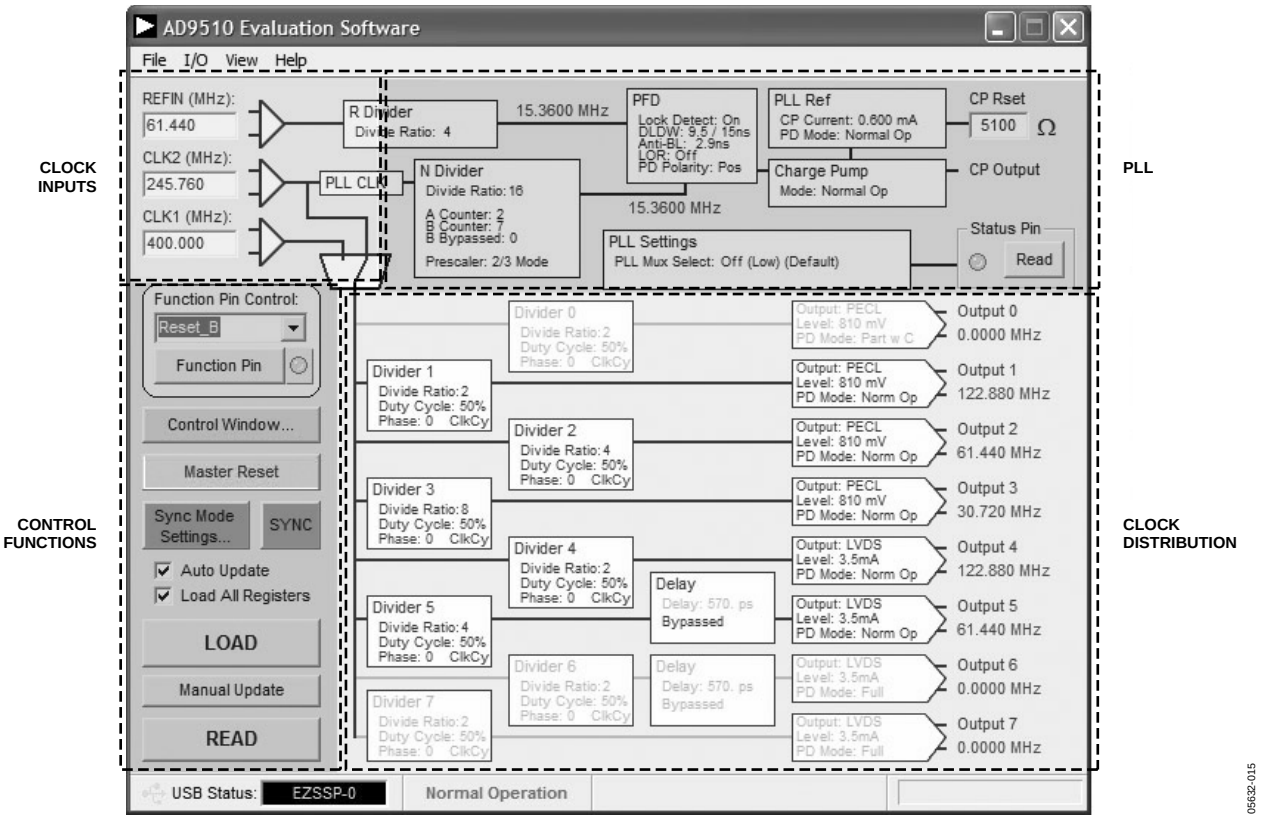

Figure 15. Main Interface Window

PLL Section

The AD9510 on-chip PLL consists of a programmable reference divider, a programmable feedback divider, a phase-frequency detector, and charge pump. All are represented as list boxes in the PLL section (Figure 16) of the main interface window of the software. Additionally, the PLL section includes list boxes for PLL reference settings and one for the status pin output.

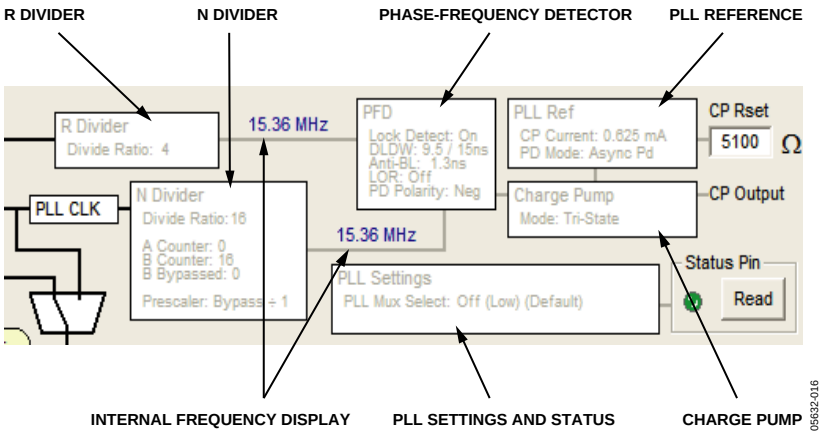

Figure 16. PLL Section, Main Interface Window

When the input frequencies and the divider values are entered, the calculated internal frequencies are displayed. If the frequencies match, they appear in blue; otherwise, they appear in red.

R Divider Window

The R divider window (Figure 17) allows you to set the R divider value. The R divider can be programmed to be 0 to 16383, which would yield a divide value range of 1 to 16384. The actual divide value is the programmed value plus one.

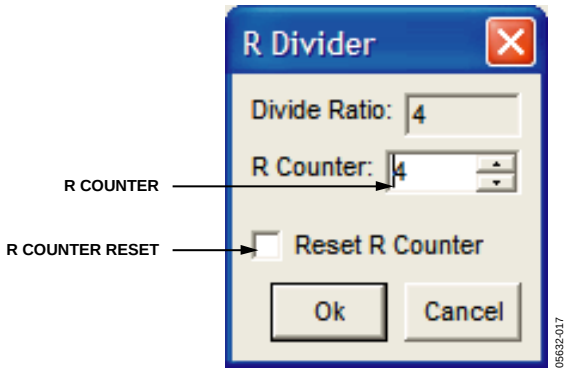

Figure 17. R Divider Window

The R divider counter can also be reset from this window.

N Divider Window

The N divider window (Figure 18) allows you to set the prescaler, A counter, and B counter that control the N divider value. The prescaler settings are selected from the list on the right. The A and B counter values are entered on the left. As each of these three variables are changed, the N counter value automatically updates. This value is equal to the N divide value for the PLL.

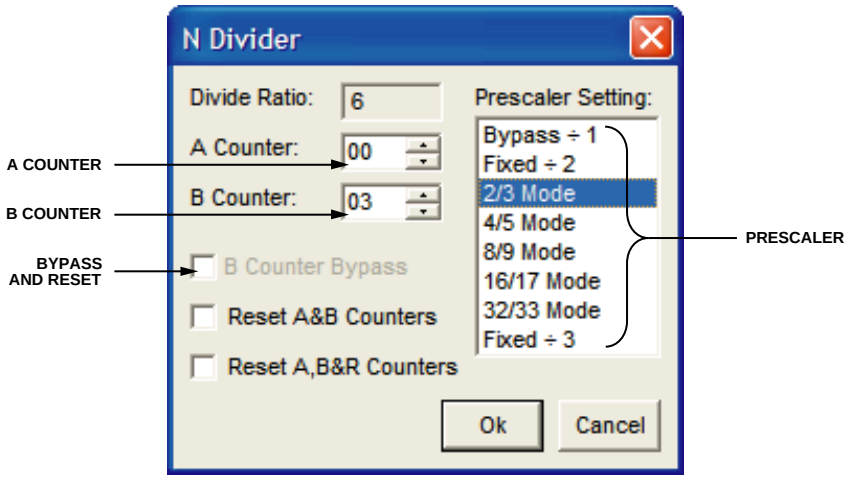

Figure 18. N Divider Window

In addition, there are check boxes to reset both counters or to bypass the B counter. For more information on the N divider setup, please refer to the AD9510 data sheet.

Phase Frequency Detector (PFD) Window

Figure 19 shows the PFD window, which gives you control over the following PFD functions:

- **Lock Detection.** Allows you to specify the precision of the lock detect function or disable it.
- **Loss of Reference.** Allows you to enable/disable the loss of reference function as well as specify the mode and the number of PFD cycles used to determine a loss of reference event.
- **Anti-Backlash Pulse Width**. The default value 1.3 ns is recommended.
- **Phase Detector Polarity.** Select either positive of negative.

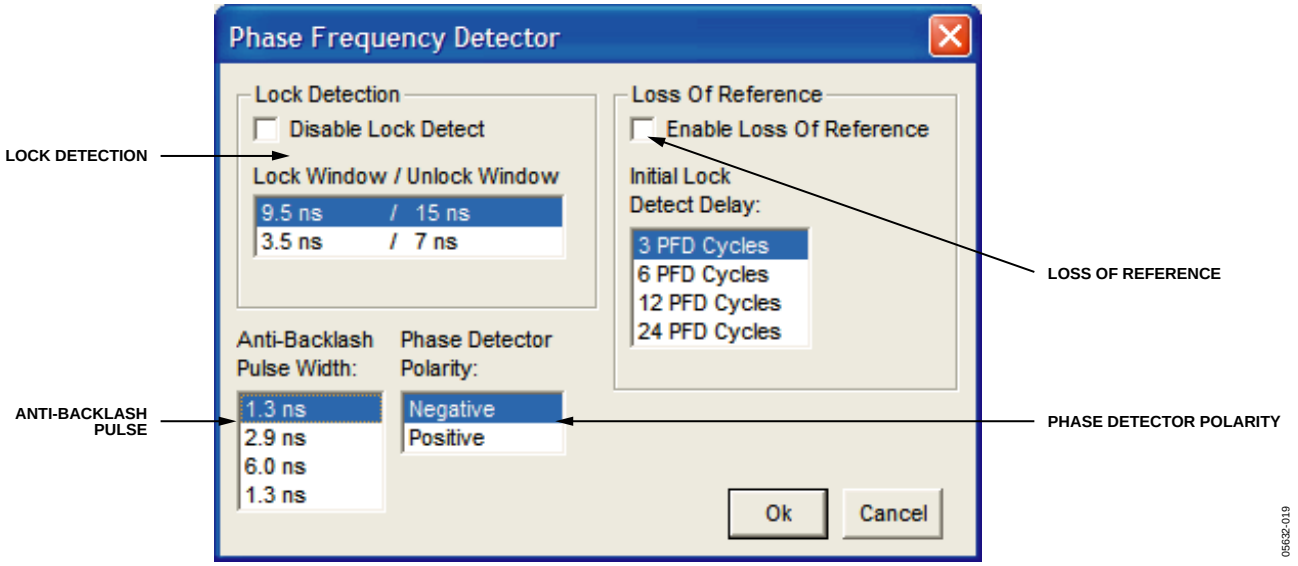

Figure 19. Phase Frequency Detector Window

For more information on any of these settings, please refer to the AD9510 data sheet.

Charge Pump Settings Window

The charge pump settings window (Figure 20) allows you to select one of four different charge pump modes: tri-state, pump up, pump down, and normal operation. For more information on the four charge pump settings, please refer to the AD9510 data sheet.

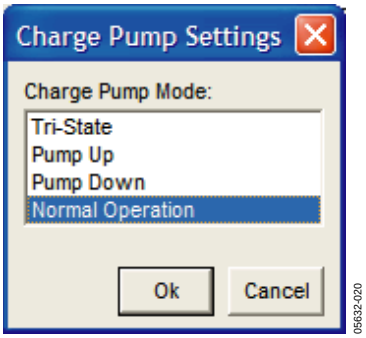

Figure 20. Charge Pump Settings Window

PLL Reference Window

The PLL reference window lets you change the charge pump current settings and change the PLL power down settings. The charge pump current settings are located on the left while the power down settings are located on the right (see Figure 21).

The charge pump current options can be changed by altering the value of the CP Rset list box in the main interface window (see Figure 15). It is located in the upper right-hand corner of the PLL section (see Figure 16). Changing this resistor alters the lowest charge pump current setting and the charge pump current increment. The CP Rset value defaults to 5.1 kΩ, which is how the AD9510 evaluation board is shipped. If you want to change this value, the software accepts Rset values between 3.1 kΩ and 11 kΩ. You must also change the physical CP Rset resistor value on the evaluation board itself. For more information on either of these two options, please refer to the AD9510 data sheet.

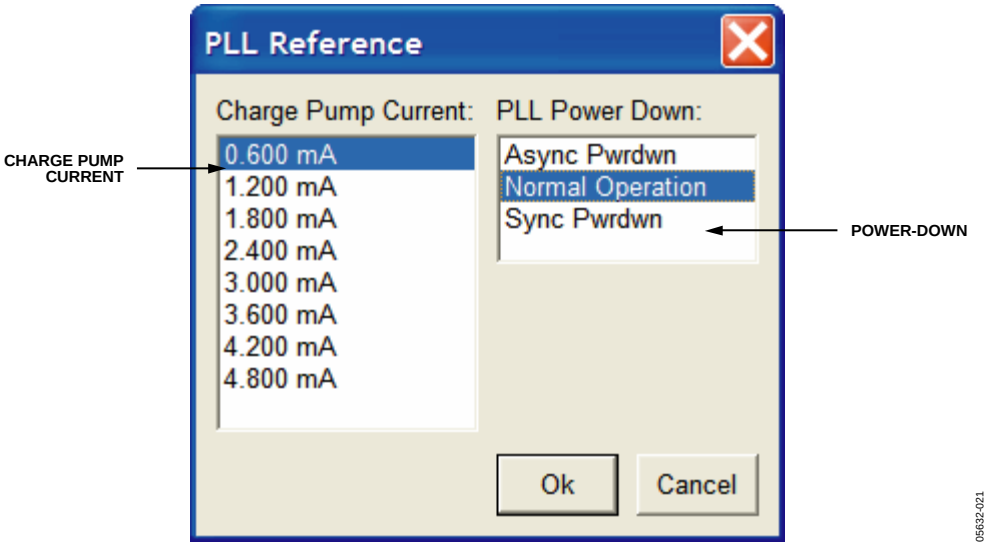

Figure 21. PLL Reference Window

PLL Settings Windows

The PLL settings window (Figure 22) allows you to select which signal is presented to the status pin. For more information on any of these outputs, please refer to the AD9510 data sheet.

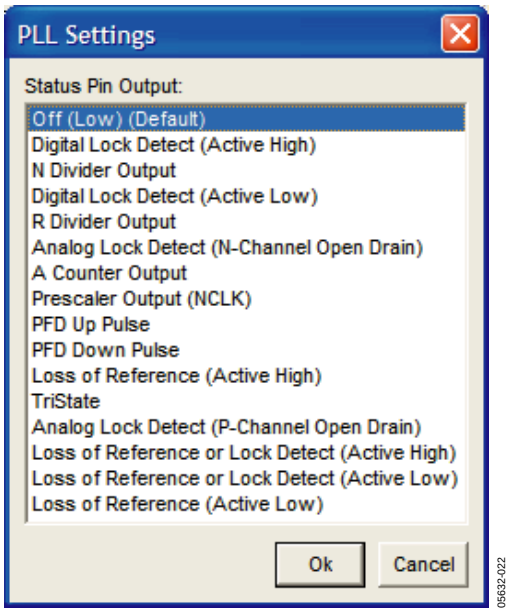

Figure 22. PLL Settings Window

Clock Inputs Section

Figure 23 shows the clock inputs section of the main interface window. It contains the settings for the three clock inputs: REFCLK, CLK1, and CLK2. These list boxes let you input the clock frequencies so that the PLL and output frequencies can be calculated automatically. The maximum input frequencies are 1500 MHz for CLK1 and CLK2, and 250 MHz for REFCLK. If the entered values exceed these amounts, the list box is outlined in red. If you try to continue, an error message is not given; however, all calculations based on the entered value are invalid.

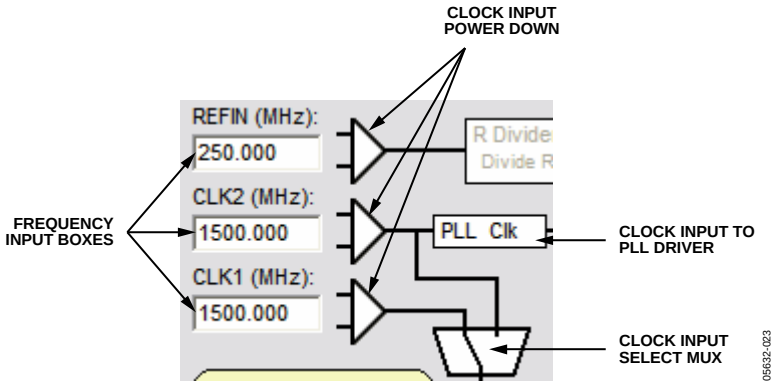

Figure 23. Clock Inputs, Main Interface Window

Additionally, left-clicking on any of the driver-signal graphics brings up the window shown in Figure 24. This clock input settings window allows for power down of each of the clock inputs as well as clock select for the distribution section. The clock select for the distribution section can also be changed by left-clicking on the mux symbol in the clock inputs section.

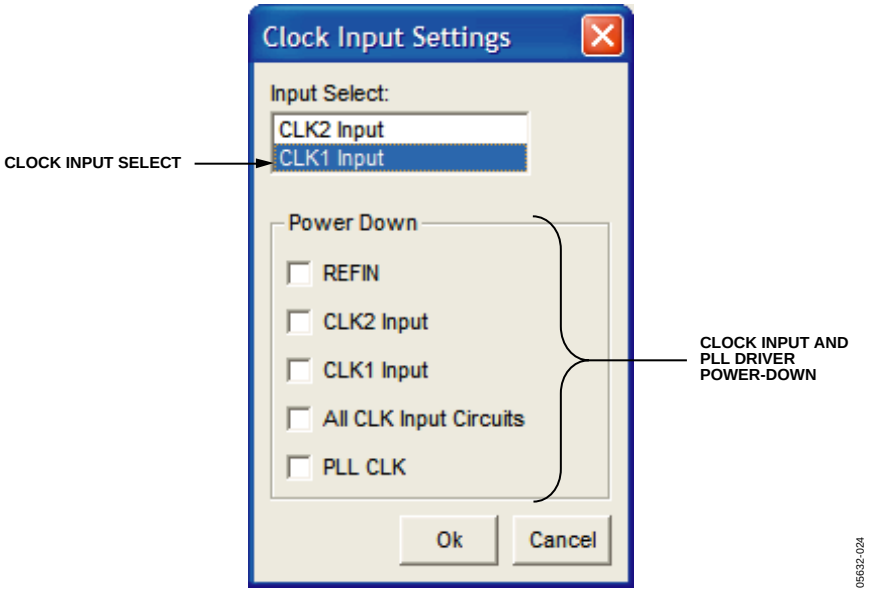

Figure 24. Clock Input Settings Window

Clock Distribution Section

The eight clock outputs are configured in the clock distribution section (Figure 25) of the main interface window. Here you can set each divider and phase settings, the fine delay control settings, the output level, and power down settings.

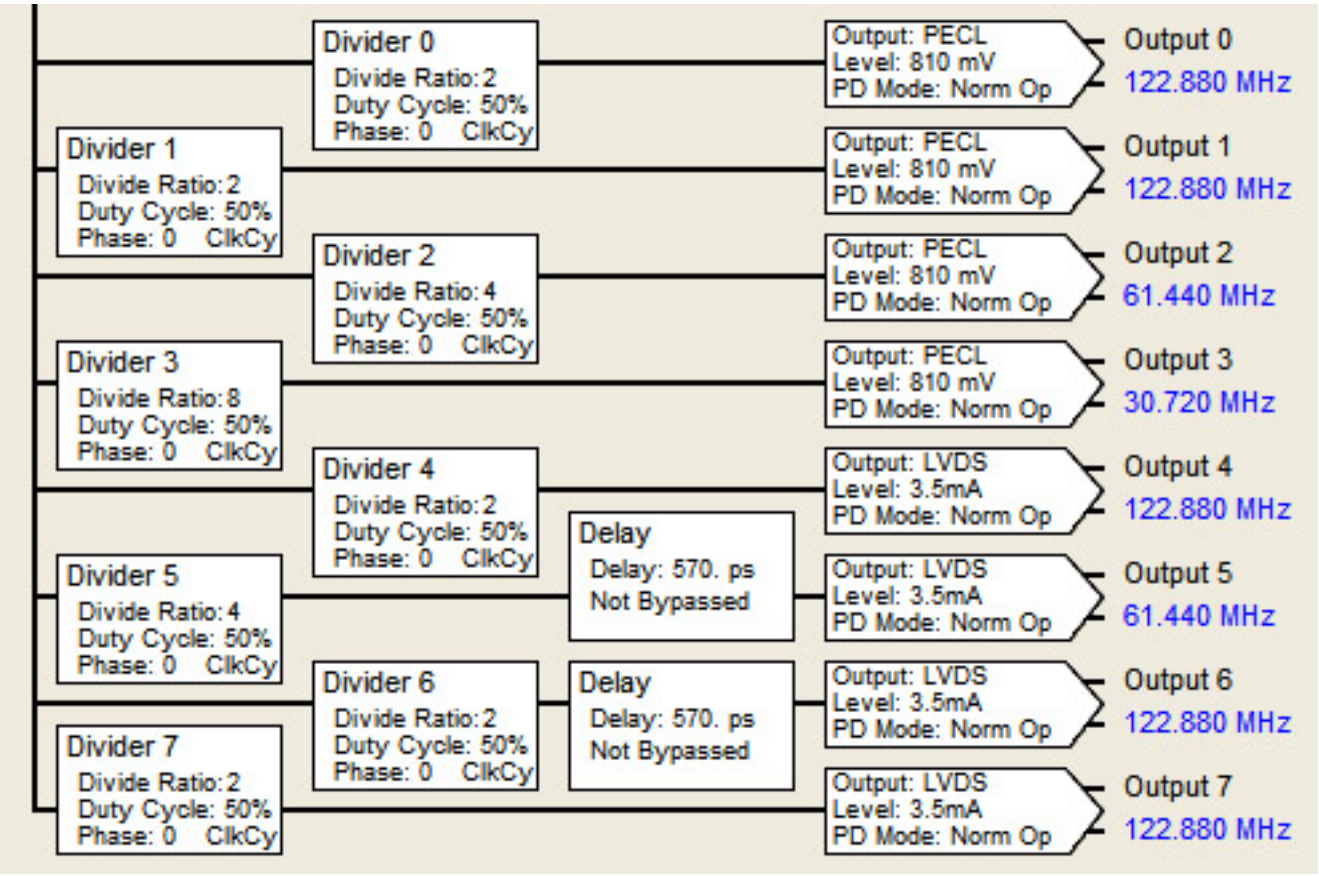

Figure 25. Clock Distribution Section, Main Interface Window

The output frequency of the eight outputs is calculated from the divider settings and the specified input clock frequency. It is then displayed on the right-hand side of the clock distribution section. If the calculated output frequency exceeds the rated driver frequency, the displayed frequency appears in red.

Divider, Phase, and Duty Cycle Settings Window

The divider, phase, and duty cycle settings window for each of the eight inputs is opened by left-clicking on the divider block for the appropriate input. The divider 2 settings window is displayed in Figure 26. The divider settings windows for outputs 1 to 7 are identical. The three major controls in the divider settings window are the divider, phase, and duty cycle settings.

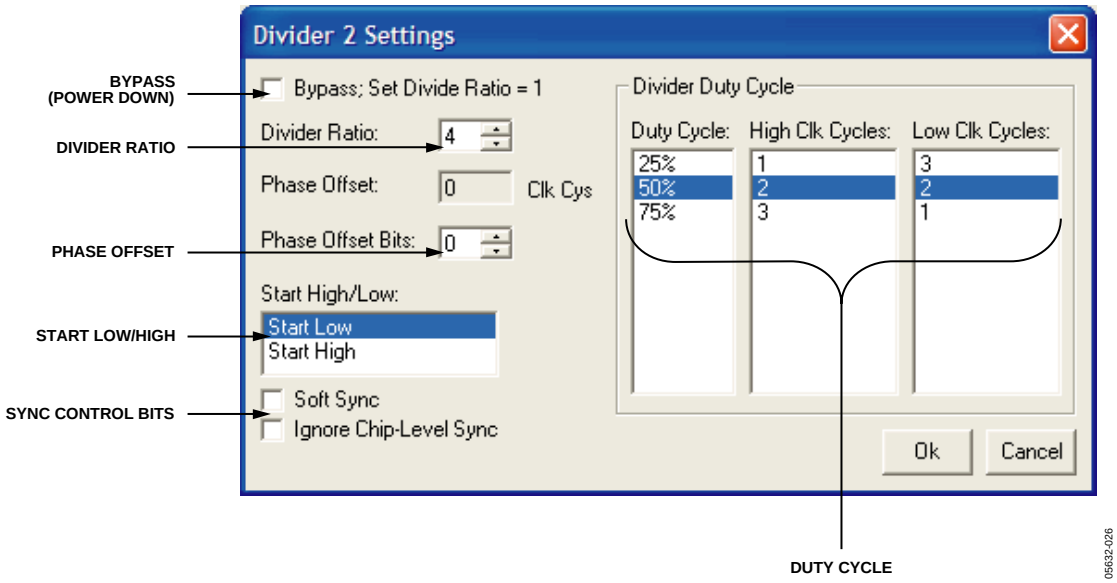

Figure 26. Divider 2 Settings Window

The divider ratio is the core of the divider block. This value specifies your output frequency. The formula is

$$f_{out} = f_{in}/M$$

where M is the divider ratio.

Next, a duty cycle needs to be determined. The duty cycle is specified by the ratio of high clock cycles to low clock cycles. High clock cycles are the number of master clock cycles that the output is high. Low clock cycles are the number of master clock cycles that the output is low. The evaluation software programs the correct number of cycles depending on the duty cycle chosen. When programming the part manually, remember that the number of high (or low) clock cycles is the value programmed plus one.

The phase offset allows you to shift the phase of the output signal by an integer number of master clock cycles. The maximum value of the phase offset is 15. Related to the phase-offset setting is the start high/low setting, which allows you to specify if the outputs start in a high state or a low state after a sync event. When coupled with the phase-offset setting, it allows for 32 phase-offset states. However, the number of unique phase-offset states is limited by the divide ratio, because the phase offset is controlled by the master clock frequency. In general, the number of unique phase offsets is equal to the divider ratio. The actual phase step, in degrees, is given by 360°/(divider ratio).

The bypass (power down) and miscellaneous control bits give you control over the sync and power down settings of the divider. When both sync bits are set, the output is frozen in a high or low state (the complimentary out is frozen in the opposite). The choice of high or low is dictated by the start high or start low setting. Please refer to the AD9510 data sheet for more information on soft sync and ignoring chip-level sync.

Output Settings Windows

The output settings windows (Figure 27) allow you to control the output driver level and complete channel power down. In addition, the LVDS/CMOS output settings window lets you select LVDS or CMOS, and activates the CMOS complimentary output driver.

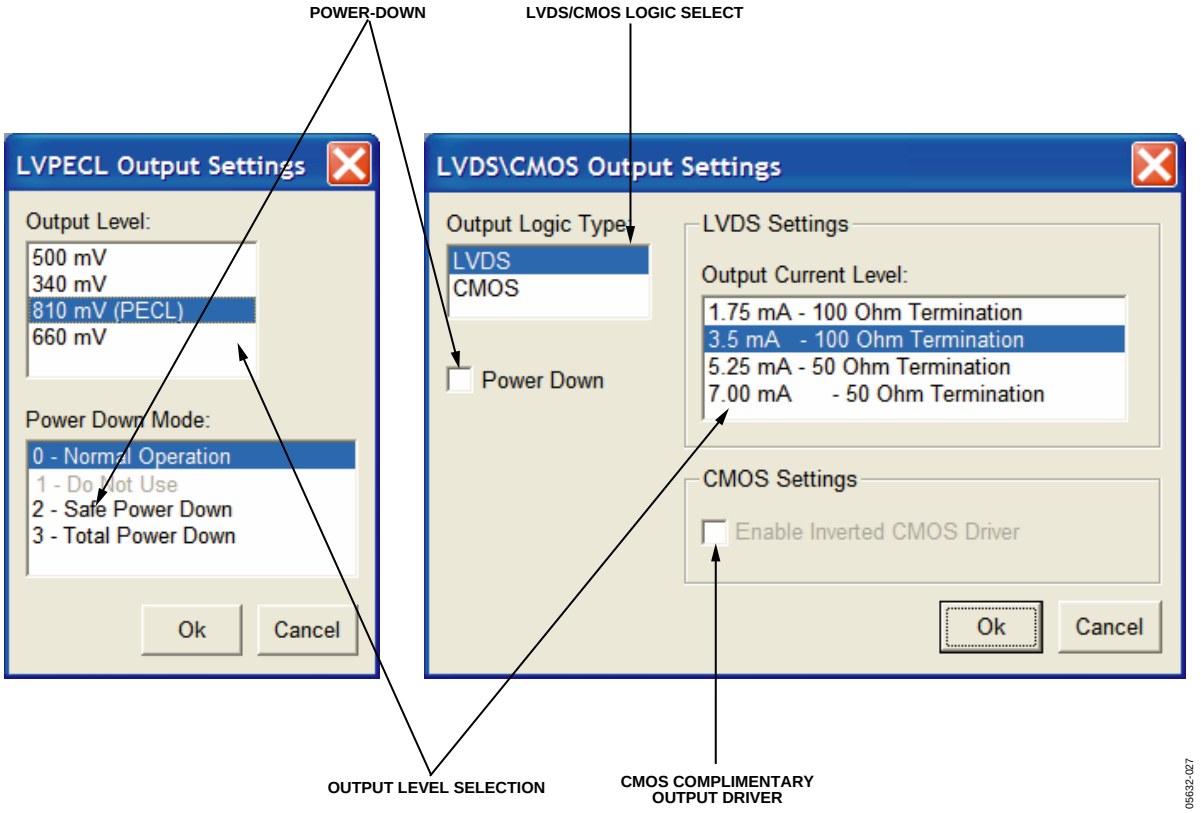

Figure 27. Output Settings Windows

Each of the drivers has four output levels. Additionally, the LVPECL has four different power down modes (one of them is normal operation). Finally, the LVDS has the logic select function and the CMOS complimentary driver enable. For more information on any of the output driver functions, please refer to the AD9510 data sheet.

Control Functions Section

The AD9510 has a number of sync and reset functions. These are controlled by the drop-down box, check boxes, and command buttons located on the lower left-hand side of the main interface window (see Figure 28).

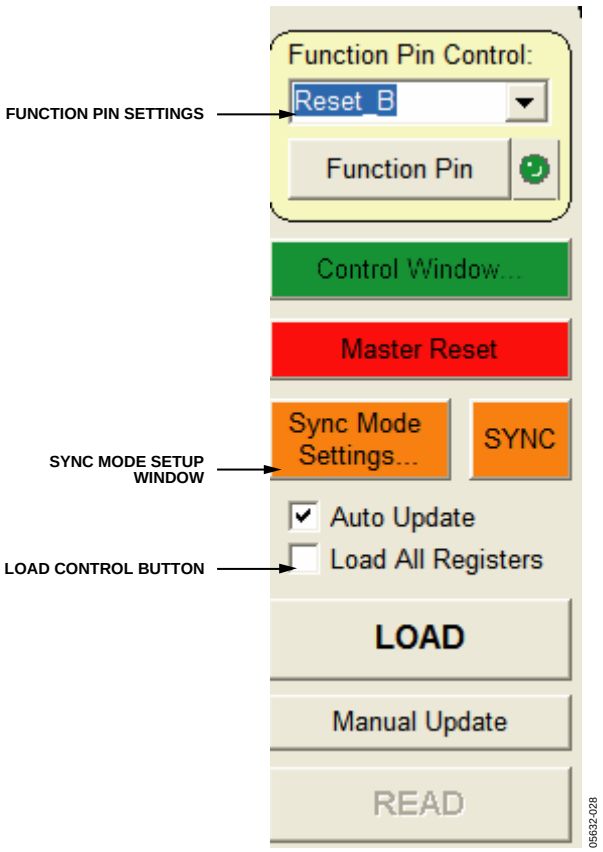

Figure 28. Control Functions Section, Main Interface Window

Function Pin Settings

The function pin can be set for three different functions. The three options are Reset_B, Sync_B, and Powerdown_B, which are accessible from the drop-down menu under Function Pin Control. They are activated by toggling the function pin button. The function pin command button sets the input to function pin high or low. If the light next to the command button is green, the function pin is high. If it is black, the function pin is low. For more information on these three functions, please refer to the AD9510 data sheet.

Control Check Window

The control window command button opens up the control check window (see Figure 29).This window is used to control miscellaneous power down and control bits that do not fit into any specific category. Currently, it only contains band gap power down.

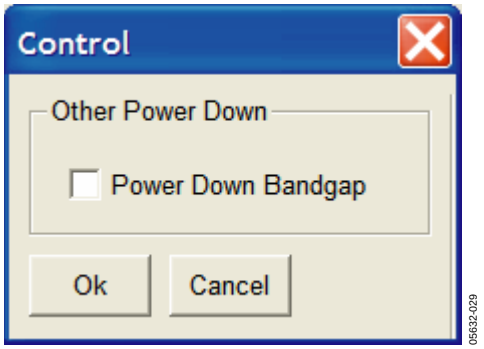

Figure 29. Control Check Window

Sync Mode Setup Window

The sync mode setup window (Figure 30) lets you control the various sync settings in the AD9510. There is an option for sync enable, interrupt timing, and soft sync. The soft sync check box is used to issue a software sync command. To issue this command, the soft sync bit must be set and then cleared. This requires two separate load commands, one to set the bit and one to clear the bit. While the bit is set, all of the outputs are frozen in a high or low state. The high or low state is determined by the start high or start low setting for each output, and the complimentary outputs are frozen opposite the true outputs. For each of these options, please refer to the AD9510 data sheet for more information.

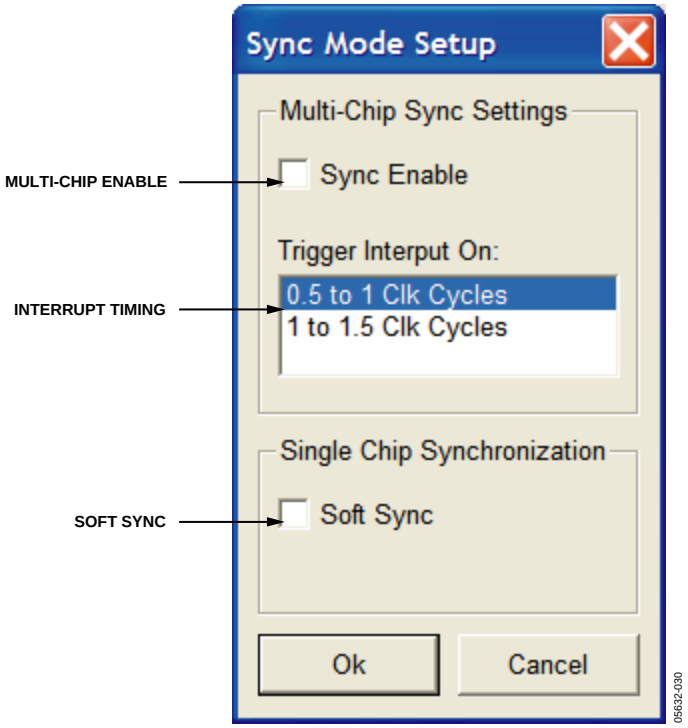

Figure 30. Sync Mode Setup Window

Master Reset and Load Control Command Buttons

There are several command buttons, diagramed in Figure 31, which are located in the lower left-hand corner of the main interface window. They serve several purposes:

- The large red command button is a master reset, which resets the AD9510 to its default power-up state. This is an asynchronous command that can be issued at any time. It automatically resets the part to the default power-up state and then reloads the interface blocks to reflect the reset values.
- The auto-update check box controls how the AD9510 is updated. When a new value is written to a given register, the AD9510 does not use the new information until an update command is given. When the auto-update check box is selected, this update command is automatically given when load is pressed.
- The load all registers check box lets you select whether to load only the changed registers or to load the entire register map. If the load all registers check box is cleared, then only the changed registers are loaded when load is pressed. Otherwise, all the registers are loaded. This can be useful if you want to set a part up exactly the way it was before a hardware reset occurred; for example, if a power supply was cutoff to the part.
- The remaining three buttons are self-explanatory. The load button loads the current settings into the part, the read button reads the current settings from the part, and the manual update button sends the update command to the part. If the auto-update check box is selected, the manual update button does not need to be pressed after a load command.

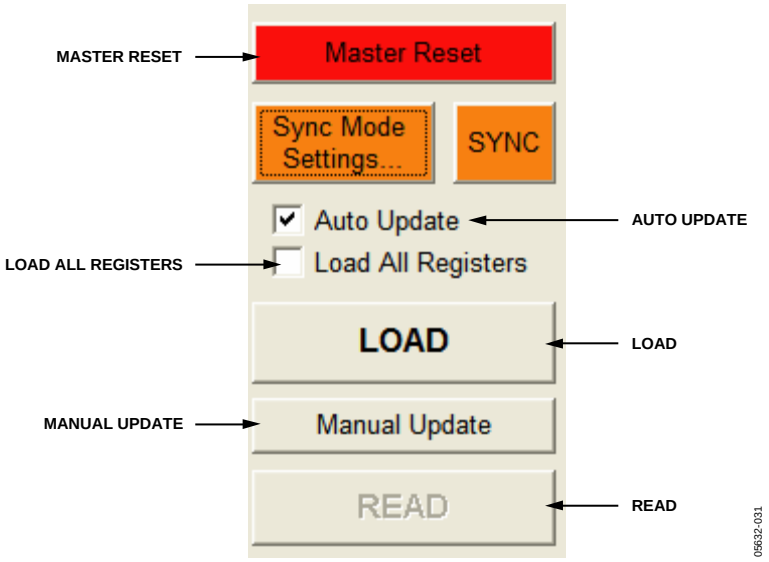

Figure 31. Master Reset and Control Buttons, Main Interface Window

SCHEMATIC

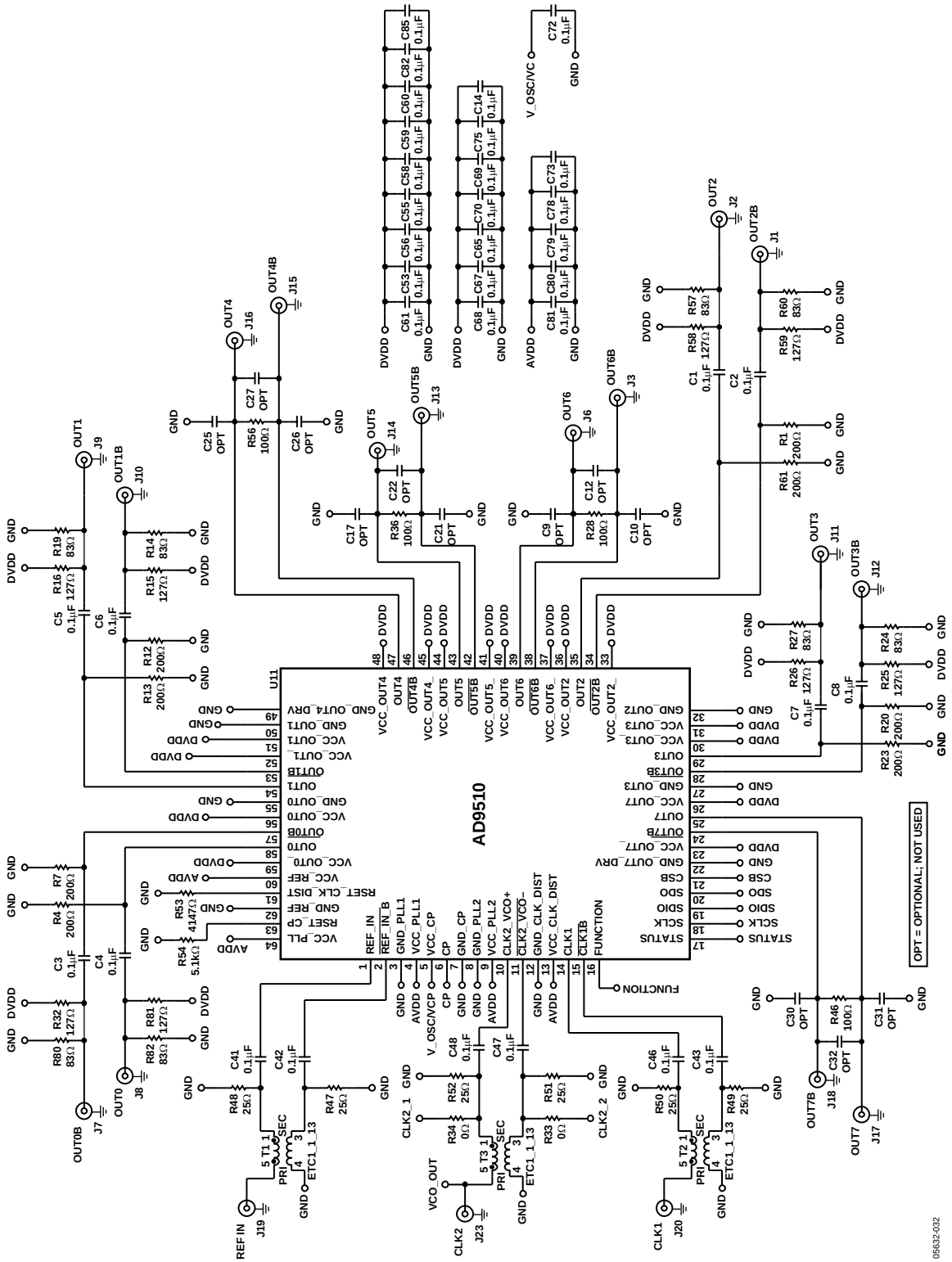

Figure 32. AD9510 Evaluation Board Schematic, Page 1

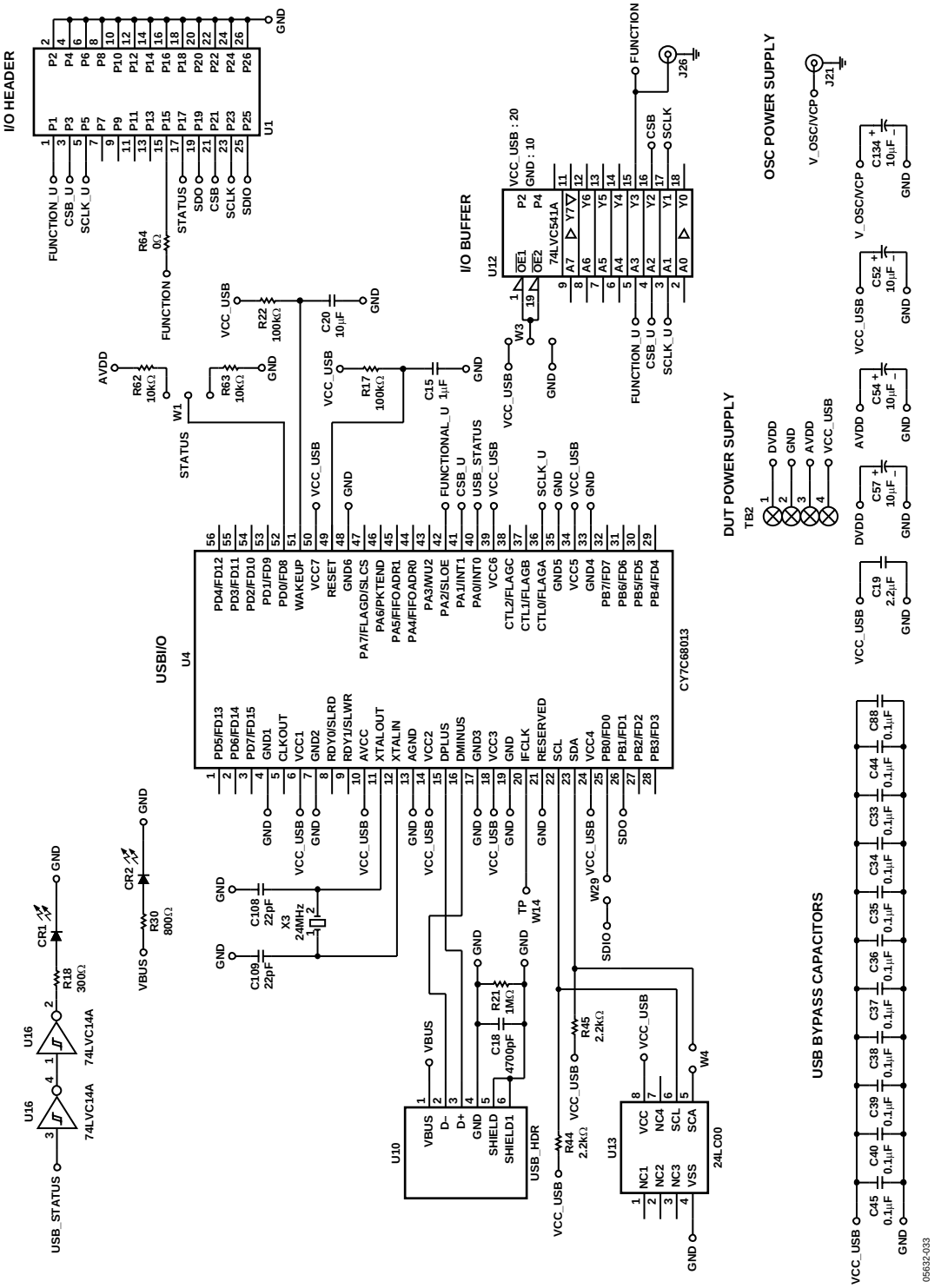

Figure 33. AD9510 Evaluation Board Schematic, Page 2

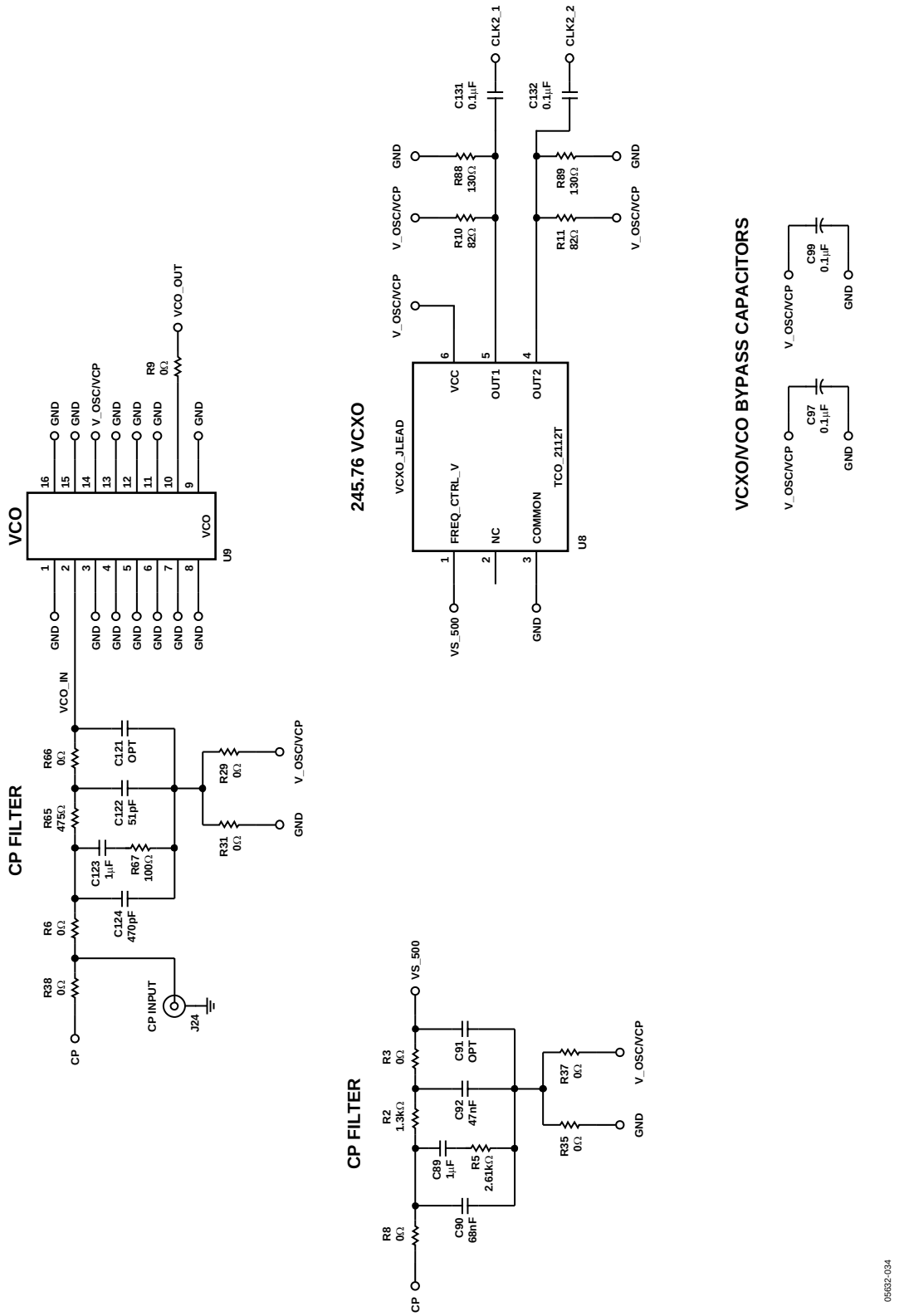

Figure 34. AD9510 Evaluation Board Schematic, Page 3

ORDERING INFORMATION

ORDERING GUIDE

Model	Description
AD9510/PCB	Evaluation Board without VCO, VCXO, or Loop Filter
AD9510-VCO/PCB	Evaluation Board with 245.76 MHz VCXO, and Loop Filter

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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