InnoSwitch3-EP Family

Off-Line CV/CC QR Flyback Switcher IC with Integrated Primary Switch, Synchronous Rectification and FluxLink Feedback

Product Highlights

Highly Integrated, Compact Footprint

- High efficiency across load range
- PowiGaN™ technology – up to 100 W without heat sinks
- Multi-mode Quasi-Resonant (QR) / CCM flyback controller, high-voltage switch, secondary-side sensing and synchronous rectification driver
- Excellent multi-output cross regulation with weighted secondary-side regulation (SSR) feedback and synchronous FETs
- Integrated FluxLink™, HIPOT-isolated, feedback link
- Exceptional CV/CC accuracy, independent of external components
- Adjustable accurate output current sense using external resistor

EcoSmart™ – Energy Efficient

- Less than 30 mW no-load including line sense
- Easily meets all global energy efficiency regulations

Advanced Protection / Safety Features

- Open SR FET-gate detection
- Fast input line UV/OV protection
- Auto-restart fault response for output OVP
- 725 V and 750 V switch for excellent surge withstand
- 900 V and 1700 V switch for industrial design or extra safety margin

Optional Features

- Output UV protection
- With auto-restart peak power delivery

Full Safety and Regulatory Compliance

- Reinforced isolation
- Isolation voltage >4000 VAC
- 100% production HIPOT tested
- UL1577 isolation voltage 4000 VAC (max), TUV (EN62368-1), CQC (GB4943.1) and DIN EN IEC 60747-17 (VDE 0884-17) safety approved. See Note 4
- Excellent noise immunity enables designs that achieve class "A" performance criteria for EN61000-4 suite; EN61000-4-2, 4-3 (30 V/m), 4-4, 4-5, 4-6, 4-8 (100 A/m) and 4-9 (1000 A/m)

Green Package

- Halogen free and RoHS compliant

Applications

- Auxiliary, standby and bias power supplies for appliances, computers and consumer products
- Utility meter, smart grid and industrial power supplies

Description

The InnoSwitch™3-EP family of ICs dramatically simplifies the design and manufacture of flyback power converters, particularly those requiring high efficiency and/or compact size. The InnoSwitch3-EP family combines primary and secondary controllers and safety-rated feedback into a single IC.

InnoSwitch3-EP family devices incorporate multiple protection features including line over and undervoltage protection, output overvoltage and over-current limiting, and over-temperature shutdown. Devices are available with standard and peak power delivery options, and commonly used auto-restart protection behaviors.

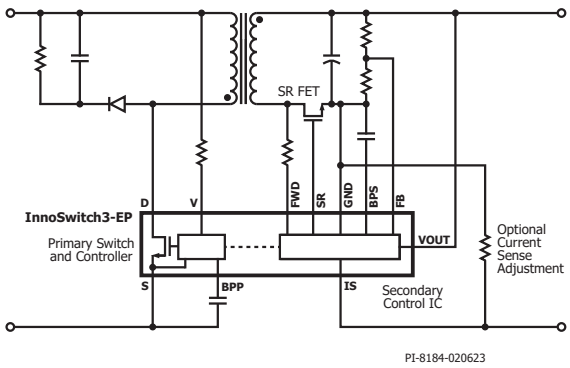


Figure 1. Typical Application Schematic.

Figure 2. High Creepage, Safety-Compliant InSOP-24D Package.

Output Power Table

Product[3]	Peak or Open Frame[1,2]	Peak or Open Frame[1,2]
725 V MOSFET	230 VAC ± 15%	85 – 265 VAC
INN3672C	12 W	10 W
INN3673C	15 W	12 W
INN3674C	25 W	20 W
INN3675C	30 W	25 W
INN3676C	40 W	36 W
INN3677C	45 W	40 W
750 V PowiGaN Switch	230 VAC ± 15%	85 – 265 VAC
INN3678C	75 W	65 W
INN3679C	85 W	75 W
INN3670C	100 W	85 W
900 V MOSFET	230 VAC ±15%	85 – 440 VAC
INN3692C	12 W	10 W
INN3694C	25 W	20 W
INN3696C	35 W	30 W
900 V PowiGaN Switch	230 VAC ±15%	85 – 400 VAC
INN3697C	55 W	50 W
INN3699C	85 W	75 W
INN3690C	100 W	85 W
1700 V Switch	85 – 670 VAC	200 – 1000 VDC
INN3647C	45 W	50 W
INN3649C	65 W	70 W

Table 1. Output Power Table.

Notes:

1. Minimum continuous power in a typical non-ventilated enclosed adapter measured at 40 °C ambient. Max output power is dependent on the design. With condition that package temperature must be < 125 °C.
2. Minimum peak power capability.
3. Package: InSOP-24D.
4. UL1577, TUV, CQC and DIN EN IEC 60747-17 are pending for INN369xC devices. While DIN IEC 60747-17 is pending for INN364xC devices.

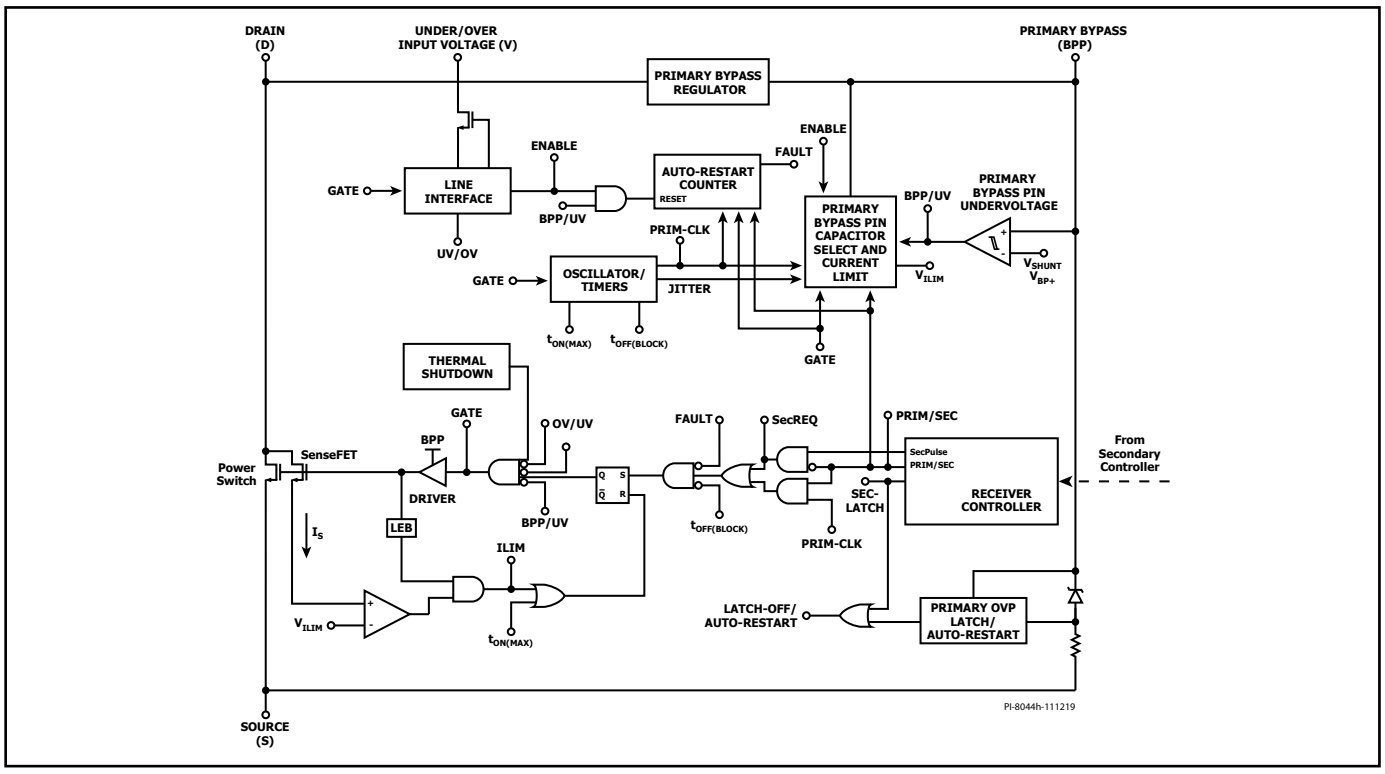


Figure 3. Primary Controller Block Diagram.

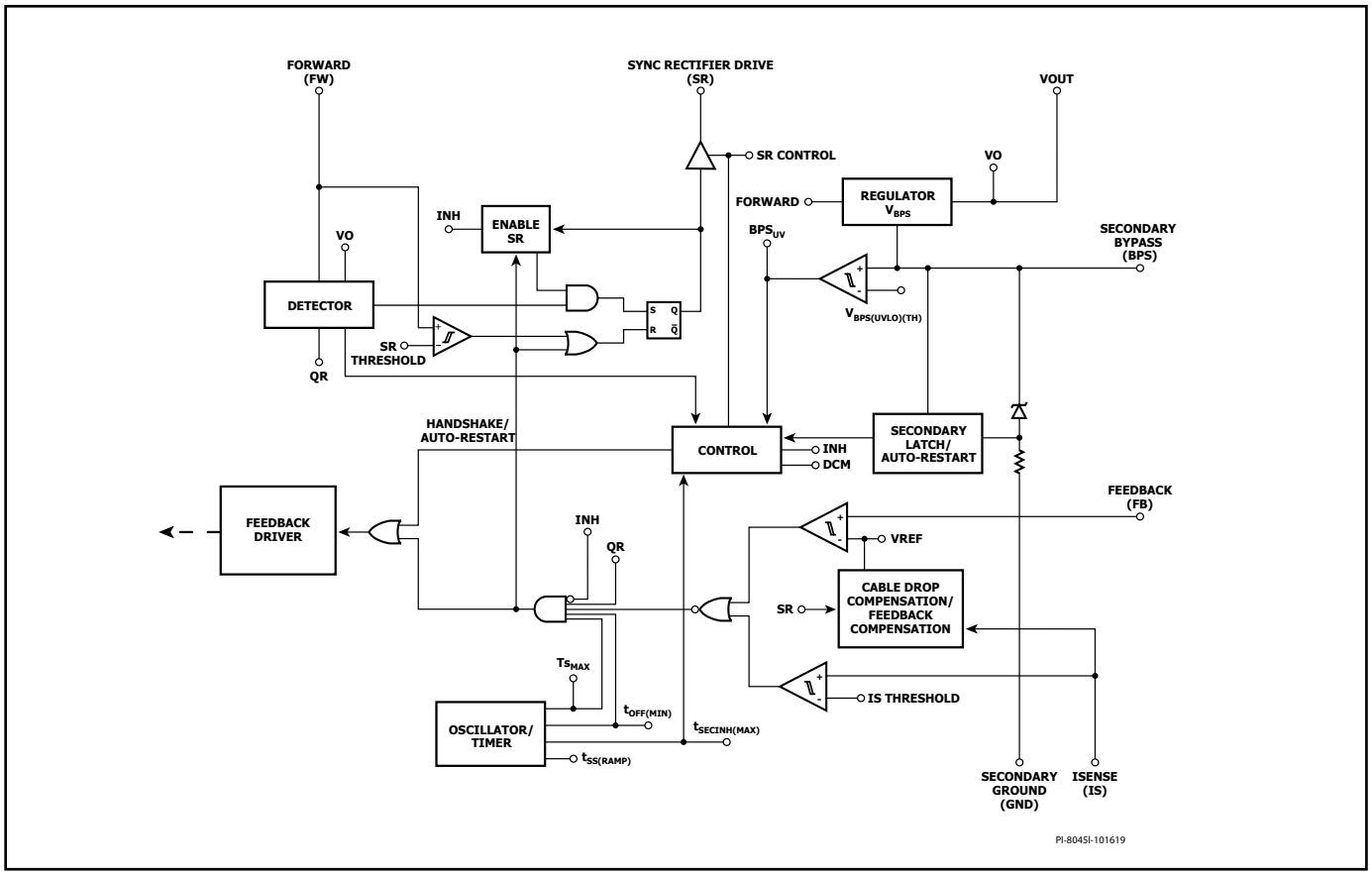


Figure 4. Secondary Controller Block Diagram.

Pin Functional Description

ISENSE (IS) Pin (Pin 1)
Connection to the power supply output terminals. An external current sense resistor should be connected between this and the GND pin. If current regulation/accurate over-current protection is not required, this pin should be tied to the GND pin.

SECONDARY GROUND (GND) (Pin 2)
GND for the secondary IC. Note this is not the power supply output GND due to the presence of the sense resistor between this and the ISENSE pin.

FEEDBACK (FB) Pin (Pin 3)
Connection to an external resistor divider to set the power supply output voltage.

SECONDARY BYPASS (BPS) Pin (Pin 4)
Connection point for an external bypass capacitor for the secondary IC supply.

SYNCHRONOUS RECTIFIER DRIVE (SR) Pin (Pin 5)
Gate driver for external SR FET. If no SR FET is used connect this pin to GND.

OUTPUT VOLTAGE (VOUT) Pin (Pin 6)
Connected directly to the output voltage, to provide current for the controller on the secondary-side and provide secondary protection.

FORWARD (FWD) Pin (Pin 7)
The connection point to the switching node of the transformer output winding providing information on primary switch timing. Provides power for the secondary-side controller when V_{OUT} is below threshold.

NC Pin (Pin 8-12)
Leave open. Should not be connected to any other pins.

UNDER/OVER INPUT VOLTAGE (V) Pin (Pin 13)
A high-voltage pin connected to the AC or DC side of the input bridge for detecting undervoltage and overvoltage conditions at the power supply input. This pin should be tied to SOURCE pin to disable UV/OV protection.

PRIMARY BYPASS (BPP) Pin (Pin 14)
The connection point for an external bypass capacitor for the primary-side supply. This is also the ILIM selection pin for choosing standard ILIM or ILIM+1.

NC Pin (Pin 15)
Leave open or connect to SOURCE pin or BPP pin.

SOURCE (S) Pin (Pin 16-19)
These pins are the power switch source connection. Also ground reference for primary BYPASS pin.

DRAIN (D) Pin (Pin 24)
Power switch drain connection.

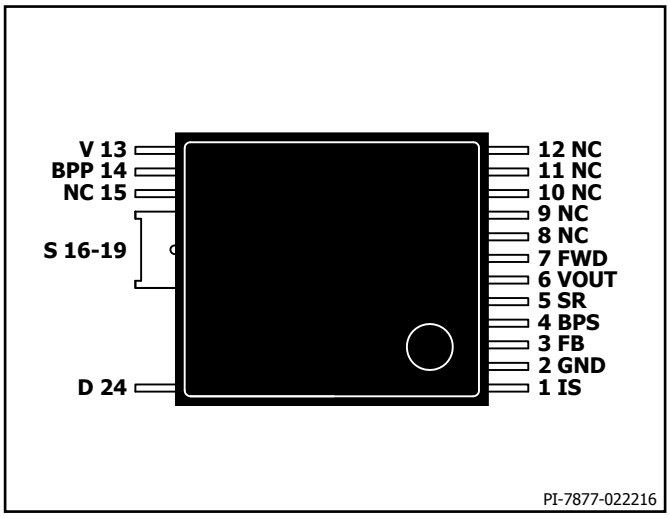


Figure 5. Pin Configuration.

InnoSwitch3-EP Functional Description

The InnoSwitch3-EP combines a high-voltage power switch, along with both primary-side and secondary-side controllers in one device.

The architecture incorporates a novel inductive coupling feedback scheme (FluxLink) using the package lead frame and bond wires to provide a safe, reliable, and cost-effective means to transmit accurate, output voltage and current information from the secondary controller to the primary controller.

The primary controller on InnoSwitch3-EP is a Quasi-Resonant (QR) flyback controller that has the ability to operate in continuous conduction mode (CCM), boundary mode (CrM) and discontinuous conduction mode (DCM). The controller uses both variable frequency and variable current control schemes. The primary controller consists of a frequency jitter oscillator, a receiver circuit magnetically coupled to the secondary controller, a current limit controller, 5 V regulator on the PRIMARY BYPASS pin, audible noise reduction engine for light load operation, bypass overvoltage detection circuit, a lossless input line sensing circuit, current limit selection circuitry, over-temperature protection, leading edge blanking, secondary output diode / SR FET short protection circuit and a power switch.

The InnoSwitch3-EP secondary controller consists of a transmitter circuit that is magnetically coupled to the primary receiver, a constant voltage (CV) and a constant current (CC) control circuit, a 4.4 V regulator on the SECONDARY BYPASS pin, synchronous rectifier FET driver, QR mode circuit, oscillator and timing circuit, and numerous integrated protection features.

Figure 3 and Figure 4 show the functional block diagrams of the primary and secondary controller, highlighting the most important features.

Primary Controller

InnoSwitch3-EP has variable frequency QR controller plus CCM/CrM/DCM operation for enhanced efficiency and extended output power capability.

PRIMARY BYPASS Pin Regulator

The PRIMARY BYPASS pin has an internal regulator that charges the PRIMARY BYPASS pin capacitor to V_{BPP} by drawing current from the DRAIN pin whenever the power switch is off. The PRIMARY BYPASS pin is the internal supply voltage node. When the power switch is on, the device operates from the energy stored in the PRIMARY BYPASS pin capacitor.

In addition, a shunt regulator clamps the PRIMARY BYPASS pin voltage to V_{SHUNT} when current is provided to the PRIMARY BYPASS pin through an external resistor. This allows the InnoSwitch3-EP to be powered externally through a bias winding, decreasing the no-load consumption to less than 30 mW in a 5 V output design.

Primary Bypass ILIM Programming

InnoSwitch3-EP ICs allows the user to adjust current limit (ILIM) settings through the selection of the PRIMARY BYPASS pin capacitor value. A ceramic capacitor can be used.

There are 2 selectable capacitor sizes - 0.47 µF and 4.7 µF for setting standard and increased ILIM settings respectively.

Primary Bypass Undervoltage Threshold

The PRIMARY BYPASS pin undervoltage circuitry disables the power switch when the PRIMARY BYPASS pin voltage drops below ~4.5 V (V_{BPP} - $V_{BP(H)}$) in steady-state operation. Once the PRIMARY BYPASS pin voltage falls below this threshold, it must rise to V_{SHUNT} to re-enable turn-on of the power switch.

Primary Bypass Output Overvoltage Function

The PRIMARY BYPASS pin has a latching/auto-restart OV protection feature depending on H Code. A Zener diode in parallel with the resistor in series with the PRIMARY BYPASS pin capacitor is typically used to detect an overvoltage on the primary bias winding and activate the protection mechanism. In the event that the current into the PRIMARY BYPASS pin exceeds ISD, the device will latch-off or disable the power switch switching for a time $t_{AR(OFF)}$, after which time the controller will restart and attempt to return to regulation (see Secondary Fault Response in the Feature Code Addendum).

VOUT OV protection is also included as an integrated feature on the secondary controller (see Output Voltage Protection).

Over-Temperature Protection

The thermal shutdown circuitry senses the primary Switch die temperature. The threshold is set to T_{SD} with either a hysteretic or latch-off response depending on H Code.

Hysteretic response: If the die temperature rises above the threshold, the power switch is disabled and remains disabled until the die temperature falls by $T_{SD(H)}$ at which point switching is re-enabled. A large amount of hysteresis is provided to prevent over-heating of the PCB due to a continuous fault condition.

Latch-off response: If the die temperature rises above the threshold the power switch is disabled. The latching condition is reset by bringing the PRIMARY BYPASS pin below $V_{BPP(RESET)}$ or by going below the UNDER/OVER INPUT VOLTAGE pin UV (I_{UV-}) threshold.

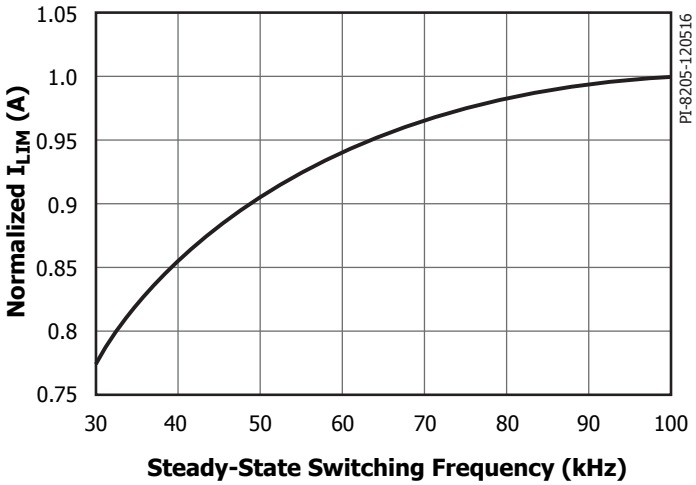


Figure 6. Normalized Primary Current vs. Frequency.

Current Limit Operation

The primary-side controller has a current limit threshold ramp that is linearly decreasing to the time from the end of the previous primary switching cycle (i.e. from the time the primary Switch turns off at the end of a switching cycle).

This characteristic produces a primary current limit that increases as the switching frequency (load) increases (Figure 6).

This algorithm enables the most efficient use of the primary switch with the benefit that this algorithm responds to digital feedback information immediately when a feedback switching cycle request is received.

At high load, switching cycles have a maximum current approaching 100% I_{LIM}. This gradually reduces to 30% of the full current limit as load decreases. Once 30% current limit is reached, there is no further reduction in current limit (since this is low enough to avoid audible noise). The time between switching cycles will continue to increase as load reduces.

Jitter

The normalized current limit is modulated between 100% and 95% at a modulation frequency of f_M. This results in a frequency jitter of ~7 kHz with average frequency of ~100 kHz.

Auto-Restart

In the event a fault condition occurs (such as an output overload, output short-circuit, or external component/pin fault), the InnoSwitch3-EP enters auto-restart (AR) or latches off. The latching condition is reset by bringing the PRIMARY BYPASS pin below ~3 V or by going below the UNDER/OVER INPUT VOLTAGE pin UV (I_{UV-}) threshold.

In auto-restart, switching of the power switch is disabled for $t_{AR(OFF)}$. There are 2 ways to enter auto-restart:

1. Continuous secondary requests at above the overload detection frequency f_{OVL} (~110 kHz) for longer than 82 ms (t_{AR}).
2. No requests for switching cycles from the secondary for $>t_{AR(SK)}$.

The second is included to ensure that if communication is lost, the primary tries to restart. Although this should never be the case in normal operation, it can be useful when system ESD events (for example) causes a loss of communication due to noise disturbing the secondary controller. The issue is resolved when the primary restarts after an auto-restart off-time.

The auto-restart is reset as soon as an AC reset occurs.

SOA Protection

In the event that there are two consecutive cycles where the 110% I_{LIM} is reached within ~500 ns (the blanking time + current limit delay time) (including leading edge current spike), the controller will skip 2.5 cycles or ~25 µs (based on full frequency of 100 kHz). This provides sufficient time for the transformer to reset with large capacitive loads without extending the start-up time.

Secondary Rectifier/SR Switch Short Protection (SRS)

In the event that the output diode or SR FET is short-circuited before or during the primary conduction cycle, the drain current (prior to the end of the leading edge blanking time) can be much higher than the maximum current limit threshold. If the controller turns the high-voltage power switch off, the resulting peak drain voltage could exceed the rated BV_{DSS} of the device, resulting in catastrophic failure even with minimum on-time.

To address this issue, the controller features a circuit that reacts when the drain current exceeds the maximum current limit threshold prior to the end of leading-edge blanking time. If the leading-edge current exceeds current limit within a cycle (200 ns), the primary controller will trigger a 30 µs off-time event. SOA mode is triggered if there are two consecutive cycles above current limit within t_{LES} (~500 ns). SRS mode also triggers $t_{AR(OFF)SH}$ off-time, if the current limit is reached within 200 ns after a 30 µs off-time.

SRS protection is not available on PowiGaN devices INN3678C, INN3679C and INN3670C.

Input Line Voltage Monitoring

The UNDER/OVER INPUT VOLTAGE pin is used for input undervoltage and overvoltage sensing and protection.

A sense resistor is tied between the high-voltage DC bulk capacitor after the bridge (or to the AC side of the bridge rectifier for fast AC reset) and the UNDER/OVER INPUT VOLTAGE pin to enable this functionality. This function can be disabled by shorting the UNDER/OVER INPUT VOLTAGE pin to SOURCE pin.

At power-up, after the primary bypass capacitor is charged and the ILIM state is latched, and prior to switching, the state of the UNDER/OVER INPUT VOLTAGE pin is checked to confirm that it is above the brown-in and below the overvoltage shutdown thresholds.

In normal operation, if the UNDER/OVER INPUT VOLTAGE pin current falls below the brown-out threshold and remains below brown-out for longer than t_{UV-}, the controller enters auto-restart. Switching will only resume once the UNDER/OVER INPUT VOLTAGE pin current is above the brown-in threshold.

In the event that the UNDER/OVER INPUT VOLTAGE pin current is above the overvoltage threshold, the controller will also enter auto-restart. Again, switching will only resume once the UNDER/OVER INPUT VOLTAGE pin current has returned to within its normal operating range.

The input line UV/OV function makes use of an internal high-voltage Switch on the UNDER/OVER INPUT VOLTAGE pin to reduce power consumption. If the cycle off-time t_{OFF} is greater than 50 µs, the internal high-voltage Switch will disconnect the external sense resistor from the internal IC to eliminate current drawn through the sense resistor. The line sensing function will activate again at the beginning of the next switching cycle.

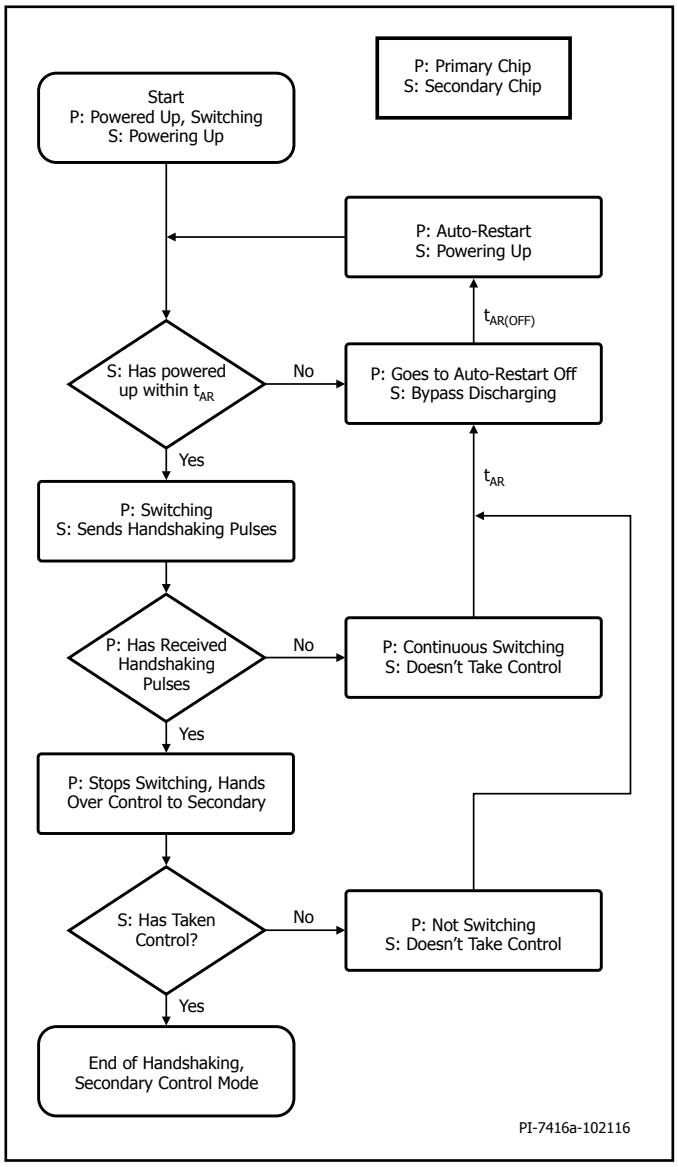


Figure 7. Primary-Secondary Handshake Flowchart.

Primary-Secondary Handshake

At start-up, the primary-side initially switches without any feedback information (this is very similar to the operation of a standard TOPSwitch™, TinySwitch™ or LinkSwitch™ controllers).

If no feedback signals are received during the auto-restart on-time (t_{AR}), the primary goes into auto-restart mode. Under normal conditions, the secondary controller will power-up via the FORWARD pin or from the OUTPUT VOLTAGE pin and take over control. From this point onwards the secondary controls switching.

If the primary controller stops switching or does not respond to cycle requests from the secondary during normal operation (when the secondary has control), the handshake protocol is initiated to ensure that the secondary is ready to assume control once the primary begins to switch again. An additional handshake is also triggered if the secondary detects that the primary is providing more cycles than were requested.

The most likely event that could require an additional handshake is when the primary stops switching as the result of a momentary line brown-out event. When the primary resumes operation, it will default to a start-up condition and attempt to detect handshake pulses from the secondary.

If the secondary does not detect that the primary responds to switching requests for 8 consecutive cycles, or if the secondary detects that the primary is switching without cycle requests for 4 or more consecutive cycles, the secondary controller will initiate a second handshake sequence. This provides additional protection against cross-conduction of the SR FET while the primary is switching. This protection mode also prevents an output overvoltage condition in the event that the primary is reset while the secondary is still in control.

Wait and Listen
When the primary resumes switching after initial power-up recovery from an input line voltage fault (UV or OV) or an auto-restart event, it will assume control and require a successful handshake to relinquish control to the secondary controller.

As an additional safety measure the primary will pause for an auto-restart on-time period, t_{AR} (~82 ms), before switching. During this "wait" time, the primary will "listen" for secondary requests. If it sees two consecutive secondary requests, separated by ~30 µs, the primary will infer secondary control and begin switching in slave mode. If no pulses occurs during the t_{AR} "wait" period, the primary will begin switching under primary control until handshake pulses are received.

Audible Noise Reduction Engine
The InnoSwitch3-EP features an active audible noise reduction mode whereby the controller (via a "frequency skipping" mode of operation) avoids the resonant band (where the mechanical structure of the power supply is most likely to resonate – increasing noise amplitude) between 5 kHz and 12 kHz - 200 µs and 83 µs period respectively. If a secondary controller switch request occurs within this time window from the last conduction cycle, the gate drive to the power switch is inhibited.

Secondary Controller

As shown in the block diagram in Figure 4, the IC is powered by a 4.4 V (V_{BPS}) regulator which is supplied by either VOUT or FWD. The SECONDARY BYPASS pin is connected to an external decoupling capacitor and fed internally from the regulator block.

The FORWARD pin also connects to the negative edge detection block used for both handshaking and timing to turn on the SR FET connected to the SYNCHRONOUS RECTIFIER DRIVE pin. The FORWARD pin voltage is used to determine when to turn off the SR FET in discontinuous conduction mode operation. This is when the voltage across the $R_{DS(ON)}$ of the SR FET drops below zero volts.

In continuous conduction mode (CCM) the SR FET is turned off when the feedback pulse is sent to the primary to demand the next switching cycle, providing excellent synchronous operation, free of any overlap for the FET turn-off.

The mid-point of an external resistor divider network between the OUTPUT VOLTAGE and SECONDARY GROUND pins is tied to the FEEDBACK pin to regulate the output voltage. The internal voltage comparator reference voltage is V_{FB} (1.265 V).

The external current sense resistor connected between ISENSE and SECONDARY GROUND pins is used to regulate the output current in constant current regulation mode.

Minimum Off-Time
The secondary controller initiates a cycle request using the inductive-connection to the primary. The maximum frequency of secondary-cycle requests is limited by a minimum cycle off-time of $t_{OFF(MIN)}$. This is in order to ensure that there is sufficient reset time after primary conduction to deliver energy to the load.

Maximum Switching Frequency
The maximum switch-request frequency of the secondary controller is f_{SREQ}.

Frequency Soft-Start
At start-up the primary controller is limited to a maximum switching frequency of f_{SW} and 75% of the maximum programmed current limit at the switch-request frequency of 100 kHz.

The secondary controller temporarily inhibits the FEEDBACK short protection threshold ($V_{FB(OFF)}$) until the end of the soft-start ($t_{SS(RAMP)}$) time. After hand-shake is completed the secondary controller linearly ramps up the switching frequency from f_{SW} to f_{SREQ} over the $t_{SS(RAMP)}$ time period.

In the event of a short-circuit or overload at start-up, the device will move directly into CC (constant-current) mode. The device will go into auto-restart (AR), if the output voltage does not rise above the $V_{FB(AR)}$ threshold before the expiration of the soft-start timer ($t_{SS(RAMP)}$) after handshake has occurred.

The secondary controller enables the FEEDBACK pin-short protection mode ($V_{FB(OFF)}$) at the end of the $t_{SS(RAMP)}$ time period. If the output short maintains the FEEDBACK pin below the short-circuit threshold, the secondary will stop requesting pulses triggering an auto-restart cycle.

If the output voltage reaches regulation within the $t_{SS(RAMP)}$ time period, the frequency ramp is immediately aborted and the secondary controller is permitted to go full frequency. This will allow the controller to maintain regulation in the event of a sudden transient loading soon after regulation is achieved. The frequency ramp will only be aborted if quasi-resonant-detection programming has already occurred.

Maximum Secondary Inhibit Period
Secondary requests to initiate primary switching are inhibited to maintain operation below maximum frequency and ensure minimum off-time. Besides these constraints, secondary-cycle requests are also inhibited during the "ON" time cycle of the primary switch (time between the cycle request and detection of FORWARD pin falling edge). The maximum time-out in the event that a FORWARD pin falling edge is not detected after a cycle requested is ~30 µs.

Output Voltage Protection
In the event that the sensed voltage on the FEEDBACK pin is 2% higher than the regulation threshold, a bleed current of ~2.5 mA (3 mA max) is applied on the OUTPUT VOLTAGE pin (weak bleed). This bleed current increases to ~200 mA (strong bleed) in the event that the FEEDBACK pin voltage is raised beyond ~10% of the internal FEEDBACK pin reference voltage. The current sink on the OUTPUT VOLTAGE pin is intended to discharge the output voltage after momentary overshoot events. The secondary does not relinquish control to the primary during this mode of operation.

If the voltage on the FEEDBACK pin is sensed to be 20% higher than the regulation threshold, a command is sent to the primary to either latch-off or begin an auto-restart sequence (see Secondary Fault Response in Feature Code Addendum). This integrated V_{OUT} OVP can be used independently from the primary sensed OVP or in conjunction.

FEEDBACK Pin Short Detection

If the sensed FEEDBACK pin voltage is below $V_{FB(OFF)}$ at start-up, the secondary controller will complete the handshake to take control of the primary complete $t_{SS(RAMP)}$ and will stop requesting cycles to initiate auto-restart (no cycle requests made to primary for longer than $t_{AR(SK)}$ second triggers auto-restart).

During normal operation, the secondary will stop requesting pulses from the primary to initiate an auto-restart cycle when the FEEDBACK pin voltage falls below the $V_{FB(OFF)}$ threshold. The deglitch filter on the protection mode is on for less than ~10 µs. By this mechanism, the secondary will relinquish control after detecting that the FEEDBACK pin is shorted to ground.

Auto-Restart Thresholds

The FEEDBACK pin includes a comparator to detect when the feedback voltage falls below $V_{FB(AR)}$, for a duration exceeding $t_{FB(AR)}$. The secondary controller will relinquish control when this fault condition is detected. This threshold is meant to limit the range of constant current (CC) operation and is included to support high power charger applications.

SECONDARY BYPASS Pin Overvoltage Protection

The InnoSwitch3-EP secondary controller features a SECONDARY BYPASS pin OV feature similar to the PRIMARY BYPASS pin OV feature. When the secondary is in control, in the event that the SECONDARY BYPASS pin current exceeds $I_{BPS(SD)}$ (~7 mA) the secondary will send a command to the primary to initiate an auto-restart off-time ($t_{AR(OFF)}$).

Output Constant Current Regulation/Output Over-Current Protection

The InnoSwitch3-EP regulates the output current through an external current sense resistor between the ISENSE and SECONDARY GROUND pins and also controls output power in conjunction with the output voltage sensed on the OUTPUT VOLTAGE pin. If constant current regulation/accurate over-current protection is not required, the ISENSE pin must be tied to the SECONDARY GROUND pin. Also see 'Peak Power Delivery' section.

SR Disable Protection

In each cycle SR is only engaged if a set cycle was requested by the secondary controller and the negative edge is detected on the FORWARD pin. In the event that the voltage on the ISENSE pin exceeds approximately 3 times the CC threshold, the SR FET drive is disabled until the surge current has diminished to nominal levels.

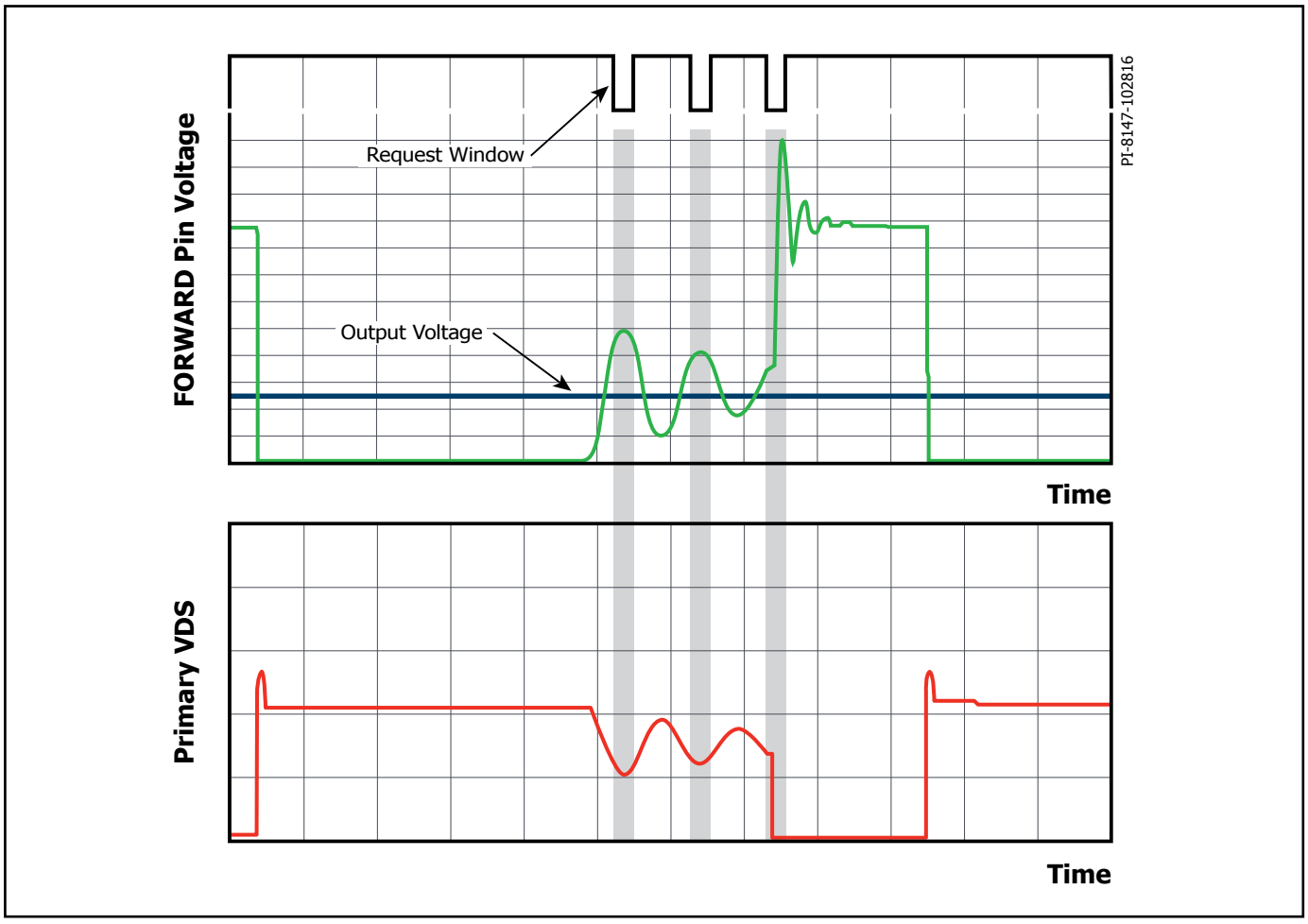


Figure 8. Intelligent Quasi-Resonant Mode Switching.

SR Static Pull-Down
To ensure that the SR gate is held low when the secondary is not in control, the SYNCHRONOUS RECTIFIER DRIVE pin has a nominally "ON" device to pull the pin low and reduce any voltage on the SR gate due to capacitive coupling from the FORWARD pin.

Open SR Protection
In order to protect against an open SYNCHRONOUS RECTIFIER DRIVE pin system fault the secondary controller has a protection mode to ensure the SYNCHRONOUS RECTIFIER DRIVE pin is connected to an external FET. If the external capacitance on the SYNCHRONOUS RECTIFIER DRIVE pin is below 100 pF, the device will assume the SYNCHRONOUS RECTIFIER DRIVE pin is "open" and there is no FET to drive. If the pin capacitance detected is above 100 pF, the controller will assume an SR FET is connected.

In the event the SYNCHRONOUS RECTIFIER DRIVE pin is detected to be open, the secondary controller will stop requesting pulses from the primary to initiate auto-restart.

If the SYNCHRONOUS RECTIFIER DRIVE pin is tied to ground at start-up, the SR drive function is disabled and the open SYNCHRONOUS RECTIFIER DRIVE pin protection mode is also disabled.

Intelligent Quasi-Resonant Mode Switching
In order to improve conversion efficiency and reduce switching losses, the InnoSwitch3-EP features a means to force switching when the voltage across the primary switch is near its minimum voltage when the converter operates in discontinuous conduction mode (DCM). This mode of operation is automatically engaged in DCM and disabled once the converter moves to continuous-conduction mode (CCM).

Rather than detecting the magnetizing ring valley on the primary-side, the peak voltage of the FORWARD pin voltage as it rises above the output voltage level is used to gate secondary requests to initiate the switch "ON" cycle in the primary controller.

The secondary controller detects when the controller enters in discontinuous-mode and opens secondary cycle request windows corresponding to minimum switching voltage across the primary power switch.

Quasi-Resonant (QR) mode is enabled for 20 µs after DCM is detected or when ring amplitude (pk-pk) >2 V. Afterwards, QR switching is disabled, at which point switching may occur at any time a secondary request is initiated.

The secondary controller includes blanking of ~1 µs to prevent false detection of primary "ON" cycle when the FORWARD pin rings below ground. See Figure 8.

Peak Power Delivery
Output overload response depends on whether the IS pin is shorted to ground or the design includes a current sense resistor to set the overload threshold.

If there is an external current sense resistor on the IS pin, the InnoSwitch has options to set the overload response in two different ways.

If the device is configured to have the FEEDBACK pin auto-restart enabled, once the load current reaches the current limit threshold set by the IS pin resistor, the output voltage will fold back and auto-restart will occur once the output voltage falls below the AR threshold for a time period exceeding the AR timer.

If the device is configured for overload response, once the load current exceeds the current sense threshold the output voltage does not fold back. The auto-restart timer will begin and auto-restart occurs if the load current remains higher than the current sense threshold for a time period exceeding the AR timer.

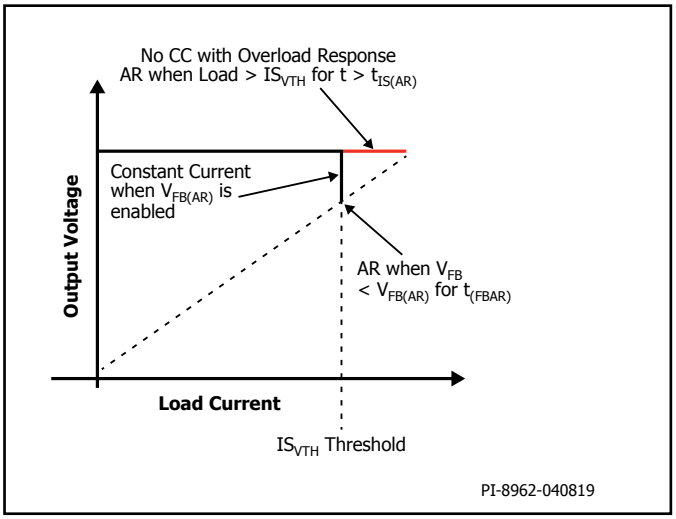


Figure 9. Current Sense Resistor in a Design.

The two cases where a current sense resistor is included in the design are shown in the Figure 9 above.

If the IS pin is shorted to the GND pin, the overload response heavily depends on the operating conditions. If the device is configured to have feedback auto-restart enabled ($V_{FB(AR)}$), auto-restart will occur if the output voltage droops below the auto-restart threshold for longer than the auto-restart timer ($t_{FB(AR)}$). Otherwise, the auto-restart occurs if the primary switches above the overload frequency limit (f_{OVL}) for longer than the auto-restart on-time (t_{AR}).

Applications Example

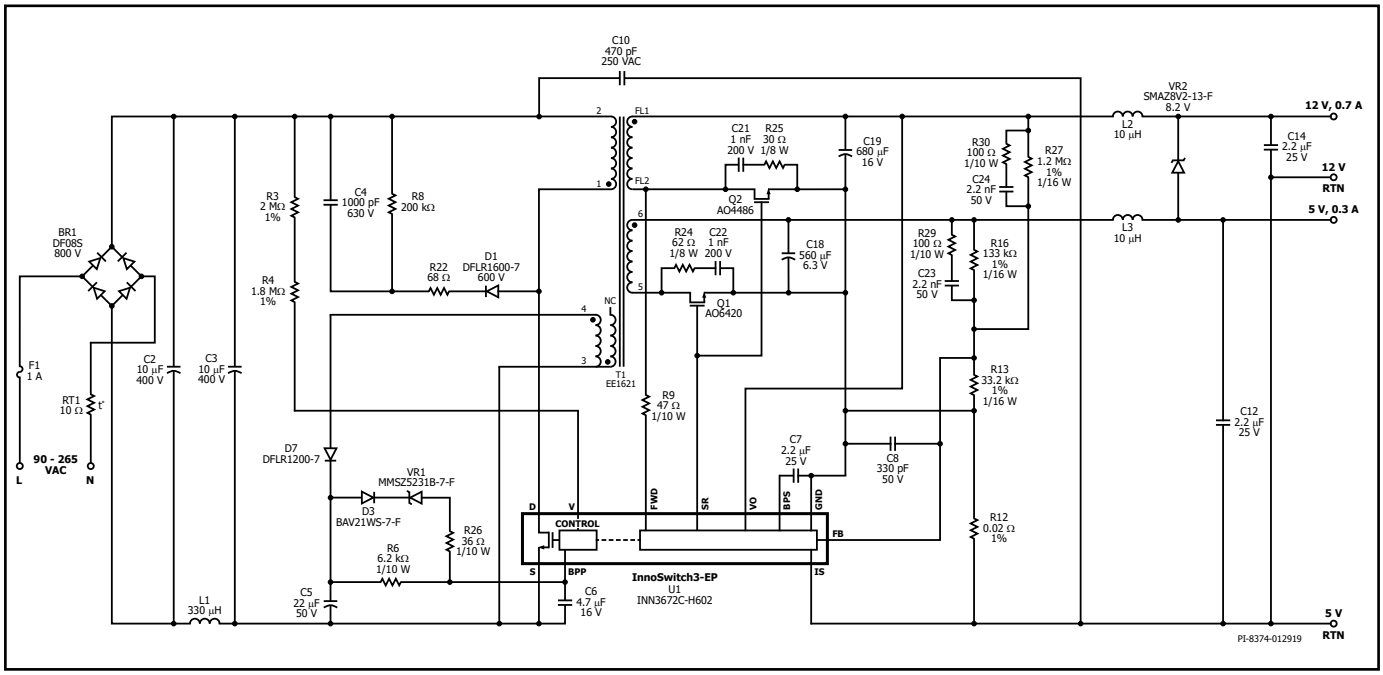


Figure 10. Schematic DER-611, 5 V, 0.3 A and 12 V, 0.7 A for HVAC (Heating, Ventilation and Air-Conditioning) Application.

The circuit shown in Figure 10 is a low cost 5 V, 0.3 A and 12 V, 0.7 A dual output power supply using INN3672C. This dual output design features high efficient design satisfying cross regulation requirement without a post-regulator.

Bridge rectifier BR1 rectifies the AC input supply. Capacitors C2 and C3 provide filtering of the rectified AC input and together with inductor L1 form a pi-filter to attenuate differential mode EMI. Y capacitor C10 connected between the power supply output and input help reduce common mode EMI.

Thermistor RT1 limits the inrush current when the power supply is connected to the input AC supply.

Input fuse F1 provides protection against excess input current resulting from catastrophic failure of any of the components in the power supply. One end of the transformer primary is connected to the rectified DC bus; the other is connected to the drain terminal of the Switch inside the InnoSwitch3-EP IC (U1).

A low-cost RCD clamp formed by diode D1, resistors R22, R8, and capacitor C4 limits the peak drain voltage of U1 at the instant of turn-off of the Switch inside U1. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The InnoSwitch3-EP IC is self-starting, using an internal high-voltage current source to charge the PRIMARY BYPASS pin capacitor (C6) when AC is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D7 and filtered using capacitor C5. Resistor R6 limits the current being supplied to the PRIMARY BYPASS pin of InnoSwitch3-EP IC (U1). The latch-off/auto-restart primary-side overvoltage protection is obtained using Zener diode VR1 with current limiting resistor R26.

The secondary-side controller of the InnoSwitch3-EP IC provides output voltage sensing, output current sensing and drive to a Switch providing synchronous rectification. The 5 V secondary of the transformer is rectified by SR FET Q1 and filtered by capacitor C18. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via a snubber (resistor R24 and capacitor C22). The 12 V secondary of the transformer is rectified by SR FET Q2 and filtered by capacitor C19. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via a snubber (resistor R25 and capacitor C21).

Synchronous rectifications (SR) are provided by Switches Q1 and Q2. Q1 and Q2 are turned on by the secondary-side controller inside IC U1, based on the winding voltage sensed via resistor R9 and fed into the FORWARD pin of the IC.

In continuous conduction mode of operation, the Switch is turned off just prior to the secondary-side's commanding a new switching cycle from the primary. In discontinuous conduction mode of operation, the power switch is turned off when the voltage drop across the Switch falls below 0 V. Secondary-side control of the primary-side power switch avoids any possibility of cross conduction of the two switches and provides extremely reliable synchronous rectification.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C7 connected to the SECONDARY BYPASS pin of InnoSwitch3-EP IC U1, provides decoupling for the internal circuitry.

Total output current is sensed by R12 between the IS and GROUND pins with a threshold of approximately 35 mV to reduce losses. Once the current sense threshold is exceeded the device adjusts the number of switch pulses to maintain a fixed output current.

The output voltages are sensed via resistor divider R13, R16, and R27, and output voltages are regulated so as to achieve a voltage of 1.265 V on the FEEDBACK pin. The 12 V phase boost circuit, R30 and C24, in parallel with 12 V feedback resistor, R27, and 5 V phase boost circuit, R29 and C23, in parallel with 5 V feedback resistor, R16, reduce the output voltage ripples. Capacitor C8 provides noise filtering of the signal at the FEEDBACK pin. Zener VR2 was added for tighter cross-regulation to limit the 12 V output when it is unloaded.

Resistors R3 and R4 provide line voltage sensing and provide a current to U1, which is proportional to the DC voltage across capacitor C3. At approximately 100 VDC, the current through these resistors exceeds the line undervoltage threshold, which results in enabling of U1. At approximately 435 VDC, the current through these resistors exceeds the line over voltage threshold, which results in disabling of U1.

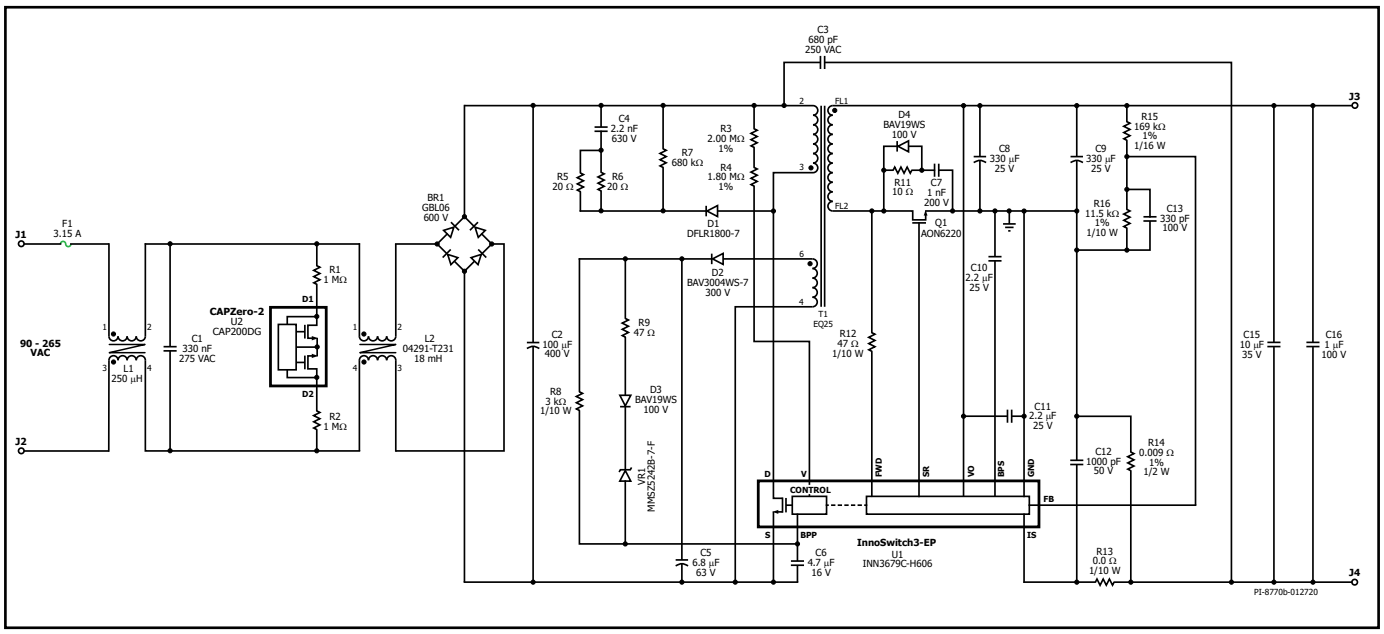


Figure 11. 20 V, 3.25 A Notebook Adapter.

The circuit shown in Figure 11 is a 20 V, 3.25 A adapter using INN3679C. This design is DOE Level 6 and EC CoC 5 compliant. Fuse F1 isolates the circuit and provides protection from component failure, and the common mode choke L1 and L2 with capacitor C1 attenuation for EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the filter capacitor C2. Capacitor C3 is used to mitigate the common mode EMI.

Resistors R1 and R2 along with U2 discharges capacitor C1 when the power supply is disconnected from AC mains.

One end of the transformer (T1) primary is connected to the rectified DC bus; the other is connected to the drain terminal of the switch inside the InnoSwitch3-EP IC (U1). Resistors R3 and R4 provide input voltage sense protection for undervoltage and overvoltage conditions.

A low-cost RCD clamp formed by diode D1, resistors R5, R6, and R7, and capacitor C4 limits the peak drain voltage of U1 at the instant of turn off of the switch inside U1. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor (C6) when AC is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C5. Resistor R8 limits the current being supplied to the BPP pin of the InnoSwitch3-EP IC (U1).

Output regulation is achieved using ramp time modulation control, the frequency and ILIM of switching cycles are adjusted based on the output load. At high load, most switching cycles are enabled which have high value of ILIM in the selected ILIM range, and at light load or no-load most cycles are disabled and the ones enabled have low value of I_{LIM} in the selected I_{LIM} range. Once a cycle is enabled, the switch will remain on until the primary current ramps to the device current limit for the specific operating state.

Zener diode VR1 along with R9 and D3 offers primary sensed output overvoltage protection. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of overvoltage at output of the converter, the auxiliary winding voltage increases and causes breakdown of VR1 which then causes a current to flow into the BPP pin of InnoSwitch3-EP IC U1. If the current flowing into the BPP pin increases above the I_{SD} threshold, the U1 controller will latch-off and prevent any further increase in output voltage.

The secondary-side of the InnoSwitch3-EP IC provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification. The secondary of the transformer is rectified by SR FET Q1 and filtered by capacitors C8 and C9. Capacitors C15 and C17 are used to reduce the high frequency output voltage ripple. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via a RCD snubber R11, C7 and D4. Diode D4 was used to minimize the dissipation in resistor R11.

The gate of Q1 is turned on by secondary-side controller inside IC U1, based on the winding voltage sensed via resistor R12 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the MOSFET is turned off just prior to the secondary-side commanding a new switching cycle from the primary. In discontinuous mode of operation, the power switch is turned off when the voltage drop across the MOSFET falls below a threshold of approximately $V_{SR(TH)}$ mV. Secondary-side control of the primary-side power switch avoids any possibility of cross conduction of the two switches and provides extremely reliable synchronous rectification.

The secondary-side of the IC U1 is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C10 connected to the BPS pin of IC U1 provides decoupling for the internal circuitry. Capacitor C11 provides decoupling for the VO pin.

Below the CC threshold, the device operates in constant voltage mode. During constant voltage mode operation, output voltage regulation is achieved through sensing the output voltage via divider resistors R15 and R16. The voltage across R16 is fed into the FB pin with an internal reference voltage threshold of 1.265 V. Output voltage is regulated so as to achieve a voltage of 1.265 V on the FB pin. Capacitor C13 provides noise filtering of the signal at the FB pin.

During CC operation, when the output voltage falls, the device will directly power itself from the secondary winding. During the on-time of the primary-side power switch, the forward voltage that appears across the secondary winding is used to charge the decoupling capacitor C10 via resistor R12 and an internal regulator. This allows output current regulation to be maintained down to ~3.4 V. Output current is sensed by monitoring the voltage drop across resistor R14 between the IS and SECONDARY GROUND pins. A threshold of approximately 35 mV reduces losses. C12 provides filtering on the IS pin from external noise. Once the internal current sense threshold is exceeded the device regulates the number of switch pulses to maintain a fixed output current.

Layout Example

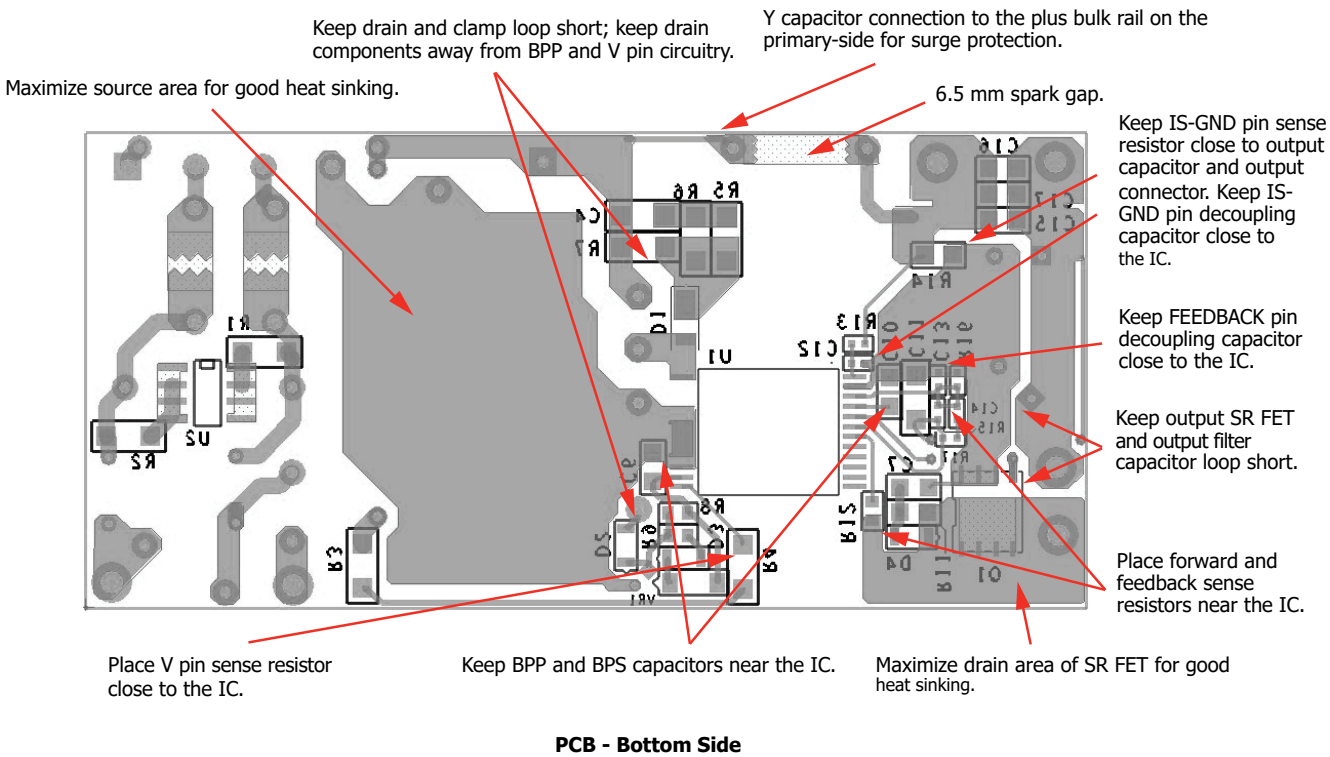


Figure 12. PCB Layout.

Key Application Considerations

Output Power Table

The data sheet output power table (Table 1) represents the maximum practical continuous output power level that can be obtained under the following conditions:

1. The minimum DC input voltage is 90 V or higher for 85 VAC input, 220 V or higher for 230 VAC input or 115 VAC with a voltage-doubler. Input capacitor voltage should be sized to meet these criteria for AC input designs.
2. Efficiency assumptions depend on power level. Smallest device power level assumes efficiency >84% increasing to >89% for the largest device (for thermally constrained environment efficiency should be >92% with larger devices).
3. Transformer primary inductance tolerance of ±10%.
4. Reflected output voltage (VOR) is set to maintain K_P = 0.8 at minimum input voltage for universal line and K_P = 1 for high input line designs.
5. Maximum conduction losses for adapters is limited to 0.6 W, 0.8 W for open frame designs.
6. Increased current limit is selected for peak and open frame power columns and standard current limit for adapter columns.
7. The part is board mounted with SOURCE pins soldered to a sufficient area of copper and/or a heat sink to keep the SOURCE pin temperature at or below 110 °C.
8. Ambient temperature of 50 °C for open frame designs and 40 °C for sealed adapters.
9. Below a value of 1, K_P is the ratio of ripple to peak primary current. To prevent reduced power delivery, due to premature termination of switching cycles, a transient K_P limit of ≥0.25 is recommended. This prevents the initial current limit (I_{INT}) from being exceeded at Switch turn-on.

Primary-Side Overvoltage Protection (Latch-Off/ Auto-Restart Mode)

Primary-side output overvoltage protection provided by the InnoSwitch3-EP IC uses an internal protection depending on H Code that is triggered by a threshold current of I_{SD} into the PRIMARY BYPASS pin. In addition to an internal filter, the PRIMARY BYPASS pin capacitor forms an external filter helping noise immunity. For the bypass capacitor to be effective as a high frequency filter, the capacitor should be located as close as possible to the SOURCE and PRIMARY BYPASS pins of the device.

The primary sensed OVP function can be realized by connecting a series combination of a Zener diode, a resistor and a blocking diode from the rectified and filtered bias winding voltage supply to the PRIMARY BYPASS pin. The rectified and filtered bias winding output voltage may be higher than expected (up to 1.5X or 2X the desired value) due to poor coupling of the bias winding with the output winding and the resulting ringing on the bias winding voltage waveform. It is therefore recommended that the rectified bias winding voltage be measured. This measurement should be ideally done at the lowest input voltage and with highest load on the output. This measured voltage should be used to select the components required to achieve primary sensed OVP. It is recommended that a Zener diode with a clamping voltage approximately 6 V lower than the bias winding rectified voltage at which OVP is expected to be triggered be selected. A forward voltage drop of 1 V can be assumed for the blocking diode. A small signal standard recovery diode is recommended. The blocking diode prevents any reverse current discharging the bias capacitor during start-up. Finally, the value of the series resistor required can be calculated such that a current higher than I_{SD} will flow into the PRIMARY BYPASS pin during an output overvoltage.

Reducing No-Load Consumption

The InnoSwitch3-EP IC can start in self-powered mode, drawing energy from the BYPASS pin capacitor charged through an internal current source. Use of a bias winding is however required to provide supply current to the PRIMARY BYPASS pin once the InnoSwitch3-EP IC has started switching. An auxiliary (bias) winding provided on the transformer serves this purpose. A bias winding driver supply to the PRIMARY BYPASS pin enables design of power supplies with no-load power consumption less than 15 mW. Resistor R6 shown in Figure 10 should be adjusted to achieve the lowest no-load input power.

Secondary-Side Overvoltage Protection (Auto-Restart Mode)

The secondary-side output overvoltage protection provided by the InnoSwitch3-EP IC uses an internal auto restart circuit that is triggered by an input current exceeding a threshold of $I_{BPS(SD)}$ into the SECONDARY BYPASS pin. The direct output sensed OVP function can be realized by connecting a Zener diode from the output to the SECONDARY BYPASS pin. The Zener diode voltage needs to be the difference between 1.25 × V_{OUT} and 4.4 V – the SECONDARY BYPASS pin voltage. It is necessary to add a low value resistor in series with the OVP Zener diode to limit the maximum current into the SECONDARY BYPASS pin.

Selection of Components

Components for InnoSwitch3-EP Primary-Side Circuit

BPP Capacitor

A capacitor connected from the PRIMARY BYPASS pin of the InnoSwitch3-EP IC to GND provides decoupling for the primary-side controller and also selects current limit. A 0.47 µF or 4.7 µF capacitor may be used. Though electrolytic capacitors can be used, often surface mount multi-layer ceramic capacitors are preferred for use on double sided boards as they enable placement of capacitors close to the IC. Their small size also makes it ideal for compact power supplies. At least 10 V, 0805 or larger size rated X5R or X7R dielectric capacitors are recommended to ensure that minimum capacitance requirements are met. The ceramic capacitor type designations, such as X7R, X5R from different manufacturers or different product families do not have the same voltage coefficients. It is recommended that capacitor data sheets be reviewed to ensure that the selected capacitor will not have more than 20% drop in capacitance at 5 V. Do not use Y5U or Z5U / 0603 rated MLCC due to this type of SMD ceramic capacitor has very poor voltage and temperature coefficient characteristics.

Bias Winding and External Bias Circuit

The internal regulator connected from the DRAIN pin of the Switch to the PRIMARY BYPASS pin of the InnoSwitch3-EP primary-side controller charges the capacitor connected to the PRIMARY BYPASS pin to achieve start-up. A bias winding should be provided on the transformer with a suitable rectifier and filter capacitor to create a bias supply that can be used to supply at least 1 mA of current to the PRIMARY BYPASS pin.

The turns ratio for the bias winding should be selected such that 7 V is developed across the bias winding at the lowest rated output voltage of the power supply at the lowest load condition. If the voltage is lower than this, no-load input power will increase.

The bias current from the external circuit should be set to $I_{S1(MAX)}$ to achieve lowest no-load power consumption when operating the power supply at 230 VAC input, (V_{BPP} > 5 V). A glass passivated standard recovery rectifier diode with low junction capacitance is recommended to avoid the snappy recovery typically seen with fast or ultrafast diodes that can lead to higher radiated EMI.

An aluminum capacitor of at least 22 µF with a voltage rating 1.2 times greater than the highest voltage developed across the capacitor is recommended. Highest voltage is typically developed across this capacitor when the supply is operated at the highest rated output voltage and load with the lowest input AC supply voltage.

Line UV and OV Protection

Resistors connected from the UNDER/OVER INPUT VOLTAGE pin to the DC bus enable sensing of input voltage to provide line undervoltage and overvoltage protection. For a typical universal input application, a resistor value of 3.8 MΩ is recommended. Figure 17 shows circuit configurations that enable either the line UV or the line OV feature only to be enabled.

InnoSwitch3-EP features a primary sensed OV protection feature that can be used to latch-off the power supply. Once the power supply is latched off, it can be reset if the UNDER/OVER INPUT VOLTAGE pin current is reduced to zero. Once the power supply is latched off, even after the input supply is turned off, it can take considerable amount of time to reset the InnoSwitch3-EP controller as the energy stored in the DC bus will continue to provide current to the controller. A fast AC reset can be achieved using the modified circuit configuration shown in Figure 18. The voltage across capacitor C_S reduces rapidly after input supply is disconnected reducing current into the INPUT VOLTAGE MONITOR pin of the InnoSwitch3-EP IC and resetting the InnoSwitch3-EP controller.

Primary Sensed OVP (Overvoltage Protection)

The voltage developed across the output of the bias winding tracks the power supply output voltage. Though not precise, a reasonably accurate detection of the amplitude of the output voltage can be achieved by the primary-side controller using the bias winding voltage. A Zener diode connected from the bias winding output to the PRIMARY BYPASS pin can reliably detect a secondary overvoltage fault and cause the primary-side controller to latch-off or auto-restart depending on H Code. It is recommended that the highest voltage at the output of the bias winding should be measured for normal steady-state conditions (at full load and lowest input voltage) and also under transient load conditions. A Zener diode rated for 1.25 times this measured voltage will typically ensure that OVP protection will only operate in case of a fault.

Primary-Side Snubber Clamp

A snubber circuit should be used on the primary-side as shown in Figure 10. This prevents excess voltage spikes at the drain of the Switch at the instant of turn-off of the Switch during each switching cycle though conventional RCD clamps can be used. RCDZ clamps offer the highest efficiency. The circuit example shown in Figure 10 uses an RCD clamp with a resistor in series with the clamp diode. This resistor dampens the ringing at the drain and also limits the reverse current through the clamp diode during reverse recovery. Standard recovery glass passivated diodes with low junction capacitance are recommended as these enable partial energy recovery from the clamp thereby improving efficiency.

Components for InnoSwitch3-EP Secondary-Side Circuit

SECONDARY BYPASS Pin – Decoupling Capacitor

A 2.2 µF, 10 V / X7R or X5R /0805 or larger size multi-layer ceramic capacitor should be used for decoupling the SECONDARY BYPASS pin of the InnoSwitch3-EP IC. Since the SECONDARY BYPASS Pin voltage needs to be 4.4 V earlier than output voltage reaches the regulation voltage level, the significantly higher BPS capacitor value could lead to output voltage overshoot during start-up. Values lower than 1.5 µF may not enough capacitance, which can cause unpredictable operation. The capacitor must be located adjacent to the IC pins. At least 10 V is recommended voltage rating to give enough margin from BPS voltage, and 0805 size is necessary to guarantee the actual value in operation since the capacitance of ceramic capacitors drops significantly with applied DC voltage especially with small package SMD such as 0603. 6.3 V / 0603 / X5U or Z5U type of MLCC is not recommended for this reason. The ceramic capacitor type designations, such as X7R, X5R from different manufacturers or different product families do not have the same voltage coefficients. It is recommended that capacitor data sheets be reviewed to ensure that the selected capacitor will not have more than 20% drop in capacitance at 4.4 V. Capacitors with X5R or X7R dielectrics should be used for best results.

FORWARD Pin Resistor

A 47 Ω, 5% resistor is recommended to ensure sufficient IC supply current. A higher or lower resistor value should not be used as it can affect device operation such as the timing of the synchronous rectifier drive. Figures 11, 12, 13 and 14 below show examples of unacceptable and acceptable FORWARD pin voltage waveforms. V_D is forward voltage drop across the SR.

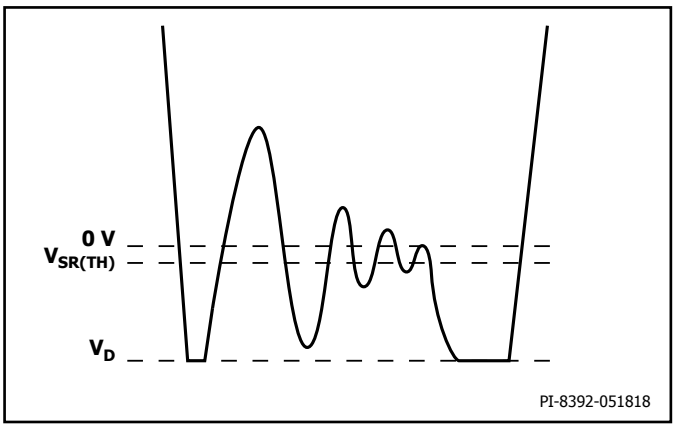


Figure 13. Unacceptable FORWARD Pin Waveform After Handshake with SR Switch Conduction During Flyback Cycle.

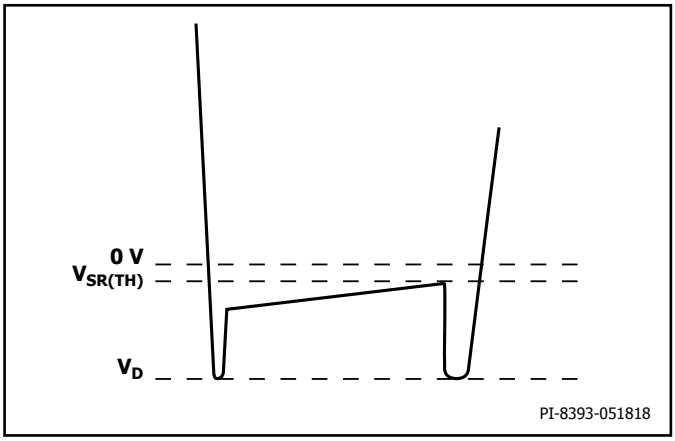


Figure 14. Acceptable FORWARD Pin Waveform After Handshake with SR Switch Conduction During Flyback Cycle.

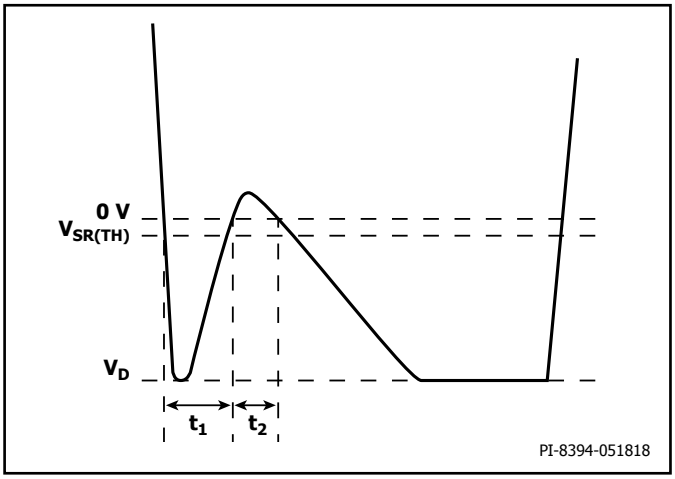


Figure 15. Unacceptable FORWARD Pin Waveform before Handshake with Body Diode Conduction During Flyback Cycle.

Note:
If $t_1 + t_2 = 1.5\ \mu s \pm 50$ ns, the controller may fail the handshake and trigger a primary bias winding OVP latch-off/auto-restart.

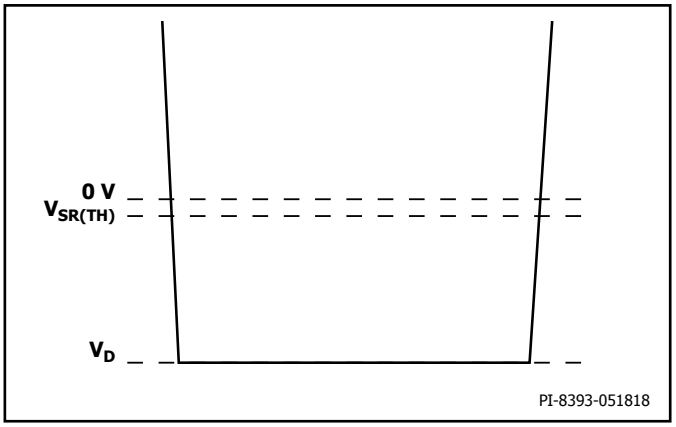


Figure 16. Acceptable FORWARD Pin Waveform before Handshake with Body Diode Conduction During Flyback Cycle.

SR Switch Operation and Selection

Although a simple diode rectifier and filter works for the output, use of an SR FET enables the significant improvement in operating efficiency often necessary to meet the European CoC and the U.S. DoE energy efficiency requirements. The secondary-side controller turns on the SR FET once the flyback cycle begins. The SR FET gate should be tied directly to the SYNCHRONOUS RECTIFIER DRIVE pin of the InnoSwitch3-EP IC (no additional resistors should be connected in the gate circuit of the SR FET). The SR FET is turned off once the V_{DS} of the SR FET reaches 0 V.

A FET with 18 mΩ $R_{DS(ON)}$ is appropriate for a 5 V, 2 A output, and a FET with 8 mΩ $R_{DS(ON)}$ is suitable for designs rated with a 12 V, 3 A output. The SR FET driver uses the SECONDARY BYPASS pin for its supply rail, and this voltage is typically 4.4 V. A FET with a high threshold voltage is therefore not suitable; FETs with a threshold voltage of 1.5 V to 2.5 V are ideal although Switches with a threshold voltage (absolute maximum) as high as 4 V may be used provided their data sheets specify $R_{DS(ON)}$ across temperature for a gate voltage of 4.5 V.

There is a slight delay between the commencement of the flyback cycle and the turn-on of the SR FET. During this time, the body diode of the SR FET conducts. If an external parallel Schottky diode is used, this current mostly flows through the Schottky diode. Once the InnoSwitch3-EP IC detects end of the flyback cycle, voltage across SR FET $R_{DS(ON)}$ reaches 0 V, any remaining portion of the flyback cycle is completed with the current commutating to the body diode of the SR FET or the external parallel Schottky diode. Use of the Schottky diode parallel to the SR FET may provide higher efficiency and typically a 1 A surface mount Schottky diode is adequate. However, the gains are modest. For a 5 V, 2 A design the external diode adds ~0.1% to full load efficiency at 85 VAC and ~0.2% at 230 VAC.

The voltage rating of the Schottky diode and the SR FET should be at least 1.4 times the expected peak inverse voltage (PIV) based on the turns ratio used for the transformer. 60 V rated FETs and diodes are suitable for most 5 V designs that use a V_{OR} < 60 V, and 100 V rated FETs and diodes are suitable for 12 V designs.

The interaction between the leakage reactance of the output windings and the SR FET capacitance (C_{OSS}) leads to ringing on the voltage waveform at the instance of voltage reversal at the winding due to primary Switch turn-on. This ringing can be suppressed using an RC snubber connected across the SR FET. A snubber resistor in the range of 10 Ω to 47 Ω may be used (higher resistance values lead to noticeable drop in efficiency). A capacitance value of 1 nF to 2.2 nF is adequate for most designs.

Output Capacitor

Low ESR aluminum electrolytic capacitors are suitable for use with most high frequency flyback switching power supplies, though the use of aluminum-polymer solid capacitors have gained considerable popularity due to their compact size, stable temperature characteristics, extremely low ESR and high RMS ripple current rating. These capacitors enable the design of ultra-compact chargers and adapters.

Typically, 200 μF to 300 μF of aluminum-polymer capacitance per ampere of output current is adequate. The other factor that influences choice of the capacitance is the output ripple. Ensure that capacitors with a voltage rating higher than the highest output voltage plus sufficient margin be used.

Output Voltage Feedback Circuit

The output voltage FEEDBACK pin voltage is 1.265 V [V_{FB}]. A voltage divider network should be connected at the output of the power supply to divide the output voltage such that the voltage at the FEEDBACK pin will be 1.265 V when the output is at its desired voltage. The lower feedback divider resistor should be tied to the SECONDARY GROUND pin. A 300 pF (or smaller) decoupling capacitor should be connected at the FEEDBACK pin to the SECONDARY GROUND pin of the InnoSwitch3-EP IC. This capacitor should be placed close to the InnoSwitch3-EP IC.

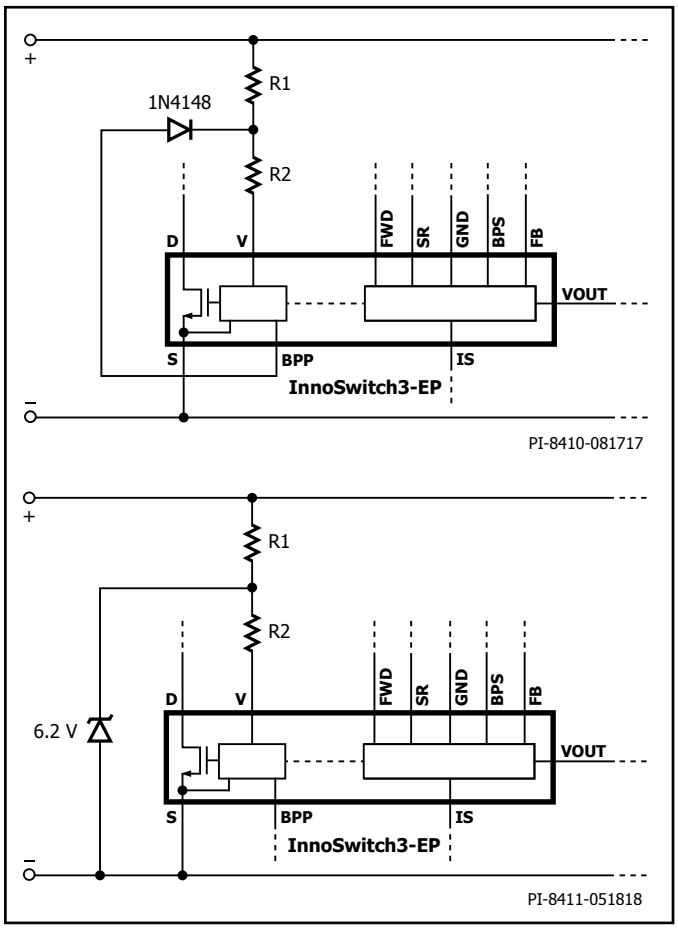


Figure 17. (Top) Line OV Only; (Bottom) Line UV Only.

Recommendations for Circuit Board Layout

See Figure 19 for a recommended circuit board layout for an InnoSwitch3-EP based power supply.

Single-Point Grounding

Use a single-point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pins.

Bypass Capacitors

The PRIMARY BYPASS and SECONDARY BYPASS pin capacitor must be located directly adjacent to the PRIMARY BYPASS-SOURCE and SECONDARY BYPASS-SECONDARY GROUND pins respectively and connections to these capacitors should be routed with short traces.

Primary Loop Area

The area of the primary loop that connects the input filter capacitor, transformer primary and IC should be kept as small as possible.

Primary Clamp Circuit

A clamp is used to limit peak voltage on the DRAIN pin at turn-off. This can be achieved by using an RCD clamp or a Zener diode (~200 V) and diode clamp across the primary winding. To reduce EMI, minimize the loop from the clamp components to the transformer and IC.

Thermal Considerations

The SOURCE pin is internally connected to the IC lead frame and provides the main path to remove heat from the device. Therefore the SOURCE pin should be connected to a copper area underneath the IC to act not only as a single point ground, but also as a heat sink. As this area is connected to the quiet source node, it can be maximized for good heat sinking without compromising EMI performance. Similarly for the output SR Switch, maximize the PCB area connected to the pins on the package through which heat is dissipated from the SR Switch.

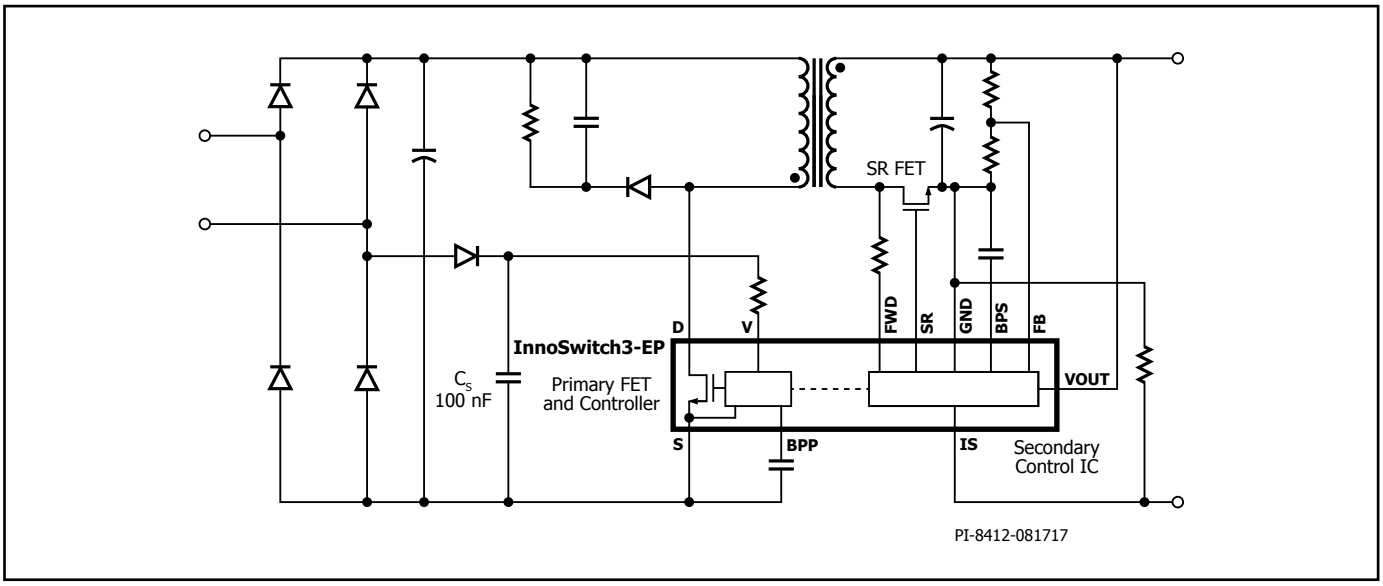


Figure 18. Fast AC Reset Configuration.

Sufficient copper area should be provided on the board to keep the IC temperature safely below the absolute maximum limits. It is recommended that the copper area provided for the copper plane on which the SOURCE pin of the IC is soldered is sufficiently large to keep the IC temperature below 110 °C when operating the power supply at full rated load and at the lowest rated input AC supply voltage.

Y Capacitor

The Y capacitor should be placed directly between the primary input filter capacitor positive terminal and the output positive or return terminal of the transformer secondary. This routes high amplitude common mode surge currents away from the IC. Note – if an input pi-filter (C, L, C) EMI filter is used then the inductor in the filter should be placed between the negative terminals of the input filter capacitors.

Output SR Switch

For best performance, the area of the loop connecting the secondary winding, the output SR Switch and the output filter capacitor, should be minimized.

ESD

Sufficient clearance should be maintained (>8 mm) between the primary-side and secondary-side circuits to enable easy compliance with any ESD / hi-pot requirements.

The spark gap is best placed directly between output positive rail and one of the AC inputs. In this configuration a 6.4 mm spark gap is often sufficient to meet the creepage and clearance requirements of many applicable safety standards. This is less than the primary to secondary spacing because the voltage across spark gap does not exceed the peak of the AC input.

Drain Node

The drain switching node is the dominant noise generator. As such the components connected the drain node should be placed close to the IC and away from sensitive feedback circuits. The clamp circuit components should be located physically away from the PRIMARY BYPASS pin and trace lengths minimized.

The loop area of the loop comprising of the input rectifier filter capacitor, the primary winding and the IC primary-side Switch should be kept as small as possible.

Layout Example

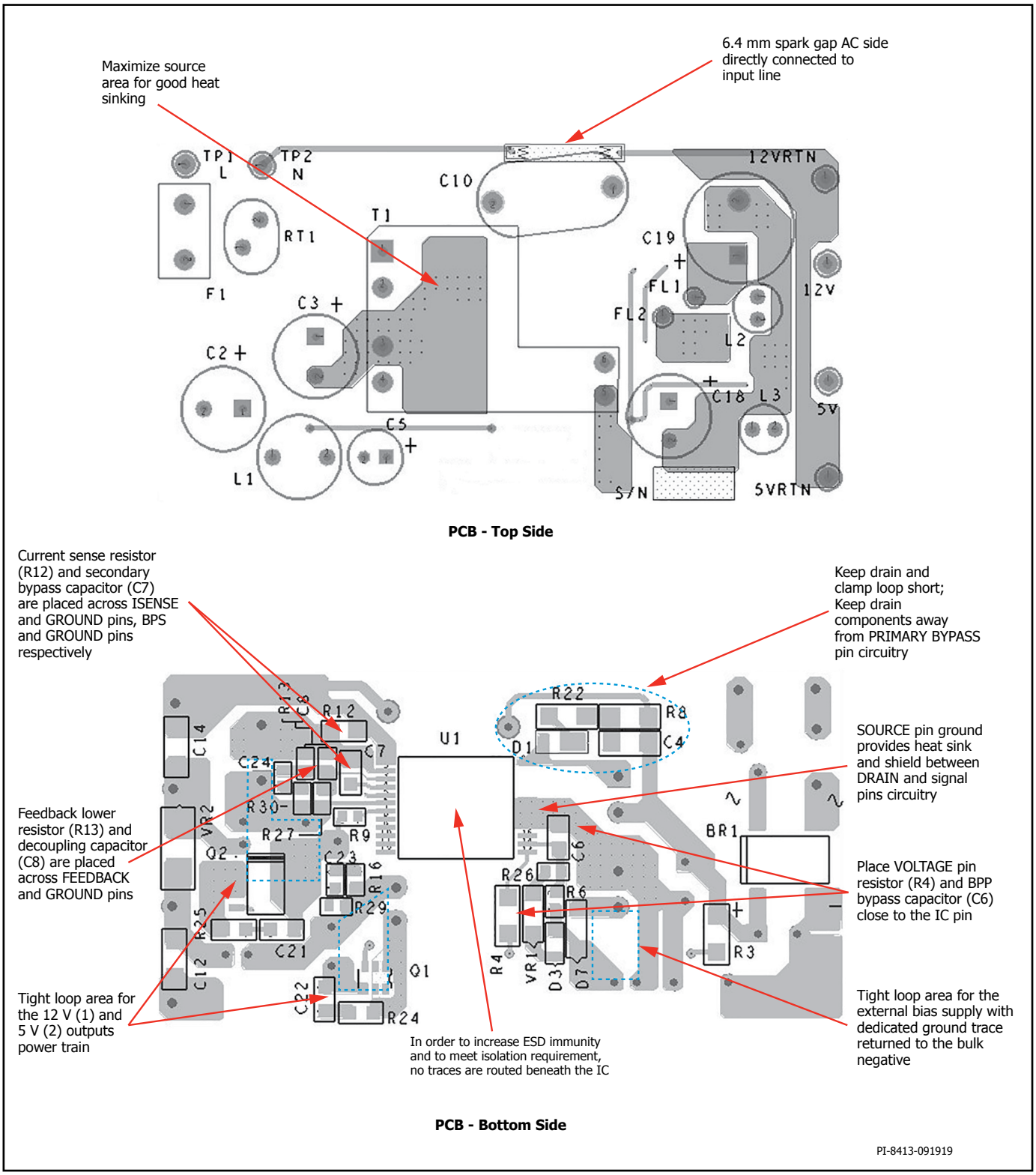


Figure 19. PCB.

Recommendations for EMI Reduction

1. Appropriate component placement and small loop areas of the primary and secondary power circuits help minimize radiated and conducted EMI. Care should be taken to achieve a compact loop area.
2. A small capacitor in parallel to the clamp diode on the primary-side can help reduce radiated EMI.
3. A resistor in series with the bias winding helps reduce radiated EMI.
4. Common mode chokes are typically required at the input of the power supply to sufficiently attenuate common mode noise. However, the same performance can be achieved by using shield windings on the transformer. Shield windings can also be used in conjunction with common mode filter inductors at input to improve conducted and radiated EMI margins.
5. Adjusting SR switch RC snubber component values can help reduce high frequency radiated and conducted EMI.
6. A pi-filter comprising differential inductors and capacitors can be used in the input rectifier circuit to reduce low frequency differential EMI.
7. A 1 µF ceramic capacitor connected at the output of the power supply helps to reduce radiated EMI.

Recommendations for Transformer Design

Transformer design must ensure that the power supply delivers the rated power at the lowest input voltage. The lowest voltage on the rectified DC bus depends on the capacitance of the filter capacitor used. At least 2 µF/W is recommended to always keep the DC bus voltage above 70 V, though 3 µF/W provides sufficient margin. The ripple on the DC bus should be measured to confirm the design calculations for transformer primary-winding inductance selection.

Switching Frequency (f_{sw})

It is a unique feature in InnoSwitch3-EP that for full load, the designer can set the switching frequency to between 25 kHz to 95 kHz. For lowest temperature, the switching frequency should be set to around 60 kHz. For a smaller transformer, the full load switching frequency needs to be set to 95 kHz. When setting the full load switching frequency it is important to consider primary inductance and peak current tolerances to ensure that average switching frequency does not exceed 110 kHz which may trigger auto-restart due to overload protection. The following table provides a guide to frequency selection based on device size. This represents the best compromise between overall device losses (conduction losses and switching losses) based on the size of the integrated high-voltage Switch.

INN3672C and INN3673C	85-90 kHz
INN3674C and INN3675C	80 kHz
INN3676C	75 kHz
INN3677C	70 kHz
INN369x	70 kHz
PowiGaN device INN3678C	70 kHz
PowiGaN device INN3679C	65 kHz
PowiGaN device INN3670C	60 kHz
INN364x	45 kHz

Reflected Output Voltage, V_{OR} (V)

This parameter describes the effect on the primary Switch drain voltage of the secondary-winding voltage during diode/SR conduction which is reflected back to the primary through the turns ratio of the transformer. To make full use of QR capability and ensure flattest efficiency over line/load, set reflected output voltage (V_{OR}) to maintain K_P = 0.8 at minimum input voltage for universal input and K_P = 1 for high-line-only conditions.

Consider the following for design optimization:

1. Higher V_{OR} allows increased power delivery at V_{MIN}, which minimizes the value of the input capacitor and maximizes power delivery from a given InnoSwitch3-EP device.
2. Higher V_{OR} reduces the voltage stress on the output diodes and SR Switches.
3. Higher V_{OR} increases leakage inductance which reduces power supply efficiency.
4. Higher V_{OR} increases peak and RMS current on the secondary-side which may increase secondary-side copper and diode losses.

There are some exceptions to this. For very high output currents the V_{OR} should be reduced to get highest efficiency. For output voltages above 15 V, V_{OR} should be higher to maintain an acceptable PIV across the output synchronous rectifier.

Ripple to Peak Current Ratio, K_P

A K_P below 1 indicates continuous conduction mode, where K_P is the ratio of ripple-current to peak-primary-current (Figure 20).

$$K_P \equiv K_{RP} = I_R / I_P$$

A value of K_P higher than 1, indicates discontinuous conduction mode. In this case K_P is the ratio of primary Switch off-time to the secondary diode conduction-time.

$$K_P \equiv K_{DP} = (1 - D) \times T/ t = V_{OR} \times (1 - D_{MAX}) / ((V_{MIN} - V_{DS}) \times D_{MAX})$$

It is recommended that a K_P close to 0.9 at the minimum expected DC bus voltage should be used for most InnoSwitch3-EP designs. A K_P value of <1 results in higher transformer efficiency by lowering the primary RMS current but results in higher switching losses in the primary-side Switch resulting in higher InnoSwitch3-EP temperature. The benefits of quasi-resonant switching start to diminish for a further reduction of K_P.

For a typical USB PD and rapid charge designs which require a wide output voltage range, K_P will change significantly as the output voltage changes. K_P will be high for high output voltage conditions and will drop as the output voltage is lowered. The PIXIs spreadsheet can be used to effectively optimize selection of K_P, inductance of the primary winding, transformer turns ratio, and the operating frequency while ensuring appropriate design margins.

Core Type

Choice of a suitable core is dependent on the physical limits of the power supply enclosure. It is recommended that only cores with low loss be used to reduce thermal challenges.

Safety Margin, M (mm)

For designs that require safety isolation between primary and secondary that are not using triple insulated wire, the width of the safety margin to be used on each side of the bobbin is important. For universal input designs a total margin of 6.2 mm is typically required – 3.1 mm being used on either side of the winding. For vertical bobbins the margin may not be symmetrical. However if a total margin of 6.2 mm is required then the physical margin can be placed on only one side of the bobbin. For designs using triple insulated wire it may still be necessary to add a small margin in order to meet required creepage distances. Many bobbins exist for each core size and each will have different mechanical spacing. Refer to the bobbin data sheet or seek guidance to determine what specific margin is required. As the margin reduces the available area for the windings, the winding area will disproportionately reduce for small core sizes.

It is recommended that for compact power supply designs using an InnoSwitch3-EP IC, triple insulated wire should be used.

Primary Layers, L

Primary layers should be in the range of 1 ≤ L ≤ 3 and in general should be the lowest number that meets the primary current density limit (CMA). A value of ≥200 Cmils / Amp can be used as a starting point for most designs. Higher values may be required due to thermal constraints. Designs with more than 3 layers are possible but the increased leakage inductance and the physical fit of the windings should be considered. A split primary construction may be helpful for designs where clamp dissipation due to leakage inductance is too high. In split primary construction, half of the primary winding is placed on either side of the secondary (and bias) winding in a sandwich arrangement. This arrangement is often disadvantageous for low power designs as this typically increases common mode noise and adds cost to the input filtering.

Maximum Operating Flux Density, B_M (Gauss)

A maximum value of 3800 gauss at the peak device current limit (at 132 kHz) is recommended to limit the peak flux density at start-up and under output short-circuit conditions. Under these conditions the output voltage is low and little reset of the transformer occurs during the Switch off-time. This allows the transformer flux density to staircase beyond the normal operating level. A value of 3800 gauss at the peak current limit of the selected device together with the built-in protection features of InnoSwitch3-EP IC provide sufficient margin to prevent core saturation under start-up or output short-circuit conditions.

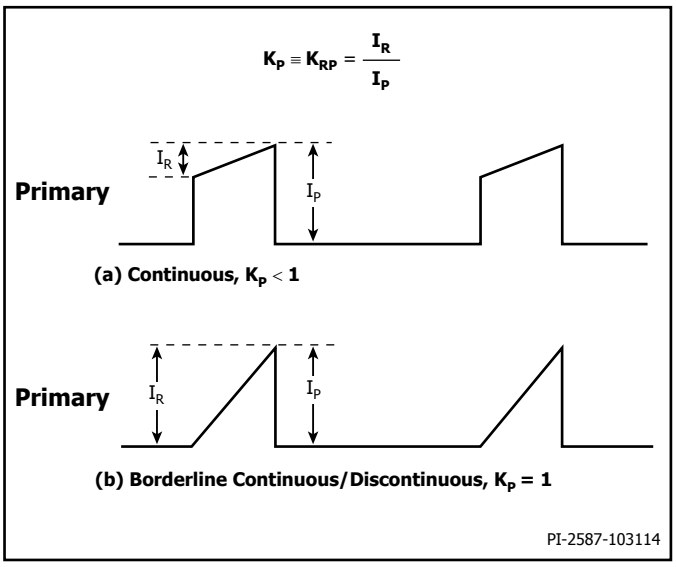


Figure 20. Continuous Conduction Mode Current Waveform, $K_P < 1$.

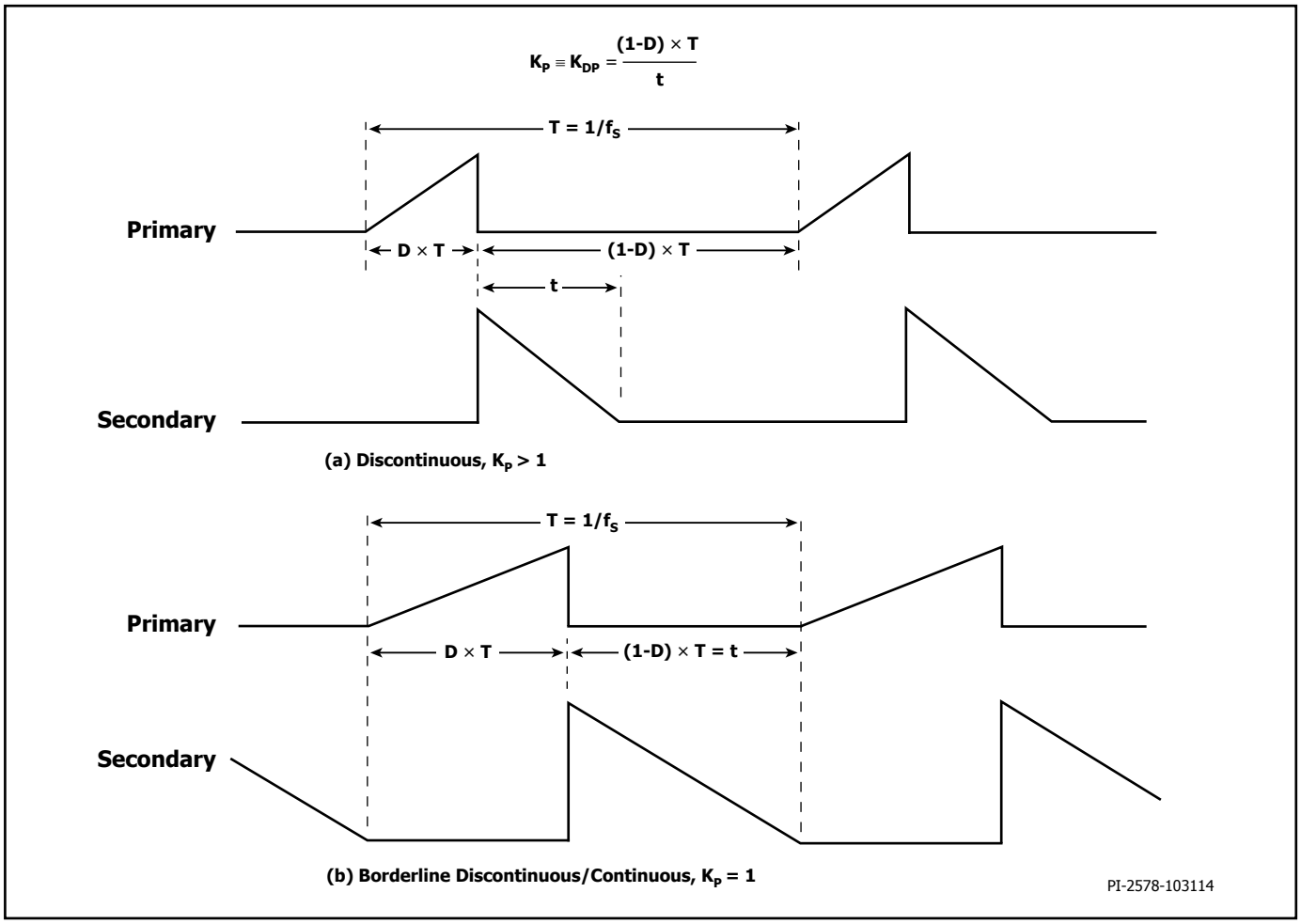


Figure 21. Discontinuous Conduction Mode Current Waveform, $K_P > 1$.

Transformer Primary Inductance, LP

Once the lowest operating input voltage, switching frequency at full load, and required VOR are determined, the transformers primary inductance can be calculated. The PIXIs design spreadsheet can be used to assist in designing the transformer.

Quick Design Checklist

As with any power supply, the operation of all InnoSwitch3-EP designs should be verified on the bench to make sure that component limits are not exceeded under worst-case conditions.

As a minimum, the following tests are strongly recommended:

1. Maximum Drain Voltage – Verify that V_{DS} of InnoSwitch3-EP and SR FET do not exceed 90% of breakdown voltages at the highest input voltage and peak (overload) output power in normal operation and during start-up.
2. Maximum Drain Current – At maximum ambient temperature, maximum input voltage and peak output (overload) power. Review drain current waveforms for any signs of transformer saturation or excessive leading-edge current spikes at start-up. Repeat tests under steady-state conditions and verify that the leading edge current spike is below $I_{LIMIT(MIN)}$ at the end of $t_{LEB(MIN)}$. Under all conditions, the maximum drain current for the primary Switch should be below the specified absolute maximum ratings.
3. Thermal Check – At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that temperature specification limits for InnoSwitch3-EP IC, transformer, output SR FET, and output capacitors are not exceeded. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of the InnoSwitch3-EP IC. Under low-line, maximum power, a maximum InnoSwitch3-EP SOURCE pin temperature of 110 °C is recommended to allow for these variations.

Design Considerations When Using 750 V and 900 V PowiGaN Devices

For a flyback converter configuration, typical voltage waveform at the DRAIN pin of the IC is shown in Figure 22 for 750 V device and Figure 23 for 900 V device.

V_{OR} is the reflected output voltage across the primary winding when the secondary is conducting. V_{BUS} is the DC voltage connected to one end of the transformer primary winding.

In addition to V_{BUS}+V_{OR}, the drain also sees a large voltage spike at turn off that is caused by the energy stored in the leakage inductance of the primary winding. To keep the drain voltage from exceeding the rated maximum continuous drain voltage, a clamp circuit is needed across the primary winding. The forward recovery of the clamp diode will add a spike at the instant of turn-OFF of the primary switch. V_{CLM} in Figure 22 and Figure 23 is the combined clamp voltage including the spike. The peak drain voltage of the primary switch is the total of V_{BUS}, V_{OR} and V_{CLM}.

V_{OR} and the clamp voltage V_{CLM} should be selected such that the peak drain voltage is lower than 650 V for 750 V device and 810 V for 900 V device for all normal operating conditions. This provides sufficient margin to ensure that occasional increase in voltage during line transients such as line surges will maintain the peak drain voltage well below 750 V and 900 V under abnormal transient operating conditions. This ensures excellent long term reliability and design margin.

To make full use of QR capability and ensure flattest efficiency over line/load, set reflected output voltage (VOR) to maintain K_P = 0.8 at minimum input voltage for universal input and $K_P \geq 1$ for high-line-only conditions.

Consider the following for design optimization:

1. Higher V_{OR} allows increased power delivery at V_{MIN}, which minimizes the value of the input capacitor and maximizes power delivery from a given PowiGaN device.
2. Higher V_{OR} reduces the voltage stress on the output diodes and SR FETs.
3. Higher V_{OR} increases leakage inductance which reduces power supply efficiency.
4. Higher V_{OR} increases peak and RMS current on the secondary-side which may increase secondary-side copper and diode losses.

There are some exceptions to this. For very high output currents the VOR should be reduced to get highest efficiency. For output voltages above 15 V, VOR should be maintained higher to maintain an acceptable PIV across the output synchronous rectifier.

V_{OR} choice will affect the operating efficiency and should be selected carefully. Table below shows the typical range of V_{OR} for optimal performance:

Output Voltage	Optimal Range for VOR
5 V	45 - 70
12 V	80 - 120
15 V	100 - 135
20 V	120 - 150
24 V	135 - 180 (for 750 V GaN) 135 - 150 (for 900 V GaN)

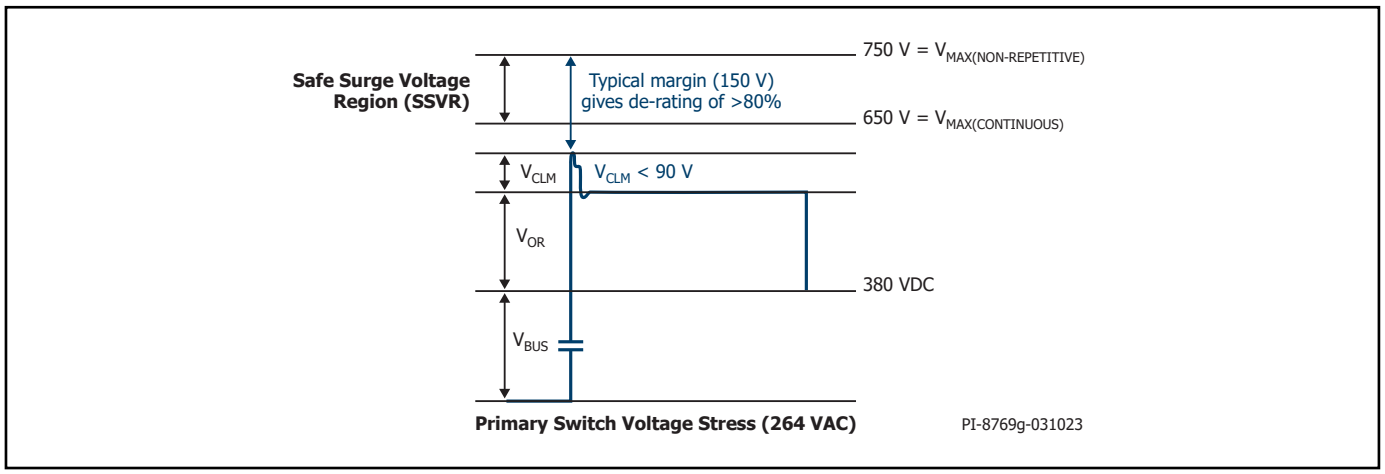


Figure 22. Peak Drain Voltage for 264 VAC Input Voltage using 750 V PowiGaN.

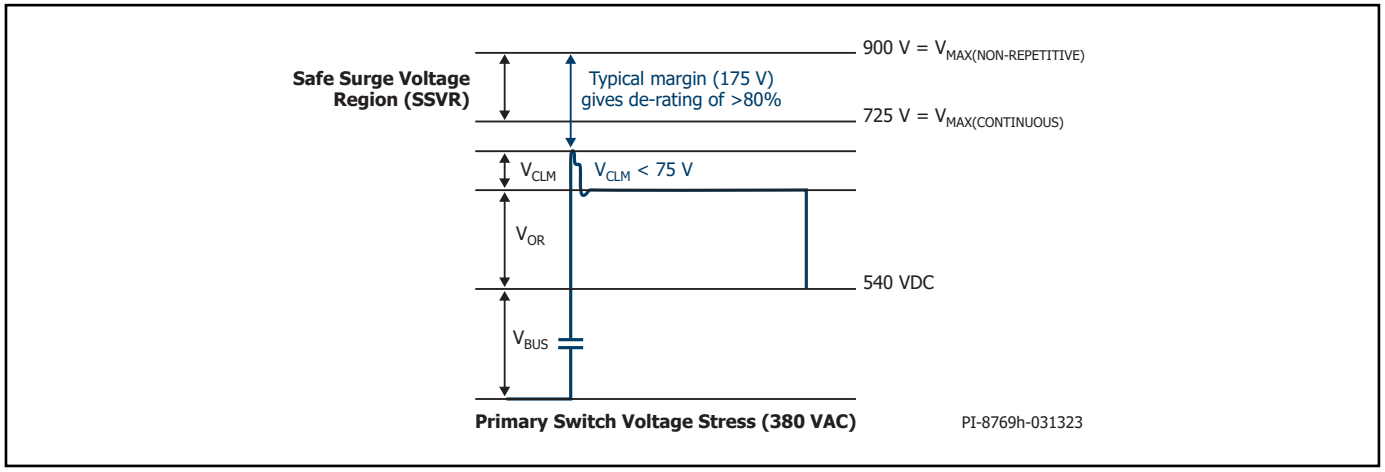


Figure 23. Peak Drain Voltage for 380 VAC Input Voltage using 900 V PowiGaN.

Thermal Resistance Test Conditions for PowiGaN Devices

Thermal resistance value is for primary power device junction to ambient only.

Testing performed on custom thermal test PCB as shown in Figure 24. The test board consists of 2 layers of 2 oz. Cu with the InSOP package mounted to the top surface and connected to a bottom layer Cu heat sinking area of 550 mm^2.

Connection between the two layers was made by 82 vias in a 5 x 17 matrix outside the package mounting area. Vias are spaced at 40 mils, with 12 mil diameter and plated through holes are not filled.

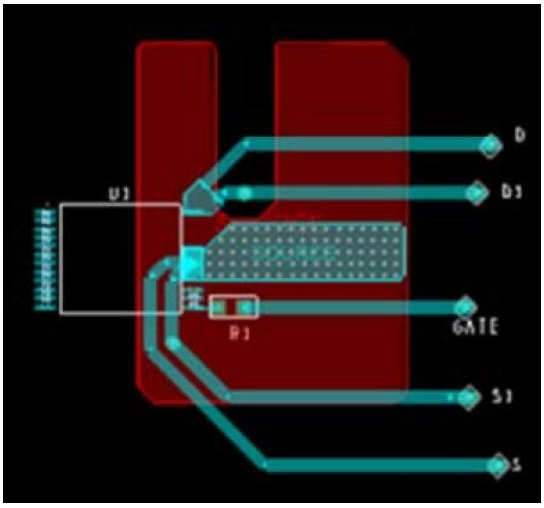


Figure 24. Thermal Resistance Test Conditions for PowiGaN Devices (INN3678C, INN3679C and INN3670C.)

Absolute Maximum Ratings[1,2]

DRAIN Pin Voltage: INN3672C - INN3677C ..... -0.3 V to 725 V
INN3678C - INN3670C ..... -0.3 V to 750 V[6]
INN369x ..... -0.3 V to 900 V[7]
INN364x ..... -0.3 V to 1700 V
DRAIN Pin Peak Current: INN3672C ..... 1.70 A[3]
INN3673C ..... 2.38 A[3]
INN3674C ..... 3.47 A[3]
INN3675C ..... 4.11 A[3]
INN3676C ..... 5.19 A[3]
INN3677C ..... 5.92 A[3]
PowiGaN device INN3678C ..... 6.5 A[3]
PowiGaN device INN3679C ..... 10 A[3]
PowiGaN device INN3670C ..... 14 A[3]
PowiGaN device INN3697C ..... 3.2 A[3]
PowiGaN device INN3699C ..... 10 A[3]
PowiGaN device INN3690C ..... 14 A[3]
INN3692C ..... 2.2 A[3]
INN3694C ..... 3.96 A[3]
INN3696C ..... 5.72 A[3]
INN3647C ..... 5 A[3]
INN3649C ..... 10 A[3]
BPP/BPS Pin Voltage ..... -0.3 to 6 V
BPP/BPS Current ..... 100 mA
FWD Pin Voltage ..... -1.5 V to 150 V
FB Pin Voltage ..... -0.3 V to 6 V
SR Pin Voltage ..... -0.3 V to 6 V
VOUT Pin Voltage ..... -0.3 V to 27 V
V Pin Voltage ..... -0.3 V to 725 V
IS Pin Voltage[8] ..... -0.3 V to 0.3 V
Storage Temperature ..... -65 to 150 °C
Operating Junction Temperature[4] ..... -40 to 150 °C
Ambient Temperature ..... -40 to 105 °C
Lead Temperature[4] ..... 260 °C

NOTES:
1. All voltages referenced to SOURCE and Secondary GROUND, T_A = 25 °C.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
3. Please refer to Figure 25, 31, 39, 43 and 47 about maximum allowable voltage and current combinations.
4. Normally limited by internal circuitry.
5. 1/16" from case for 5 seconds.
6. PowiGaN devices: INN367x
   Maximum drain voltage (non-repetitive pulse) ..... -0.3 V to 750 V
   Maximum continuous drain voltage ..... -0.3 V to 650 V
7. PowiGaN devices: INN369x
   Maximum drain voltage (non-repetitive pulse) ..... -0.3 V to 900 V
   Maximum continuous drain voltage ..... -0.3 V to 725 V
8. Absolutely maximum voltage for less than 500 µsec is 3 V.

Thermal Resistance

Thermal Resistance: INN3672C to INN3677C & INN3692C to INN3696C
(θ_{JA}) ..... 76 °C/W[1], 65 °C/W[2]
(θ_{JC}) ..... 8 °C/W[3]
PowiGan Devices
(θ_{JA}) ..... 50 °C/W[4]
INN3647C
(θ_{JA}) ..... 92 °C/W[1], 64 °C/W[2]
(θ_{JC}) ..... 19 °C/W[3]
INN3649C
(θ_{JA}) ..... 76 °C/W[1], 70 °C/W[2]
(θ_{JC}) ..... 11 °C/W[3]

Notes:
1. Soldered to 0.36 sq. inch (232 mm²) 2 oz. (610 g/m²) copper clad.
2. Soldered to 1 sq. inch (645 mm²), 2 oz. (610 g/m²) copper clad.
3. The case temperature is measured on the top of the package.
4. Please see Figure 23.

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Startup Switching Frequency	f_{SW}	T_J = 25 °C		23	25	27	kHz
Jitter Frequency	f_M	T_J = 25 °C f_{SW} = 100 kHz		0.80	1.25	1.70	kHz
Maximum On-Time	$t_{ON(MAX)}$	T_J = 25 °C		12.4	14.6	16.9	µs
Minimum Primary Feedback Block-Out Timer	t_{BLOCK}					$t_{OFF(MIN)}$	µs
BPP Supply Current	I_{S1}	V_{BPP} = V_{BPP} + 0.1 V (Switch not Switching) T_J = 25 °C	INN36xxC	145	200	300	µA
			INN3678C - INN3670C INN3647C INN3649C	145	266	425	µA
	I_{S2}	V_{BPP} = V_{BPP} + 0.1 V (Switch Switching at 132 kHz) T_J = 25 °C	INN3672C	0.33	0.44	0.60	mA
			INN3673C	0.36	0.48	0.65	
			INN3674C	0.44	0.58	0.83	
			INN3675C	0.59	0.79	1.10	
			INN3676C	0.77	1.02	1.38	
			INN3677C	0.90	1.20	1.73	
			INN3692C	0.33	0.44	0.60	
			INN3694C	0.44	0.58	0.85	
			INN3696C	0.7	0.90	1.35	
			INN3678C	0.93	1.24	1.79	
			INN3679C - INN3670C	1.46	1.95	2.81	
			INN3697C	TBD	1.95	TBD	
			INN3699C	TBD	1.95	TBD	
			INN3690C	TBD	1.95	TBD	
			INN3647C	0.93	1.25	1.80	
			INN3649C	1.46	1.95	2.81	
BPP Pin Charge Current	I_{CH1}	V_{BP} = 0 V, T_J = 25 °C		-1.75	-1.35	-0.88	mA
	I_{CH2}	V_{BP} = 4 V, T_J = 25 °C		-5.98	-4.65	-3.32	
BPP Pin Voltage	V_{BPP}	INN36xxC		4.65	4.90	5.15	V
		INN3647C INN3649C		4.65	4.90	5.20	
BPP Pin Voltage Hysteresis	$V_{BPP(H)}$	T_J = 25 °C			0.39		V
BPP Shunt Voltage	V_{SHUNT}	I_{BPP} = 2 mA		5.15	5.36	5.65	V
BPP Power-Up Reset Threshold Voltage	$V_{BPP(RESET)}$	T_J = 25 °C		2.80	3.15	3.50	V
UV/OV Pin Brown-In Threshold	I_{UV+}	T_J = 25 °C	INN36xxC INN369xC	23.9	26.1	28.2	µA
			INN3678C - INN3670C INN3647C / INN3649C	22.4	24.4	26.7	

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
UV/OV Pin Brown-Out Threshold	I_{UV-}	T_J = 25 °C	INN36xxC INN369xC	21.0	23.7	25.5	µA
			INN3678C - INN3670C INN3647C / INN3649C	19	21.6	23.5	
Brown-Out Delay Time	t_{UV-}	T_J = 25 °C			35		ms
UV/OV Pin Line Overvoltage Threshold	I_{OV+}	T_J = 25 °C	INN36xxC INN369xC	106	115	118	µA
			INN3678C - INN3670C	106	112	118	
			INN3647C INN3649C				
UV/OV Pin Line Overvoltage Hysteresis	$I_{OV(H)}$	T_J = 25 °C	INN36xxC		7		µA
			INN3678C - INN3670C INN369xC		8		
			INN3647C INN3649C		7		
UV/OV Pin Line Overvoltage Recovery Threshold	I_{OV-}	T_J = 25 °C		100			µA
Line Fault Protection							
VOLTAGE Pin Line Over-voltage Deglitch Filter	t_{OV+}	T_J = 25 °C See Note B			3		µs
VOLTAGE Pin Voltage Rating	V_V	T_J = 25 °C		650			V
Circuit Protection							
Standard Current Limit (BPP) Capacitor = 0.47 µF See Note C	I_{LIMIT}	di/dt = 138 mA/µs T_J = 25 °C	INN3672C	418	450	482	mA
		di/dt = 163 mA/µs T_J = 25 °C	INN3673C	511	550	589	
		di/dt = 188 mA/µs T_J = 25 °C	INN3674C	697	750	803	
		di/dt = 213 mA/µs T_J = 25 °C	INN3675C	883	950	1017	
		di/dt = 238 mA/µs T_J = 25 °C	INN3676C	1162	1250	1338	
		di/dt = 300 mA/µs T_J = 25 °C	INN3677C	1255	1350	1445	
		di/dt = 375 mA/µs T_J = 25 °C	INN3678C	1581	1700	1819	
		di/dt = 425 mA/µs T_J = 25 °C	INN3679C	1767	1900	2033	
		di/dt = 525 mA/µs T_J = 25 °C	INN3670C	2139	2300	2461	
		di/dt = 138 mA/µs T_J = 25 °C	INN3692C	416	450	483	
		di/dt = 188 mA/µs T_J = 25 °C	INN3694C	693	750	806	
		di/dt = 238 mA/µs T_J = 25 °C	INN3696C	1156	1250	1344	

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection (cont.)							
Standard Current Limit (BPP) Capacitor = 0.47 µF See Note C	I_{LIMIT}	di/dt = 300 mA/µs T_J = 25 °C	INN3647C	1488	1600	1712	mA
		di/dt = 425 mA/µs T_J = 25 °C	INN3649C	1767	1900	2033	
		di/dt = 325 mA/µs T_J = 25 °C	INN3697C	TBD	1300	TBD	
		di/dt = 425 mA/µs T_J = 25 °C	INN3699C	TBD	1900	TBD	
		di/dt = 525 mA/µs T_J = 25 °C	INN3690C	TBD	2300	TBD	
Increased Current Limit (BPP) Capacitor = 4.7 µF See Note C	$I_{LIMIT+1}$	di/dt = 138 mA/µs T_J = 25 °C	INN3672C	500	550	600	mA
		di/dt = 163 mA/µs T_J = 25 °C	INN3673C	591	650	709	
		di/dt = 188 mA/µs T_J = 25 °C	INN3674C	864	950	1036	
		di/dt = 213 mA/µs T_J = 25 °C	INN3675C	1046	1150	1254	
		di/dt = 238 mA/µs T_J = 25 °C	INN3676C	1319	1450	1581	
		di/dt = 300 mA/µs T_J = 25 °C	INN3677C	1410	1550	1689	
		di/dt = 375 mA/µs T_J = 25 °C	INN3678C	1767	1900	2033	
		di/dt = 425 mA/µs T_J = 25 °C	INN3679C	1980	2130	2279	
		di/dt = 525 mA/µs T_J = 25 °C	INN3670C	2395	2576	2756	
		di/dt = 138 mA/µs T_J = 25 °C	INN3692C	495	550	605	
		di/dt = 188 mA/µs T_J = 25 °C	INN3694C	855	950	1045	
		di/dt = 238 mA/µs T_J = 25 °C	INN3696C	1305	1450	1595	
		di/dt = 300 mA/µs T_J = 25 °C	INN3647C	1674	1800	1926	
		di/dt = 425 mA/µs T_J = 25 °C	INN3649C	1980	2130	2279	
		di/dt = 325 mA/µs T_J = 25 °C	INN3697C	TBD	1460	TBD	
		di/dt = 425 mA/µs T_J = 25 °C	INN3699C	TBD	2130	TBD	
		di/dt = 525 mA/µs T_J = 25 °C	INN3690C	TBD	2576	TBD	

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection (cont.)							
Overload Detection Frequency	f_{OVL}	T_J = 25 °C		102	110	118	kHz
BYPASS Pin Latching Shutdown Threshold Current	I_{SD}	T_J = 25 °C		6.0	7.5	11.3	mA
Auto-Restart On-Time	t_{AR}	T_J = 25 °C		75	82	89	ms
Auto-Restart Trigger Skip Time	$t_{AR(SK)}$	T_J = 25 °C See Note A			1.3		sec
Output							
Auto-Restart Off-Time	$t_{AR(OFF)}$	T_J = 25 °C		1.7		2.11	sec
Short Auto-Restart Off-Time	$t_{AR(OFF)SH}$	T_J = 25 °C See Note B	INN36xxC	0.17	0.20	0.23	sec
			INN3647C INN3649C		0.20		
ON-State Resistance	$R_{DS(ON)}$	INN3672C $I_D = I_{LIMIT+1}$	T_J = 25 °C		6.30	7.25	Ω
			T_J = 100 °C		9.77	11.24	
		INN3673C $I_D = I_{LIMIT+1}$	T_J = 25 °C		4.42	5.08	
			T_J = 100 °C		6.85	7.88	
		INN3674C $I_D = I_{LIMIT+1}$	T_J = 25 °C		3.22	3.70	
			T_J = 100 °C		4.99	5.74	
		INN3675C $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.95	2.24	
			T_J = 100 °C		3.02	3.47	
		INN3676C $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.34	1.54	
			T_J = 100 °C		2.08	2.39	
		INN3677C $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.20	1.38	
			T_J = 100 °C		1.86	2.14	
		INN3678C $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.52	0.68	
			T_J = 100 °C		0.78	1.02	
		INN3679C $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.35	0.44	
			T_J = 100 °C		0.49	0.62	
		INN3670C $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.29	0.39	
			T_J = 100 °C		0.41	0.54	
		INN3692C $I_D = I_{LIMIT+1}$	T_J = 25 °C		6.0	7.2	
			T_J = 100 °C		9.5	11.2	
		INN3694C $I_D = I_{LIMIT+1}$	T_J = 25 °C		3.5	4.1	
			T_J = 100 °C		5.2	6.0	
		INN3696C $I_D = I_{LIMIT+1}$	T_J = 25 °C		2.35	2.8	
			T_J = 100 °C		3.4	4.2	
		INN3647C $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.20	1.53	
			T_J = 100 °C		1.98	2.52	

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Output (cont.)							
ON-State Resistance	$R_{DS(ON)}$	INN3649C $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.45	0.62	Ω
			T_J = 100 °C		0.74	1.02	
		INN3697C $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.85	TBD	
			T_J = 100 °C		TBD	TBD	
		INN3699C $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.35	TBD	
			T_J = 100 °C		TBD	TBD	
		INN3690C $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.29	TBD	
			T_J = 100 °C		TBD	TBD	
OFF-State Drain Leakage Current	I_{DSS1}	$V_{BPP} = V_{BPP}$ + 0.1 V V_{DSS} = 80% Peak Drain Voltage T_J = 125 °C				200	µA
	I_{DSS2}	$V_{BPP} = V_{BPP}$ + 0.1 V V_{DSS} = 325 V T_J = 25 °C			15		µA
Drain Supply Voltage		See Note A		30			V
Thermal Shutdown	T_{SD}	See Note A		135	142	150	°C
Thermal Shutdown Hysteresis	$T_{SD(H)}$	See Note A	INN367x INN369x		70		°C
			INN364x		30		
Secondary							
FEEDBACK Pin Voltage	V_{FB}	T_J = 25 °C		1.25	1.265	1.280	V
Maximum Switching Frequency	f_{SREQ}	T_J = 25 °C		118	132	145	kHz
FEEDBACK Pin Auto-Restart Threshold	$V_{FB(AR)}$				90		%
FEEDBACK and IS Pin Auto-Restart Timer	$t_{FB(AR)}$ $t_{IS(AR)}$	T_J = 25 °C			49.5		ms
BPS Pin Current at No-Load	I_{SNL}	T_J = 25 °C			325	485	µA
BPS Pin Voltage	V_{BPS}			4.20	4.40	4.60	V
BPS Pin Undervoltage Threshold	$V_{BPS(UVLO)(TH)}$			3.60	3.80	4.00	V
BPS Pin Undervoltage Hysteresis	$V_{BPS(UVLO)(H)}$				0.65		V
Current Limit Voltage Threshold	$I_{SV(TH)}$	Set By External Resistor T_J = 25 °C		35.17	35.90	36.62	mV
FWD Pin Breakdown Voltage	V_{FWD}			150			V
Minimum Off-Time	$t_{OFF(MIN)}$			2.48	3.38	4.37	µs

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)			Min	Typ	Max	Units
Secondary (cont.)								
Soft-Start Frequency Ramp Time	$t_{SS(RAMP)}$	T_J = 25 °C			7.5	11.8	19.0	ms
BPS Pin Latch/ Auto-Restart Command Shutdown Threshold Current	$I_{BPS(SD)}$				5.2	8.9	12	mA
FEEDBACK Pin Short-Circuit	$V_{FB(OFF)}$	T_J = 25 °C				112	135	mV
Synchronous Rectifier @ T_J = 25 °C								
SR Pin Drive Voltage	V_{SR}				4.2	4.4	4.6	V
SR Pin Voltage Threshold	$V_{SR(TH)}$					-2.5	0	mV
SR Pin Pull-Up Current	$I_{SR(PU)}$	T_J = 25 °C C_{LOAD} = 2 nF, f_{SW} = 100 kHz	INN367x, INN369x		125	165	195	mA
			INN364x		135	165	195	
SR Pin Pull-Down Current	$I_{SR(PD)}$	T_J = 25 °C C_{LOAD} = 2 nF, f_{SW} = 100 kHz	INN367x, INN369x		87	97	115	mA
			INN364x		260	298	336	
Rise Time	t_R	T_J = 25 °C C_{LOAD} = 2 nF See Note B	10-90%	INN367x INN369x		50		ns
				INN364x		40		
Fall Time	t_F	T_J = 25 °C C_{LOAD} = 2 nF See Note B	90-10%	INN367x INN369x		80		ns
				INN364x		15		
Output Pull-Up Resistance	R_{PU}	T_J = 25 °C V_{BPS} = 4.4 V I_{SR} = 10 mA	INN367x INN369x		7.2	8.3	12	Ω
			INN364x		7.2	8.5	9.6	
Output Pull-Down Resistance	R_{PD}	T_J = 25 °C V_{BPS} = 4.4 V I_{SR} = 10 mA	INN367x INN369x		10.0	12.1	15	Ω
			INN364x		3.52	3.95	4.39	

NOTES:
A. This parameter is derived from characterization.
B. This parameter is guaranteed by design.
C. To ensure correct current limit it is recommended that nominal 0.47 µF / 4.7 µF capacitors are used. In addition, the BPP capacitor value tolerance should be equal or better than indicated below across the ambient temperature range of the target application. The minimum and maximum capacitor values are guaranteed by characterization.

Nominal BPP Pin Capacitor Value	BPP Capacitor Value Tolerance	
	Minimum	Maximum
0.47 µF	-60%	+100%
4.7 µF	-50%	N/A

Recommended to use at least 10 V / 0805 / X7R SMD MLCC.

Typical Performance Curves

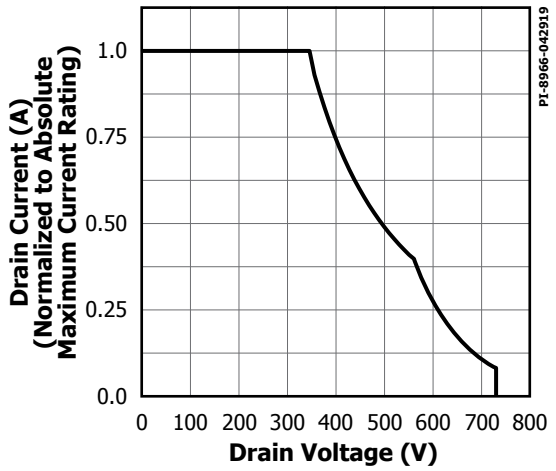


Figure 25. Maximum Allowable Drain Current vs. Drain Voltage (INN3672-INN3677).

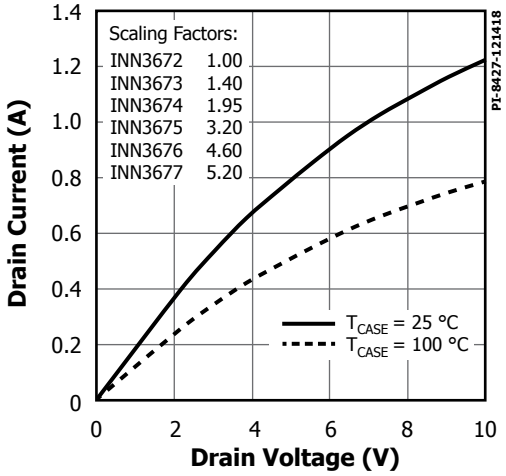


Figure 26. Output Characteristics.

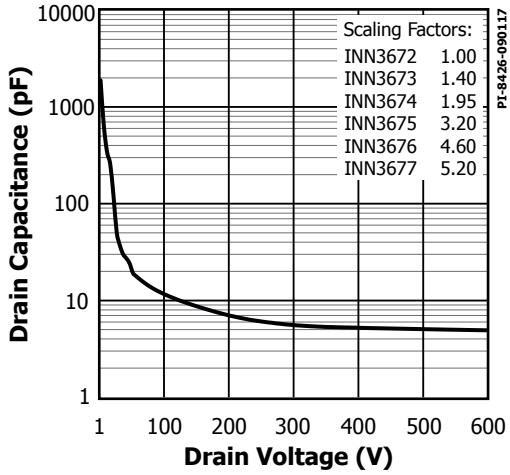


Figure 27. C_{OSS} vs. Drain Voltage.

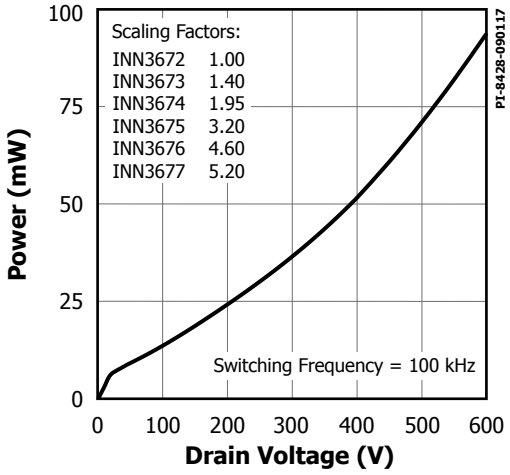


Figure 28. Drain Capacitance Power.

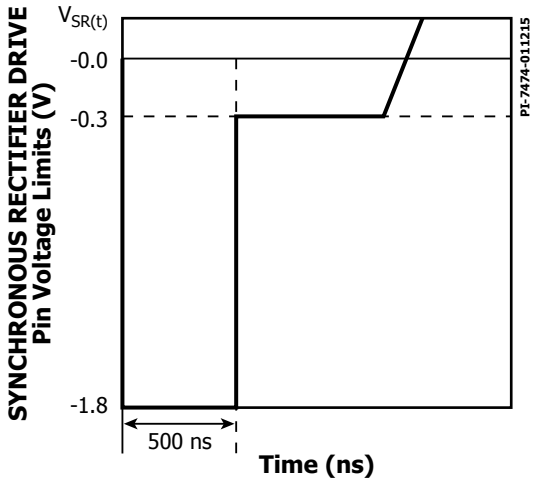


Figure 29. SYNCHRONOUS RECTIFIER DRIVE Pin Negative Voltage.

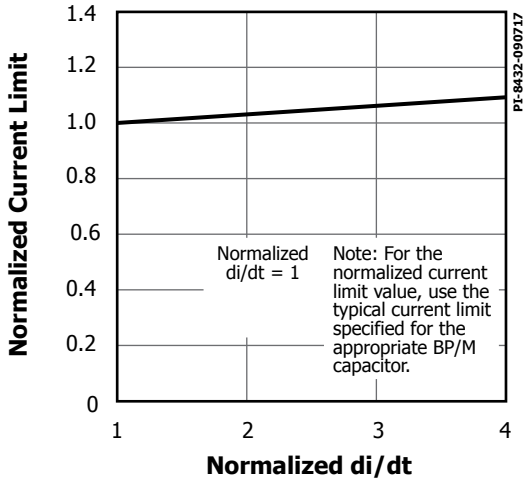


Figure 30. Standard Current Limit vs. di/dt.

Typical Performance Curves

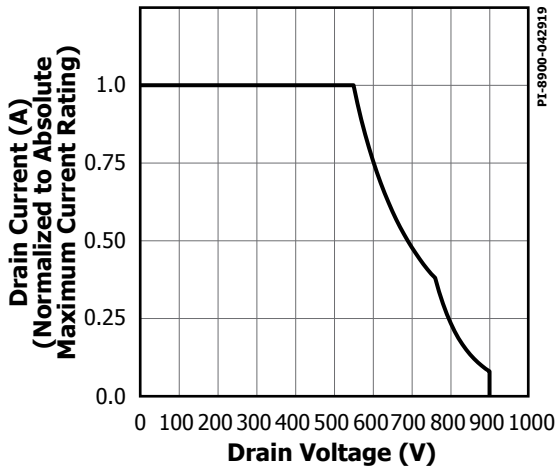


Figure 31. Maximum Allowable Drain Current vs. Drain Voltage (INN369x).

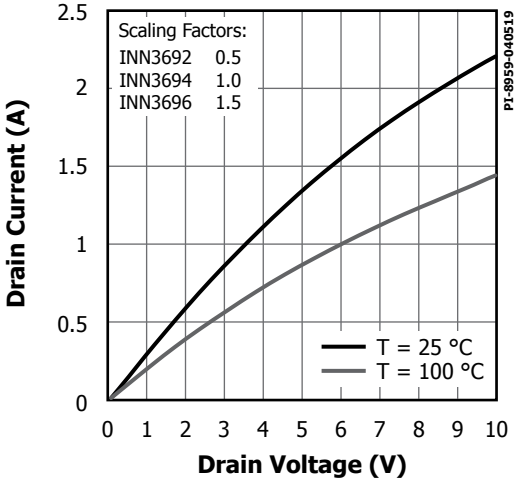


Figure 32. Output Characteristics.

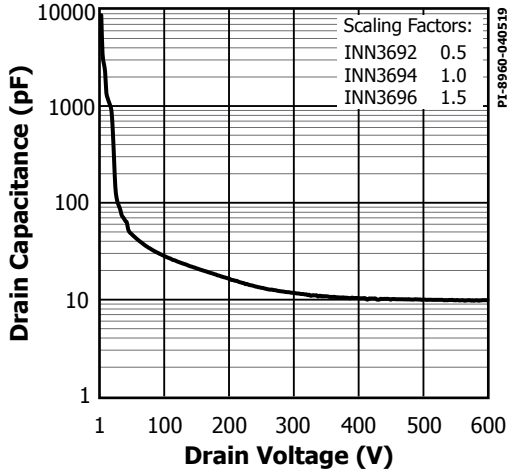


Figure 33. C_{OSS} vs. Drain Voltage.

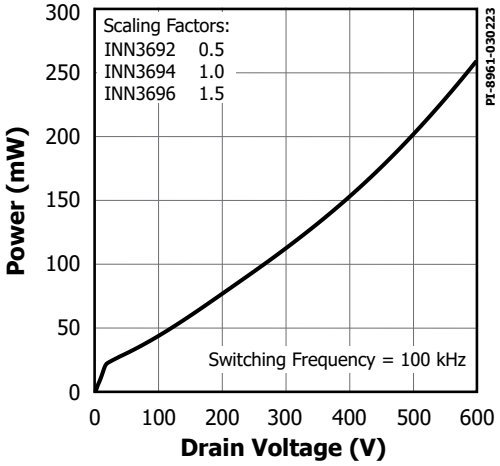


Figure 34. Drain Capacitance Power.

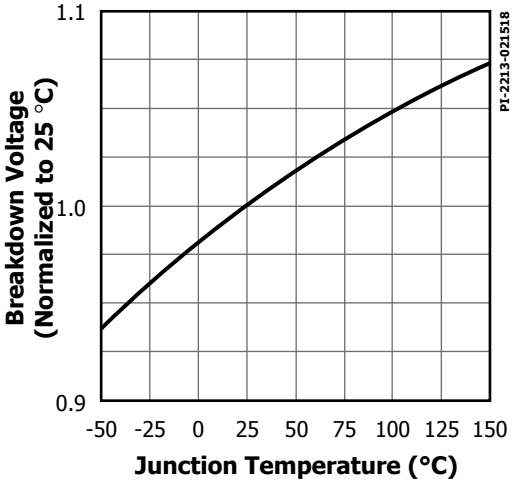


Figure 35. Breakdown vs. Temperature (Exclude INN3678C / INN3679C / INN3670C / INN3647C / INN3649C).

Typical Performance Curves

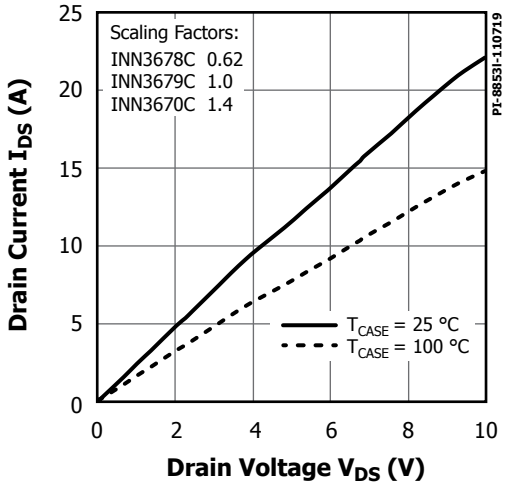


Figure 36. Output Characteristics.

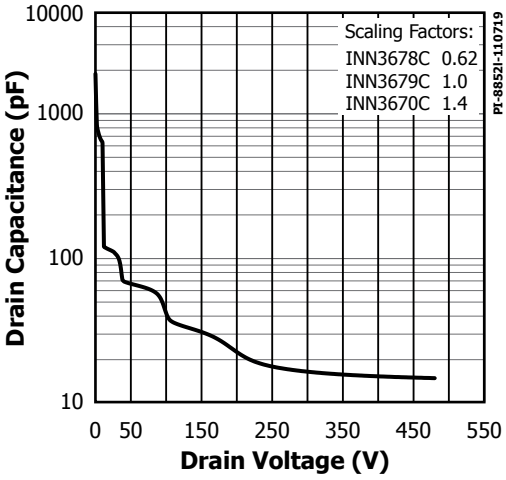


Figure 37. C_{OSS} vs. Drain Voltage.

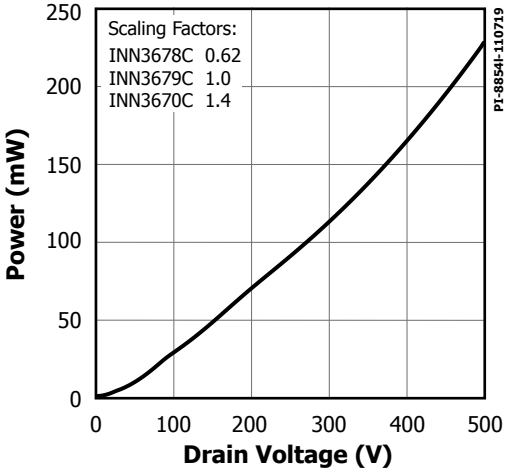


Figure 38. Drain Capacitance Power.

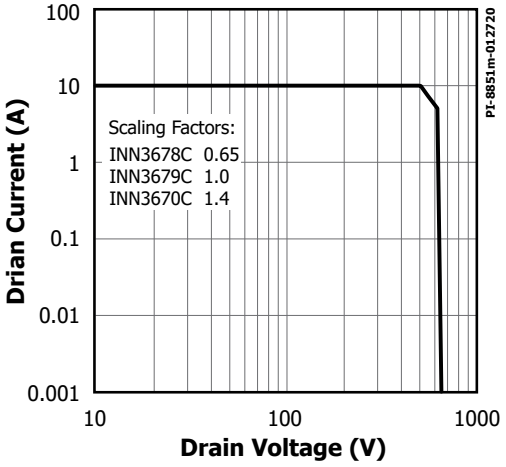


Figure 39. Maximum Allowable Drain Current vs. Drain Voltage (PowiGaN Devices INN3678C / INN3679C / INN3670C).

Typical Performance Curves

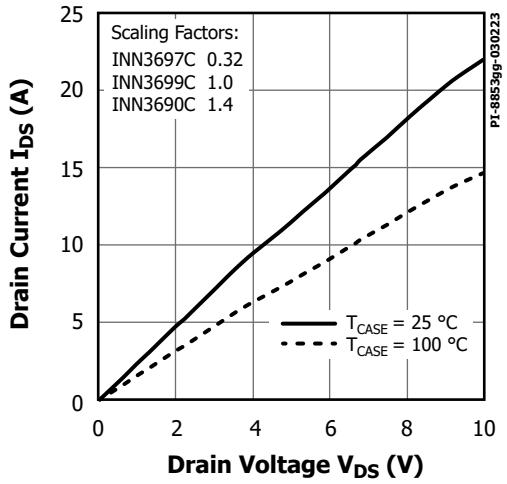


Figure 40. Output Characteristics.

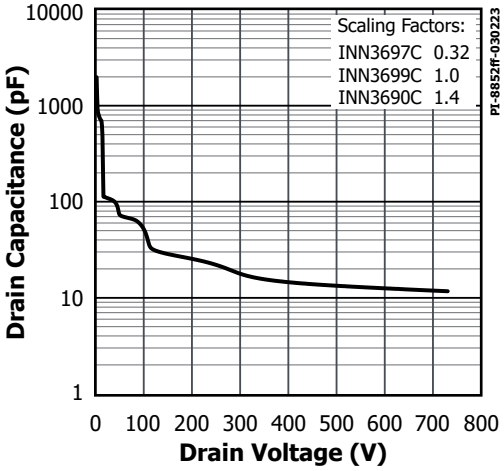


Figure 41. C_{OSS} vs. Drain Voltage.

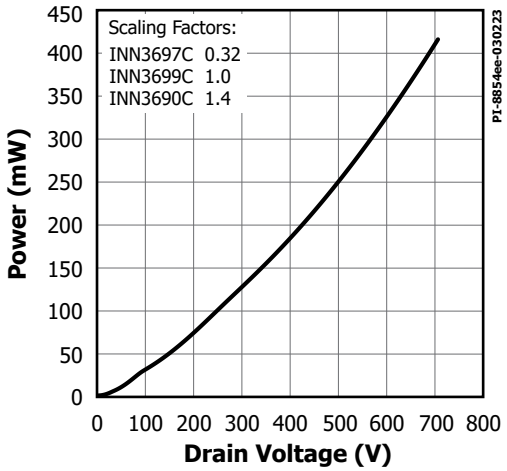


Figure 42. Drain Capacitance Power.

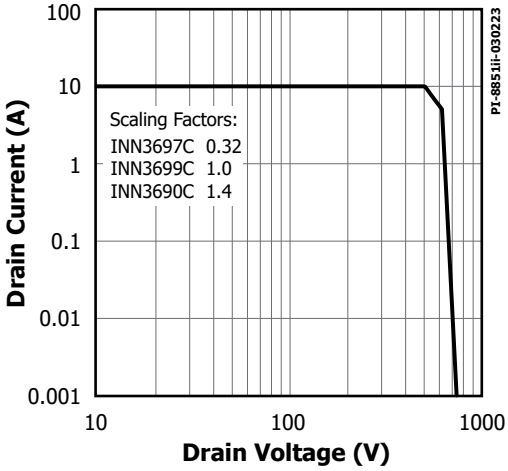


Figure 43. Maximum Allowable Drain Current vs. Drain Voltage (PowiGaN Devices INN3697C / INN3699C / INN3690C).

Typical Performance Curves

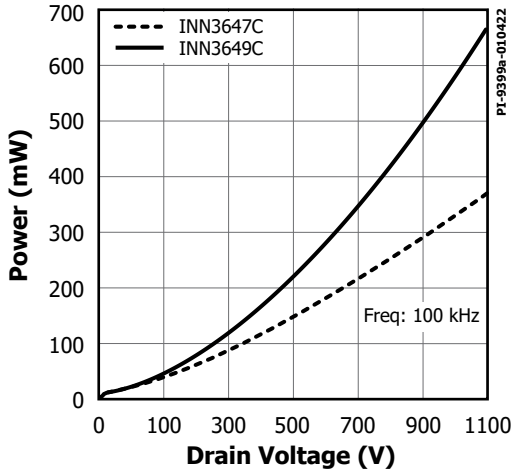


Figure 44. Drain Capacitance Power.

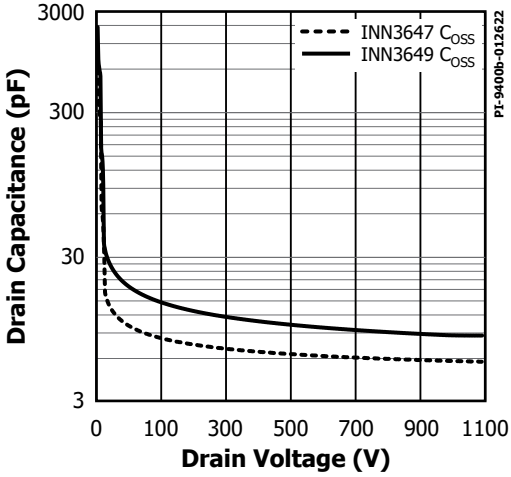


Figure 45. C_{OSS} vs. Drain Voltage.

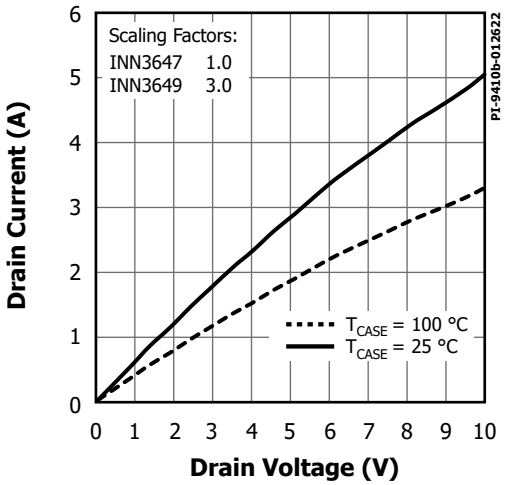


Figure 46. Output Characteristics.

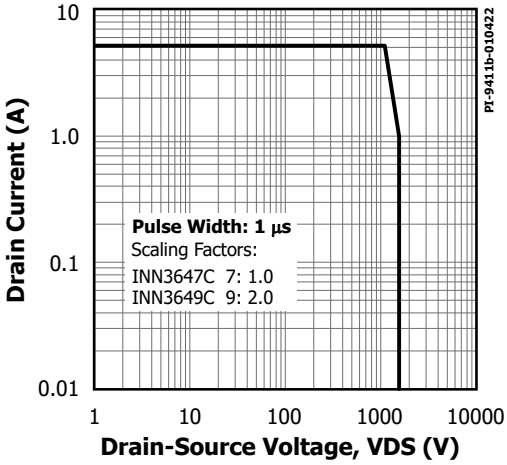
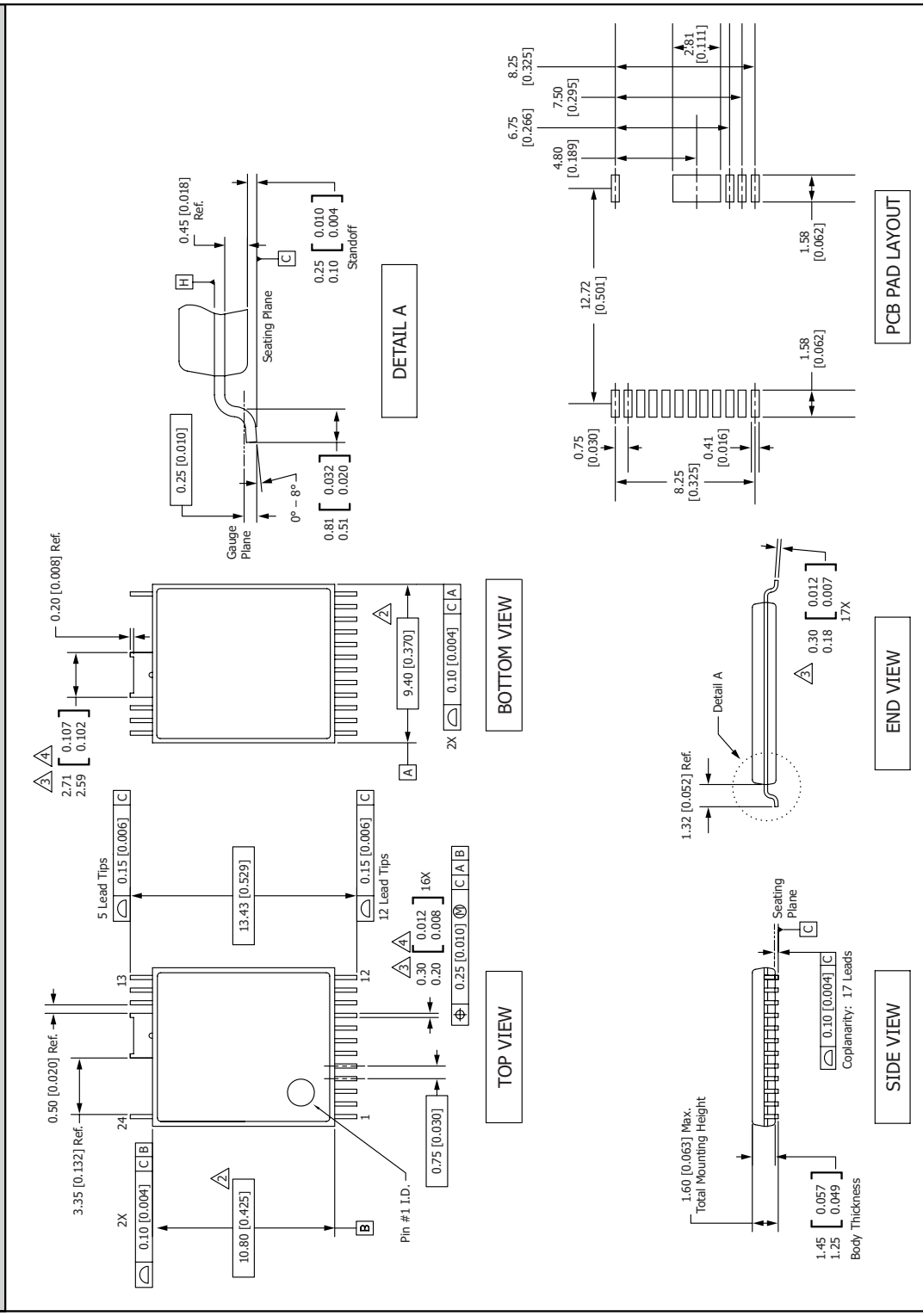


Figure 47. Maximum Allowable Drain Current vs. Drain Voltage.

InSOP-24D



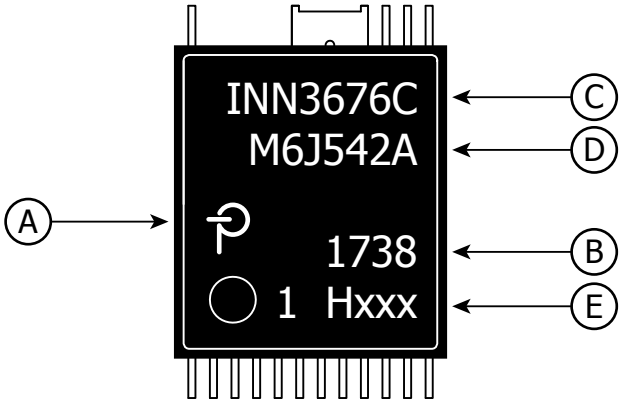
Notes:

1. Dimensioning and Tolerancing per ASME Y14.5M – 1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.18 [0.007] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in millimeters [inches].
6. Datums A & B to be determined at Datum H.

PI-8106-052620
POD-InSOP-24D Rev B

PACKAGE MARKING

InSOP-24D



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code
E. Test Sublot and Feature Code

PI-8727-050418

Parameter	Conditions	Rating	Units
Ratings for UL1577			
Primary-Side Current Rating	Current from pin (16-19) to pin 24	1.5	A
Primary-Side Power Rating	T_{AMB} = 25 °C (Device mounted in socket resulting in T_{CASE} = 120 °C)	1.35	W
Secondary-Side Power Rating	T_{AMB} = 25 °C (Device mounted in socket)	0.125	W

Parameter	Symbol	Conditions		Rating	Units
Package Characteristics					
Clearance	CLR			11.4	mm (min)
Creepage	CPG			11.4	mm (min)
Distance Through Insulation	DTI			0.4	mm
Comparative Tracking Index	CTI			>600	V
Isolation Resistance, Input to Output	R_{IO}	V_{IO} = 500 V, T_J = 25 °C (See Note 1)		10^{12}	Ω (min)
		V_{IO} = 500 V, 100 °C ≤ T_J ≤ 125 °C (See Note 1)		10^{11}	
Isolation Capacitance, Input to Output	C_{IO}	(See Note 1)		1	pF
Package Insulation Characteristics (See Note 2)					
Maximum RMS Working Isolation Voltage	$V_{IORM(RMS)}$	INN3672C to INN3677C		512	V_{RMS} (max)
		INN3678C to INN3670C		530	
		INN3692C to INN3690C		636	
Maximum Repetitive Peak Isolation Voltage	$V_{IORM(PK)}$	INN3672C to INN3277C		725	V_{PK} (max)
		INN3678C to INN3670C		750	
		INN3692C to INN3690C		900	
		INN3647C to INN3649C		1700	
Maximum Transient Peak Isolation Voltage	V_{IOTM}	Test Voltage = V_{IOTM}, t = 60 s (Qualification)	INN367xC	6.6	kV_{PK} (max)
			INN369xC	6.6	
		t = 1 s (100% Production)	INN367xC	8	
			INN369xC	8	
Maximum Surge Isolation Voltage	V_{IOSM}	Surge Test 1.2/50 usec Table 2 IEC 60747-17	INN367xC	10.4	kV_{PK} (max)
			INN369xC	10.4	
Input to Output Test Peak Voltage	V_{PD}	Method A, After Environmental Tests Subgroup 1, VPD = 1.6 × V_{IORM}, t = 10 s (qualification) Partial Discharge < 5 pC	INN3672C to INN3677C	1160	V_{PEAK}(min)
			INN3678C to INN3670C	1200	
			INN3692C to INN3690C	140	
		Method A, After Input / Output Safety Test Subgroup 2/3, V_{PD} = 1.2 × V_{IORM}, t = 10 s, (qualification) Partial Discharge < 5 pC	INN3672C to INN3677C	870	
			INN3678C to INN3670C	900	
			INN3692C to INN3690C	1080	
		Method B1, 100% Production Test, V_{PD} = 1.875 × V_{IORM}, t = 1 s Partial Discharge < 5 pC	INN3672C to INN3677C	1360	
			INN3678C to INN3670C	1406	
			INN3692C to INN3690C	1688	
			INN3647C to INN3649C	3188	
Insulation Resistance	R_S	V_{IO} = 500 V at T_J = 150 ºC		>10^9	Ω
Climatic Category				40/125/21	

Parameter	Conditions	Specifications
IEC 60664-1 Rating Table		
Basic Isolation Group	Material Group	I
Insulation Classification	Rated Mains RMS voltage ≤ 150 V	I - IV
	Rated Mains RMS voltage ≤ 300 V	I - IV
	Rated Mains RMS voltage ≤ 600V	I - IV
	Rated Mains RMS voltage ≤ 1000 V	I - III

Note 1: All pins on each side of the barrier tied together creating a two-terminal device
Note 2: VDE 0884-17 (IEC/EN 60747-17) Only applies to devices with following H-Codes: -H608, -H609, -H610, -H611 and –H612
Note 3: VDE 0884-17 certification is pending for INN3697C, INN3699C, INN3690C and INN364xC devices.

Feature Code Table[1]

Features	H601[2]	H602[2]	H605[3]	H606
Feedback Resistors	External	External	External	External
I_S Sense Resistor	External	External	External	External
I_{LIM} Selectable	Yes	Yes	Yes	Yes
Primary Fault Response	Auto-Restart	Auto-Restart	Auto-Restart	Auto-Restart
Secondary Fault Response	Auto-Restart	Auto-Restart	Auto-Restart	Auto-Restart
Auto-Restart	$V_{FB(AR)}$ = 90% x V_{FB}	$V_{FB(AR)}$ = Overload	$V_{FB(AR)}$ = 90% × V_{FB}	$V_{FB(AR)}$ = Overload
Over-Temperature Protection	Hysteretic	Hysteretic	Hysteretic	Hysteretic
Line OV/UV	Enabled	Enabled	OV Disabled UV Enabled	Enabled
UV Timer	t_{UV-} = 35 ms (Typ)	t_{UV-} = 35 ms (Typ)	t_{UV-} = 35 ms (Typ)	t_{UV-} = 35 ms (Typ)
Secondary Switch/Diode Short-Circuit Protection	Enabled	Enabled	Disabled	Disabled
Integrated V_{OUT} OVP	Enabled	Enabled	Enabled	Enabled
Peak Power Delivery	No	Yes	No	Yes

[1]For the latest updates, please visit www.power.com InnoSwitch Family page to Build Your Own InnoSwitch.
[2]Available only on INN3672C – INN3677C.
[3]Available only on INN3674C – INN3677C and PowiGaN devices.

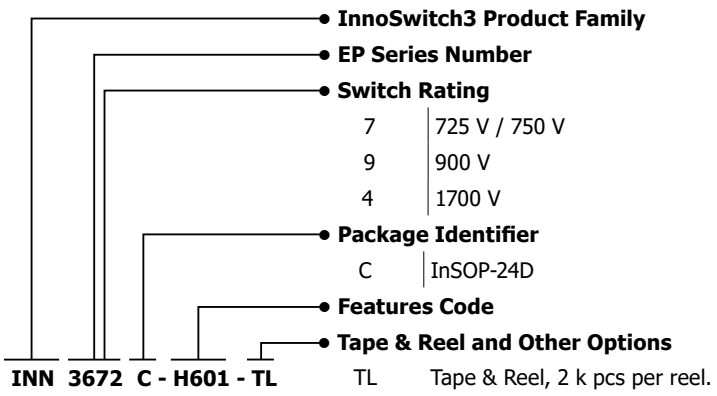
MSL Table

Part Number	MSL Rating
INN36xxC	3

ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	JESD78D	> ±100 mA or > 1.5 × V_{MAX} on all pins
Human Body Model ESD	ANSI/ESDA/JEDEC JS-001-2014	> ±2000 V on all pins
Charge Device Model ESD	ANSI/ESDA/JEDEC JS-002-2014	> ±500 V on all pins

Part Ordering Information



Revision	Notes	Date
A	Preliminary release.	02/17
B	Introduction release.	05/17
C	Production release.	09/17
D	Added InSOP-24D package marking and made minor text edits.	06/18
D	Updated Full Safety and Regulatory Compliance section on page 1 and added CTI to the parameter table.	08/18
E	Added INN369x series.	04/19
F	Updated page 1 Advanced Protection / Safety Features section.	06/19
G	Added GaN-based INN3679C and INN3670C parts. Updated I_{DSS1} and I_{DSS2} parameters.	08/19
H	Added 'PowiGaN' trademark name.	09/19
I	PCN-19281 – Updated Figure 17. Updated parameters: $V_{BPP(H)}$, I_{UV-}, $I_{OV(H)}$, I_{OV-}, V_V, $t_{SS(RAMP)}$, $I_{SR(PU)}$, t_R, t_F, R_{PU}, V_{SR} and $I_{BPS(SD)}$.	10/19
J	Added INN3678C part for introduction release.	11/19
K	Production release. Added new application design example.	02/20
L	Updated I_{DSS1} parameter to read V_{DS} = 80% Peak Drain Voltage.	03/20
M	Updated safety information on page 1 and corrected typo in Package drawing on page 33.	06/20
N	Update Package Characteristics Table and VDE 0884-11 device list.	07/21
O	Updated Package Characteristics Table and VDE-0884-17 device list.	09/21
P	Production release of 1700 V part numbers.	06/22
Q	Updated I_{UV+}, I_{UV-}, I_{OV+} and $I_{OV(H}$) parameters.	09/22
R	Updated isolation voltage on page 1. Updated V_{IOTM} and deleted V_{ISO} parameters.	11/22
S	Introduction release of INN3697C, INN3699C, INN3690C part numbers.	03/23

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