3A, 18V, 650kHz, ACOT™ Synchronous Step-Down Converter

General Description

The RT6259A/B are high-performance 650kHz 3A step-down regulators with internal power switches and synchronous rectifiers. They feature quick transient response using their Advanced Constant On-Time (ACOT™) control architecture that provides stable operation with small ceramic output capacitors and without complicated external compensation, among other benefits. The input voltage range is from 4.5V to 18V and the output is adjustable from 0.765V to 7V.

The proprietary ACOT™ control improves upon other fast-response constant on-time architectures, achieving nearly constant switching frequency over line, load, and output voltage ranges. Since there is no internal clock, response to transients is nearly instantaneous and inductor current can ramp quickly to maintain output regulation without large bulk output capacitance. The RT6259A/B are stable with and optimized for ceramic output capacitors.

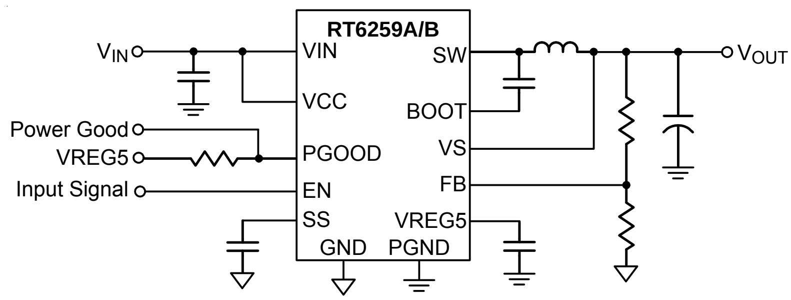
With internal 70mΩ switches and 70mΩ synchronous rectifiers, the RT6259A/B display excellent efficiency and good behavior across a range of applications, especially for low output voltages and low duty cycles. Cycle-by-cycle current limit, input under-voltage lockout, externally-adjustable soft-start, output under- and over-voltage protection, and thermal shutdown provide safe and smooth operation in all operating conditions.

The RT6259A and RT6259B are each available in the WQFN-16L 3x3 package, with exposed thermal pads. The RT6259B switches continuously even at light loads to avoid low-frequency interference while the RT6259A features a power-saving discontinuous operating mode at light loads.

Features

- **Fast Transient Response**
- **Steady 650kHz Switching Frequency At all Load Current (RT6259B)**
- **Discontinuous Operating Mode at Light Load (RT6259A)**
- **3A Output Current**
- **Advanced Constant On-Time (ACOT™) Control**
- **Optimized for Ceramic Output Capacitors**
- **4.5V to 18V Input Voltage Range**
- **Internal 70mΩ Switch and 70mΩ Synchronous Rectifier**
- **0.765V to 7V Adjustable Output Voltage**
- **Externally-adjustable, Pre-biased Compatible Soft-Start**
- **Cycle-by-Cycle Current Limit**
- **Optional Output Discharge Function**
- **Output Over- and Under-voltage Shut Down**
- **Latched (RT6259ALGQW/RT6259BLGQW Only)**
- **With Hiccup Mode (RT6259AHGQW/RT6259BHGQW Only)**
- **Input Under-Voltage Lockout**
- **Thermal Shutdown**
- **RoHS Compliant and Halogen Free**

Simplified Application Circuit

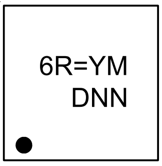


Applications

- Industrial and Commercial Low Power Systems
- Computer Peripherals
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation for High-Performance DSPs, FPGAs, and ASICs

Marking Information

RT6259AHGQW



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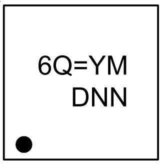
RT6259ALGQW



6Q= : Product Code
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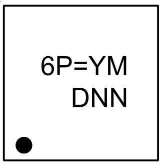
RT6259BHGQW



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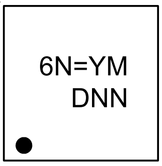
RT6259BLGQW



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Ordering Information

RT6259A/B□□□

Package Type
QW : WQFN-16L 3x3 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

H : Hiccup Mode OVP & UVP
L : Latched OVP & UVP

A : PSM
B : PWM

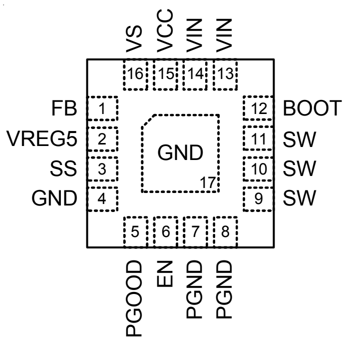
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configurations

(TOP VIEW)

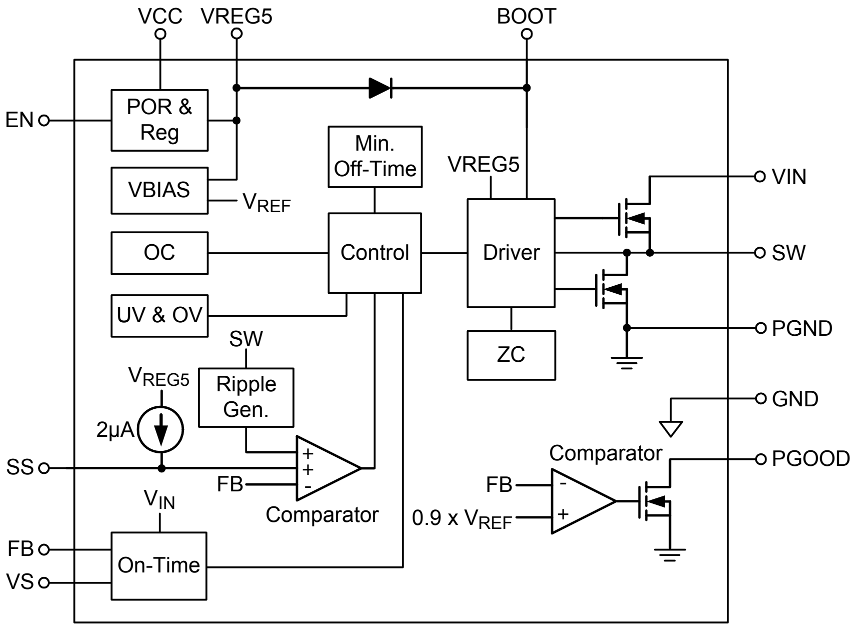


WQFN-16L 3x3

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	FB	Feedback Voltage Input. Connect FB to the midpoint of the external feedback resistive divider to sense the output voltage. Place the resistive divider within 5mm from the FB pin. The IC regulates V_{FB} at 0.765V (typical).
2	VREG5	Internal Regulator Output. Connect a 1μF capacitor to GND to stabilize output voltage.
3	SS	Soft-Start Control. Connect an external capacitor between this pin and GND to set the soft-start time.
4	GND	Ground.
5	PGOOD	Open-Drain Power-good Output. PGOOD connects to PGND whenever VFB is less than 90% of its regulation threshold (typical).
6	EN	Enable Control Input. A logic-high enables the converter; a logic-low forces the IC into shutdown mode reducing the supply current to less than 10μA.
7, 8, 17 (Exposed pad)	PGND	Power Ground. PGND connects to the Source of the internal N-channel MOSFET synchronous rectifier and to other power ground nodes of the IC. The exposed pad and the 2 PGND pins should be well soldered to the input and output capacitors and to a large PCB area for good power dissipation.
9, 10, 11	SW	Switch Node. SW is the Source of the internal N-channel MOSFET switch and the Drain of the internal N-channel MOSFET synchronous rectifier. Connect SW to the inductor with a wide short PCB trace and minimize its area to reduce EMI.
12	BOOT	Bootstrap Supply for High-Side Gate Driver. Connect a 0.1μF capacitor between BOOT and SW to power the internal gate driver.
13, 14	VIN	Power Input. The input voltage range is from 4.5V to 18V. Must bypass with a suitably large (≥10μF x 2) ceramic capacitors at this pin.
15	VCC	Internal Linear Regulator Supply Input. VCC supplies power for the internal linear regulator that powers the IC. Connect VIN to the input voltage and bypass to ground with a 0.1μF ceramic capacitor.
16	VS	Output Voltage Sense Input.

Function Block Diagram



Detailed Description

The RT6259A/B are high-performance 650kHz 3A step-down regulators with internal power switches and synchronous rectifiers. They feature an Advanced Constant On-Time (ACOT^{TM}) control architecture that provides stable operation with ceramic output capacitors without complicated external compensation, among other benefits. The input voltage range is from 4.5V to 18V and the output is adjustable from 0.765V to 7V.

The proprietary ACOT^{TM} control scheme improves upon other constant on-time architectures, achieving nearly constant switching frequency over line, load, and output voltage ranges. The RT6259A/B are optimized for ceramic output capacitors. Since there is no internal clock, response to transients is nearly instantaneous and inductor current can ramp quickly to maintain output regulation without large bulk output capacitance.

Constant On-Time (COT) Control

The heart of any COT architecture is the on-time one-shot. Each on-time is a pre-determined "fixed" period that is triggered by a feedback comparator. This robust arrangement has high noise immunity and is ideal for low duty cycle applications. After the on-time one-shot period, there is a minimum off-time period before any further regulation decisions can be considered. This arrangement avoids the need to make any decisions during the noisy time periods just after switching events, when the switching node (SW) rises or falls. Because there is no fixed clock, the high-side switch can turn on almost immediately after load transients and further switching pulses can ramp the inductor current higher to meet load requirements with minimal delays.

Traditional current mode or voltage mode control schemes typically must monitor the feedback voltage, current signals (also for current limit), and internal ramps and compensation signals, to determine when to turn off the high-side switch and turn on the synchronous rectifier. Weighing these small signals in a switching environment is difficult to do just after switching large currents, making those architectures problematic at low duty cycles and in less than ideal board layouts.

Because no switching decisions are made during noisy time periods, COT architectures are preferable in low duty cycle and noisy applications. However, traditional COT control schemes suffer from some disadvantages that preclude their use in many cases. Many applications require a known switching frequency range to avoid interference with other sensitive circuitry. True constant on-time control, where the on-time is actually fixed, exhibits variable switching frequency. In a step-down converter, the duty factor is proportional to the output voltage and inversely proportional to the input voltage. Therefore, if the on-time is fixed, the off-time (and therefore the frequency) must change in response to changes in input or output voltage.

Modern pseudo-fixed frequency COT architectures greatly improve COT by making the one-shot on-time proportional to V_{OUT} and inversely proportional to V_{IN}. In this way, an on-time is chosen as approximately what it would be for an ideal fixed-frequency PWM in similar input/output voltage conditions. The result is a big improvement but the switching frequency still varies considerably over line and load due to losses in the switches and inductor and other parasitic effects.

Another problem with many COT architectures is their dependence on adequate ESR in the output capacitor, making it difficult to use highly-desirable, small, low-cost, but low-ESR ceramic capacitors. Most COT architectures use AC current information from the output capacitor, generated by the inductor current passing through the ESR, to function in a way like a current mode control system. With ceramic capacitors, the inductor current information is too small to keep the control loop stable, like a current mode system with no current information.

ACOT^{TM} Control Architecture

Making the on-time proportional to V_{OUT} and inversely proportional to V_{IN} is not sufficient to achieve good constant-frequency behavior for several reasons. First, voltage drops across the MOSFET switches and inductor cause the effective input voltage to be less than the measured input voltage and the effective output voltage to be greater than the measured output voltage. As the load changes, the switch voltage drops change causing a switching frequency variation with load current. Also, at light loads if the inductor current goes negative, the switch dead-time between the synchronous rectifier turn-off and the high-side switch turn-on allows the switching node to rise to the input voltage. This increases the effective on-time and causes the switching frequency to drop noticeably.

One way to reduce these effects is to measure the actual switching frequency and compare it to the desired range. This has the added benefit eliminating the need to sense the actual output voltage, potentially saving one pin connection. ACOT^{TM} uses this method, measuring the actual switching frequency (at SW) and modifying the on-time with a feedback loop to keep the average switching frequency in the desired range.

To achieve good stability with low-ESR ceramic capacitors, ACOT^{TM} uses a virtual inductor current ramp generated inside the IC. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

ACOT^{TM} One-shot Operation

The RT6259A/B control algorithm is simple to understand. The feedback voltage, with the virtual inductor current ramp added, is compared to the reference voltage. When the combined signal is less than the reference the on-time one-shot is triggered, as long as the minimum off-time one-shot is clear and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching time and allow the feedback voltage and current sense signals to settle. The minimum off-time is kept short (260ns typical) so that rapidly-repeated on-times can raise the inductor current quickly when needed.

Discontinuous Operating Mode (RT6259A Only)

After soft-start, the RT6259B operates in fixed frequency mode to minimize interference and noise problems. The RT6259A uses variable-frequency discontinuous switching at light loads to improve efficiency. During discontinuous switching, the on-time is immediately increased to add "hysteresis" to discourage the IC from switching back to continuous switching unless the load increases substantially.

The IC returns to continuous switching as soon as an on-time is generated before the inductor current reaches zero. The on-time is reduced back to the length needed for 650kHz switching and encouraging the circuit to remain in continuous conduction, preventing repetitive mode transitions between continuous switching and discontinuous switching.

Current Limit

The RT6259A/B current limit is a cycle-by-cycle "valley" type, measuring the inductor current through the synchronous rectifier during the off-time while the inductor current ramps down. The current is determined by measuring the voltage between Source and Drain of the synchronous rectifier, adding temperature compensation for greater accuracy. If the current exceeds the upper current limit, the on-time one-shot is inhibited until the inductor current ramps down below the upper current limit plus a wide hysteresis band of about 1A until it drops below the lower current limit level. Thus, only when the inductor current is well below the upper current limit is another on-time permitted. This arrangement prevents the average output current from greatly exceeding the guaranteed upper current limit value, as typically occurs with other valley-type current limits. If the output current exceeds the available inductor current (controlled by the current limit mechanism), the output voltage will drop. If it drops below the output under-voltage protection level (see next section) the IC will stop switching to avoid excessive heat.

The RT6259B also includes a negative current limit to protect the IC against sinking excessive current and possibly damaging the IC. If the voltage across the synchronous rectifier indicates the negative current is too high, the synchronous rectifier turns off until after the next high-side on-time. The RT6259A does not sink current and therefore does not need a negative current limit.

Hiccup Mode

The RT6259AHGQW/ RT6259BHGQW, use hiccup mode OVP and UVP. When the protection function is triggered, the IC will shut down for a period of time and then attempt to recover automatically. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the overload or short circuit is removed. During hiccup mode, the shutdown time is determined by the capacitor at SS. A 0.5μA current source discharges V_{SS} from its starting voltage (normally VREG5). The IC remains shut down until V_{SS} reaches 0.2V, about 38ms for a 3.9nF capacitor. At that point the IC begins to charge the SS capacitor at 2μA, and a normal start-up occurs. If the fault remains, OVP and UVP protection will be enabled when V_{SS} reaches 2.2V (typical). The IC will then shut down and discharge the SS capacitor from the 2.2V level, taking about 16ms for a 3.9nF SS capacitor.

Latch-Off Mode

The RT6259ALGQW/ RT6259BLGQW, uses latch-off mode OVP and UVP. When the protection function is triggered, the IC will shut down. The IC stops switching, leaving both switches open, and is latched off. To restart operation, toggle EN or power the IC off and then on again.

Input Under-Voltage Lockout

In addition to the enable function, the RT6259A/B feature an under-voltage lockout (UVLO) function that monitors the internal linear regulator output (VREG5). To prevent operation without fully-enhanced internal MOSFET switches, this function inhibits switching when VREG5 drops below the UVLO-falling threshold. The IC resumes switching when VREG5 exceeds the UVLO-rising threshold.

Shut-down, Start-up and Enable (EN)

The enable input (EN) has a logic-low level of 0.4V. When V_{EN} is below this level the IC enters shutdown mode and supply current drops to less than 10μA. When V_{EN} exceeds its logic-high level of 2V the IC is fully operational.

EN is a high voltage input that can be safely connected to VIN (up to 18V) for automatic start-up.

Soft-Start (SS)

The RT6259A/B soft-start uses an external pin (SS) to clamp the output voltage and allow it to slowly rise. After V_{EN} is high and VREG5 exceeds its UVLO threshold, the IC begins to source 2μA from the SS pin. An external capacitor at SS is used to adjust the soft-start timing. The available capacitance range is from 2.7nF to 220nF. Do not leave SS unconnected.

During start-up, while the SS capacitor charges, the RT6259A/B operates in discontinuous mode with very small pulses. This prevents negative inductor currents and keeps the circuit from sinking current. Therefore, the output voltage may be pre-biased to some positive level before start-up. Once the V_{SS} ramp charges enough to raise the internal reference above the feedback voltage, switching will begin and the output voltage will smoothly rise from the pre-biased level to its regulated level. After V_{SS} rises above about 2.2V output over-and under-voltage protections are enabled and the RT6259B begins continuous-switching operation.

An internal linear regulator (VREG5) produces a 5.1V supply from VIN that powers the internal gate drivers, PWM logic, reference, analog circuitry, and other blocks. If VIN is 6V or greater, VREG5 is guaranteed to provide significant power for external loads.

PGOOD Comparator

PGOOD is an open-drain output controlled by a comparator connected to the feedback signal. If FB exceeds 90% of the internal reference voltage, PGOOD will be high impedance. Otherwise, the PGOOD output is connected to PGND.

External Bootstrap Capacitor

Connect a 0.1μF low ESR ceramic capacitor between BOOT and SW. This bootstrap capacitor provides the gate driver supply voltage for the high side N-channel MOSFET switch.

Over-Temperature Protection

The RT6259A/B includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 20°C the IC will resume normal operation with a complete soft-start. For continuous operation, provide adequate cooling so that the junction temperature does not exceed 150°C.

Output Discharge Control

When EN pin is low, the RT6259A/B will discharge the output with an internal 50Ω MOSFET connected between VS to GND pin.

OVP/UVP Protection

The RT6259A/B detects over- and under-voltage conditions by monitoring the feedback voltage on FB pin. The two functions are enabled after approximately 1.7 times the soft-start time. When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator will go high to turn off both internal high-side and low-side MOSFETs. When the feedback voltage is lower than 70% of the target voltage for 250μs, the UVP comparator will go high to turn off both internal high-side and low-side MOSFETs.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VIN, VCC ---------- −0.3V to 20V
- Switch Voltage, SW ---------- −0.3V to (V_{IN} + 0.3V)
  < 10ns ---------- −5V to 25V
- BOOT to SW ---------- −0.3V to 6V
- VREG5 to VIN or VCC ---------- −17V to 0.3V
- EN, VS Pin ---------- −0.3V to 20V
- Other Pins ---------- −0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-16L 3x3 ---------- 2.1W
- Package Thermal Resistance (Note 2)
  WQFN-16L 3x3, θ_{JA} ---------- 47.4°C/W
  WQFN-16L 3x3, θ_{JC} ---------- 7.5°C/W
- Junction Temperature Range ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- −65°C to 150°C

Recommended Operating Conditions (Note 3)

- Supply Voltage, VIN ---------- 4.5V to 18V
- Junction Temperature Range ---------- −40°C to 125°C
- Ambient Temperature Range ---------- −40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current							
Shutdown Current		I_{SHDN}	V_{EN} = 0V	--	1	10	μA
Quiescent Current		I_Q	V_{EN} = 5V, V_{FB} = 0.8V	--	1	1.3	mA
Logic Threshold							
EN Input Voltage	Logic-High			2	--	18	V
	Logic-Low			--	--	0.4	
V_{FB} Voltage and Discharge Resistance							
Feedback Threshold Voltage		V_{FB}		0.757	0.765	0.773	V
Feedback Input Current		I_{FB}	V_{FB} = 0.8V	--	0.01	0.1	μA
VOUT Discharge Resistance		R_{DIS}	V_{EN} = 0V, V_S = 0.5V	--	50	100	Ω
V_{REG5} Output							
V_{REG5} Output Voltage		V_{REG5}	6V ≤ V_{IN} ≤ 18V, 0 < I_{VREG5} < 5mA	4.8	5.1	5.4	V
Line Regulation			6V ≤ V_{IN} ≤ 18V, I_{VREG5} = 5mA	--	--	20	mV
Load Regulation			0 < I_{VREG5} < 5mA	--	--	100	mV
Output Current		I_{VREG5}	V_{IN} = 6V, V_{REG5} = 4V	--	70	--	mA

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
$R_{DS(ON)}$							
Switch On Resistance	High-Side	$R_{DS(ON)\_H}$	$(V_{BOOT} - V_{SW}) = 5.5V$	--	70	--	mΩ
	Low-Side	$R_{DS(ON)\_L}$		--	70	--	
Current Limit							
Current Limit		I_{LIM}		4	5	6	A
Thermal Shutdown							
Thermal Shutdown Threshold		T_{SD}	Shutdown Temperature	--	150	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	20	--	
On-Time Timer Control							
On-Time		t_{ON}	V_{IN} = 12V, V_{OUT} = 1.05V	--	135	--	ns
Minimum Off-Time		$t_{OFF(MIN)}$	V_{FB} = 0.7V	--	260	310	ns
Soft-Start							
SS Charge Current			V_{SS} = 0V	1.4	2	2.6	μA
SS Discharge Current			V_{SS} = 0.5V (Latch Mode)	0.1	0.2	--	mA
			V_{SS} = 0.5V (Hiccup Mode)	--	0.5	--	μA
UVLO							
UVLO Threshold			Wake Up V_{REG5}	3.6	3.85	4.1	V
Hysteresis				0.13	0.35	0.47	
Power Good							
PGOOD Threshold			V_{FB} Rising	85	90	95	%
			V_{FB} Falling	--	85	--	
PGOOD Sink Current			PGOOD = 0.5V	2.5	5	--	mA
Output Under Voltage and Over Voltage Protection							
OVP Trip Threshold			OVP Detect	114	120	126	%
OVP Prop Delay				--	5	--	μs
UVP Trip Threshold				65	70	75	%
UVP Hysteresis				--	10	--	
UVP Prop Delay				--	250	--	μs
UVP Enable Delay		t_{UVPEN}	Relative to Soft-Start Time	--	t_{SS} x 1.7	--	ms

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

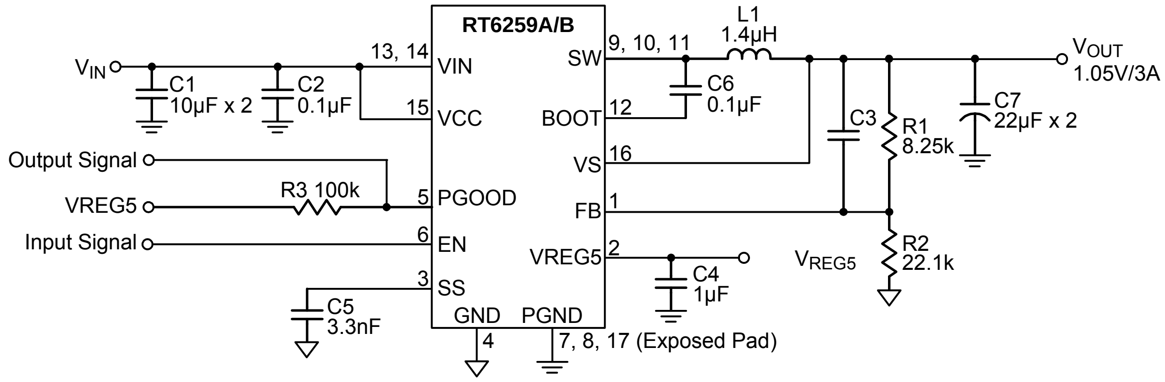
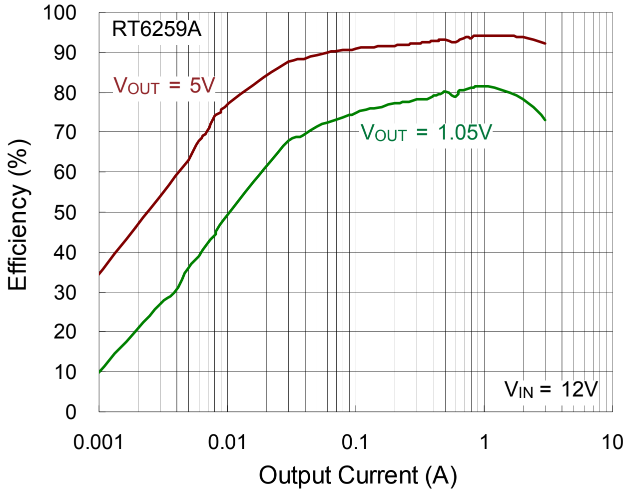


Table 1. Suggested Component Values (V_{IN} = 12V)

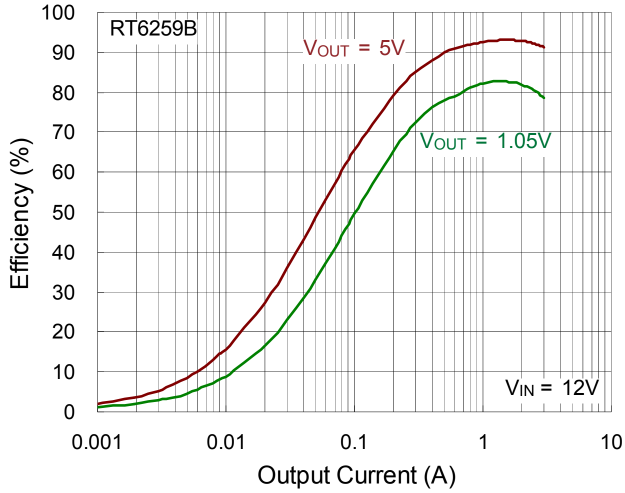
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C3 (pF)	L1 (μH)	C7 (μF)
1	6.81	22.1	--	1.4	22 to 68
1.05	8.25	22.1	--	1.4	22 to 68
1.2	12.7	22.1	--	1.4	22 to 68
1.8	30.1	22.1	5 to 22	2	22 to 68
2.5	49.9	22.1	5 to 22	2	22 to 68
3.3	73.2	22.1	5 to 22	2	22 to 68
5	124	22.1	5 to 22	3.3	22 to 68
7	180	22.1	5 to 22	3.3	22 to 68

Typical Operating Characteristics

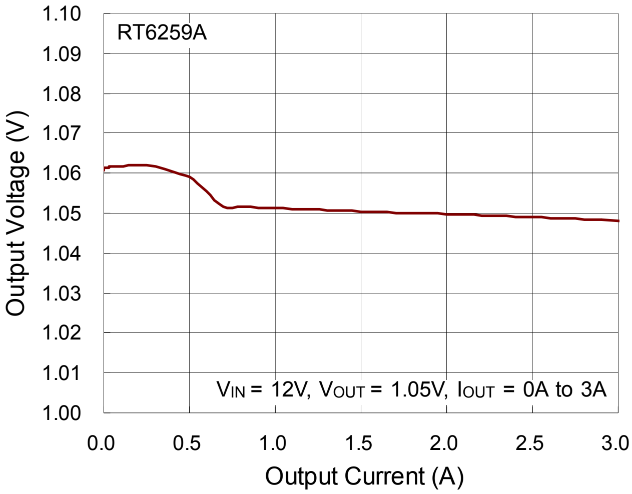
Efficiency vs. Output Current



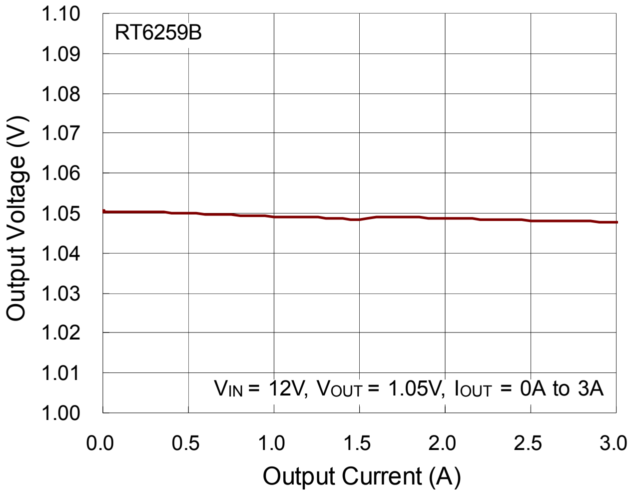
Efficiency vs. Output Current



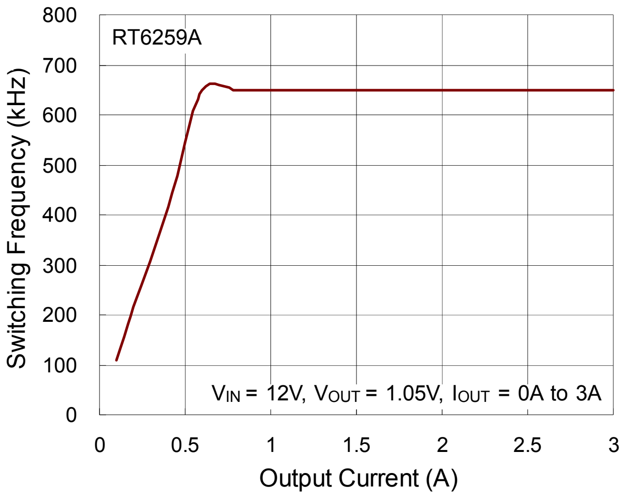
Output Voltage vs. Output Current



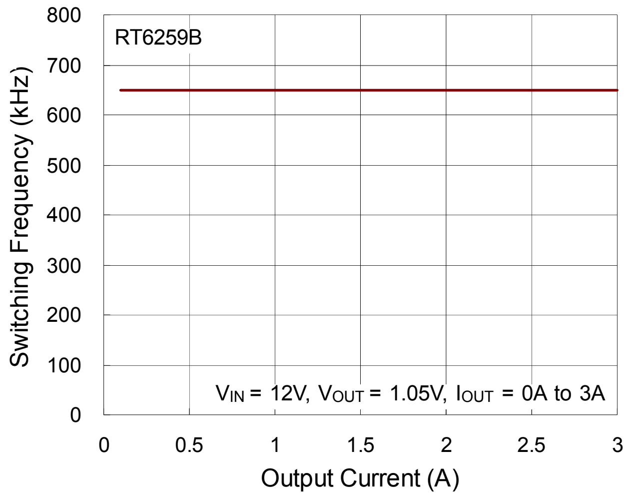
Output Voltage vs. Output Current



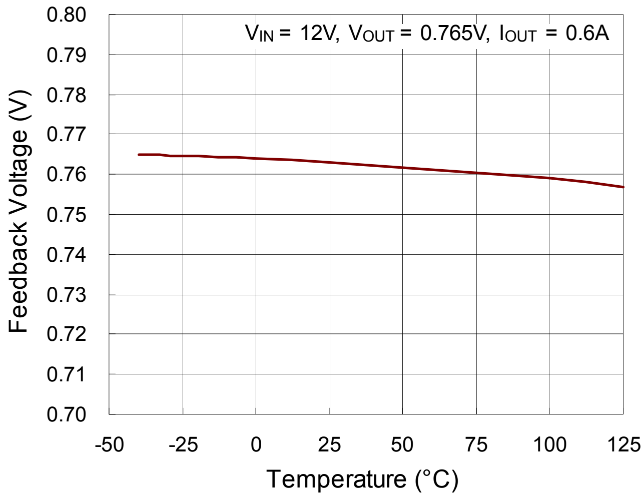
Switching Frequency vs. Output Current



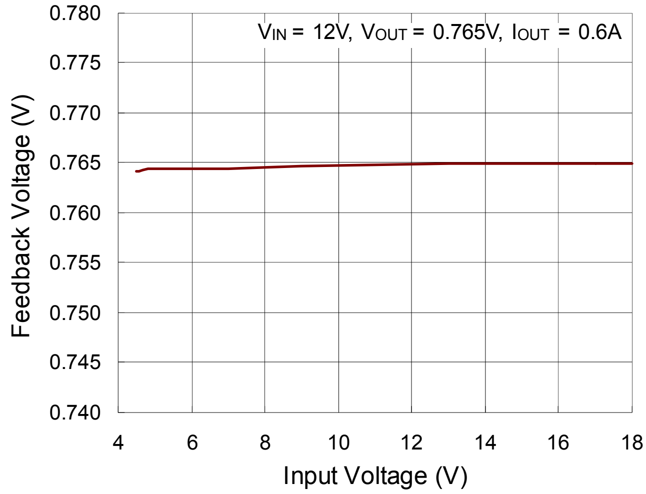
Switching Frequency vs. Output Current



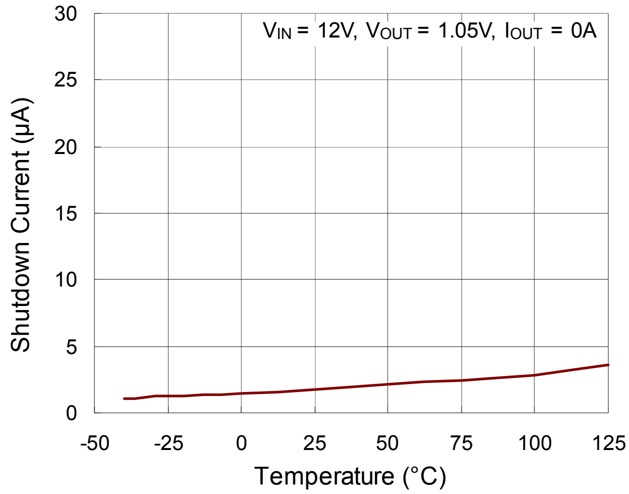
Feedback Voltage vs. Temperature



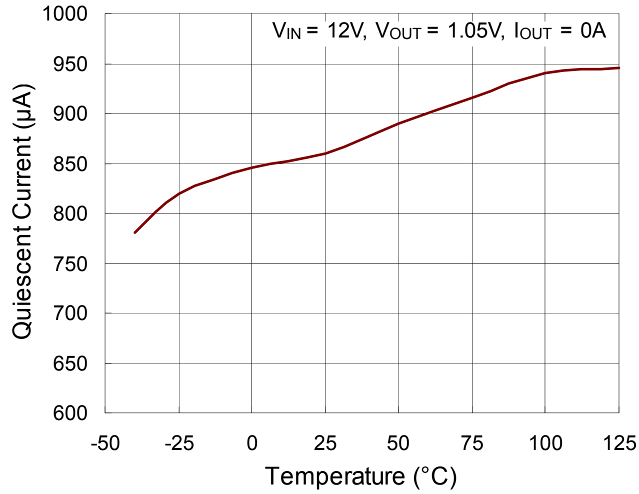
Feedback Voltage vs. Input Voltage



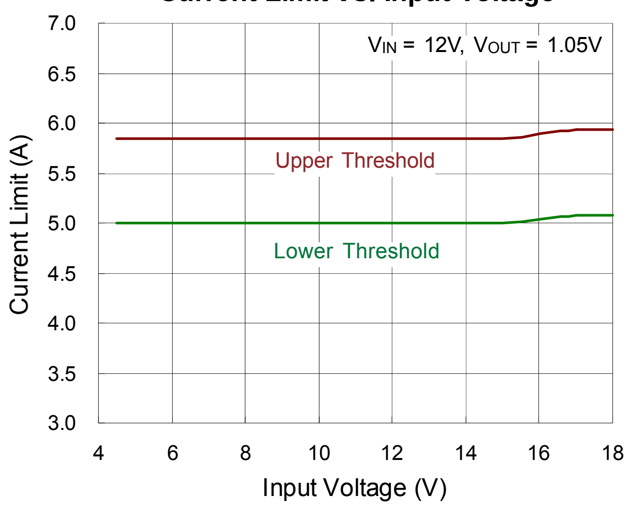
Shutdown Current vs. Temperature



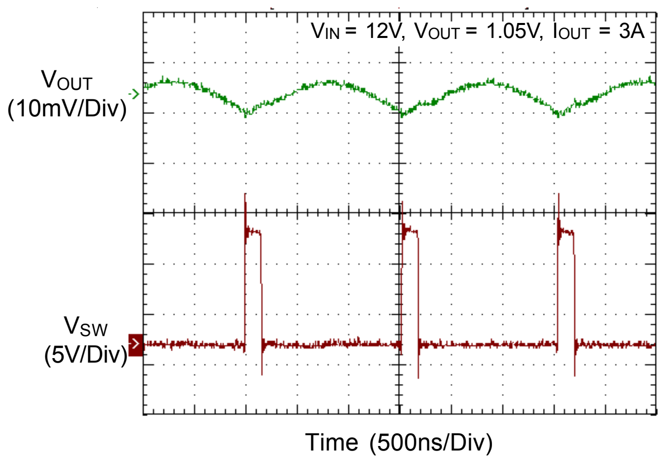
Quiescent Current vs. Temperature



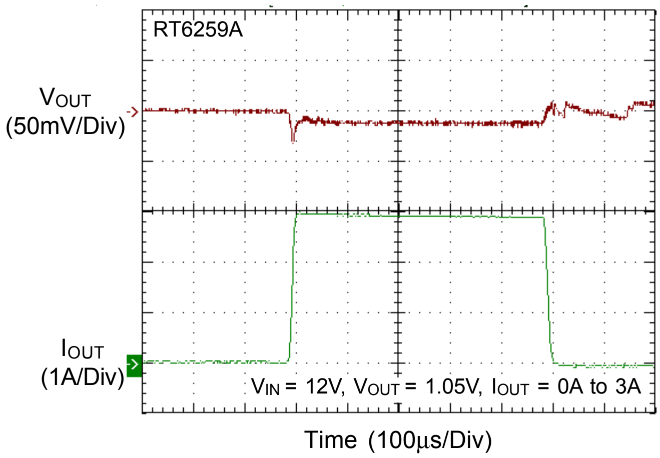
Current Limit vs. Input Voltage



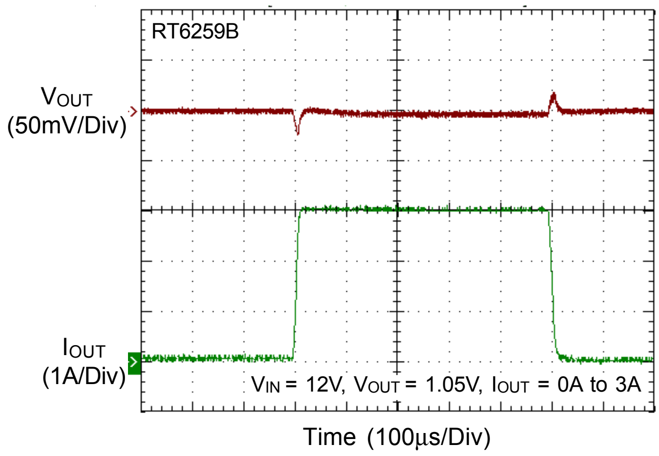
Output Ripple Voltage



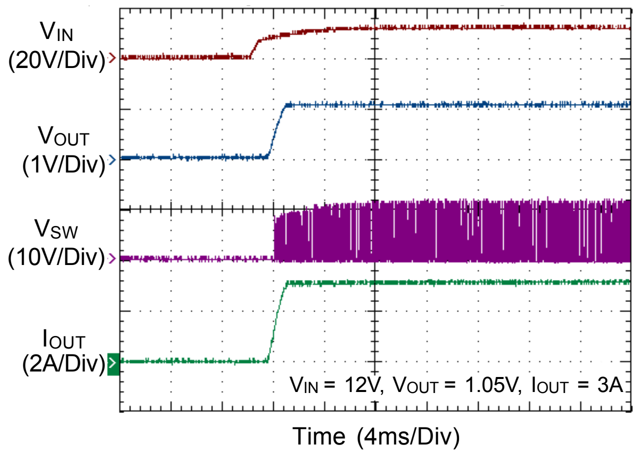
Load Transient Response



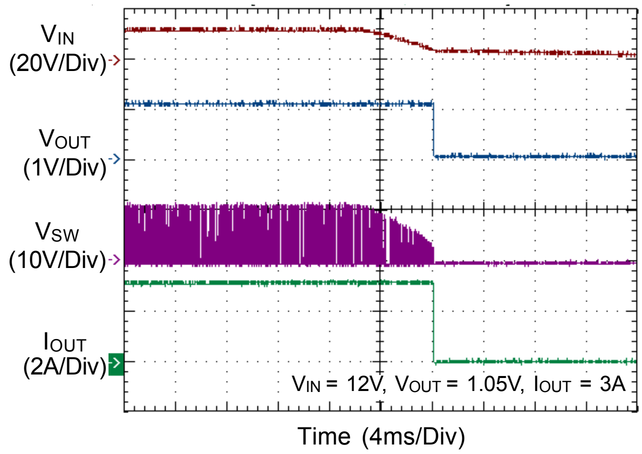
Load Transient Response



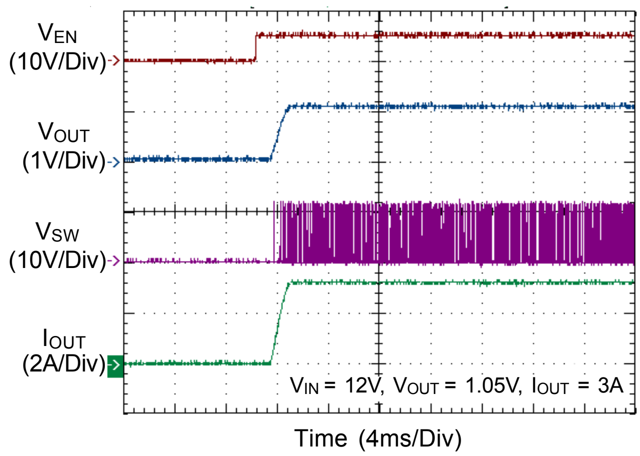
Power On from VIN



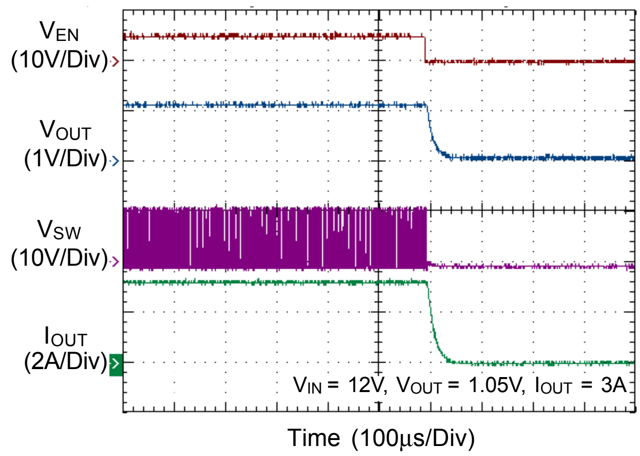
Power Off from VIN



Power On from EN



Power Off from EN



Applications Information

Soft-Start (SS)

The RT6259A/B soft-start uses an external capacitor at SS to adjust the soft-start timing according to the following equation :

$$t_{SS}(ms) = \frac{C_{SS}\ (nF) \times 0.765V}{I_{SS}\ (\mu A)}$$

The soft-start timing is the output voltage rising time from 0V to settled level and can be programmed by the external capacitor between the SS and GND pins. The available capacitance range is from 2.7nF to 220nF. If a 3.9nF capacitor is used, the typical soft-start will be 1.5ms. Do not leave SS unconnected.

Enable Operation (EN)

For automatic start-up the high-voltage EN pin can be connected to V_{IN}, either directly or through a 100kΩ resistor. Its large hysteresis band makes EN useful for simple delay and timing circuits. EN can be externally pulled to V_{IN} by adding a resistor-capacitor delay (R_{EN} and C_{EN} in Figure 1). Calculate the delay time using EN's internal threshold where switching operation begins (1.4V, typical).

An external MOSFET can be added to implement digital control of EN when no system voltage above 2V is available (Figure 2). In this case, a 100kΩ pull-up resistor, R_{EN}, is connected between VIN and the EN pin. MOSFET Q1 will be under logic control to pull down the EN pin. To prevent enabling circuit when VIN is smaller than the VOUT target value or some other desired voltage level, a resistive voltage divider can be placed between the input voltage and ground and connected to EN to create an additional input under-voltage lockout threshold (Figure 3).

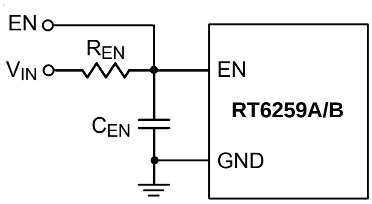


Figure 1. External Timing Control

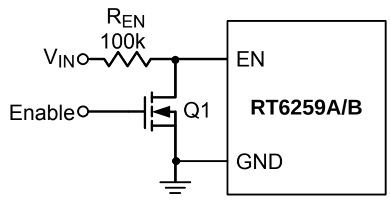


Figure 2. Digital Enable Control Circuit

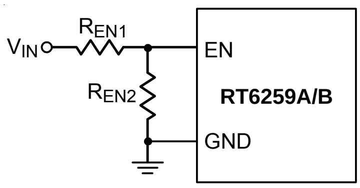


Figure 3. Resistor Divider for Lockout Threshold Setting

Output Voltage Setting

Set the desired output voltage using a resistive divider from the output to ground with the midpoint connected to FB. The output voltage is set according to the following equation :

$$V_{OUT} = 0.765 \times \left(1 + \frac{R1}{R2}\right)$$

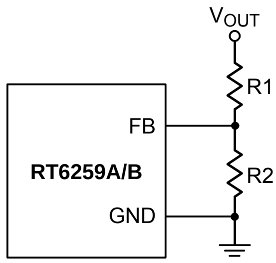


Figure 4. Output Voltage Setting

Place the FB resistors within 5mm of the FB pin. Choose R2 between 10kΩ and 100kΩ to minimize power consumption without excessive noise pick-up and calculate R1 as follows :

$$R1 = \frac{R2 \times (V_{OUT} - 0.765V)}{0.765V}$$

For output voltage accuracy, use divider resistors with 1% or better tolerance.

Under-Voltage Lockout Protection

The RT6259A/B feature an under-voltage lock-out (UVLO) function that monitors the internal linear regulator output (PVCC) and prevents operation if V_{PVCC} is too low. In some multiple input voltage applications, it may be desirable to use a power input that is too low to allow V_{PVCC} to exceed the UVLO threshold.

External BOOT Bootstrap Diode

When the input voltage is lower than 5.5V it is recommended to add an external bootstrap diode between VIN (or VINR) and the BOOT pin to improve enhancement of the internal MOSFET switch and improve efficiency. The bootstrap diode can be a low cost one such as 1N4148 or BAT54.

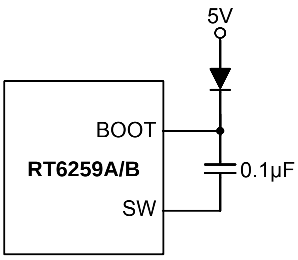


Figure 5. External Bootstrap Diode

External BOOT Capacitor Series Resistance

The internal power MOSFET switch gate driver is optimized to turn the switch on fast enough for low power loss and good efficiency, but also slow enough to reduce EMI. Switch turn-on is when most EMI occurs since V_{SW} rises rapidly. During switch turn-off, SW is discharged relatively slowly by the inductor current during the dead-time between high-side and low-side switch on-times.

In some cases it is desirable to reduce EMI further, at the expense of some additional power dissipation. The switch turn-on can be slowed by placing a small (<10Ω) resistance between BOOT and the external bootstrap capacitor. This will slow the high-side switch turn-on and V_{SW}'s rise. To remove the resistor from the capacitor charging path (avoiding poor enhancement due to under-charging the BOOT capacitor), use the external diode shown in figure 5 to charge the BOOT capacitor and place the resistance between BOOT and the capacitor/diode connection.

PVCC Capacitor Selection

Decouple PVCC to PGND with a 1μF ceramic capacitor. High grade dielectric (X7R, or X5R) ceramic capacitors are recommended for their stable temperature and bias voltage characteristics.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-16L 3x3 package, the thermal resistance, θ_{JA}, is 47.4°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (47.4°C/W) = 2.1W for WQFN-16L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

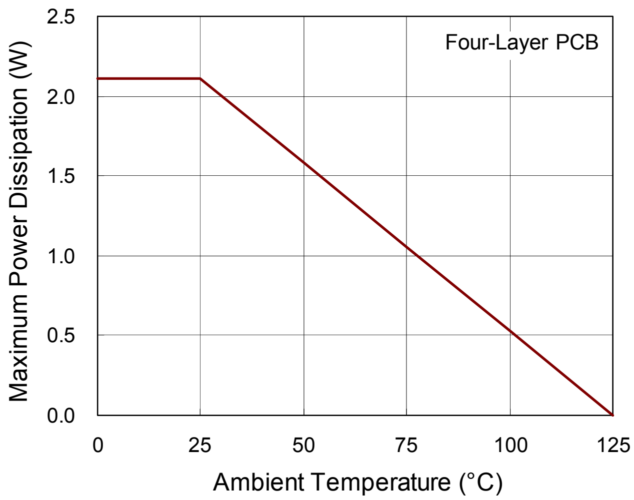


Figure 6. Derating Curve of Maximum Power Dissipation

Layout Considerations

Follow the PCB layout guidelines for optimal performance of the RT6259A/B.

- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and PGND).
- The high-frequency switching node (SW) has large voltage swings and fast edges and can easily radiate noise to adjacent components. Keep its area small to prevent excessive EMI, while providing wide copper traces to minimize parasitic resistance and inductance. Keep sensitive components away from the SW node or provide ground traces between for shielding, to prevent stray capacitive noise pickup.
- Connect the feedback network to the output capacitors rather than the inductor. Place the feedback components near the FB pin.
- The exposed pad, PGND, and GND should be connected to large copper areas for heat sinking and noise protection. Provide dedicated wide copper traces for the power path ground between the IC and the input and output capacitor grounds, rather than connecting each of these individually to an internal ground plane.
- Avoid using vias in the power path connections that have switched currents (from C_{IN} to PGND and C_{IN} to VIN) and the switching node (SW).

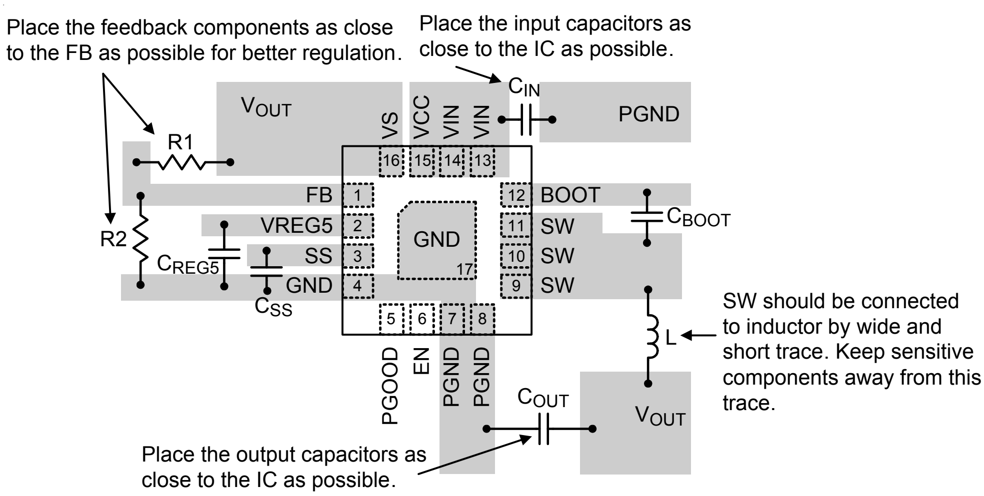
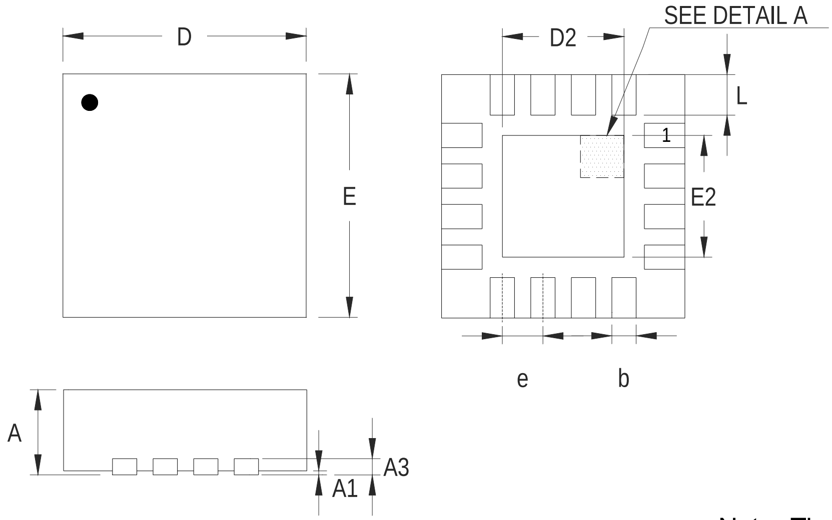
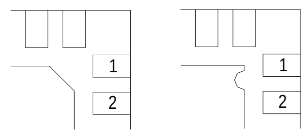


Figure 7. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 16L QFN 3x3 Package

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