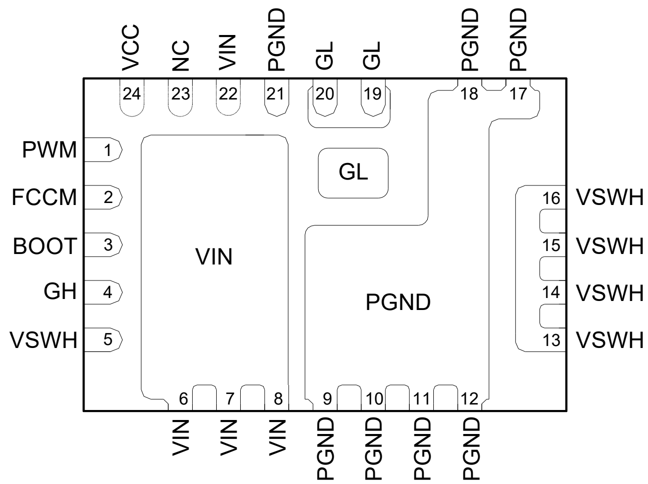
Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ5048QI	-40°C to +85°C	QFN3.5x5_24L	RoHS

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

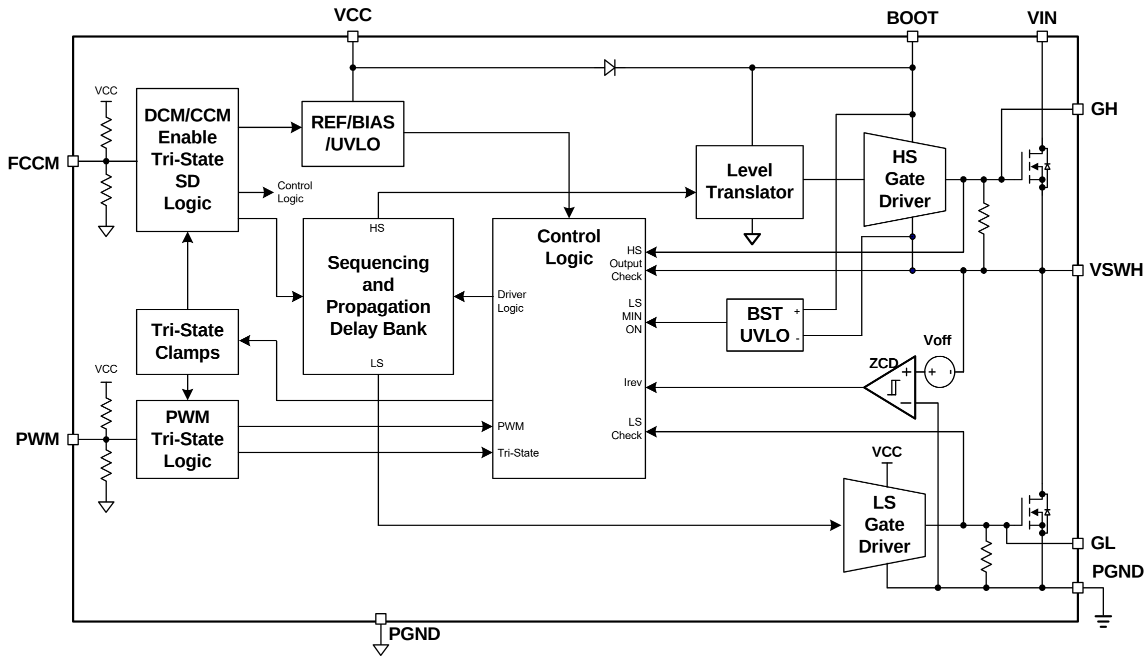


QFN3.5X5_24L
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	PWM	PWM input signal from the controller IC. This input is compatible with 5V and Tri-State logic levels.
2	FCCM	Continuous conduction mode of operation is allowed when FCCM = High. Discontinuous mode is allowed and diode emulation mode is active when FCCM = Low. High impedance on the input of FCCM will shutdown both High Side and Low Side MOSFETs.
3	BOOT	High Side MOSFET Gate Driver supply rail (5V with reference to VSWH). Connect a 100nF ceramic capacitor between BOOT and the VSWH (Pin 5).
4	GH	High Side MOSFET Gate connection. This is for test purposes.
5	VSWH	Switching node connected to the source of High Side MOSFET and the drain of Low Side MOSFET. This pin is dedicated for booststrap capacitor connection to BOOT pin. It is required to be connected to Pin 13 externally on PCB.
6, 7, 8	VIN	Power stage high voltage input pin.
9, 10, 11, 12, 17, 18	PGND	Power Ground pin for power stage.
13, 14, 15, 16	VSWH	Switching node connected to the source of High Side MOSFET and the drain of Low Side MOSFET. These pins are being used for Zero Cross Detect, Booststrap UVLO and Anti-Overlap Control.
19, 20	GL	Low Side MOSFET Gate connection. This is for test purposes.
21	PGND	Power Ground pin for Low Side MOSFET Gate Driver.
22	VIN	Power stage high voltage input pin.
23	NC	Connect to Pin 24
24	VCC	5V Power Pin for both the Bias Logic Blocks and HS and LS MOSFET Gate Driver Supply Rail. Add a 4.7µF MLCC directly between Vcc (Pin 24) and PGND (Pin 21).

Functional Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Low Voltage Supply (V_{CC})	-0.3V to 6V
High Voltage Supply (V_{IN})	-0.3V to 30V
Control Inputs (PWM, FCCM)	-0.3V to (V_{CC}+0.3V)
Bootstrap Voltage DC (BOOT-PGND)	-0.3V to 33V
Bootstrap Voltage DC (BOOT-VSWH)	-0.3V to 6V
BOOT Voltage Transient(1) (BOOT-VSWH)	-0.3V to 9V
Switch Node Voltage DC (VSWH)	-0.3V to 30V
Switch Node Voltage Transient(1) (VSWH)	-8V to 38V
High Side Gate Voltage DC (GH)	(VSWH-0.3V) to BOOT
High Side Gate Voltage Transient(1) (GH)	(VSWH-5V) to BOOT
Low Side Gate Voltage DC (GL)	(PGND-0.3V) to (V_{CC}+0.3V)
Low Side Gate Voltage Transient(1) (GL)	(PGND-2.5V) to (V_{CC}+0.3V)
Storage Temperature (T_S)	-65°C to +150°C
Max Junction Temperature (T_J)	150°C
ESD Rating(2)	2kV

Notes:

1. Peak voltages can be applied for 20ns per switching cycle.
2. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1kΩ in series with 100pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
High Voltage Supply (V_{IN})	4.5V to 25V
Low Voltage Supply {V_{CC}, (BOOT-VSWH)}	4.5V to 5.5V
Control Inputs (PWM, FCCM)	0V to (V_{CC}-0.3V)
Operating Frequency	200kHz to 2MHz

Electrical Characteristics(3)

T_A = 25°C, V_{IN} = 12V, V_{CC} = 5V unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IN}	Power Stage Power Supply		4.5		25	V
V_{CC}	Driver Power Supply	V_{CC} = 5V	4.5		5.5	V
$R_{\theta JC}$	Thermal Resistance	PCB Temp = 100°C		3		°C/W
$R_{\theta JA}$		AOS Demo Board		10		°C/W
INPUT SUPPLY AND UVLO						
V_{CC}	Under-Voltage Lockout	V_{CC} Rising		3.5	3.9	V
		V_{CC} Falling		3.1		V
V_{CC_HYST}	Under-Voltage Lockout Hysteresis			400		mV
I_{VCC_SD}	Shutdown Bias Supply Current	FCCM = Floating. VPWM = Floating (internally pulled down)		3	5	µA
I_{VCC}	Control Circuit Bias Current	FCCM = 5V, VPWM = Floating (internally clamped to 2.5V)		170		µA
		FCCM = 0V, VPWM = Floating (internally clamped to 2.5V)		180		µA
BOOTSTRAPPED DIODE						
V_F	Forward Voltage	Forward Current = 2mA		0.55		V
PWM INPUT						
V_{PWMH}	PWM Input High Threshold	V_{PWM} Rising, V_{CC} = 5V	4.1			V
V_{PWML}	PWM Input Low Threshold	V_{PWM} Falling, V_{CC} = 5V			0.7	V
I_{PWM}	PWM Pin Input Current	Source, V_{PWM} = 5V		+200		µA
		Sink, V_{PWM} = 0V		-200		µA
V_{TRI}	PWM Input Tri-State Threshold Window	PWM = High Impedance	1.5		3.3	V
FCCM INPUT						
V_{FCCMH}	FCCM Input High Threshold	FCCM Rising, V_{CC} = 5V Shutdown ⟶ CCM	3.9			V
V_{FCCML}	FCCM Input Low Threshold	FCCM Falling, V_{CC} = 5V Shutdown ⟶ DCM			1.2	V
I_{FCCM}	FCCM Pin Input Current	Source, FCCM = 5V		+50		µA
		Sink, FCCM = 0V		-50		µA
V_{TRI_HYST}	FCCM Input Threshold Hysteresis	Shutdown ⟶ CCM⟶ Shutdown DCM ⟶ Shutdown ⟶ DCM		200		mV
V_{TRI}	FCCM Input Tri-State Threshold Window	FCCM = High Impedance, Shutdown Operation	2.1		3.1	V
V_{TRI_CMLP}	Tri-State Open Voltage			2.5		V
t_{PS4_EXIT}	PS4 Exit Latency	V_{CC} = 5V		5	15	µs
GATE DRIVER TIMING						
t_{PDLU}	PWM Falling to GH Turn-Off	PWM 10%, GH 90%		30		ns
t_{PDLL}	PWM Raising to GL Turn-Off	PWM 90%, GL 90%		25		ns
t_{PDHU}	GL Falling to GH Rising Deadtime	GL 10%, GH 10%		15		ns
t_{PDHL}	GH/VSWH Falling to GL Rising Deadtime	VSWH @ 1V, GL 10%		13		ns
t_{TSSHD}	Tri-State Shutdown Delay	TS to GH Falling, TS to GL Falling		150		ns
t_{PTS}	Tri-State Propagation Delay	Tri-state exit, (see Figure 6)		45		ns
t_{LGMIN}	Low-Side Minimum On-Time	FCCM = 0V		350		ns

Note:

3. All voltages are specified with respect to the corresponding PGND pin.

Timing Diagram

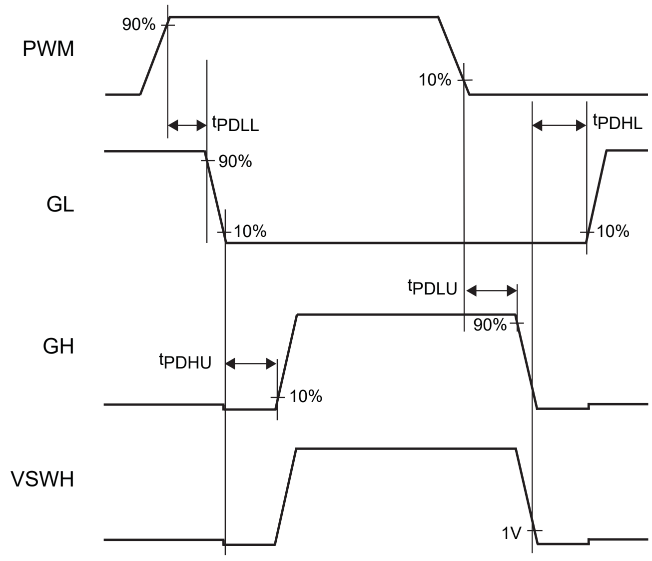


Figure 1. PWM Logic Input Timing Diagram

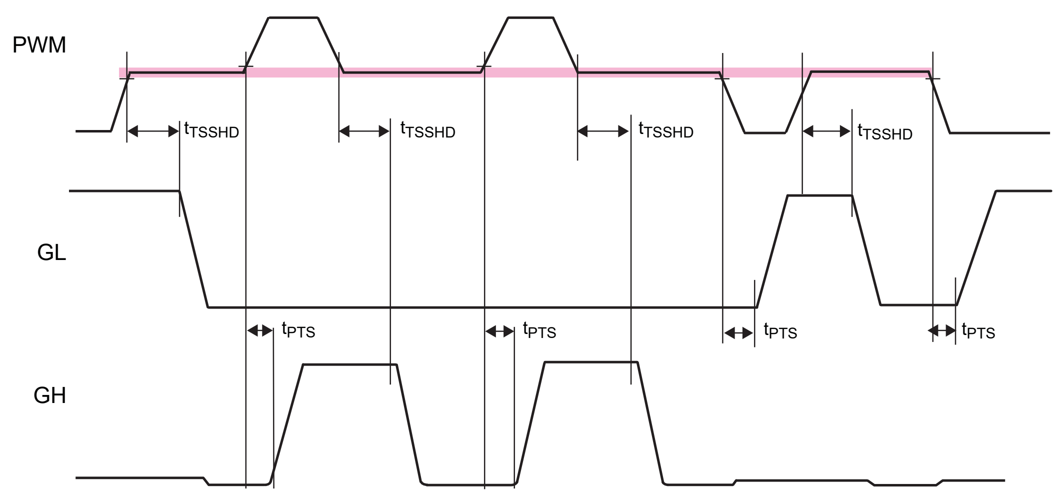


Figure 2. Tri-State Input Logic Timing Diagram

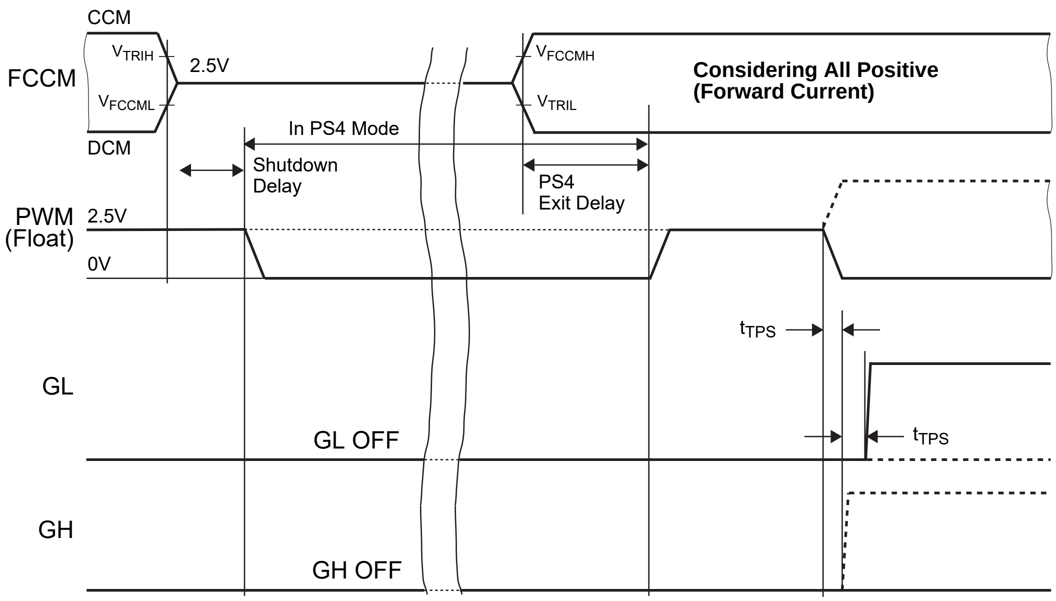


Figure 3. FCCM Logic during High Impedance at PWM Input

Typical Performance Characteristics

T_A = 25°C, V_{IN} = 12V, V_{CC} = 5V, unless otherwise specified.

Figure 4. Efficiency vs. Load Current

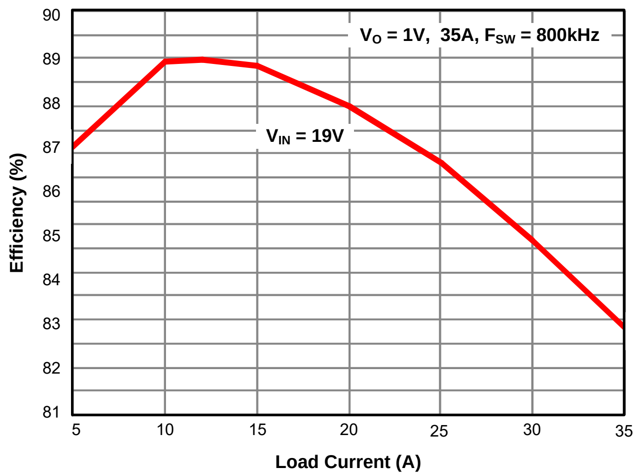


Figure 5. Power Loss vs. Load Current

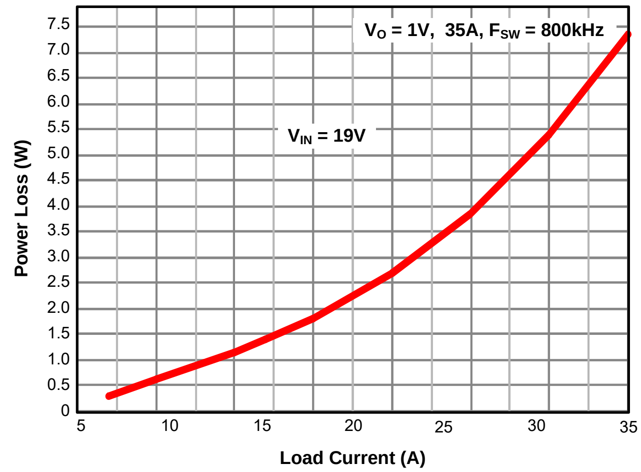


Figure 6. Supply Current vs. Switching Frequency

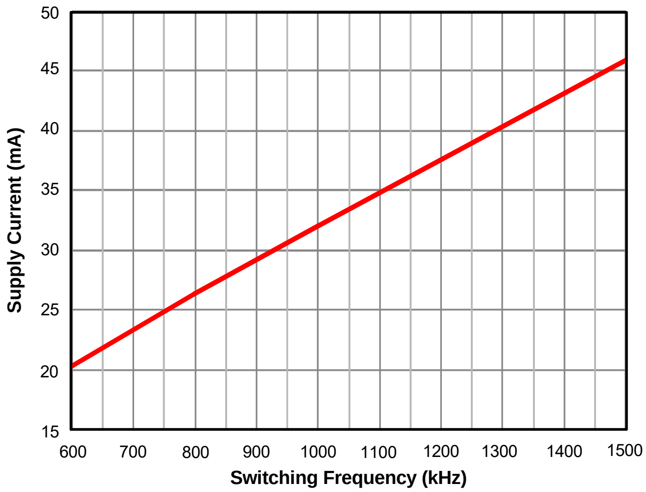


Figure 7. FCCM Input Threshold vs. Temperature

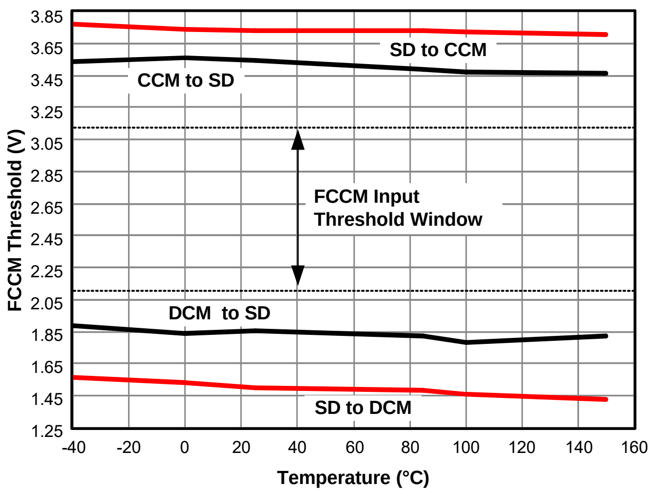


Figure 8. PWM Threshold vs. Temperature

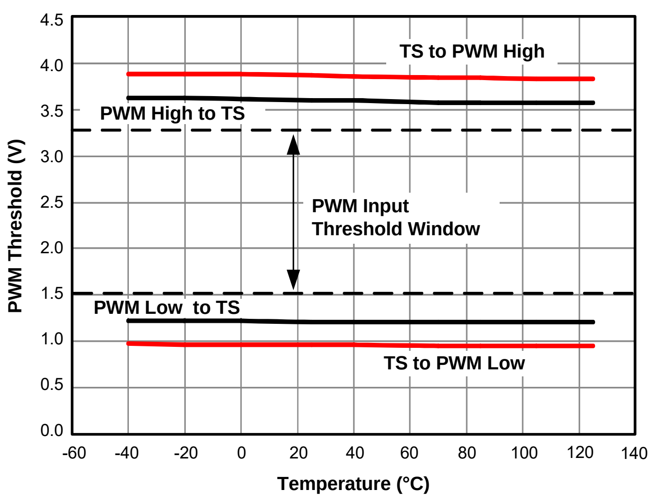
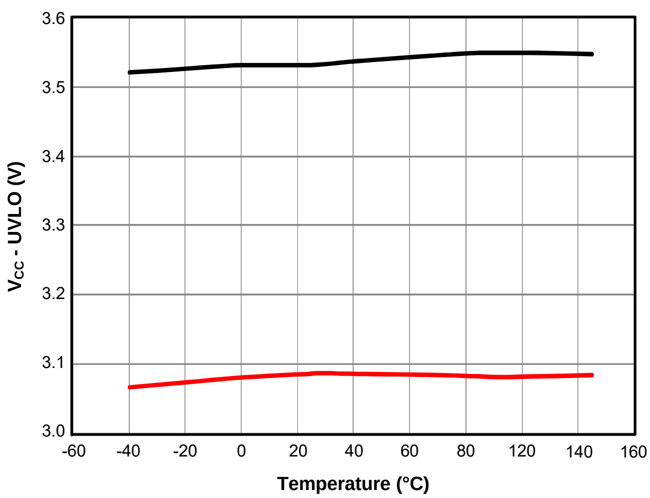


Figure 9. V_{CC} UVLO vs. Temperature



Typical Performance Characteristics

T_A = 25°C, V_{IN} = 12V, V_{CC} = 5V, unless otherwise specified.

Figure 10. V_{CC} Shutdown Current vs. Temperature

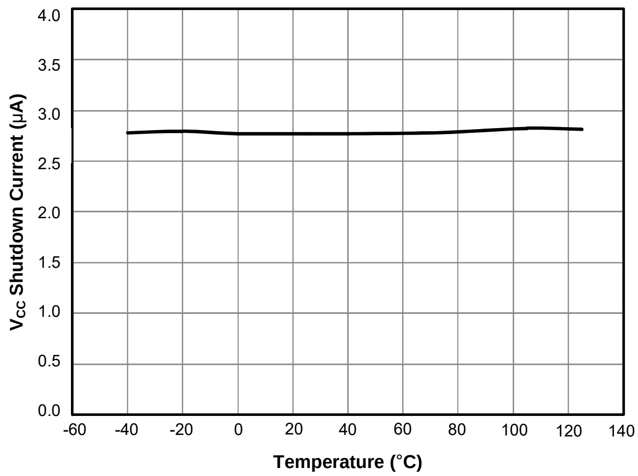
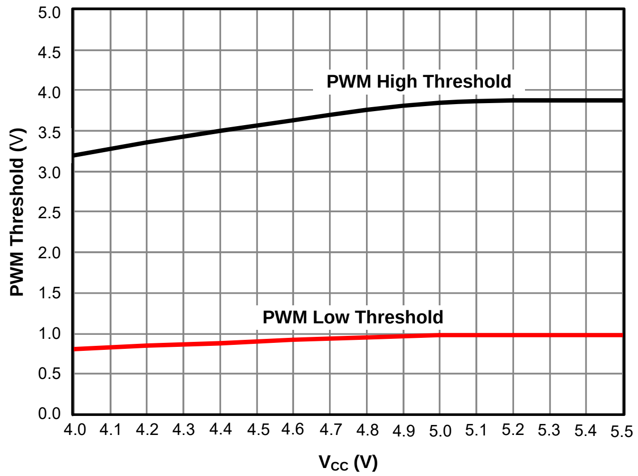


Figure 11. PWM Threshold vs. V_{CC}



Application Information

AOZ5048QI is a fully integrated power module designed to work over an input voltage range of 4.5V to 25V with a separate 5V supply for gate drive and internal control circuits. A number of desirable features make AOZ5048QI a highly versatile power module. The MOSFETs are individually optimized for efficient operation on either high side or low side switches in a low duty cycle synchronous buck converter. A high current driver is also integrated in the package which minimizes the gate drive loop and results in extremely fast switching The modules are fully compatible with Intel DrMOS specification IMVP8 in form fit and function.

Powering the Module and the Gate Drives

An external supply V_{CC} of 5V is required for driving the MOSFETs. The MOSFETs are designed with low gate thresholds so that lower drive voltage can be used to reduce the switching and drive losses without compromising the conduction losses. The integrated gate driver is capable of supplying large peak current into the Low Side MOSFET to achieve extremely fast switching. A ceramic bypass capacitor of 4.7µF or higher is recommended from V_{CC} to PGND. For effective filtering it is strongly recommended to directly connect this capacitor to PGND (pin 21).

The BOOT supply for driving the High Side MOSFET is generated by connecting a small capacitor (100nF) between BOOT pin and the switching node VSWH (Pin 5). It is recommended that this capacitor Cboot be connected as close as possible to the device across pins 3 and 5. Boost diode is integrated into the package. A resistor in series with Cboot can be optionally used by designers to slow down the turn on speed of the high side MOSFET. Typically, values between 1Ω to 5Ω is a compromise between the need to keep both the switching time and VSWH node spikes as low as possible.

Undervoltage Lockout

In a UVLO event, both GH and GL outputs are actively held low until adequate gate supply becomes available. The under-voltage lockout is set to 3.5V with a 400mV hysteresis. The AOZ5048QI must be powered up before the PWM input is applied.

Since the PWM control signals are provided typically from an external controller or a digital processor, extra care must be taken during start up. It should be ensured that PWM signal goes through a proper soft start sequence to minimize in-rush current through the converter during start up. Powering the module with a full duty cycle PWM signal may lead to a number of undesirable consequences as explained below. In general it should be noted that AOZ5048QI is a combination of two MOSFETs with an IMVP8 compliant driver, all of which are optimized for switching at the highest efficiency. Other than UVLO, it does not have any monitoring or protection functions built in. The PWM controller should be designed in to perform these functions under all possible operating and transient conditions.

Input Voltage V_{IN}

AOZ5048QI is rated to operate over a wide input range of 4.5V to 25V. As with any other synchronous buck converter, large pulse currents at high frequency and extremely high di/dt rates will be drawn by the module during normal operation. It is strongly recommended to bypass the input supply very close to package leads with X7R or X5R quality surface mount ceramic capacitors.

The high side MOSFET in AOZ5048QI is optimized for fast switching with low duty ratios. It has ultra low gate charges which have been achieved as a trade off with higher $R_{DS(ON)}$ value. When the module is operated at low V_{IN} the duty ratio will be higher and conduction losses in the HS MOSFET will also be correspondingly higher. This will be compensated to some extent by reduced switching losses. The total power loss in the module may appear to be low even though in reality the HS MOSFET losses may be disproportionately high. Since the two MOSFETs have their own exposed pads and PCB copper areas for heat dissipation, the HS MOSFET may be much hotter than the LS MOSFET. It is recommended that worst case junction temperature be measured and ensured to be within safe limits when the module is operated with high duty ratios.

PWM Input

AOZ5048QI is offered to interface with PWM logic compatible with 5V (TTL). Refer to Fig. 1 for the timing and propagation delays between the PWM input and the gate drives.

The PWM is also a tri-state compatible input. When the input is high impedance or unconnected both the gate drives will be off and the gates are held active low. The PWM Threshold Table in Table 1 lists the thresholds for high and low level transitions as well as tri-state operation. As shown in Fig. 2, there is a hold off delay between the corresponding gate drive is pulled low. This delay is typically 150ns and intended to prevent spurious triggering of the tri-state mode which may be caused either by noise induced glitches in the PWM waveform or slow rise and fall times.

Table 1. PWM Input and Tri-State Thresholds

Thresholds →	V_{PWMH}	V_{PWML}	V_{TRIH}	V_{TRIL}
AOZ5048QI	4.1 V	0.7 V	1.65 V	3.50 V

Note: See Figure 2 for propagation delays and tri-state window.

Diode Mode Emulation of Low Side MOSFET (FCCM)

AOZ5048QI can be operated in the diode emulation or skip mode using the FCCM pin. This is useful if the converter has to operate in asynchronous mode during start up, light load or under pre bias conditions. If FCCM is taken high, the controller will use the PWM signal as reference and generate both the high and low side complementary gate drive outputs with the minimal delays necessary to avoid cross conduction. When the pin is taken low the HS MOSFET drive is not affected but diode emulation mode is activated for the LS MOSFET. See Table 2 for a comprehensive view of all logic inputs and corresponding drive conditions. A high impedance state at the FCCM pin shuts down the AOZ5048QI.

Function of FCCM When Signal is Rising

FCCM = 0V

1. The power stage is enabled and in DCM (Discontinuous Conduction Mode).
2. GH and GL will follow PWM signal
3. Zero Current Detection (ZCD) is enabled. When VSWH = 4mV and MIN_ON expires, ZCD will trigger state machine to turn off GL. If VSWH reaches 4mV before than MIN_ON, MIN_ON time takes priority and will continue until this time period has completed.

FCCM = 0V to 2.1V

1. GH and GL will turn off after shutdown delay (2.5µs).

FCCM = Tri-State Window

1. Input to FCCM is high impedance.
2. An internal buffer clamps FCCM to 2.5V.
3. GH and GL remain Off and ignore PWM signal.

FCCM = Tri-State to 3.9V (Fast Ramping)

1. The power stage is in CCM (Continuous Conduction Mode)
2. GH and GL will follow PWM command
3. ZCD: is disabled

FCCM = 5V

1. The power stage is in CCM (Continuous Mode of Operation)
2. Zero Current Detection (ZCD) is disabled
3. GH and GL follow PWM signal:

   PWM = Logic Hi → GH = Hi, GL = Lo

   PWM = Logic Lo → GH = Lo, GL = Hi
4. No detection for direction of inductor current
5. No detection for Voltage Level at VSWH node

Function of FCCM When Signal is Falling

FCCM = 5V → 3.1V

1. Re-enter shutdown mode
2. Shutdown delay: 2.5µs
3. Occurs when Controller FCCM output enter high impedance state

FCCM = Tri-State Window
(Ramp down window is 3.1 to 1.2V)

1. FCCM will be internally clamped to 2.5V
2. Remains in Shutdown Mode

FCCM = Tri-State → 1.2V
(**250 to 300mV lower than the DCM → TS threshold**)

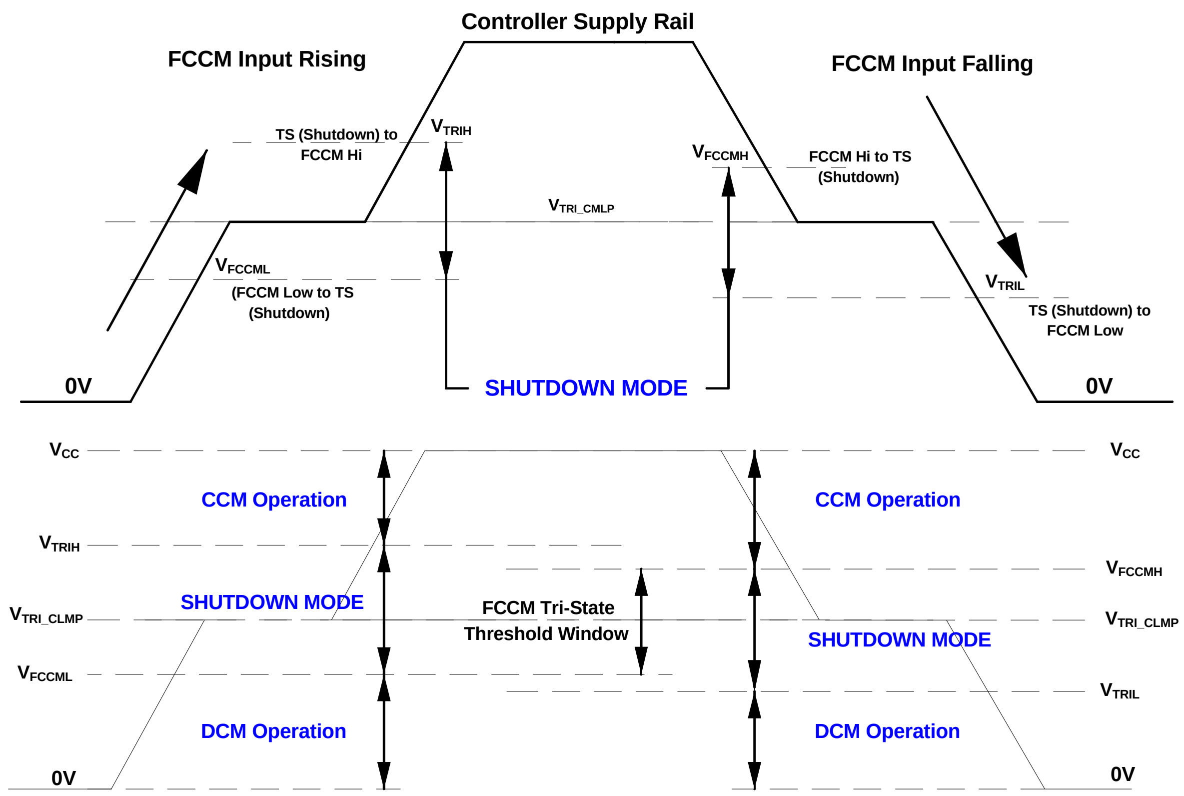
1. Re-enable power stage
2. Controller pulls down on FCCM pin exiting shutdown mode into DCM
3. Enable Delay: 5µs
4. Re-enable ZCD

Table 2. Control Logic Truth Table

FCCM	PWM	GH	GL
L	L	L	L (ZCD)
L	H	H	L
H	L	L	H
H	H	H	L
L	Tri-State	L	L
H	Tri-State	L	L
Tri-State	X	L	L

Note: Diode emulation mode is activated when FCCM pin is held low.

FCCM Timing Diagram and Truth Table



FCCM	ZCD	PWM	VSWH	GH	GL	Main Inductor Current Direction
0V	ON	L	<-4mV	L	L	Forward Current
0V		L	Equal -4mV	L	MinOn Time	VSWH= -(Rdson x $IL_{FORWARD}$)
0V		Tri-S	V_{OUT}	L	L	Don't Care
0V		H	V_{IN}	H	L	Forward Only
5V	OFF	L	X	L	H	Bi-Directional
5V		Tri-S	V_{OUT}	L	L	Forward (Body)
5V		H	V_{IN}	H	L	Bi-Directional
Tri-State		X	V_{OUT}	L	L	Don't Care

Figure 12. FCCM Timing Diagram and Truth Table

As the primary and secondary AC current loops move through V_{IN} to VSWH and through PGND to VSWH, large positive and negative voltage spike appear at the VSWH terminal which are caused by the large internal di/dts produced through the in package parastics. To minimize the effects of this interference, the VSWH terminal at which the main inductor L1 is mounted to, is sized just so the inductor can physically fit. The goal is to employ the least amount of copper area for this VSWH terminal just enough so the inductor can be securely mounted.

To minimize the effects of switching noise coupling to the rest of the sensitive areas of the PCB, the area directly underneath the designated VSWH copper plane on the top layer is voided and the shape of this void is replicated descending down through the rest of the layers as shown on Fig. 14 which is the bottom layer of the PCB as an example.

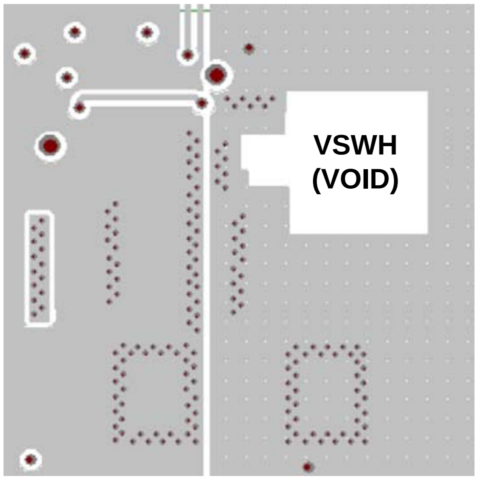


Figure 14. Bottom Layer PCB Layout with VSWH Copper Plane Voided on Descending Layers

The AOZ5048QI can be operated at a switching frequency of up to 1.5MHz. This implies that the inherent capacitive parameters of the High Side and Low Side MOSFETs need to be charged and discharge on each and every cycle. Due to the back and forth conduction of these AC currents flowing in and out of the Input Capacitors, the exposed pads (V_{IN} and PGND) would tend to heat up, hence requiring thermal venting.

Positioning vias through the landing pattern of the V_{IN} and PGND thermal pads will help quickly facilitate the thermal build up and spread the heat much more quickly towards the surrounding copper layers descending from the top layer.

The exposed pads dimensional footprint of the 3.5x5 QFN package is shown on Fig.13. For optimal thermal relief, it is recommended to fill the PGND and V_{IN} exposed landing pattern with 10mil diameter vias.

10mil diameter is a commonly used via diameter as it is optimally cost effective based on the tooling bit used in manufacturing. Each via is associated with a 20mil diameter keep out. Maintain a 5mil clearance (127um) around the inside edge of each exposed pad in an event of solder overflow, potentially shorting with the adjacent expose thermal pad.

Adding Vias Through Exposed Pads Landing Pattern

The AOZ5048QI can be operated at a switching frequency of up to 1.5MHz. This implies that the inherent capacitive parameters of the High Side and Low Side MOSFETs need to be charged and discharged on each and every cycle. Due to the back and forth conduction of these AC currents flowing in and out of the Input Capacitors, the exposed pads (V_{IN} and PGND) would tend to heat up, hence requiring thermal venting. Positioning vias through the landing pattern of the V_{IN} and PGND thermal pads will help quickly facilitate the thermal build up and spread the heat much more quickly towards the surrounding copper layers descending from the top layer.

The exposed pads dimensional footprint of the 3.5x5 QFN package is shown on Fig.15. For optimal thermal relief, it is recommended to fill the PGND and V_{IN} exposed landing pattern with 10mil diameter vias. 10mil via diameter is a commonly used, as it is optimally cost effective based on the tooling bit used in manufacturing. Each via is associated with a 20mil diameter keep out. Maintain a 5mil clearance (127um) around the inside edge of each exposed pad in an event of solder overflow, potentially shorting with the adjacent expose thermal pad.

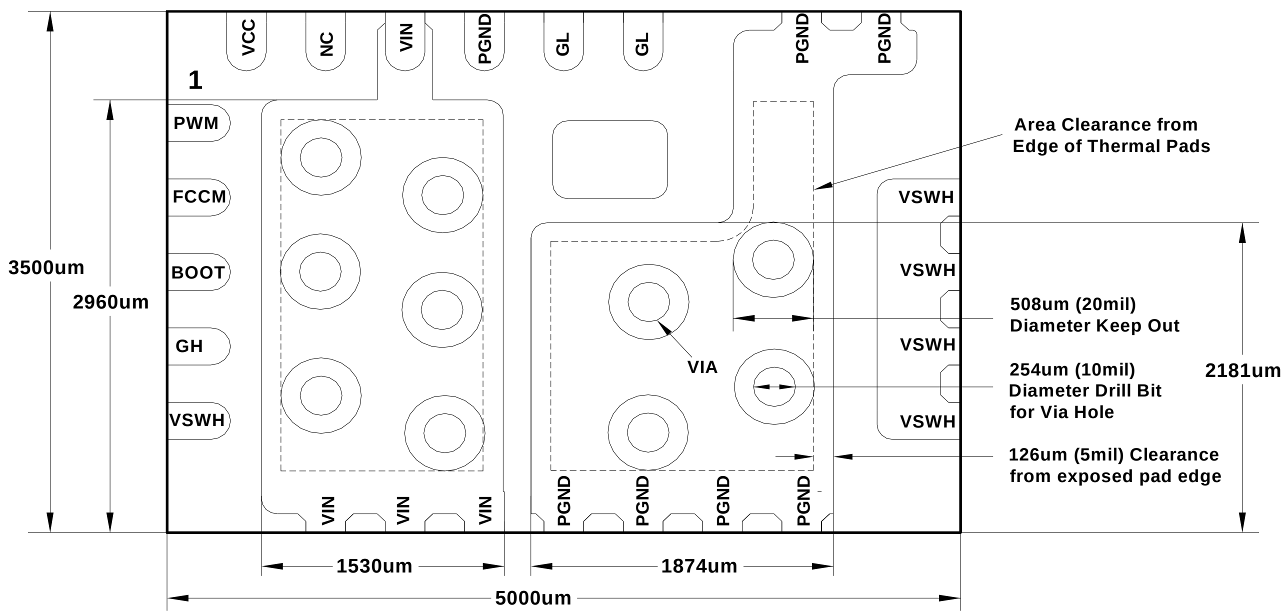
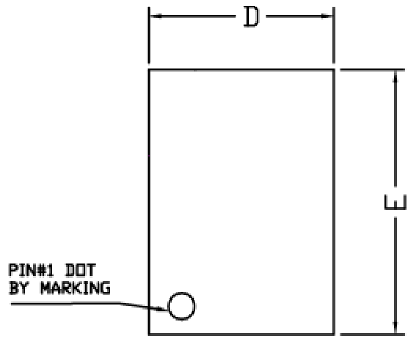
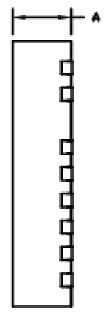


Figure 15. Exposed Pad Land Pattern and Recommended Via Placements

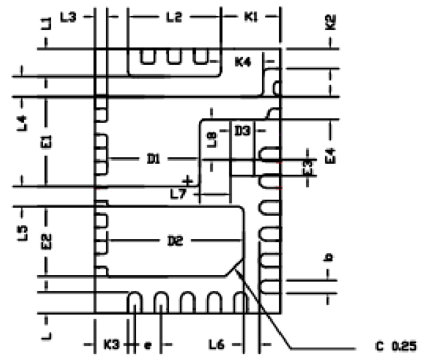
Package Dimensions, QFN3.5x5A_24L



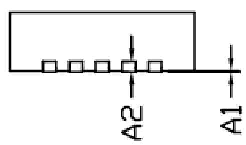
TOP VIEW



SIDE VIEW



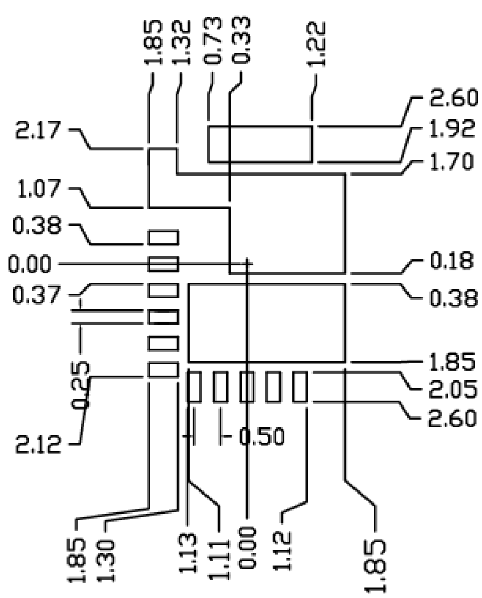
BOTTOM VIEW



SIDE VIEW

SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.10	1.20	0.039	0.043	0.047
A1	0.00	-	0.05	0.000	-	0.002
A2	0.2REF			0.008REF		
E	4.90	5.00	5.10	0.193	0.197	0.201
E1	1.66	1.71	1.76	0.065	0.067	0.069
E2	1.27	1.32	1.37	0.050	0.052	0.054
E3	0.25	0.30	0.35	0.010	0.012	0.014
E4	0.38	0.43	0.48	0.015	0.017	0.019
D	3.40	3.50	3.60	0.134	0.138	0.142
D1	1.70	1.75	1.80	0.067	0.069	0.071
D2	2.53	2.58	2.63	0.100	0.102	0.104
D3	0.40	0.45	0.50	0.016	0.018	0.020
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.48	0.53	0.58	0.019	0.021	0.023
L2	1.70	1.75	1.80	0.067	0.069	0.071
L3	0.18	0.23	0.28	0.007	0.009	0.011
L4	0.32	0.37	0.42	0.013	0.015	0.017
L5	0.33	0.38	0.43	0.013	0.015	0.017
L6	0.25	0.30	0.35	0.010	0.012	0.014
L7	0.53	0.58	0.63	0.021	0.023	0.025
L8	0.72	0.77	0.82	0.028	0.030	0.032
K1	1.08	1.13	1.18	0.042	0.044	0.046
K2	0.33	0.38	0.43	0.013	0.015	0.017
K3	0.58	0.63	0.68	0.023	0.025	0.027
K4	0.75	0.80	0.85	0.030	0.031	0.033
b	0.20	0.25	0.30	0.008	0.010	0.012
e	0.50BSC			0.02BSC		

RECOMMENDED LAND PATTERN

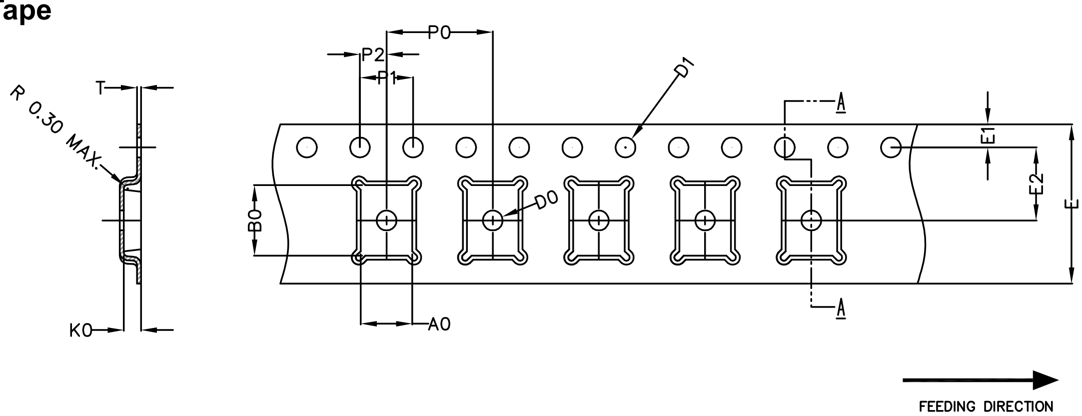


UNIT: mm

NOTE
CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Tape and Reel Dimensions, QFN_3.5x5_24L_EPS_2

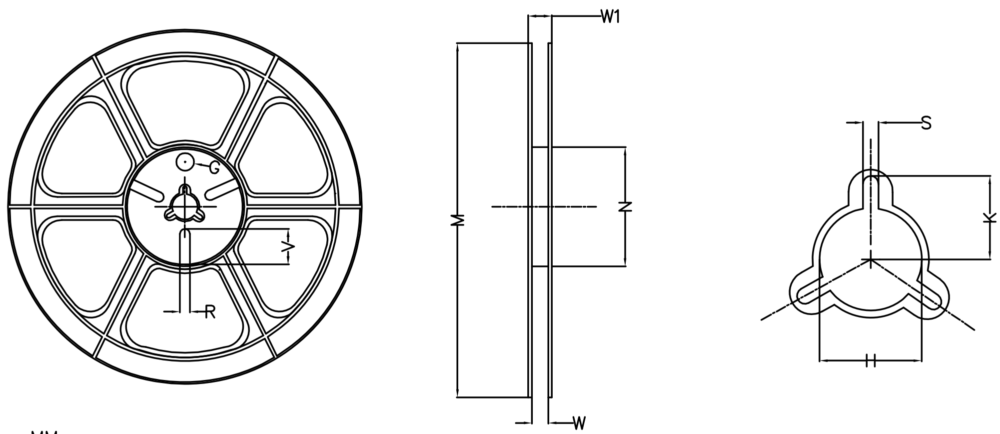
Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN3.5x5 (12 mm)	3.89 ±0.10	5.31 ±0.10	1.30 ±0.10	1.50 MIN.	1.50 $^{+0.10}_{-0.00}$	12.00 ±0.30	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

Reel

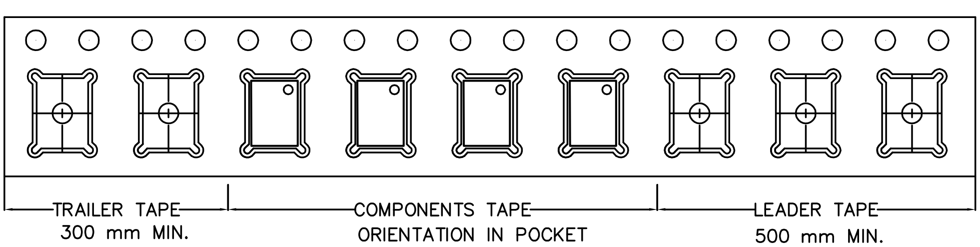


UNIT: MM

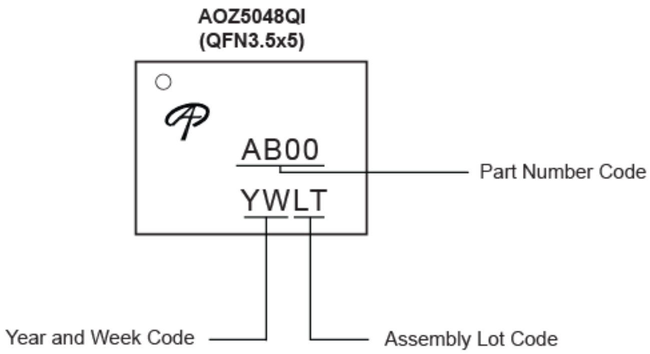
TAPE SIZE	REEL SIZE	M	N	W	W1	H	S	K	G	R	V
12 mm	ø330	ø330.00 ±2.00	ø101.6 ±2.00	12.40 +2.00 −0.00	12.40 +3.00 −0.20	ø13.20 ±0.30	1.70−2.60	---	---	---	---

Leader / Trailer & Orientation

Unit Per Reel:
3000pcs



Part Marking



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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.