

NCP81253

5 V MOSFET Driver Compatible with Single-Phase IMVP8 Controllers

The NCP81253 is a high performance dual MOSFET gate driver in a small 2 mm x 2 mm package, optimized to drive the gates of both high-side and low-side power MOSFETs in a synchronous buck converter. The driver outputs can be placed into a high-impedance state via the tri-state PWM and EN inputs. The NCP81253 comes packaged with an integrated boost diode to minimize external components. A VCC UVLO function guarantees the outputs are low when the supply voltage is low.

Features

- Space-efficient 2 mm x 2 mm DFN8 Thermally-enhanced Package
- VCC Range of 4.5 V to 5.5 V
- Internal Bootstrap Diode
- 5 V 3-stage PWM Input
- Diode Braking Capability via EN Mid-state
- Adaptive Anti-cross Conduction Circuit Protects against Cross-conduction during FET Turn-on and Turn-off
- Output Disable Control Turns Off both MOSFETs via Enable Pin
- VCC Undervoltage Lockout
- These devices are Pb-free, Halogen-free/BFR-free and are RoHS compliant

Typical Applications

- Power Solutions for Notebook and Desktop Systems



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DFN8
CASE 506AA

MARKING DIAGRAM



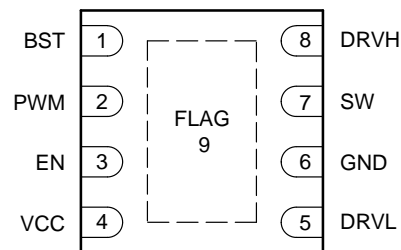
CG = Specific Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

PINOUT DIAGRAM



(Top View)

ORDERING INFORMATION

| Device | Package | Shipping† |
|---------------|-------------------|-----------------------|
| NCP81253MNTBG | DFN8 (Pb-Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCP81253

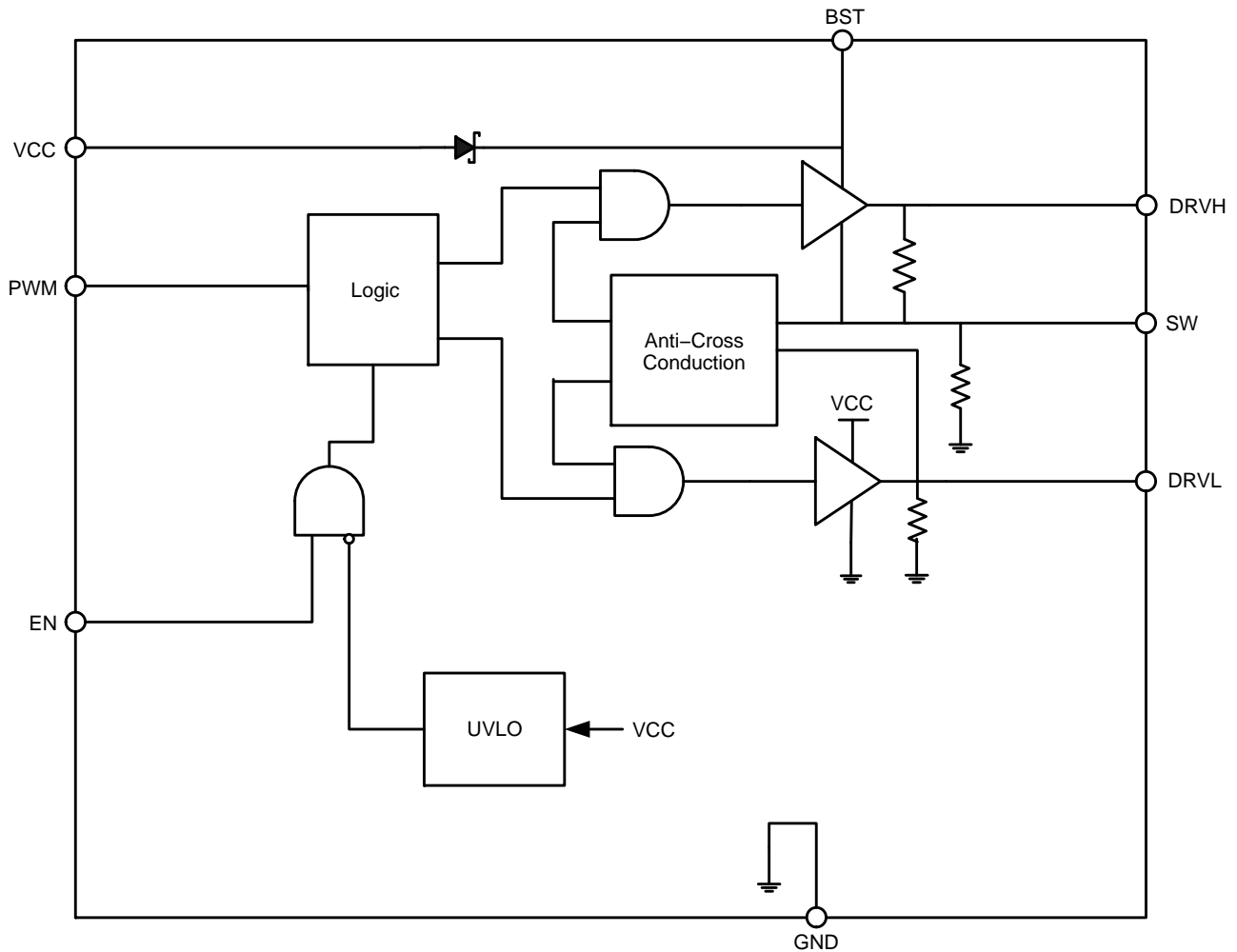


Figure 1. Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Description |
|---------|----------|---|
| 1 | BST | Floating bootstrap supply pin for the high-side gate driver. Connect the external bootstrap capacitor between this pin and SW. |
| 2 | PWM | Control input: PWM = High → DRVH is high, DRVL is low. PWM = Mid → DRVH and DRVL are low. PWM = Low → DRVH is low, DRVL is high. |
| 3 | EN | 3-state input: EN = High → Driver is enabled; normal PWM operation. EN = Mid → Driver is enabled; DRVH and DRVL are low (body diode braking). EN = Low → Driver is disabled. |
| 4 | VCC | Power supply input. Connect a bypass capacitor from this pin to ground. |
| 5 | DRVL | Low-side gate drive output. Connect to the gate of the low-side MOSFET. |
| 6 | GND | Bias and reference ground. All signals are referenced to this node. |
| 7 | SW | Switch node. Connect this pin to the source of the high-side MOSFET and drain of the low-side MOSFET. |
| 8 | DRVH | High-side gate drive output. Connect to the gate of the high-side MOSFET. |
| 9 | FLAG | Thermal flag. There is no electrical connection to the IC. Connect to the ground plane. |

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Table 2. ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Min | Max |
|--------------------------------------|-----------------|---|--|
| Main Supply Voltage (Note 1) | V _{CC} | -0.3 V | 6.5 V |
| Bootstrap Supply Voltage | BST | -0.3 V wrt/SW | 35 V wrt/GND 40 V (≤ 50 ns) wrt/GND 6.5 V wrt/SW |
| Switch Node Voltage | SW | -5 V -10 V (≤ 200 ns) | 35 V 40 V (≤ 50 ns) |
| High-Side Driver Output | DRVH | -0.3 V wrt/SW -2 V (≤ 200 ns) wrt/SW | BST + 0.3 V wrt/SW |
| Low-Side Driver Output | DRVL | -0.3 V -5 V (≤ 200 ns) | V _{CC} + 0.3 V |
| DRVH/DRVL Control Input, Enable Pin | PWM, EN | -0.3 V | 6.5 V |
| Ground | GND | 0 V | 0 V |
| Storage Temperature Range | TSTG | -55°C | 150°C |
| Operating Junction Temperature Range | TJ | -40°C | 150°C |
| Moisture Sensitivity Level | MSL | | 1 |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

Table 3. THERMAL CHARACTERISTICS

| Rating | Symbol | Value | Unit |
|---|------------------|-------|------|
| Thermal Characteristics, DFN8, 2x2 mm (Note 2) Thermal Resistance, Junction-to-Air | R _{θJA} | 119 | °C/W |

2. Values based on copper area of 645 mm² (or 1 in²) of 1 oz copper thickness and FR4 PCB substrate.

Table 4. OPERATING RANGES (Note 3)

| Rating | Symbol | Min | Max | Unit |
|---------------------|-----------------|-----|-----|------|
| Input Voltage | V _{CC} | 4.5 | 5.5 | V |
| Ambient Temperature | T _A | -40 | 100 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

Table 5. ELECTRICAL CHARACTERISTICS V_{CC} = 4.5 V to 5.5 V, V_{BST-SWN} = 4.5 V to 5.5 V, BST = 4.5 V to 30 V, SW = 0 V to 21 V; for typical values T_A = 25°C, for min/max values T_A = -40°C to 100°C; unless otherwise noted. (Notes 4, 5)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|-----------------------------------|---|-----------------------|-----|------|-----|------|
| SUPPLY VOLTAGE | | | | | | |
| V _{CC} Operation Voltage | | V _{CC} | 4.5 | | 5.5 | V |
| UNDERVOLTAGE LOCKOUT | | | | | | |
| V _{CC} Start Threshold | V _{CC} rising | V _{UVLO} | 3.8 | 4.35 | 4.5 | V |
| V _{CC} UVLO Hysteresis | | V _{UVLO_HYS} | 150 | 200 | 250 | mV |
| SUPPLY CURRENT | | | | | | |
| Shutdown Mode | ICC + IBST, EN = GND | I _{shutdown} | | 1 | 20 | μA |
| Normal Mode | ICC + IBST, EN = 5 V, PWM = 400 kHz No load on driver outputs. | I _{normal} | | 1.6 | | mA |
| Standby Current 1 | ICC + IBST, EN = 5 V, PWM = 0 V | I _{standby} | | 0.9 | | mA |

4. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.

5. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

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Table 5. ELECTRICAL CHARACTERISTICS VCC = 4.5 V to 5.5 V, VBST–SWN = 4.5 V to 5.5 V, BST = 4.5 V to 30 V, SW = 0 V to 21 V; for typical values T_A = 25°C, for min/max values T_A = –40°C to 100°C; unless otherwise noted. (Notes 4, 5)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|-----------|-----------------|--------|-----|-----|-----|------|
|-----------|-----------------|--------|-----|-----|-----|------|

BOOTSTRAP DIODE

| | | | | | | |
|-----------------|--|--|-----|-----|-----|---|
| Forward Voltage | VCC = 5 V, Forward bias current = 2 mA | | 0.1 | 0.4 | 0.6 | V |
|-----------------|--|--|-----|-----|-----|---|

PWM INPUT

| | | | | | | |
|----------------|--|--------------------|-----|--|-----|---|
| PWM Input High | | PWM _{HI} | 3.4 | | | V |
| PWM Mid-State | | PWM _{MID} | 1.3 | | 2.7 | V |
| PWM Input Low | | PWM _{LO} | | | 0.7 | V |

HIGH-SIDE DRIVER

| | | | | | | |
|------------------------------------|---|----------------------|----|-----|-----|----|
| Output Impedance, Sourcing Current | VBST – VSW = 5 V | | | 0.9 | 1.7 | Ω |
| Output Impedance, Sinking Current | VBST – VSW = 5 V | | | 0.7 | 1.7 | Ω |
| DRVH Rise Time | VCC = 5 V, C _{load} = 3 nF, VBST–VSW = 5 V, DRVH–SW = 90% to 10% | tr _{DRVH} | | 16 | 25 | ns |
| DRVH Fall Time | VCC = 5 V, C _{load} = 3 nF, VBST–VSW = 5 V, DRVH–SW = 90% to 10% | tf _{DRVH} | | 11 | 18 | ns |
| DRVH Turn-Off Propagation Delay | C _{load} = 3 nF, PWM = PWM _{LO} to DRVH = 90% | tpd _{DRVH} | 10 | 18 | 30 | ns |
| DRVH Turn-On Propagation Delay | C _{load} = 3 nF, DRVH–SW = 1 V to DRVH–SW = 10% | tpdh _{DRVH} | 10 | 15 | 40 | ns |
| SW Pull-down Resistance | SW to GND | | | 45 | | kΩ |
| DRVH Pull-down Resistance | DRVH to SW | | | 45 | | kΩ |

LOW-SIDE DRIVER

| | | | | | | |
|------------------------------------|--|----------------------|----|-----|-----|----|
| Output Impedance, Sourcing Current | VCC = 5 V | | | 0.9 | 1.7 | Ω |
| Output Impedance, Sinking Current | VCC = 5 V | | | 0.4 | 0.8 | Ω |
| DRVL Rise Time | VCC = 5 V, C _{load} = 3 nF, VBST–VSW = 5 V, DRVL = 90% to 10% | tr _{DRVL} | | 11 | 25 | ns |
| DRVL Fall Time | VCC = 5 V, C _{load} = 3 nF, VBST–VSW = 5 V, DRVL = 90% to 10% | tf _{DRVL} | | 8 | 15 | ns |
| DRVL Turn-Off Propagation Delay | C _{load} = 3 nF, PWM = PWM _{HI} to DRVL = 90% | tpd _{DRVL} | 10 | 15 | 30 | ns |
| DRVL Turn-On Propagation Delay | C _{load} = 3 nF, DRVH–SW = 1 V to DRVL = 10% | tpdh _{DRVL} | 5 | 8 | 25 | ns |
| DRVL Pull-down Resistance | DRVL to GND, VCC = GND | | | 45 | | kΩ |

EN INPUT

| | | | | | | |
|--------------------------------|--|----------------------|------|----|-----|----|
| Enable Voltage High | | EN _{HI} | 3.3 | | | V |
| Enable Voltage Mid | | EN _{MID} | 1.35 | | 1.8 | V |
| Enable Voltage Low | | EN _{LO} | | | 0.6 | V |
| Input Bias Current | | | –1.0 | | 1.0 | μA |
| EN High Propagation Delay Time | PWM = 0 V, EN going from 0 V to EN _{HI} to DRVL rising to 10% | tpd _{EN_HI} | | 20 | 40 | ns |

SWITCH NODE

| | | | | | | |
|-------------------------|--|--|--|--|----|----|
| SW Node Leakage Current | | | | | 20 | μA |
|-------------------------|--|--|--|--|----|----|

4. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
5. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

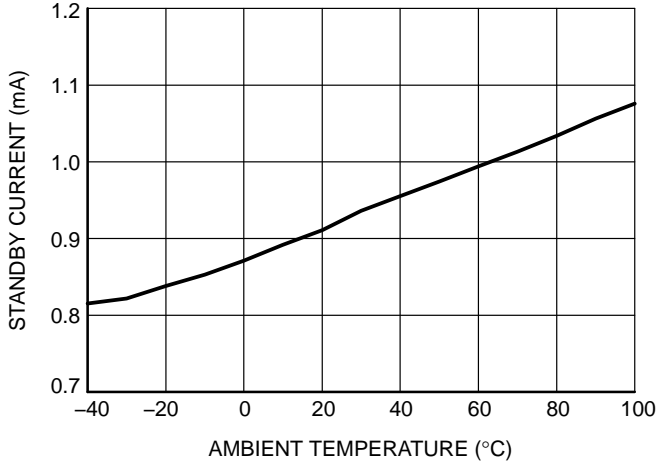


Figure 2. Standby Current vs. Temperature ($V_{CC} = 5\text{ V}$, $EN = 5\text{ V}$, $PWM = 0\text{ V}$)

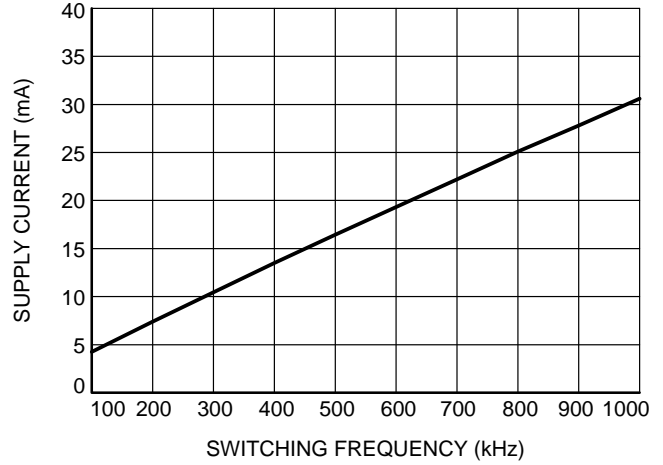


Figure 3. Supply Current vs. Switching Frequency ($V_{CC} = 5\text{ V}$, $C_{load} = 3\text{ nF}$)

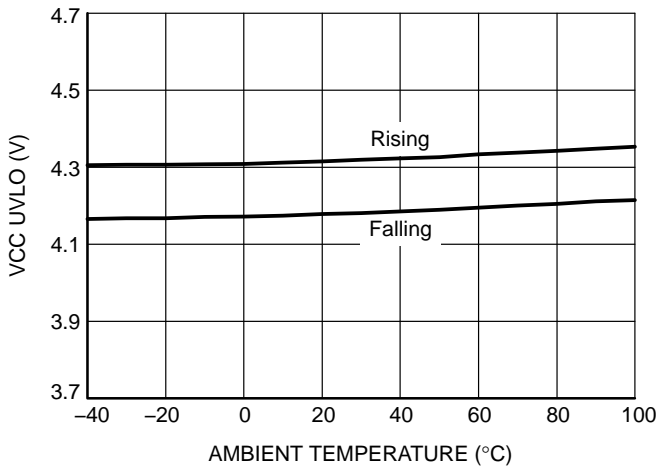


Figure 4. V_{CC} UVLO vs. Temperature ($EN = 5\text{ V}$)

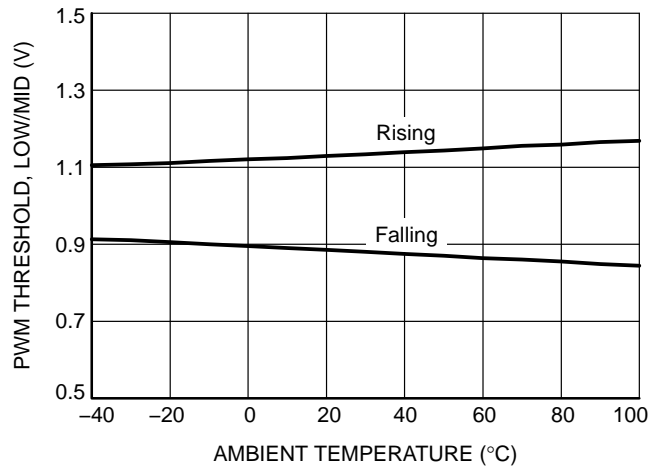


Figure 5. PWM Low/Mid Thresholds vs. Temperature ($V_{CC} = 5\text{ V}$)

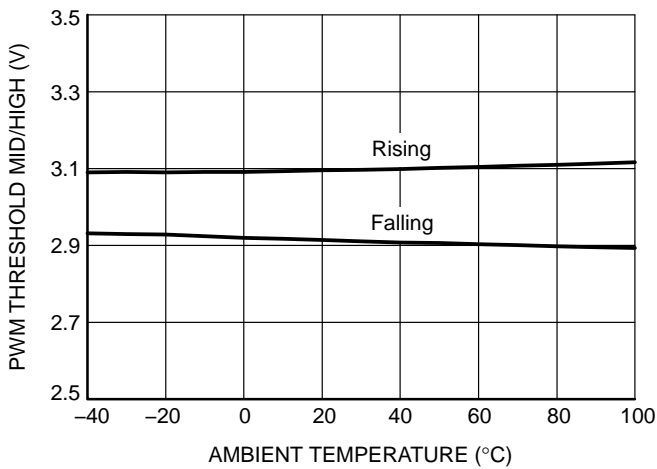


Figure 6. PWM Mid/High Thresholds vs. Temperature ($V_{CC} = 5\text{ V}$)

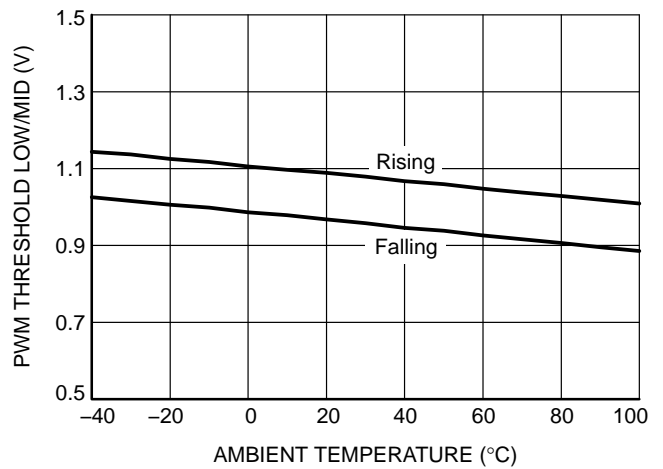


Figure 7. Enable Low/Mid Thresholds vs. Temperature ($V_{CC} = 5\text{ V}$)

TYPICAL CHARACTERISTICS

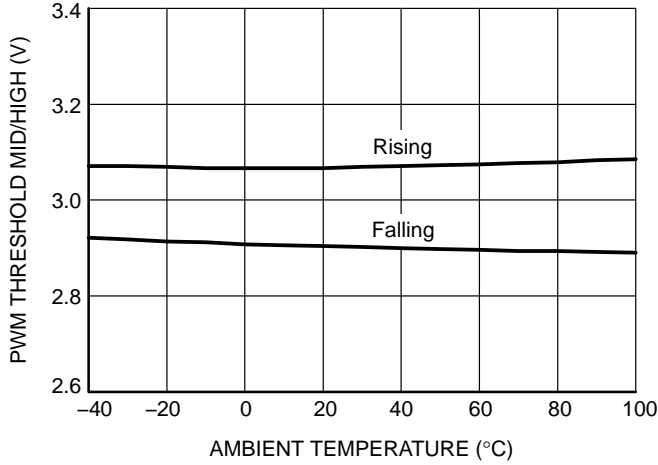


Figure 8. Enable Mid/High Thresholds vs. Temperature ($V_{CC} = 5\text{ V}$)

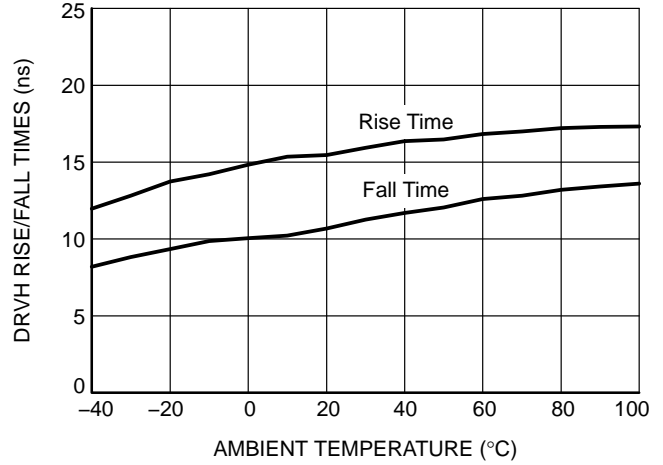


Figure 9. DRVH Rise/Fall Times vs. Temperature ($V_{BST} - V_{SW} = 5\text{ V}$, $C_{load} = 3\text{ nF}$)

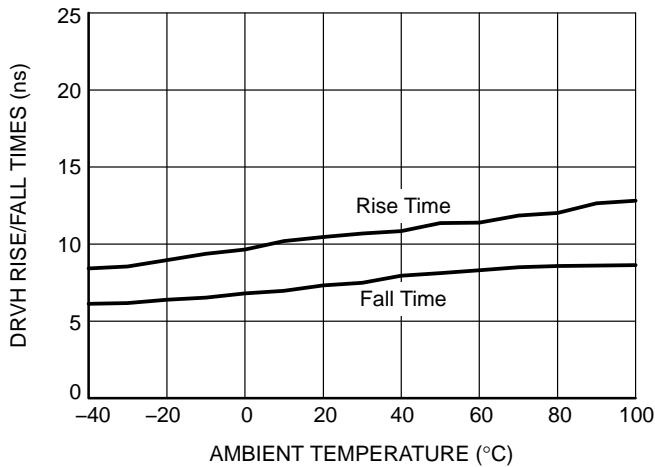


Figure 10. DRVH Rise/Fall Times vs. Temperature ($V_{CC} = 5\text{ V}$, $C_{load} = 3\text{ nF}$)

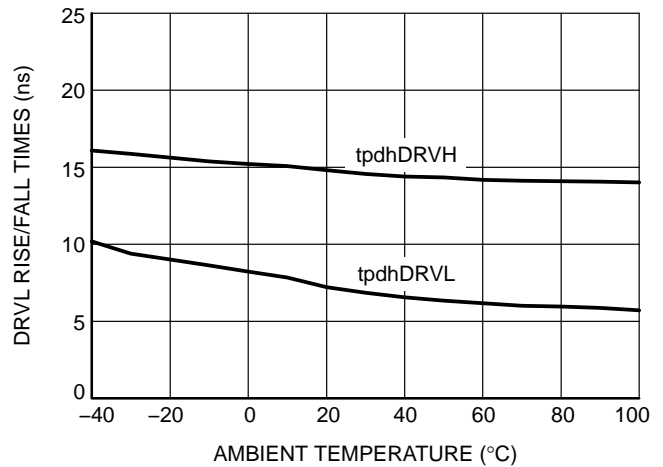


Figure 11. Dead Times vs. Temperature ($V_{CC} = 5\text{ V}$, $C_{load} = 3\text{ nF}$)

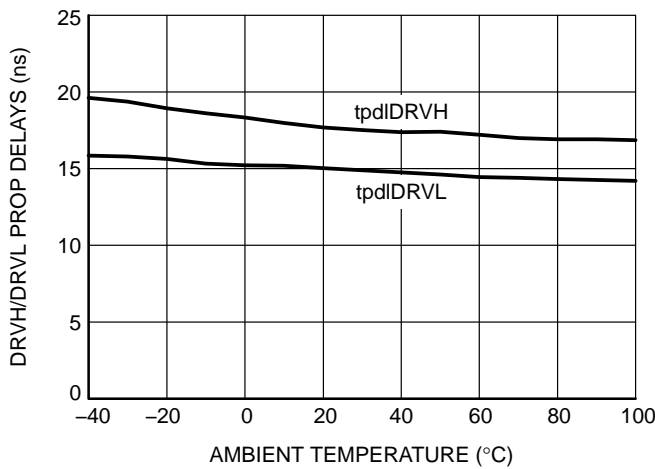


Figure 12. DRVH/DRVH Prop Delays vs. Temperature ($V_{CC} = 5\text{ V}$, $C_{load} = 3\text{ nF}$)

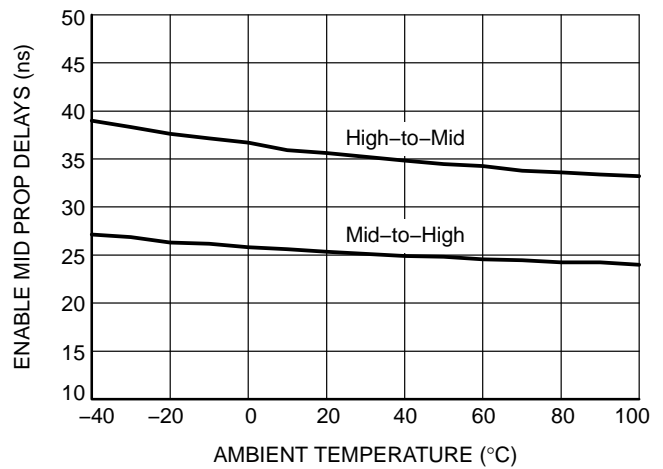


Figure 13. Enable Mid Prop Delays vs. Temperature ($V_{CC} = 5\text{ V}$, $C_{load} = 3\text{ nF}$)

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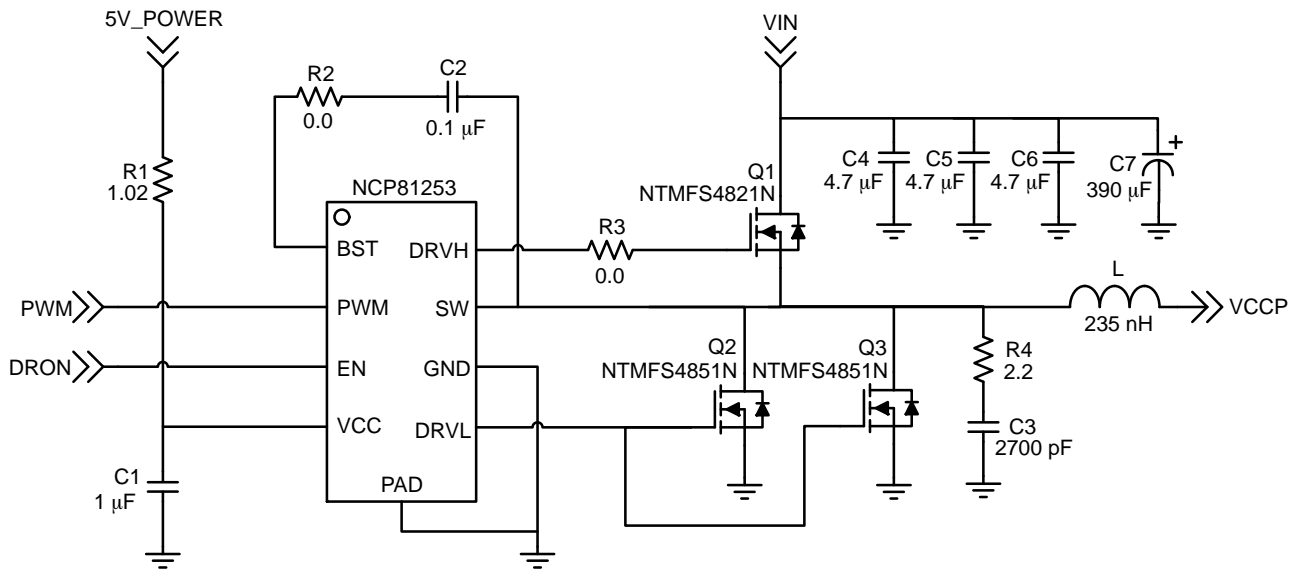


Figure 14. Application Circuit

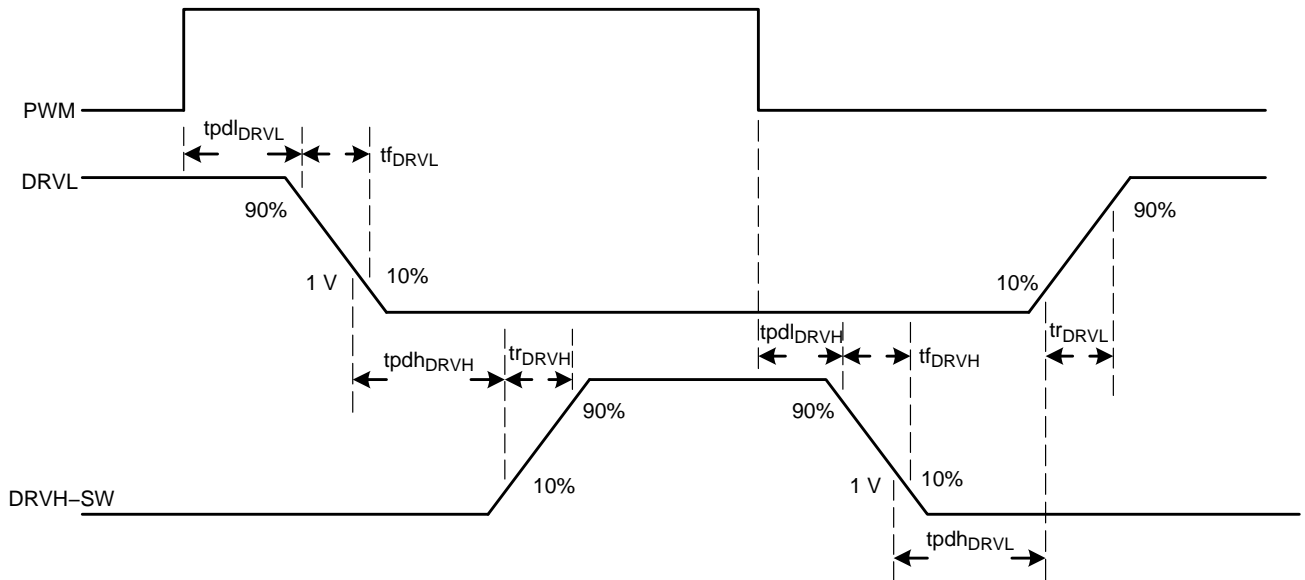


Figure 15. Gate Timing Diagram

NCP81253

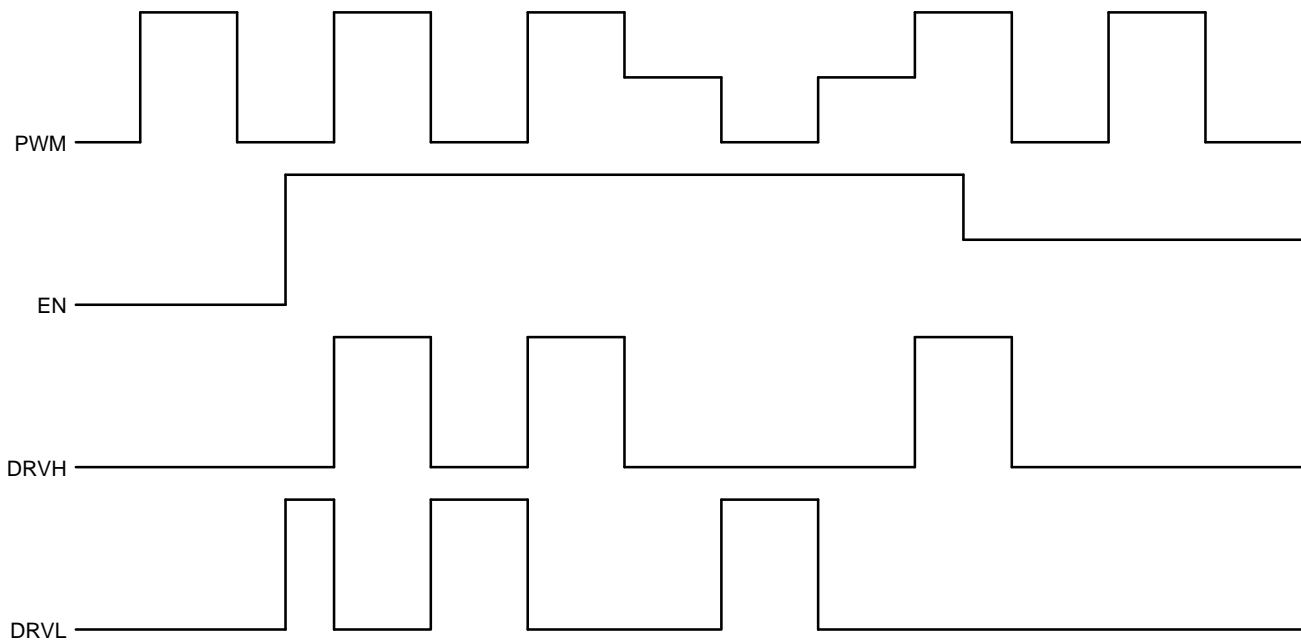


Figure 16. PWM/EN Logic Diagram

APPLICATIONS INFORMATION

The NCP81253 gate driver is a single-phase MOSFET driver designed for driving N-channel MOSFETs in a synchronous buck converter topology. The NCP81253 is designed to work with single-phase IMVP8 controllers such as the NCP81206.

Low-Side Driver

The low-side driver is designed to drive a ground-referenced low- $R_{DS(on)}$ N-channel MOSFET. The voltage supply for the low-side driver is internally connected to the VCC and GND pins.

High-Side Driver

The high-side driver is designed to drive a floating low- $R_{DS(on)}$ N-channel MOSFET. The gate voltage for the high-side driver is developed by a bootstrap circuit referenced to the SW pin.

The bootstrap circuit is comprised of the integrated diode and an external bootstrap capacitor. When the NCP81253 is starting up, the SW pin is held at ground, allowing the bootstrap capacitor to charge up to VCC through the bootstrap diode. When the PWM input is driven high, the high-side driver will turn on the high-side MOSFET using the stored charge of the bootstrap capacitor. As the high-side MOSFET turns on, the SW pin rises. When the high-side MOSFET is fully turned on, SW will settle to VIN and BST will settle to VIN + VCC (excluding parasitic ringing).

Bootstrap Circuit

The bootstrap circuit relies on an external charge storage capacitor (C_{BST}) and an integrated diode to provide current to the high-side driver. A multi-layer ceramic capacitor (MLCC) with a value greater than 100 nF should be used for C_{BST} .

Power Supply Decoupling

The NCP81253 can source and sink relatively large currents to the gate pins of the MOSFETs. In order to maintain a constant and stable supply voltage, a low-ESR capacitor should be placed near the VCC and GND pins. A MLCC between 1 μ F and 4.7 μ F is typically used.

Undervoltage Lockout

DRVH and DRVL are low until VCC reaches the VCC UVLO threshold, typically 4.35 V. Once VCC reaches this threshold, the PWM signal will control DRVH and DRVL. There is a 200 mV hysteresis on VCC UVLO. There are pull-down resistors on DRVH, DRVL and SW to prevent the gates of the MOSFETs from accumulating enough charge to turn on when the driver is powered off.

Three-State EN Input

Placing EN into a logic-high and logic-low will turn the driver on and off, respectively, as long as VCC is greater than the UVLO threshold. The EN threshold limits are specified

in the electrical characteristics table in this datasheet. Setting the voltage on EN to a mid-state level will pull both DRVH and DRVL low. Refer to Table 6 for the EN/PWM logic table.

Setting EN to the mid-state level can be used for body diode braking to quickly reduce the inductor current. By turning the LS FET off and having the current conduct through the LS FET body diode, the voltage at the switch node will be at a greater negative potential compared to having the LS FET on. This greater negative potential on switch node allows there to be a greater voltage across the output inductor, since the opposite terminal of the inductor is connected to the converter output voltage. The larger voltage across the inductor causes there to be a greater inductor current slew rate, allowing the current to decrease at a faster rate.

Three-State PWM Input

Switching PWM between logic-high and logic-low states will allow the driver to operate in continuous conduction mode as long as VCC is greater than the UVLO threshold and EN is high. The threshold limits are specified in the electrical characteristics table in this datasheet. Refer to Figure 15 for the gate timing diagrams and Table 6 for the EN/PWM logic table.

When PWM is set above PWM_{HI}, DRVL will first turn off after a propagation delay of tpd_{DRVL}. To ensure non-overlap between DRVL and DRVH, there is a delay of tpd_{DRVH} from the time DRVL falls to 1 V, before DRVH is allowed to turn on.

When PWM falls below PWM_{LO}, DRVH will first turn off after a propagation delay of tpd_{DRVH}. To ensure non-overlap between DRVH and DRVL, there is a delay of tpd_{DRVL} from the time DRVH – SW falls to 1 V, before DRVL is allowed to turn on.

When PWM enters the mid-state voltage range (and thereby exiting the logic high or logic low states), both DRVH and DRVL are pulled low for the non-overlap delay (tpdh). If PWM is still in the mid-state at the conclusion of the non-overlap delay, both DRVH and DRVL will remain in the off states.

To minimize power consumption when the NCP81253 is in a disabled state, the internal voltage rails that determine the low/mid/high PWM logic states are shut down when EN is low. When EN is brought high (while VCC is above the UVLO threshold), the PWM internal voltage rails are

brought up, but require some time to rise to their proper levels. To prevent a PWM signal from being interpreted incorrectly during this time, there is a delay from EN rising to the driver responding to PWM signals, which is set at a typical value of 50 μs.

Table 6. EN/PWM LOGIC TABLE

| EN | PWM | DRVH | DRVL |
|------|------|------|------|
| LOW | X | LOW | LOW |
| HIGH | LOW | LOW | HIGH |
| HIGH | MID | LOW | LOW |
| HIGH | HIGH | HIGH | LOW |
| MID | LOW | LOW | LOW |
| MID | MID | LOW | LOW |
| MID | HIGH | LOW | LOW |

Thermal Considerations

As power in the NCP81253 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCP81253 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCP81253 can handle is given by:

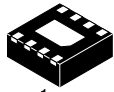
$$P_{D(MAX)} = \frac{[T_{J(MAX)} - T_A]}{R_{\theta JA}} \quad \text{(eq. 1)}$$

Since T_J is not recommended to exceed 150°C, the NCP81253, soldered on to a 645 mm² copper area, using 1 oz. copper and FR4, can dissipate up to 1.05 W when the ambient temperature (T_A) is 25°C. The power dissipated by the NCP81253 can be calculated from the following equation:

$$P_D \approx VCC \cdot [(n_{HS} \cdot Qg_{HS} + n_{LS} \cdot Qg_{LS}) \cdot f + I_{standby}] \quad \text{(eq. 2)}$$

Where n_{HS} and n_{LS} are the number of high-side and low-side FETs, respectively, Qg_{HS} and Qg_{LS} are the gate charges of the high-side and low-side FETs, respectively and f is the switching frequency of the converter.

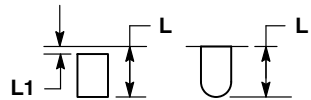
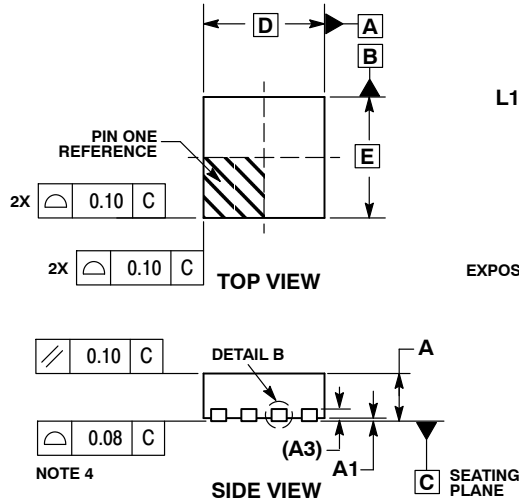
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 4:1

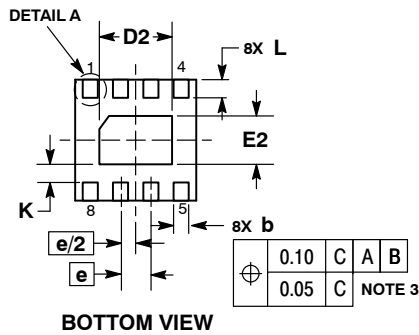
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CASE 506AA
ISSUE F

DATE 04 MAY 2016

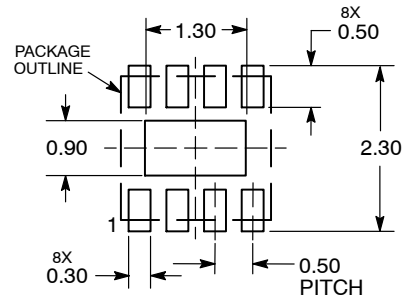


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
 4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS | | |
|-------------|----------|------|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 2.00 BSC | |
| D2 | 1.10 | 1.30 |
| E | 2.00 BSC | |
| E2 | 0.70 | 0.90 |
| e | 0.50 BSC | |
| K | 0.30 REF | |
| L | 0.25 | 0.35 |
| L1 | --- | 0.10 |

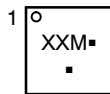


RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Device

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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