Data Sheet

ADCA5190

5 MHz to 1800 MHz Broadband CATV Amplifier

FEATURES

- Frequency range of 5 MHz to 1800 MHz
- High gain of 19.1 dB at 1800 MHz
- Excellent NPR (MER) performance: 48 dB at 67 dBmV TCP
- Excellent S11 return losses:
  - −18 dB at 45 MHz to 1218 MHz
  - −20 dB at 1218 MHz to 1800 MHz
- V_{DD} operation: 5.0 V to 8.0 V
- Configurable dc current from 200 mA to 450 mA
- 32-lead, 5 mm × 5 mm LFCSP

APPLICATIONS

- 45 MHz to 1800 MHz CATV infrastructure amplifier systems
- 5 MHz to 700 MHz upstream
- Remote physical layer (PHY)
- DOCSIS 3.1 and DOCSIS 4.0 compliant

FUNCTIONAL BLOCK DIAGRAM

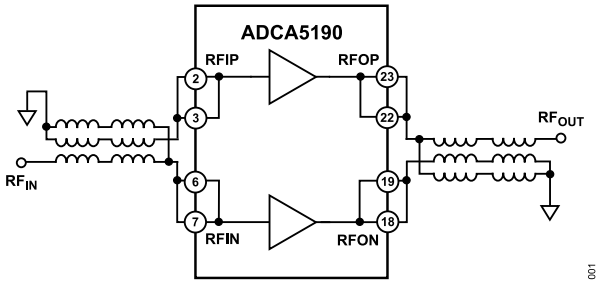

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADCA5190 is a medium power gain block amplifier that provides excellent linearity across a flexible bias range allowing power efficient design implementation for various applications.

The device provides 19.1 dB of flat gain up to 1800 MHz, making this ideal for Data Over Cable Service Interface Specification (DOCSIS®) 4.0 downstream applications. The device is also well suited for upstream applications to 700 MHz as the output stage. The device is conveniently packaged in an industry-standard, 32-lead, 5 mm × 5 mm lead frame chip-scale package (LFCSP) with an exposed pad on the bottom of the package for improved thermal performance.

Rev. A

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REVISION HISTORY

4/2023—Rev. 0 to Rev. A

Changes to Table 10 ... 18
Changes to Figure 32 ... 19
Changes to Layout Considerations Section ... 21

7/2022—Revision 0: Initial Version

SPECIFICATIONS

GENERAL DOWNSTREAM PERFORMANCE

See the application circuit in Figure 31. Supply voltage (V_{DD}) = 8.0 V, supply current (I_{DD}) = 375 mA, paddle temperature (T_{PADDLE}) = 35 °C, and source impedance (Z_S) = load impedance (Z_L) = 75 Ω, unless otherwise noted.

Table 1. Downstream Performance

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
BANDWIDTH		45		1800	MHz	
POWER GAIN	S21		19.1		dB	f = 45 MHz
			19.3		dB	f = 1218 MHz
			19.1		dB	f = 1800 MHz
SLOPE OF STRAIGHT LINE[1]			0.2		dB	f = 45 MHz to 1218 MHz
			0.0		dB	f = 45 MHz to 1800 MHz
FLATNESS OF FREQUENCY RESPONSE[2]			0.2		dB	f = 45 MHz to 1800 MHz
INPUT IMPEDANCE	Z_{IN}		37.5		Ω	RFIP and RFIP
REVERSE ISOLATION	S12		−23.5		dB	f = 45 MHz to 1800 MHz
OUTPUT IMPEDANCE	Z_{OUT}		37.5		Ω	RFOP and RFON
RETURN LOSS						
Input	S11		−18		dB	f = 45 MHz to 1218 MHz
			−20		dB	f = 1218 MHz to 1800 MHz
Output	S22		−17		dB	f = 45 MHz to 1218 MHz
			−16		dB	f = 1218 MHz to 1800 MHz
NOISE FIGURE						Includes losses of baluns shown in the Downstream Applications Circuit with Passive Biasing section
			2.6		dB	f = 45 MHz
			3.0		dB	f = 1218 MHz
			4.1		dB	f = 1800 MHz
SUPPLY						
Operating Voltage	V_{DD}	5.0		8.0	V	Can be biased between 5.0 V and 8.0 V
DC Current	I_{DD}		375		mA	Using the downstream applications circuit with passive biasing, (V_{DD}) = 8.0 V (see the Downstream Applications Circuit with Passive Biasing section); can be adjusted between 200 mA and 450 mA (see the Supply Voltage and Bias Current section)

[1] The slope is defined as the delta of the gain at the start frequency and the gain at the stop frequency.

[2] Flatness is defined as the maximum deviation from a linear best-fit of the gain in the frequency range of operation.

SPECIFICATIONS

DISTORTION DATA

Downstream All Digital Channel Plan, 8× Orthogonal Frequency Division Multiplexing (OFDM) Channels, 258 MHz to 1794 MHz

See the application circuit in Figure 31. V_{DD} = 8.0 V, I_{DD} = 375 mA, T_{PADDLE} = 35°C, and Z_S = Z_L = 75 Ω, unless otherwise noted.

Table 2. Distortion Data

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
NOISE POWER RATIO[1]	NPR					
			48		dB	10 dB tilt, 6 dB offset at 1026 MHz, total composite power (TCP) = 67 dBmV, V_{DD} = 8.0 V, I_{DD} = 375 mA
			43		dB	10 dB tilt, 6 dB offset at 1026 MHz, TCP = 63 dBmV, V_{DD} = 5.0 V, I_{DD} = 250 mA
			50		dB	10 dB tilt, no offset, TCP = 67 dBmV, V_{DD} = 8.0 V, I_{DD} = 375 mA
			44		dB	10 dB tilt, no offset, TCP = 63 dBmV, V_{DD} = 5.0 V, I_{DD} = 250 mA

[1] The noise power ratio gives an equivalent result to the standard modulation error rate (MER) testing but with improved dynamic range using an industry-accepted method.

Downstream All Digital Channel Plan, 190×, ITU-T J.83B, Single-Channel Quadrature Amplitude Modulation (SCQAM) 6 MHz Channels, 54 MHz to 1218 MHz

See the application circuit in Figure 31. T_{PADDLE} = 35 °C, and Z_S = Z_L = 75 Ω, unless otherwise noted.

Table 3. Distortion Data

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
NOISE POWER RATIO[1]	NPR					
			48		dB	10 dB tilt, TCP = 67 dBmV, V_{DD} = 8.0 V, I_{DD} = 375 mA
			46		dB	10 dB tilt, TCP = 63 dBmV, V_{DD} = 5.0 V, I_{DD} = 250 mA

[1] The noise power ratio gives an equivalent result to the standard MER testing but with improved dynamic range using an industry-accepted method.

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

Parameter	Rating
V_{DD}	
DC Supply over Voltage (5 Minutes)	10 V
I_{DD} Bias Supply Current	500 mA
RF Input Power	60 dBmV
Temperature	
Operating Range, T_{PADDLE}	−40°C to +100°C
Peak Reflow (Moisture Sensitivity Level (MSL) 3)	260°C
Junction (T_J) to Maintain 1 Million Hour Mean Time to Failure (MTTF)	150°C
Nominal Junction (T_J)	
T_{PADDLE} = 100 °C, I_{DD} = 375 mA, V_{DD} = 8.0 V	122°C
Storage (T_S) Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the thermal resistance from the operating portion of the pseudomorphic, high electron mobility transistor (pHEMT) device to the outside surface of the package closest to the device mounting area (the exposed pad on the bottom of the case). See the Thermal Considerations section for additional information.

Table 5. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-32-13	7.5	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADCA5190

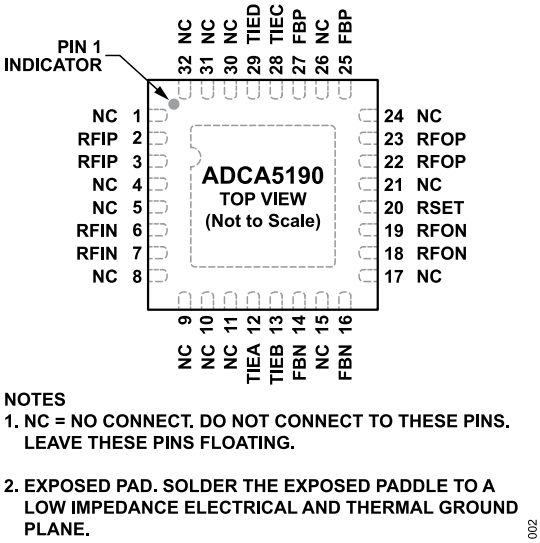
Table 6. ADCA5190, 32-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	350	Class 1A, passed

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THESE PINS. LEAVE THESE PINS FLOATING.

2. EXPOSED PAD. SOLDER THE EXPOSED PADDLE TO A LOW IMPEDANCE ELECTRICAL AND THERMAL GROUND PLANE.

Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4, 5, 8, 9, 10, 11, 15, 16, 17, 21, 24, 26, 30, 31, 32	NC	No Connect. Do not connect to these pins. Leave these pins floating.
2, 3	RFIP	Positive RF Amplifier Input. RFIP and RFIN form a differential input.
6, 7	RFIN	Negative RF Amplifier Input. RFIP and RFIN form a differential input.
12	TIEA	Connect TIEA and TIEB (Pin 13) together externally.
13	TIEB	Connect TIEB and TIEA (Pin 12) together externally.
18, 19	RFON	Negative Amplifier RF Output. A choke inductor is required to provide dc current and RF isolation. A dc blocking capacitor is also required. See Figure 31 for specific recommendations.
14, 16	FBN	Negative Feedback Path. Place an 0201 capacitor between Pin 14 and Pin 16. See Figure 31 for specific recommendations.
20	RSET	Bias Resistor. The voltage must be pulled up or down depending on target bias voltage (see Supply Voltage and Bias Current). See Figure 31 for specific recommendations.
22, 23	RFOP	Positive Amplifier RF Output. A choke inductor is required to provide dc current and RF isolation. A dc blocking capacitor is also required. See Figure 31 for specific recommendations.
25, 27	FBP	Positive Feedback Path. Place an 0201 capacitor between Pin 25 and Pin 27. See Figure 31 for specific recommendations.
28	TIEC	Connect TIEC and TIED (Pin 29) together externally.
29	TIED	Connect TIED and TIEC (Pin 28) together externally.
	EPAD	Exposed Pad. Solder the exposed paddle to a low impedance electrical and thermal ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 8.0 V, I_{DD} = 375 mA, T_{PADDLE} = 35°C, and Z_S = Z_L = 75 Ω, unless otherwise noted.

S-PARAMETERS FOR DOWNSTREAM APPLICATION (SEE FIGURE 31)

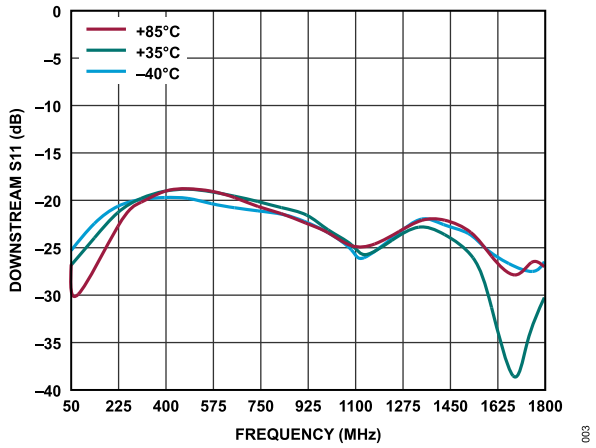


Figure 3. Downstream S11 vs. Frequency Over Temperature, V_{DD} = 8.0 V

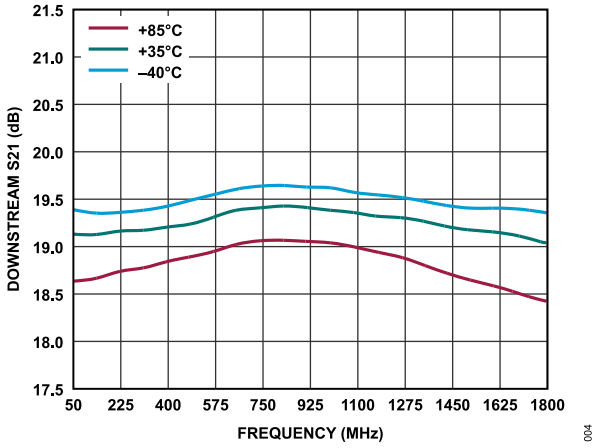


Figure 4. Downstream S21 vs. Frequency Over Temperature, V_{DD} = 8.0 V

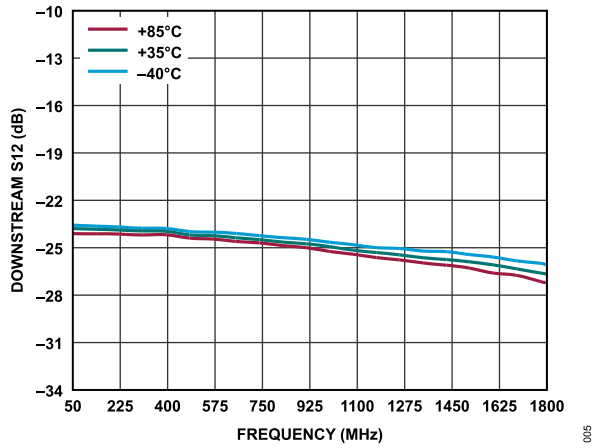


Figure 5. Downstream S12 vs. Frequency Over Temperature, V_{DD} = 8.0 V

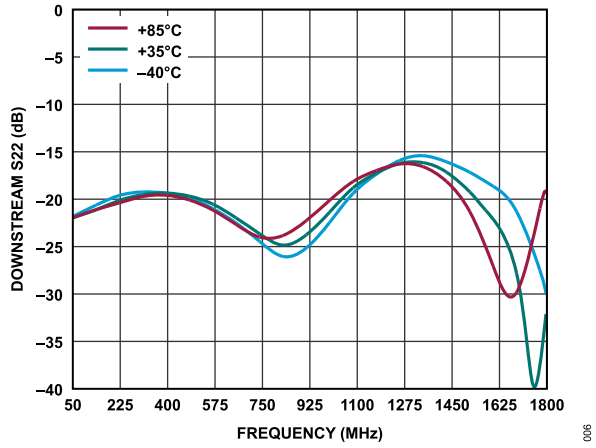


Figure 6. Downstream S22 vs. Frequency Over Temperature, V_{DD} = 8.0 V

TYPICAL PERFORMANCE CHARACTERISTICS

DOCSIS 4.0 DOWNSTREAM PERFORMANCE (SEE FIGURE 31)

8× OFDM channels, 258 MHz to 1794 MHz, and 6 dB offset at 1026 MHz, unless otherwise noted. In Figure 7 to Figure 18, the performance at the lower output power is limited by the test equipment and is not indicative of the noise performance of the device.

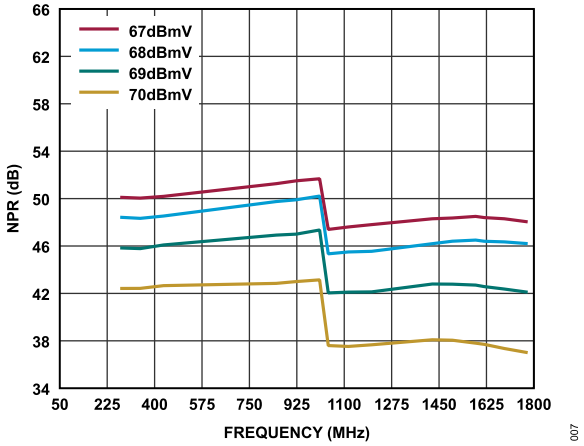


Figure 7. NPR vs. Frequency Over TCP, 10 dB Tilt, V_{DD} = 8.0 V, I_{DD} = 375 mA

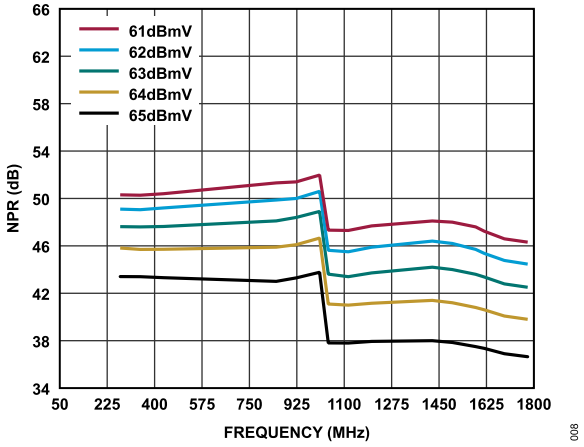


Figure 8. NPR vs. Frequency Over TCP, 10 dB Tilt, V_{DD} = 5.0 V, I_{DD} = 250 mA

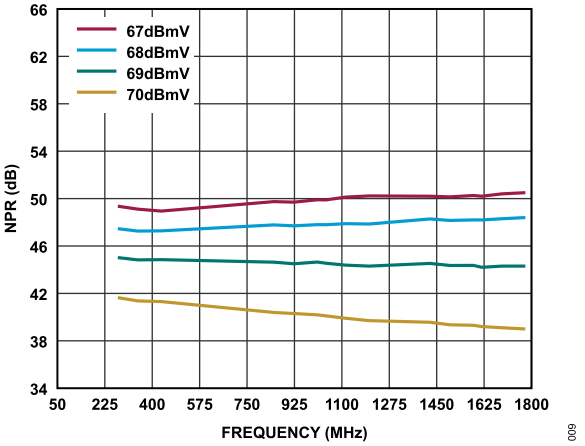


Figure 9. NPR vs. Frequency Over TCP, 10 dB Tilt, No Offset at 1026 MHz, V_{DD} = 8.0 V, I_{DD} = 375 mA

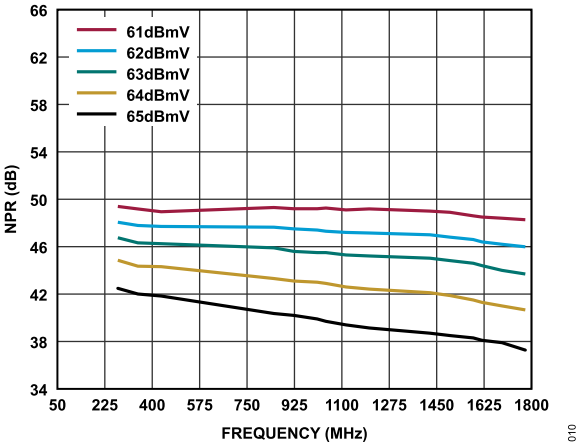


Figure 10. NPR vs. Frequency Over TCP, 10 dB Tilt, No Offset at 1026 MHz, V_{DD} = 5.0 V, I_{DD} = 250 mA

TYPICAL PERFORMANCE CHARACTERISTICS

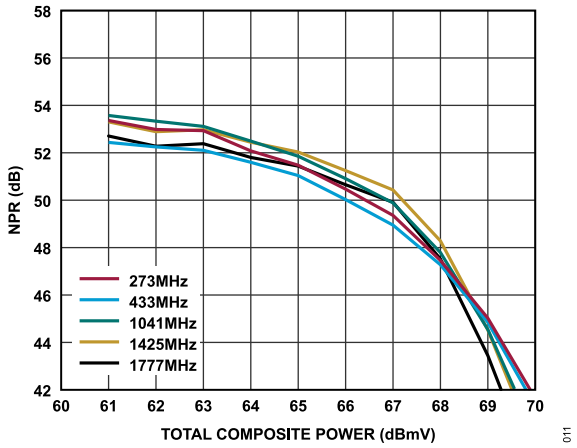


Figure 11. NPR vs. Total Composite Power Over Frequency, No Offset at 1026 MHz, 10 dB Tilt, V_{DD} = 8.0 V, I_{DD} = 375 mA

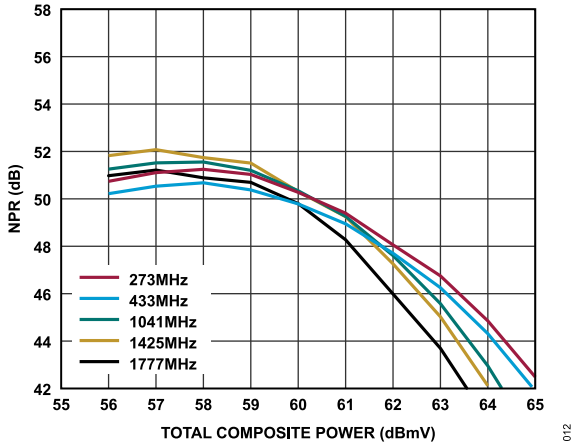


Figure 12. NPR vs. Total Composite Power Over Frequency, No Offset at 1026 MHz, 10 dB Tilt, V_{DD} = 5.0 V, I_{DD} = 250 mA

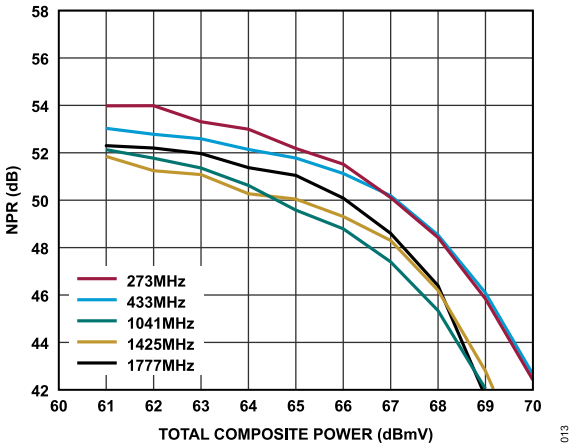


Figure 13. NPR vs. Total Composite Power Over Frequency, 10 dB Tilt, V_{DD} = 8.0 V, I_{DD} = 375 mA

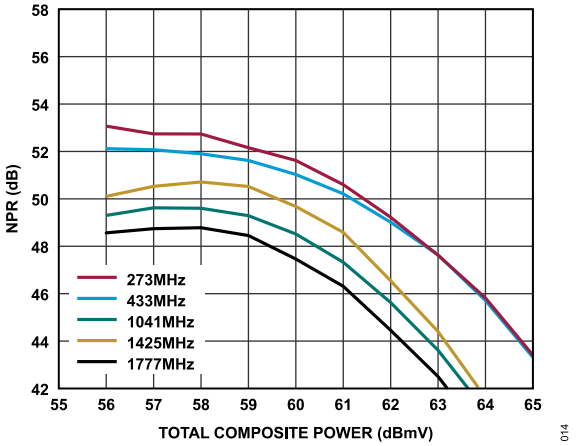


Figure 14. NPR vs. Total Composite Power Over Frequency, 10 dB Tilt, V_{DD} = 5.0 V, I_{DD} = 250 mA

TYPICAL PERFORMANCE CHARACTERISTICS

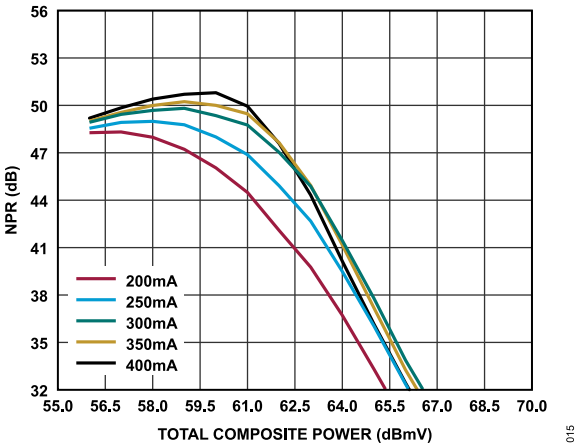


Figure 15. NPR vs. Total Composite Power Over Current, Worst Case Frequency, 10 dB Tilt, V_{DD} = 5.0 V

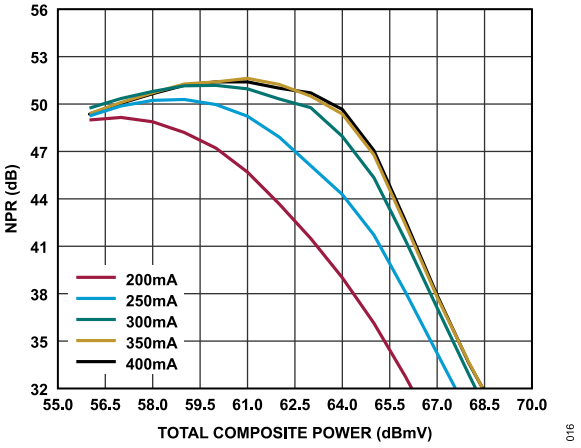


Figure 16. NPR vs. Total Composite Power Over Current, Worst Case Frequency, 10 dB Tilt, V_{DD} = 6.0 V

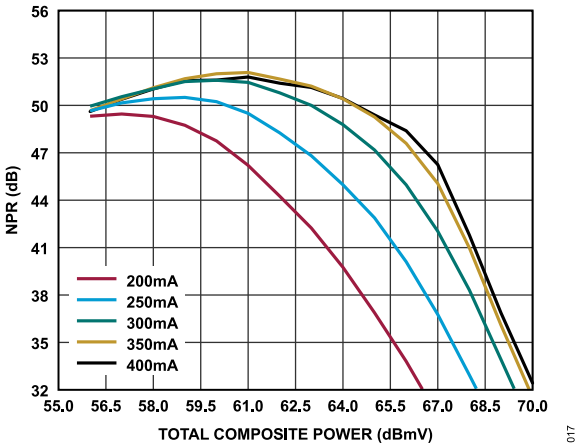


Figure 17. NPR vs. Total Composite Power Over Current, Worst Case Frequency, 10 dB Tilt, V_{DD} = 7.0 V

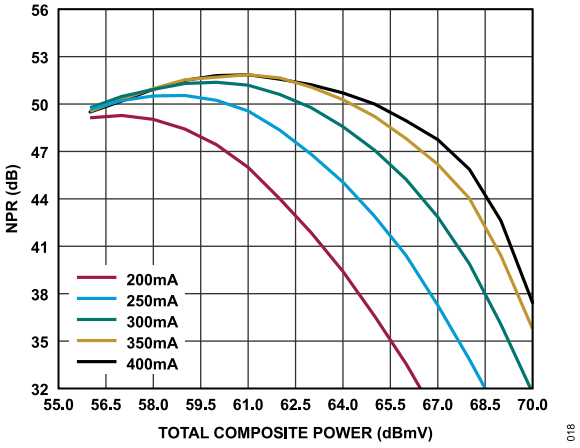


Figure 18. NPR vs. Total Composite Power Over Current, Worst Case Frequency, 10 dB Tilt, V_{DD} = 8.0 V

TYPICAL PERFORMANCE CHARACTERISTICS

DOCSIS 3.1 DOWNSTREAM PERFORMANCE (SEE FIGURE 31)

190×, ITU-T J.83B, SCQAM 6 MHz channels, and 54 MHz to 1218 MHz, unless otherwise noted. In Figure 19 to Figure 26, the performance at the lower output power is limited by the test equipment and is not indicative of the noise performance of the device.

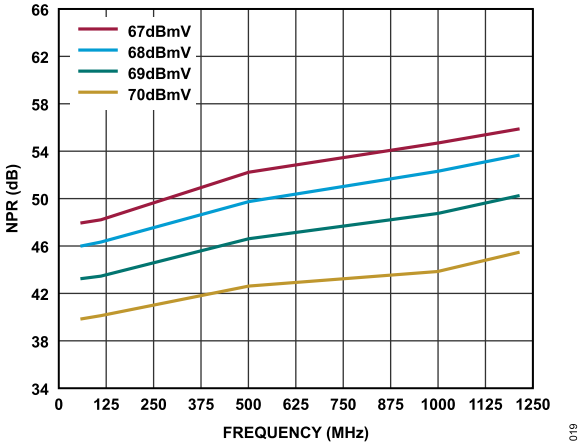


Figure 19. NPR vs. Frequency Over TCP, 10 dB Tilt, V_{DD} = 8.0 V, I_{DD} = 375 mA

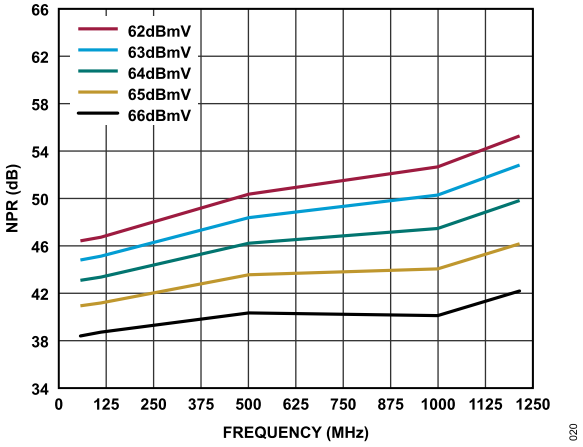


Figure 20. NPR vs. Frequency Over TCP, 10 dB Tilt, V_{DD} = 5.0 V, I_{DD} = 250 mA

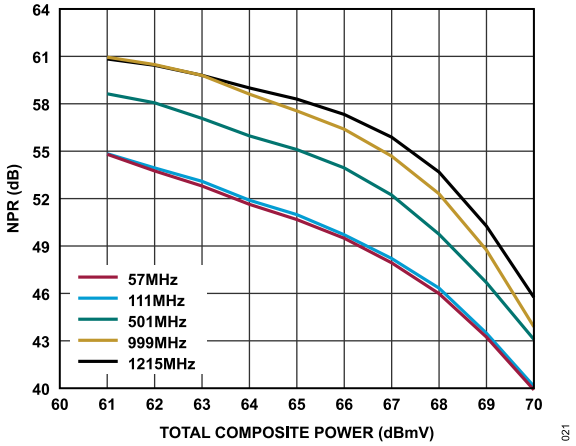


Figure 21. NPR vs. Total Composite Power Over Frequency, 10 dB Tilt, V_{DD} = 8.0 V, I_{DD} = 375 mA

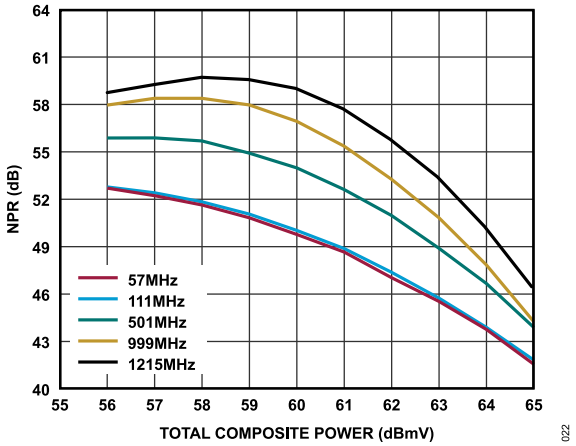


Figure 22. NPR vs. Total Composite Power Over Frequency, 10 dB Tilt, V_{DD} = 5.0 V, I_{DD} = 250 mA

TYPICAL PERFORMANCE CHARACTERISTICS

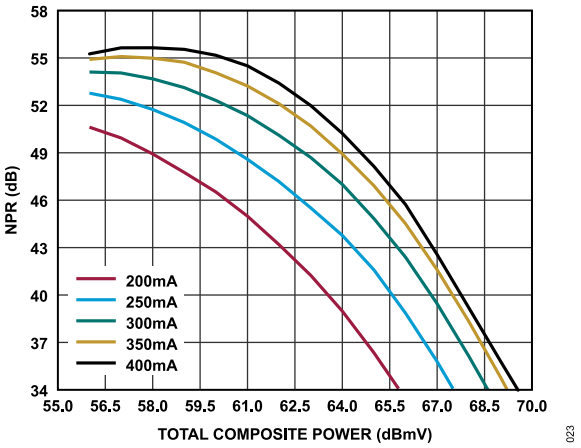


Figure 23. NPR vs. Total Composite Power Over Current, Worst Case Frequency, 10 dB Tilt, V_{DD} = 5.0 V

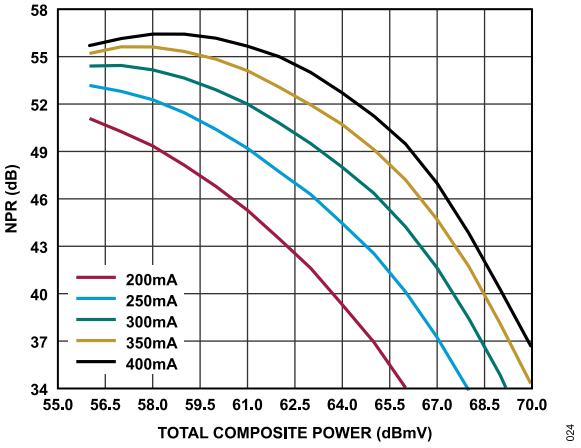


Figure 24. NPR vs. Total Composite Power Over Current, Worst Case Frequency, 10 dB Tilt, V_{DD} = 6.0 V

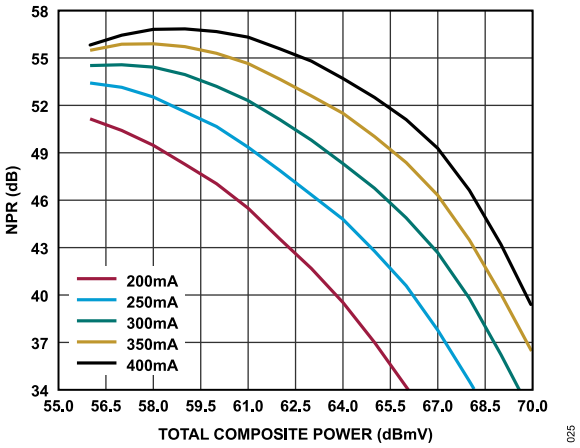


Figure 25. NPR vs. Total Composite Power Over Current, Worst Case Frequency, 10 dB Tilt, V_{DD} = 7.0 V

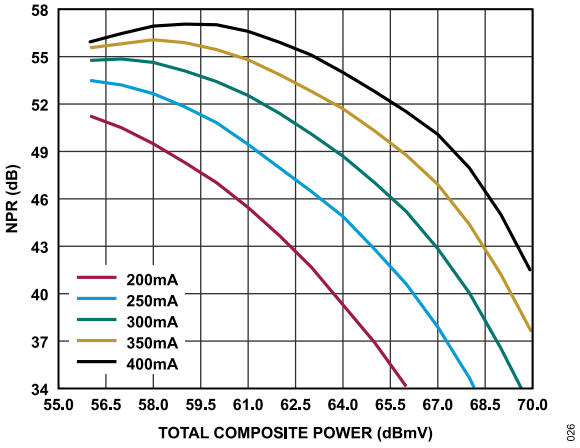


Figure 26. NPR vs. Total Composite Power Over Current, Worst Case Frequency, 10 dB Tilt, V_{DD} = 8.0 V

TYPICAL PERFORMANCE CHARACTERISTICS

NOISE PERFORMANCE

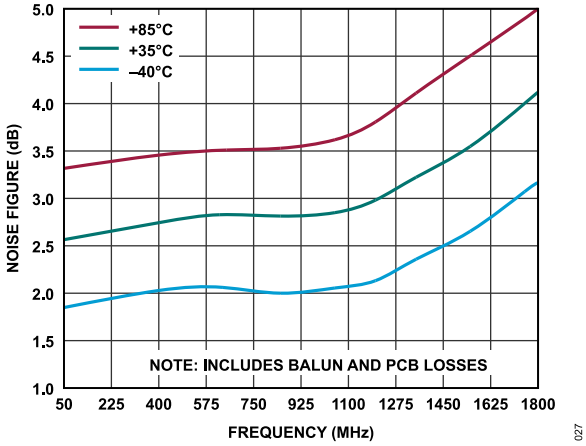


Figure 27. Noise Figure vs. Frequency Over Temperature, V_{DD} = 8.0 V, I_{DD} = 375 mA

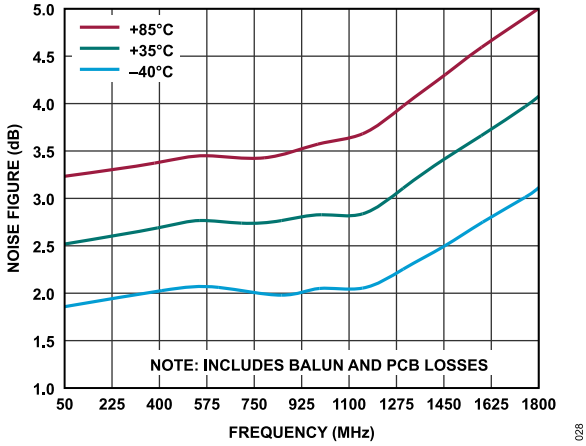


Figure 28. Noise Figure vs. Frequency Over Temperature, V_{DD} = 5.0 V, I_{DD} = 250 mA

THEORY OF OPERATION

The ADCA5190 is a single-die, 1800 MHz differential cascode amplifier fabricated on a linear gallium arsenide (GaAs), pHEMT process. The device provides general-purpose linear gain suitable for a wide range of applications.

When used with a recommended balun, the ADCA5190 can achieve a 4.1 dB noise figure at 1800 MHz (3.0 dB noise figure at 1218 MHz) while holding excellent linearity for extended spectrum line extender input stage applications.

The device has suitable drive capability to overcome nominal insertion losses introduced from automatic gain control and tilt functions.

The ADCA5190 can also serve as an output stage for the upstream path at any DOCSIS 4.0 frequency split.

Depending on the application, the ADCA5190 can be biased from 5.0 V through 8.0 V with currents from 200 mA to 450 mA.

APPLICATIONS INFORMATION

THERMAL CONSIDERATIONS

The ADCA5190 is packaged in a thermally efficient, 32-lead LFCSP. The thermal resistance from junction to case, θ_{JC}, is 7.5°C/W, where the case is defined by the exposed pad on the bottom of the package. For the best thermal performance, it is recommended to add as many thermal vias as possible under the exposed pad of the LFCSP and to fill these vias with a paste that has high thermal conductivity. It is also recommended that the array of vias under the ADCA5190 interface to an external heat sink such as a pedestal on the system chassis.

SOLDERING INFORMATION AND RECOMMENDED PCB LAND PATTERN

Figure 29 shows the recommended land pattern for the ADCA5190. To minimize thermal impedance, the exposed pad on the 5 mm × 5 mm LFCSP is soldered to a ground plane. To improve thermal dissipation, 45 thermal vias are arranged in an array under the exposed pad. The array consists of alternating rows of six vias and seven vias, maximizing the number of vias within the area. The area under the pad is also tied to ground on the bottom layer of the PCB. If multiple ground layers exist, tie these layers together by the vias. The external layer of the PCB must be a minimum of 1 oz. copper. The minimum average plated hole wall thickness of the vias must not be less than 0.001 inches, and it is recommended that the vias be filled with a conductive paste, such as Tatsuta AE3030, and plated over.

For further information on optimizing the thermal performance while using the ADCA5190, refer to the AN-1604 Application Note, Thermal Management Calculations for RF Amplifiers in LFCSP and Flange Packages.

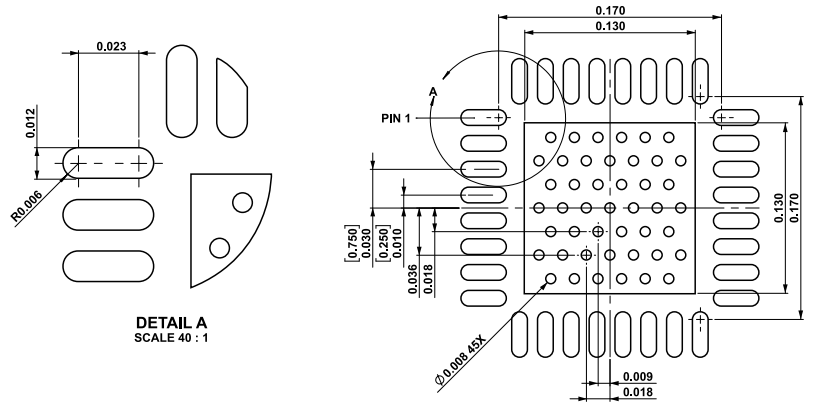


Figure 29. Recommended PCB Layout (Dimensions Shown in Inches)

APPLICATIONS INFORMATION

SUPPLY VOLTAGE AND BIAS CURRENT

The ADCA5190 provides flexible options for biasing for various applications. The voltage can be adjusted from 5 V to 8 V depending on the RF demand and the available supplies. The bias current can be adjusted between 200 mA and 450 mA to optimize power consumption and linearity for a given application. The RSET pin (Pin 20) can also be used to optimize performance for a given supply voltage.

There are several options for setting the bias current, I_{DD}, of the ADCA5190. The passive bias approach is the most basic and provides a dc voltage at the RF inputs, RFIP (Pin 2 and Pin 3) and RFIN (Pin 6 and Pin 7), that is generated from a resistor divider (R4 and R3) off the V_{DD} supply rail, as seen in Figure 31. The output voltage of the resistor divider, V_{BIAS_ADJ}, is connected through a ferrite bead (E1) to the ac ground terminal of T1. This voltage also sets the dc bias at the outputs of T1, which drive the RF inputs. The typical relationship between V_{BIAS_ADJ} and I_{DD} is shown in Figure 30. This approach requires the fewest components, but process variation results in the bias current varying ~±15% from the typical I_{DD} value. This also affects device performance similarly to intentionally adjusting the current of a nominal device. Noise or variation on the V_{DD} supply also directly affects the bias current. In applications where some variation in performance is acceptable, this simple approach to biasing is ideal.

If more tightly controlled bias current is desired, there are several options available. When supply voltage imprecision is a concern, adding a voltage reference diode, such as the ADR5041 to develop the gate voltages, removes bias current dependence on the supply rail. If process variation is a concern, there is a simple and low cost analog circuit employing matched PNP devices that can be used to compensate for the vast majority of process variation in the ADCA5190. This circuit is referred to as active biasing. A schematic for such a circuit is provided in Figure 32. The values of the three resistors (R2, R13, and R15) surrounding the dual PNP (Q1) vary depending on the supply voltage and target current. Values for two typical bias targets are supplied in Table 9, but the same approach can be used for any supply voltage and current combination desired. If the target application already has a digital-to-analog converter (DAC) available with an extra output, driving the voltage at Pin 1 of E1 in Downstream Cable Application Circuit with Passive Biasing Bill of Materials, and monitoring I_{DD}, allows the user to precisely servo the targeted I_{DD} level.

In both the passive and active biasing approaches, performance is optimized by setting the voltage at the RSET pin (Pin 20). This voltage can be pulled up or down by selecting the values of R8 and R20, as shown in Table 8.

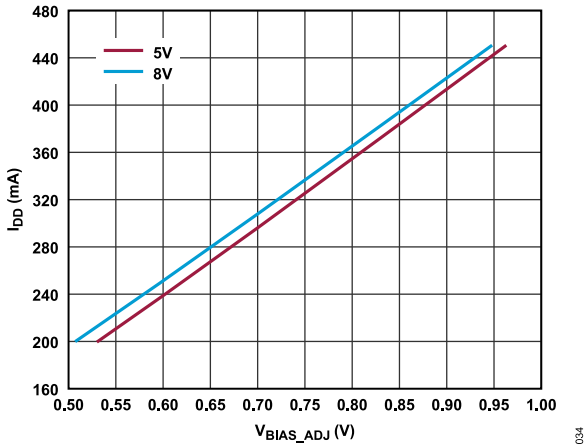


Figure 30. I_{DD} vs. V_{BIAS_ADJ}

Table 8. Suggested Values for R8 and R20 vs. V_{DD} [1]

V_{DD}	R8	R20
5.0 V	DNP	6490 Ω
6.0 V	10 kΩ	DNP
7.0 V	3.16 kΩ	DNP
8.0 V	2 kΩ	DNP

[1] DNP means do not populate.

Table 9. Suggested Values for R2, R13, and R15 vs. Bias Target

Configuration	R13	R15	R2
V_{DD} = 8 V, I_{DD} = 375 mA	5110 Ω	44,200 Ω	1180 Ω
V_{DD} = 5 V, I_{DD} = 250 mA	7150 Ω	49,900 Ω	1500 Ω

APPLICATIONS INFORMATION

DOWNSTREAM APPLICATIONS CIRCUIT WITH PASSIVE BIASING

The schematic in Figure 31 and the PCB layout in Figure 34 are recommended for downstream cable system applications from 45 MHz to 1800 MHz that employ passive biasing. Recommended values for all components are in the BOM listed in Table 10. T1 is an RF transformer configured to transform the single-ended 75 Ω RF input to a differential signal that drives the 37.5 Ω inputs of the ADCA5190 (RFIN and RFIP). The voltage at Pin 1 of E2 is the filtered supply voltage, V_{DD}. A resistor divider (R4 and R3) sets V_{BIAS_ADJ}. See Supply Voltage and Bias Current for more information about how to set this voltage to adjust I_{DD}. C6 stabilizes this reference and serves as the ac ground for the RF input signal. Capacitor C29 between the FBN pins (Pin 14 and Pin 16) provides feedback for the negative side of the amplifier, and Capacitor C30 between the FBP pins (Pin 25 and Pin 27) provides feedback for the positive side of the amplifier.

T2 is an RF transformer configured to transform the differential 37.5 Ω outputs (RFON and RFOP) to a single-ended 75 Ω RF output.

The C3, C5, C7, C8, C13, C14, C18, C20, L8, L9, L10, and L11 components are intended for impedance matching, and these components must be optimized to match the RF input source and RF output load. Capacitor C4 blocks the dc voltage of the RF input source. Capacitor C27 and Capacitor C28 block the dc voltage at the RFOP (Pin 22 and Pin 23) and RFON (Pin 18 and Pin 19) output pins. The L2 and L3 inductors are RF chokes connected to the filtered V_{DD} supply voltage.

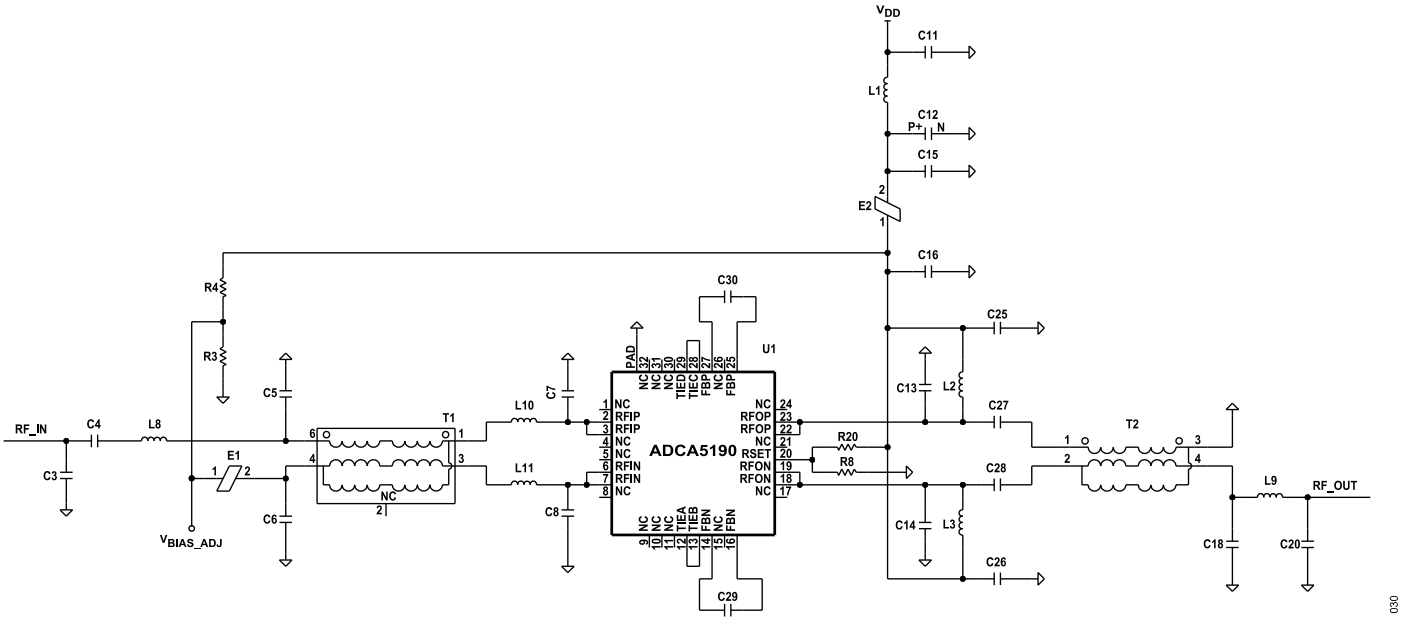


Figure 31. Suggested Downstream Cable TV (CATV) Application Circuit with Passive Biasing Schematic

APPLICATIONS INFORMATION

DOWNSTREAM CABLE APPLICATION CIRCUIT WITH PASSIVE BIASING BILL OF MATERIALS

Table 10. Downstream Bill of Materials with Passive Biasing[1]

Reference Designator	Value	Tolerance	Minimum Rating	Footprint	Suggested Vendor	Suggested Part Number
C3	0.2 pF	±0.1 pF	100 V	0402	Murata	GRM1555C2AR20BA01D
C4, C16, C25, C26	0.01 µF	10%	100 V	0402	TDK	810-C1005X7S2A103K
C6	0.01 µF	10%	50 V	0201	Taiyo Yuden	UMK063BJ103KP-F
C10, C12	2.2 µF	10%	50 V	1411	Kyocera AVX	TAJB225K050RNJ
C11	0.01 µF	20%	100 V	0603	TDK	C1608X7R2A103M080AA
C15	0.047 µF	10%	50 V	0603	TDK	06035C473KAT4A
C27, C28	180 pF	1%	50 V	0402	Murata	GRT1555C1H181FA02D
C29, C30	220 pF	10%	50 V	0201	Murata	GRM033R71H221KA12D
E1	1000 Ω ferrite	25%	170 mA	0201	Murata	BLM03BX102SN1D
E2	220 Ω ferrite	25%	1.8 A	0603	Taiyo Yuden	FBMH1608HM221-T
L1	2.2 µH	20%	1.6 A	1210	Taiyo Yuden	BRL3225T2R2M
L2, L3	270 nH	5%	590 mA	0402	Coilcraft	0402DF-271XJRW
L8, L10, L11	0 Ω	N/A	0.1 W	0402	Panasonic	ERJ-2GE0R00X
L9	1.5 nH	0.2 nH	2.1 A	0402	Murata	LQW15AN1N5C8ZD
R3	1 kΩ	1%	0.1 W	0402	Panasonic	ERJ-2RKF1001X
R4	8.87 kΩ	1%	100 mW	0402	Panasonic	RC0201FR-072KL
R8	Select[2]	1%	100 mW	0201	N/A	N/A
R20	Select[2]	1%	50 mW	0201	N/A	N/A
T1	1:1 transformer	N/A	N/A	AT224-3	Mini-Circuits	TC1-33-75G2+
T2	1:1 transformer	N/A	N/A	99-01-1618-2	Mini-Circuits	TRS1-182-75-3+
U1	CATV amplifier	N/A	N/A	5 mm × 5 mm, 32-lead LFSCP	Analog Devices, Inc.	ADCA5190
C5, C7, C8, C13, C14, C18, C20	Do not install	N/A	N/A	N/A	N/A	Do not install

[1] N/A means not applicable.

[2] See Table 8 for suggested values.

APPLICATIONS INFORMATION

DOWNSTREAM APPLICATIONS CIRCUIT WITH ACTIVE BIASING

The schematic in Figure 32 and the PCB layout in Figure 33 are recommended for downstream cable system applications from 45 MHz to 1800 MHz that employ active biasing. Recommended values for all components are in the BOM listed in the Downstream Cable Application Circuit with Active Biasing Bill of Materials section. The voltage at Pin 1 of E2 is the filtered supply voltage, V_{DD}. T1 is an RF transformer configured to transform the single-ended 75 Ω RF input to a differential signal that drives the 37.5 Ω inputs of the ADCA5190 (RFIN and RFIP). The active bias circuit comprises the C19, C31, C32, Q1, R2, R11, R12, R13, and R15 components. The circuit is connected to Pin 1 of E1. See Supply Voltage and Bias Current for more information about how to control I_{DD} using this circuit. C6 stabilizes the output of the active bias circuit and serves as the ac ground for the RF input signal. Capacitor C29 between the FBN pins (Pin 14 and Pin 16) provides feedback for the negative side of the amplifier, and Capacitor C30 between the FBP pins (Pin 25 and Pin 27) provides feedback for the positive side of the amplifier.

T2 is an RF transformer configured to transform the differential 37.5 Ω outputs (RFON and RFOP) to a single-ended 75 Ω RF output.

The C3, C5, C7, C8, C13, C14, C18, C20 L8, L9, L10, and L11 components are intended for impedance matching, and these components must be optimized to match the RF input source and RF output load. Capacitor C4 blocks the dc voltage of the RF input source. Capacitor C27 and Capacitor C28 block the dc voltage at the RFOP (Pin 22 and Pin 23) and RFON (Pin 18 and Pin 19) output pins. The L2 and L3 inductors are RF chokes connected to the filtered V_{DD} supply voltage.

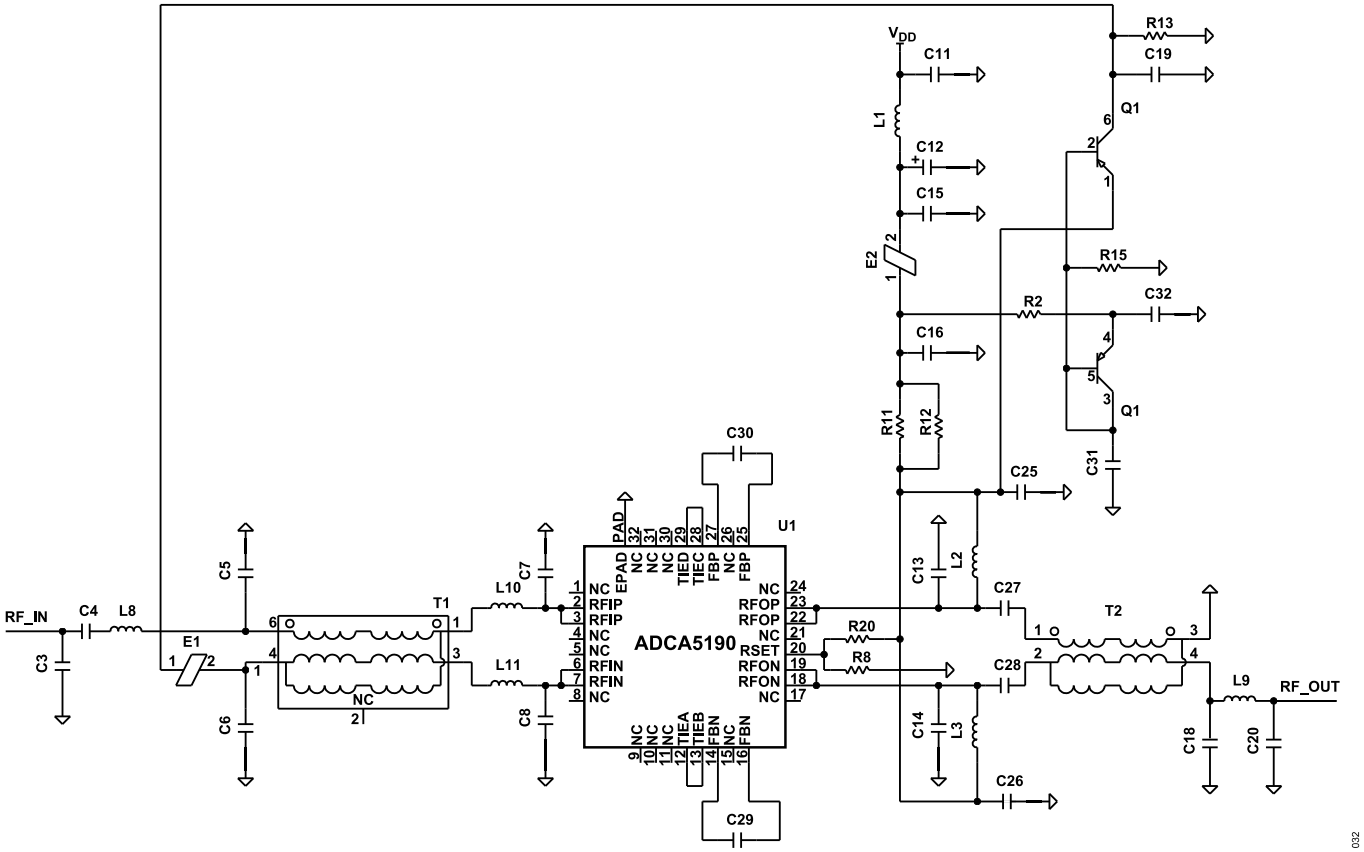


Figure 32. Suggested Downstream CATV Application Circuit with Active Biasing Schematic

APPLICATIONS INFORMATION

DOWNSTREAM CABLE APPLICATION CIRCUIT WITH ACTIVE BIASING BILL OF MATERIALS

Table 11. Downstream Bill of Materials with Active Biasing[1]

Reference Designator	Value	Tolerance	Minimum Rating	Footprint	Suggested Vendor	Suggested Part Number
C3	0.2 pF	±0.1 pF	100 V	0402	Murata	GRM1555C2AR20BA01D
C4, C16, C19, C25, C26, C31, C32	0.01 µF	10%	100 V	0402	TDK	810-C1005X7S2A103K
C6	0.01 µF	10%	50 V	0201	Taiyo Yuden	UMK063BJ103KP-F
C10, C12	2.2 µF	10%	50 V	1411	Kyocera AVX	TAJB225K050RNJ
C11	0.01 µF	20%	100 V	0603	TDK	C1608X7R2A103M080AA
C15	0.047 µF	10%	50 V	0603	TDK	06035C473KAT4A
C27, C28	180 pF	1%	50 V	0402	Murata	GRT1555C1H181FA02D
C29, C30	220 pF	10%	50 V	0201	Murata	GRM033R71H221KA12D
E1	1000 Ω ferrite	25%	170 mA	0201	Murata	BLM03BX102SN1D
E2	220 Ω ferrite	25%	1.8 A	0603	Taiyo Yuden	FBMH1608HM221-T
L1	2.2 µH	20%	1.6 A	1210	Taiyo Yuden	BRL3225T2R2M
L2, L3	270 nH	5%	590 mA	0402	Coilcraft	0402DF-271XJRW
L8, L10, L11	0 Ω	N/A	0.1 W	0402	Panasonic	ERJ-2GE0R00X
L9	1.5 nH	0.2 nH	2.1 A	0402	Murata	LQW15AN1N5C8ZD
Q1	Dual PNP	N/A	100 mA	SOT-666-6	Nexperia	BCM857BV
R2, R13, R15	Select[2]	1%	62.5 mW	0402	N/A	N/A
R8	Select[3]	1%	50 mW	0201	Panasonic	ERJ-1GNF2001C
R11, R12	1 Ω	1%	200 mW	0402	Vishay	CRCW04021R00FKEDHP
R20	Select[3]	1%	50 mW	0201	N/A	N/A
T1	1:1 transformer	N/A	N/A	AT224-3	Mini-Circuits	TC1-33-75G2+
T2	1:1 transformer	N/A	N/A	99-01-1618-2	Mini-Circuits	TRS1-182-75-3+
U1	CATV amplifier	N/A	N/A	5 mm × 5 mm, 32-lead LFSCP	Analog Devices, Inc.	ADCA5190
C5, C7, C8, C13, C14, C18, C20	Do not install	N/A	N/A	0402	N/A	Do not install

[1] N/A means not applicable.

[2] See Table 9 for suggested values.

[3] See Table 8 for suggested values.

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS

The layouts in Figure 33 and Figure 34 are similar to that used in the evaluation circuit for the ADCA5190. When deviating from this recommended layout, keep the following points in mind:

- All RF components must be kept as close as possible to the ADCA5190. These components include the transformers and all tuning components in series or shunt to the RF traces.
- Symmetry must be strictly maintained between the input and output balun.
- C29 and C30, the feedback capacitors, must be kept as close as possible to the ADCA5190 and must be referenced to the RF ground plane.
- When using active biasing, components around Q1 must be kept physically close to Q1.

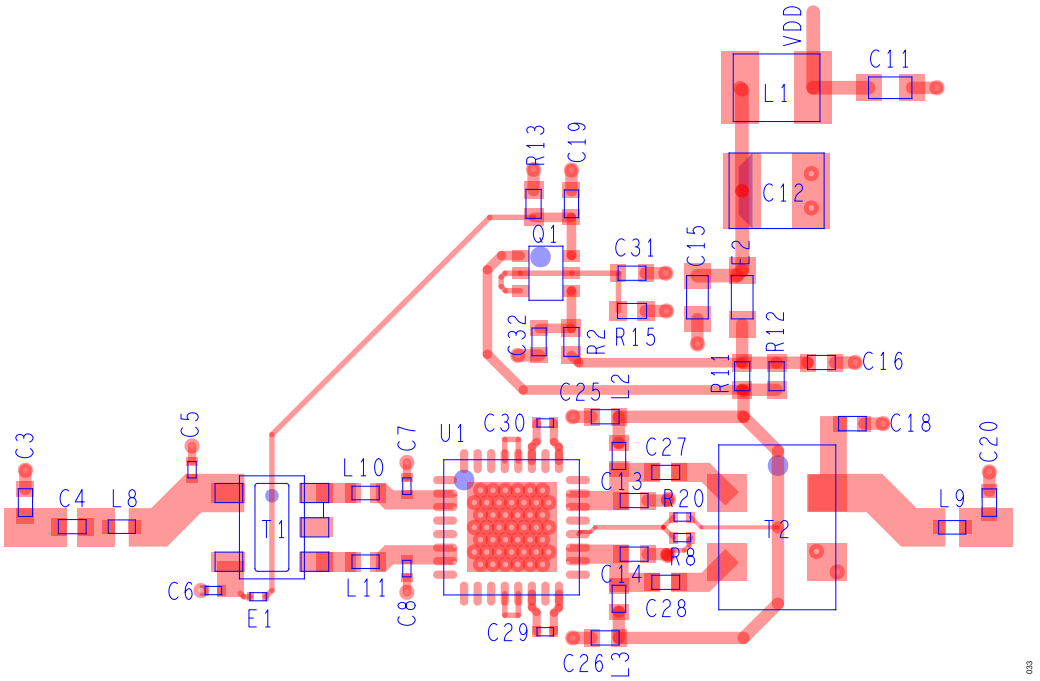


Figure 33. Suggested Downstream CATV Application Circuit with Active Biasing Layout

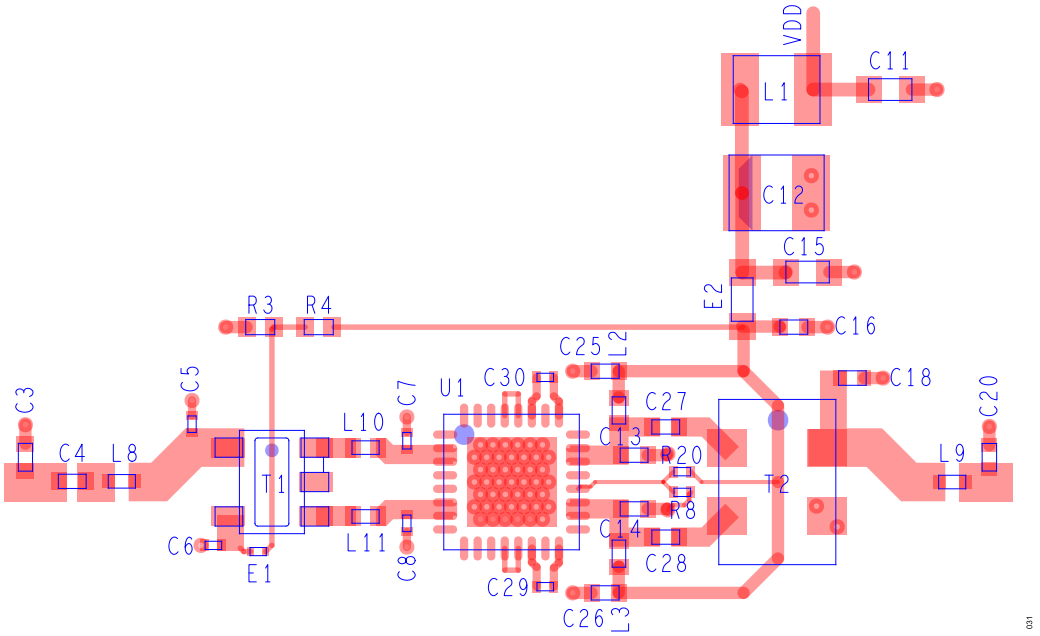


Figure 34. Suggested Downstream CATV Application Circuit with Passive Biasing Layout

OUTLINE DIMENSIONS

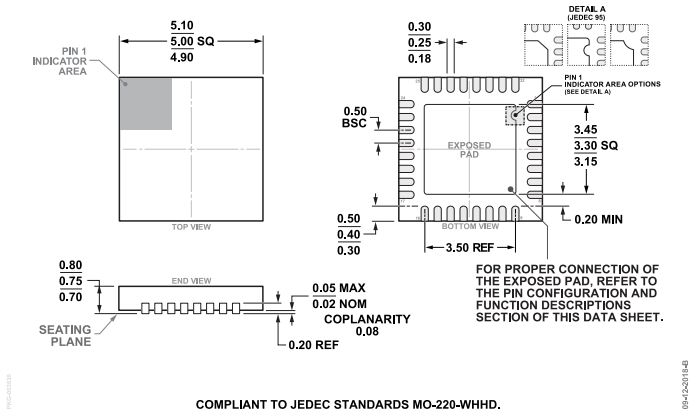


Figure 35. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-13)
Dimensions shown in millimeters

Updated: April 11, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADCA5190ACPZ	-40°C to +100°C	32-Lead LFCSP (5mm x 5mm x 0.75mm w/ EP)		CP-32-13
ADCA5190ACPZ-R7	-40°C to +100°C	32-Lead LFCSP (5mm x 5mm x 0.75mm w/ EP)	Reel, 1500	CP-32-13

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
ADCA5190-EVALZ	Evaluation Board for the Downstream Cable System Application

[1] Z = RoHS Compliant Part.