

MOSFET – Small Signal, N-Channel, Single

60 V, 340 mA, SC-70

2N7002W, 2V7002W

Features

- ESD Protected
- Low $R_{DS(on)}$
- Small Footprint Surface Mount Package
- 2V Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Low Side Load Switch
- Level Shift Circuits
- DC-DC Converter
- Portable Applications i.e. DSC, PDA, Cell Phone, etc.

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Rating	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DS}	60	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Drain Current (Note 1) Steady State	I_D	$T_A = 25^\circ\text{C}$	310	mA
		$T_A = 85^\circ\text{C}$	220	
$t < 5\text{ s}$	I_D	$T_A = 25^\circ\text{C}$	340	mA
		$T_A = 85^\circ\text{C}$	240	
Power Dissipation (Note 1) Steady State	P_D		280	mW
		$t < 5\text{ s}$	330	
Pulsed Drain Current ($t_p = 10\ \mu\text{s}$)	I_{DM}	1.4	A	
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	250	mA	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	
Gate-Source ESD Rating (HBM, Method 3015)	ESD	2000	V	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

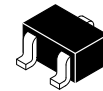
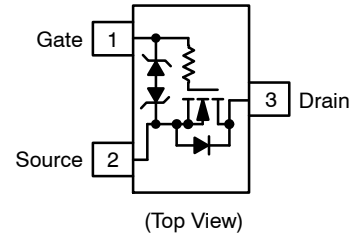
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	450	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – $t \leq 5\text{ s}$ (Note 1)	$R_{\theta JA}$	375	

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)

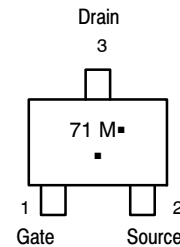
$V_{(BR)DSS}$	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$ (Note 1)
60 V	1.6 Ω @ 10 V	340 mA
	2.5 Ω @ 4.5 V	

SIMPLIFIED SCHEMATIC



SC-70/SOT-323
CASE 419
STYLE 8

MARKING DIAGRAM & PIN ASSIGNMENT



71 = Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
2N7002WT1G	SC-70 (Pb-Free)	3000/Tape & Reel
2V7002WT1G	SC-70 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

2N7002W, 2V7002W

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60	-	-	V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$		-	71	-	$\text{mV}/^\circ\text{C}$	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$	$T_J = 25^\circ\text{C}$	-	-	1.0	μA
			$T_J = 150^\circ\text{C}$	-	-	15	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}$	$T_J = 25^\circ\text{C}$	-	-	100	nA
			$T_J = 150^\circ\text{C}$	-	-	10	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	-	-	± 10	μA	
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 10\text{ V}$	-	-	450	nA	
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 5.0\text{ V}$	-	-	150	nA	

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.0	-	2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$		-	4.0	-	$\text{mV}/^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 500\text{ mA}$	-	1.19	1.6	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 200\text{ mA}$	-	1.33	2.5	
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 200\text{ mA}$	-	530	-	mS

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 20\text{ V}$	-	24.5	-	pF
Output Capacitance	C_{OSS}		-	4.2	-	
Reverse Transfer Capacitance	C_{RSS}		-	2.2	-	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}; I_D = 200\text{ mA}$	-	0.7	-	nC
Threshold Gate Charge	$Q_{G(TH)}$		-	0.1	-	
Gate-to-Source Charge	Q_{GS}		-	0.3	-	
Gate-to-Drain Charge	Q_{GD}		-	0.1	-	

SWITCHING CHARACTERISTICS, $V_{GS} = V$ (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DD} = 25\text{ V}, I_D = 500\text{ mA}, R_G = 25\ \Omega$	-	12.2	-	ns
Rise Time	t_r		-	9.0	-	
Turn-Off Delay Time	$t_{d(OFF)}$		-	55.8	-	
Fall Time	t_f		-	29	-	

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 200\text{ mA}$	$T_J = 25^\circ\text{C}$	-	0.8	1.2	V
			$T_J = 85^\circ\text{C}$	-	0.7	-	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

3. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

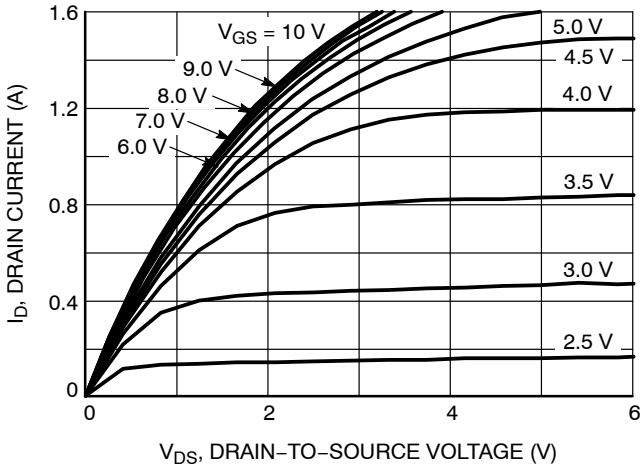


Figure 1. On-Region Characteristics

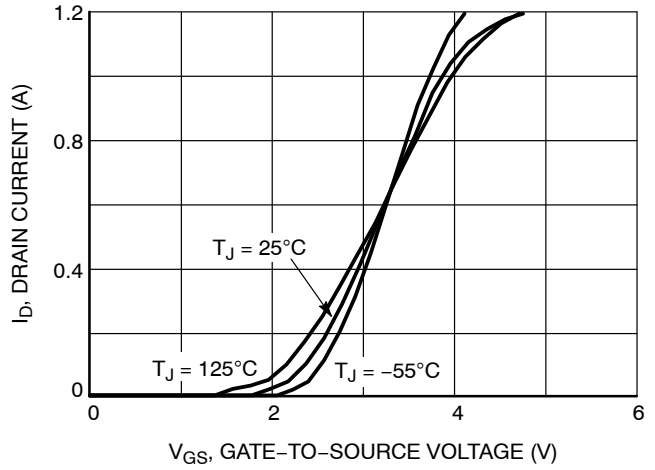


Figure 2. Transfer Characteristics

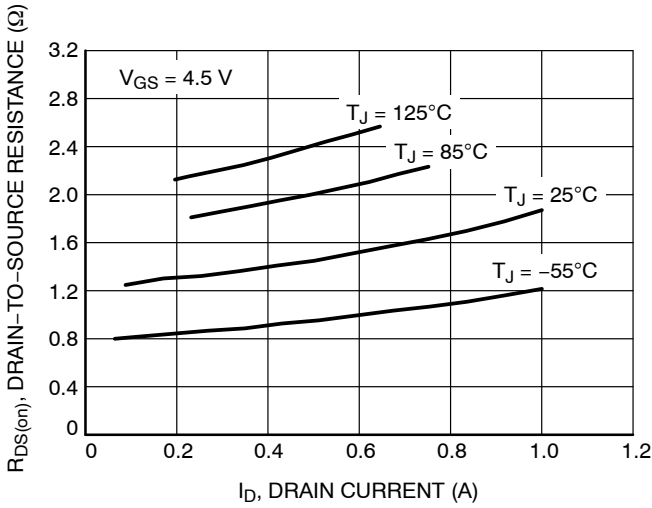


Figure 3. On-Resistance vs. Drain Current and Temperature

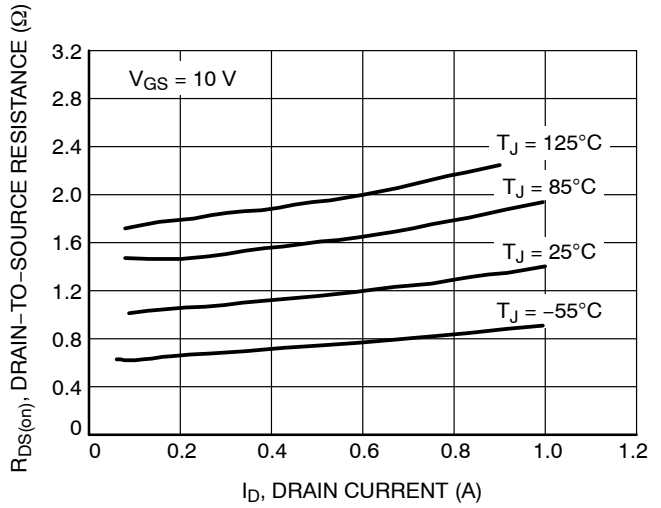


Figure 4. On-Resistance vs. Drain Current and Temperature

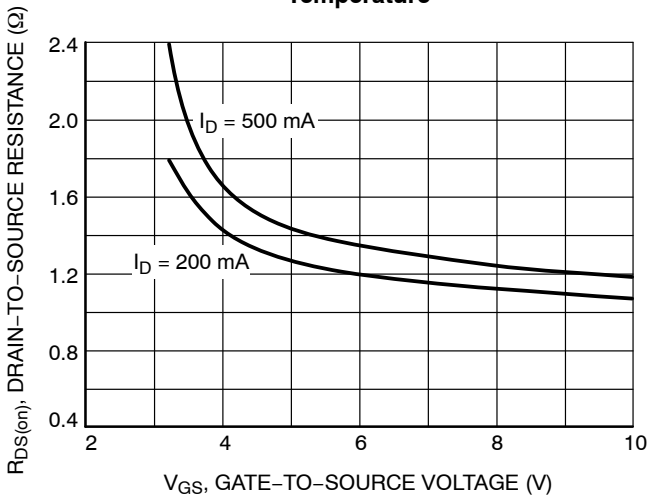


Figure 5. On-Resistance vs. Gate-to-Source Voltage

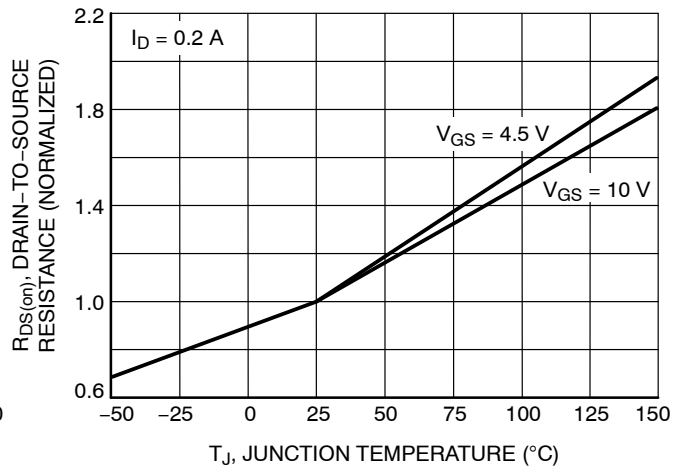


Figure 6. On-Resistance Variation with Temperature

TYPICAL CHARACTERISTICS

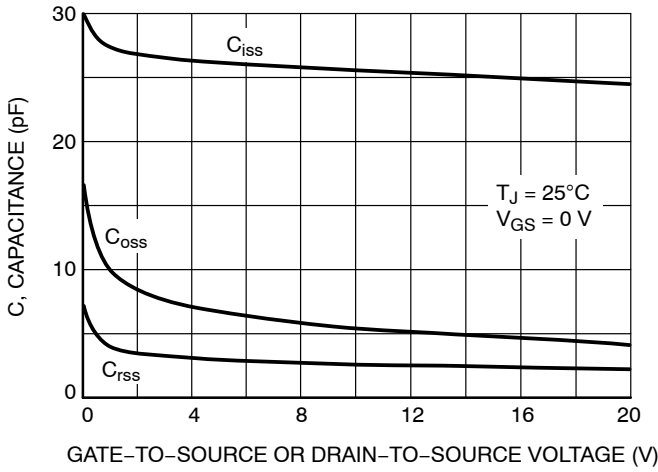


Figure 7. Capacitance Variation

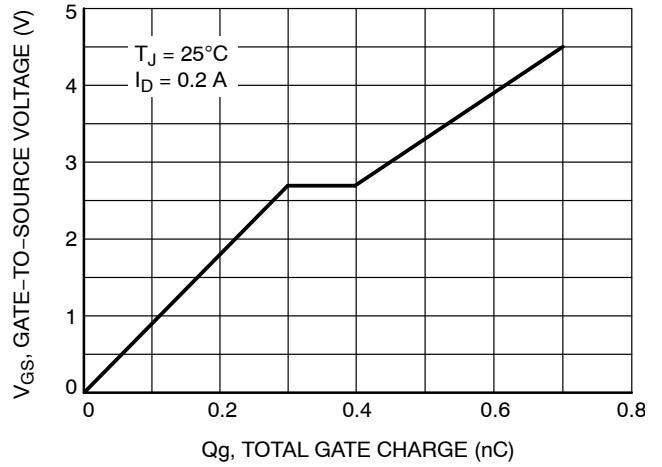


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

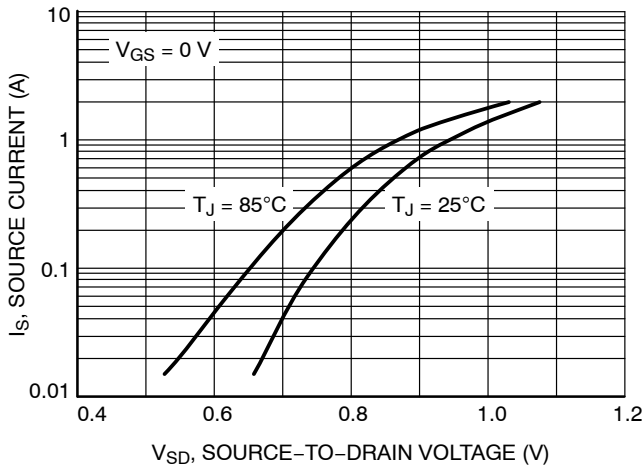


Figure 9. Diode Forward Voltage vs. Current

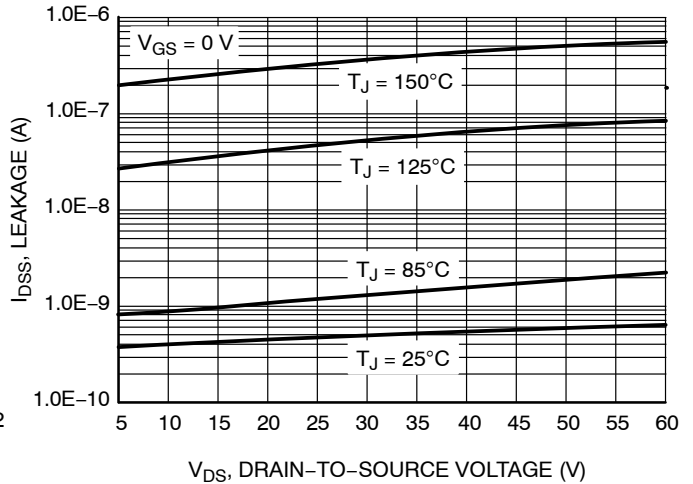


Figure 10. Drain-to-Source Leakage Current vs. Voltage

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 4:1

SC-70 (SOT-323) CASE 419 ISSUE R

DATE 11 OCT 2022



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2	0.70 REF			0.028 BSC		
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.00	2.20	0.071	0.080	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1	0.65 BSC			0.026 BSC		
L	0.20	0.38	0.56	0.008	0.015	0.022
H _E	2.00	2.10	2.40	0.079	0.083	0.095

GENERIC MARKING DIAGRAM



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.



* For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

SOLDERING FOOTPRINT

- | | | | | | |
|---|---|---|--|---|---|
| STYLE 1:
CANCELLED | STYLE 2:
PIN 1. ANODE
2. N.C.
3. CATHODE | STYLE 3:
PIN 1. BASE
2. EMITTER
3. COLLECTOR | STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE | STYLE 5:
PIN 1. ANODE
2. ANODE
3. CATHODE | |
| STYLE 6:
PIN 1. EMITTER
2. BASE
3. COLLECTOR | STYLE 7:
PIN 1. BASE
2. EMITTER
3. COLLECTOR | STYLE 8:
PIN 1. GATE
2. SOURCE
3. DRAIN | STYLE 9:
PIN 1. ANODE
2. CATHODE
3. CATHODE-ANODE | STYLE 10:
PIN 1. CATHODE
2. ANODE
3. ANODE-CATHODE | STYLE 11:
PIN 1. CATHODE
2. CATHODE
3. CATHODE |

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