

MPSW51, MPSW51A

One Watt High Current Transistors

PNP Silicon

Features

- These Devices are Pb-Free and are RoHS Compliant*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector - Emitter Voltage MPSW51 MPSW51A	V_{CEO}	-30 -40	Vdc
Collector - Base Voltage MPSW51 MPSW51A	V_{CBO}	-40 -50	Vdc
Emitter - Base Voltage	V_{EBO}	-5.0	Vdc
Collector Current - Continuous	I_C	-1000	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0 8.0	mW mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	2.5 20	W mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	125	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	50	$^\circ\text{C}/\text{W}$

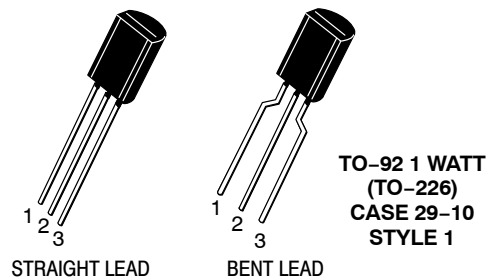
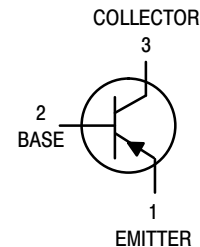
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

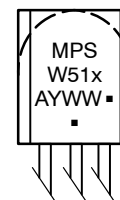


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MARKING DIAGRAM



- x = 51A Devices
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MPSW51, MPSW51A

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector – Emitter Breakdown Voltage (Note 1) (I _C = -1.0 mAdc, I _B = 0)	MPSW51 MPSW51A	V _{(BR)CEO}	-30 -40	- -	Vdc
Collector – Base Breakdown Voltage (I _C = -100 μAdc, I _E = 0)	MPSW51 MPSW51A	V _{(BR)CBO}	-40 -50	- -	Vdc
Emitter – Base Breakdown Voltage (I _E = -100 μAdc, I _C = 0)		V _{(BR)EBO}	-5.0	-	Vdc
Collector Cutoff Current (V _{CB} = -30 Vdc, I _E = 0) (V _{CB} = -40 Vdc, I _E = 0)	MPSW51 MPSW51A	I _{CBO}	- -	-0.1 -0.1	μAdc
Emitter Cutoff Current (V _{EB} = -3.0 Vdc, I _C = 0)		I _{EBO}	-	-0.1	μAdc

ON CHARACTERISTICS

DC Current Gain (I _C = -10 mAdc, V _{CE} = -1.0 Vdc) (I _C = -100 mAdc, V _{CE} = -1.0 Vdc) (I _C = -1000 mAdc, V _{CE} = -1.0 Vdc)		h _{FE}	55 60 50	- - -	-
Collector – Emitter Saturation Voltage (I _C = -1000 mAdc, I _B = -100 mAdc)		V _{CE(sat)}	-	-0.7	Vdc
Base – Emitter On Voltage (I _C = -1000 mAdc, V _{CE} = -1.0 Vdc)		V _{BE(on)}	-	-1.2	Vdc

SMALL-SIGNAL CHARACTERISTICS

Current-Gain – Bandwidth Product (I _C = -50 mAdc, V _{CE} = -10 Vdc, f = 20 MHz)		f _T	50	-	MHz
Output Capacitance (V _{CB} = -10 Vdc, I _E = 0, f = 1.0 MHz)		C _{obo}	-	30	pF

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

ORDERING INFORMATION

Device	Package	Shipping [†]
MPSW51G	TO-92 (Pb-Free)	5000 Units / Bulk
MPSW51AG	TO-92 (Pb-Free)	5000 Units / Bulk
MPSW51RLRAG	TO-92 (Pb-Free)	2000 / Tape & Reel
MPSW51ARLRAG	TO-92 (Pb-Free)	2000 / Tape & Reel
MPSW51ARLRPG	TO-92 (Pb-Free)	2000 / Ammo Pack

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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TYPICAL CHARACTERISTICS

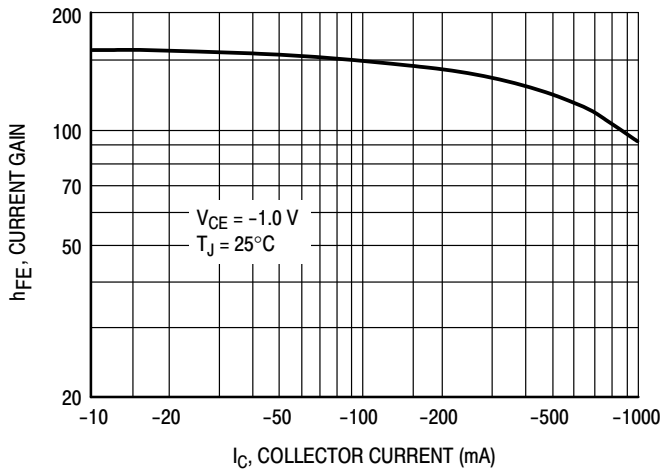


Figure 1. DC Current Gain

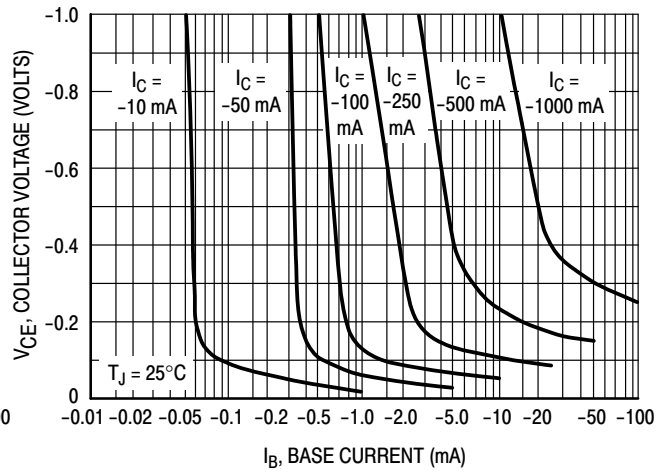


Figure 2. Collector Saturation Region

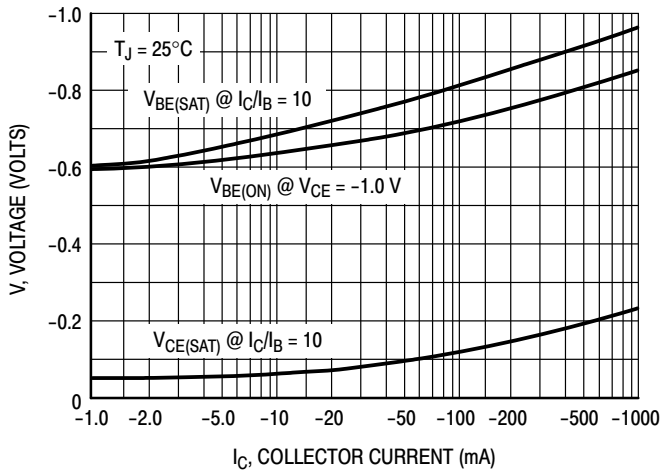


Figure 3. "ON" Voltages

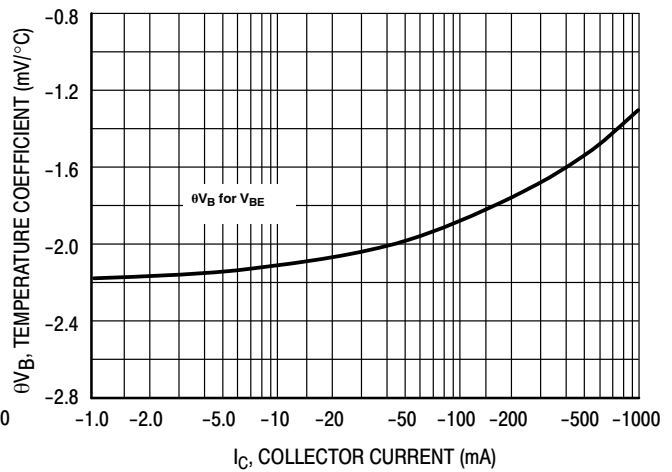


Figure 4. Temperature Coefficient

MPSW51, MPSW51A

TYPICAL CHARACTERISTICS

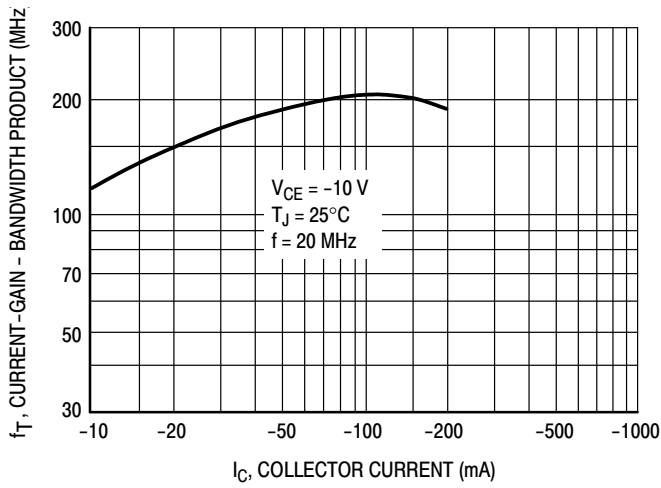


Figure 5. Current Gain — Bandwidth Product

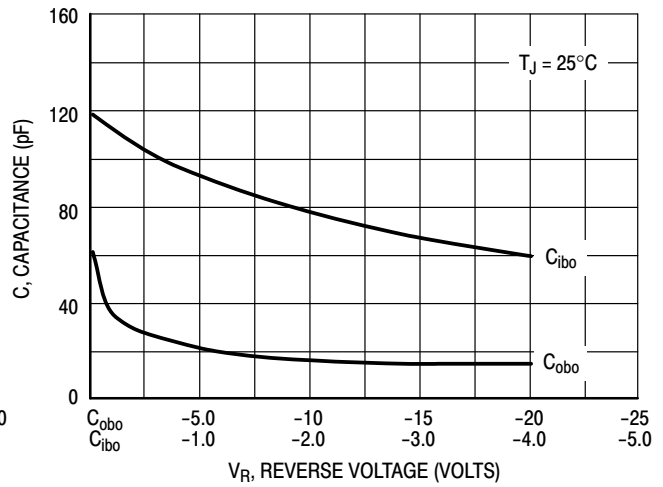


Figure 6. Capacitance

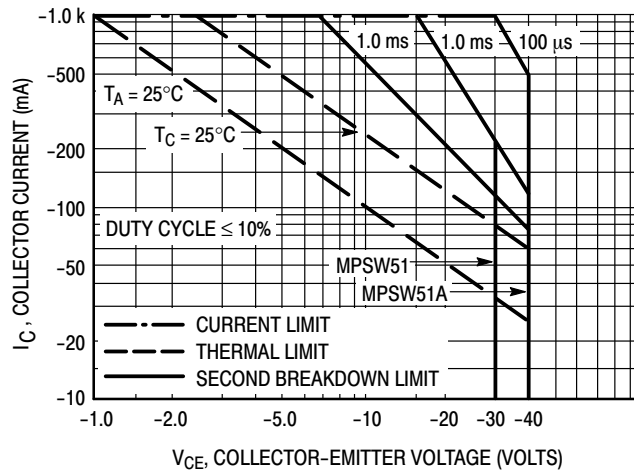


Figure 7. Active Region — Safe Operating Area

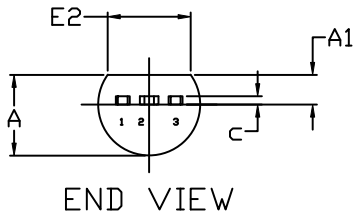
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



TO-92 (TO-226) 1 WATT
CASE 29-10
ISSUE D

DATE 05 MAR 2021

STRAIGHT LEAD



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	3.75	3.90	4.05
A1	1.28	1.43	1.58
b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	1.27 BSC		
L	13.80	14.00	14.20

STYLES AND MARKING ON PAGE 3

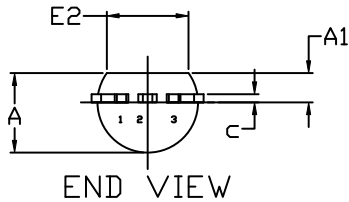
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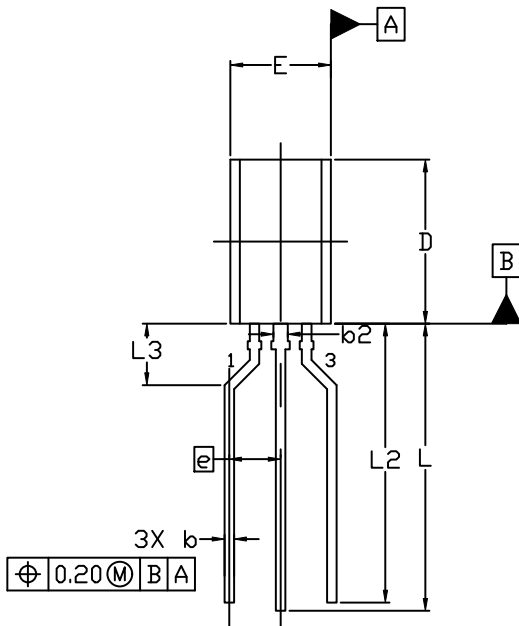
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FORMED LEAD



END VIEW



TOP VIEW

NOTES:

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DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
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D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	2.50 BSC		
L	13.80	14.00	14.20
L2	13.20	13.60	14.00
L3	3.00 REF		

STYLES AND MARKING ON PAGE 3

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**TO-92 (TO-226) 1 WATT
CASE 29-10
ISSUE D**

DATE 05 MAR 2021

- | | | | | |
|-----------------------------------------------------------------------------|--------------------------------------------------------------------------------|----------------------------------------------------------------------------|---------------------------------------------------------------------------|-----------------------------------------------------------------------|
| <p>STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR</p> | <p>STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR</p> | <p>STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE</p> | <p>STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE</p> | <p>STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE</p> |
| <p>STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN</p> | <p>STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE</p> | <p>STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE</p> | <p>STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2</p> | <p>STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE</p> |
| <p>STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE</p> | <p>STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2</p> | <p>STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2</p> | <p>STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE</p> | <p>STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2</p> |
| <p>STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE</p> | <p>STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER</p> | <p>STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED</p> | <p>STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE</p> | <p>STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE</p> |
| <p>STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE</p> | <p>STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN</p> | <p>STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN</p> | <p>STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE</p> | <p>STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2</p> |
| <p>STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT</p> | <p>STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT</p> | <p>STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE</p> | <p>STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE</p> | <p>STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE</p> |
| <p>STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE</p> | <p>STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER</p> | <p>STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT</p> | <p>STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC</p> | <p>STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER</p> |

**GENERIC
MARKING DIAGRAM***



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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