1 A/0.6 A DC to DC Switching Regulator with Independent Positive and Negative Outputs

Data Sheet **ADP5072**

FEATURES

- Input supply voltage range: 2.85 V to 5.5 V
- Generates well regulated, independently resistor programmable V_{POS} and V_{NEG} outputs
- Boost regulator to generate V_{POS} output
  - Adjustable positive output to 35 V
  - Integrated 1.0 A main switch
- Inverting regulator to generate V_{NEG} output
  - Adjustable negative output to −30 V
  - Integrated 0.6 A main switch
- 1.2 MHz/2.4 MHz switching frequency with optional external frequency synchronization from 1.0 MHz to 2.6 MHz
- Resistor programmable soft start timer
- Slew rate control for lower system noise
- Individual precision enable and flexible start-up sequence control for symmetric start, V_{POS} first, or V_{NEG} first
- Out of phase operation
- UVLO, OCP, OVP, and TSD protection
- 1.61 mm × 2.18 mm, 20-ball WLCSP
- −40°C to +125°C junction temperature range

APPLICATIONS

- Bipolar amplifiers, ADCs, DACs, and multiplexers
- Charge coupled device (CCD) bias supply
- Optical module supply
- RF power amplifier bias
- Time of flight module supply

TYPICAL APPLICATION CIRCUIT

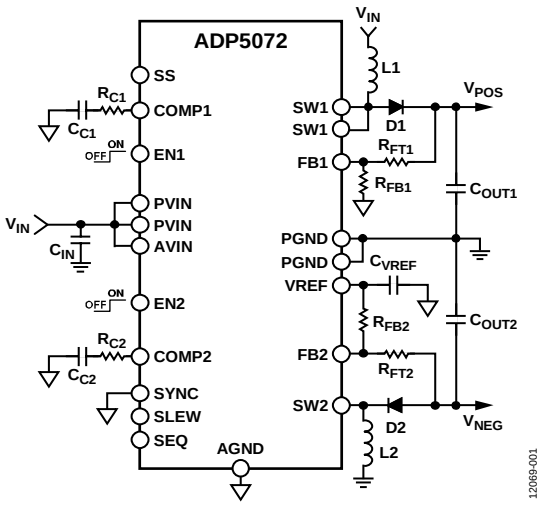

Figure 1.

GENERAL DESCRIPTION

The ADP5072 is a dual, high performance dc-to-dc regulator that generates independently regulated positive and negative rails.

The input voltage range of 2.85 V to 5.5 V supports a wide variety of applications. The integrated main switch in both regulators enables generation of an adjustable positive output voltage up to 35 V and a negative output voltage down to −30 V.

The ADP5072 operates at a pin selected 1.2 MHz or 2.4 MHz switching frequency. The ADP5072 can synchronize with an external oscillator from 1.0 MHz to 2.6 MHz to ease noise filtering in sensitive applications. Both regulators implement programmable slew rate control circuitry for the MOSFET driver stage to reduce electromagnetic interference (EMI). Flexible start-up sequencing is provided with the options of manual enable, simultaneous mode, positive supply first, and negative supply first.

The ADP5072 includes a fixed internal or resistor programmable soft start timer to prevent inrush current at power-up.

Other key safety features in the ADP5072 include overcurrent protection (OCP), overvoltage protection (OVP), thermal shutdown (TSD), and input undervoltage lockout (UVLO).

The ADP5072 is available in a 20-ball WLCSP and is rated for a −40°C to +125°C junction temperature range.

Table 1. Family Models

Model	Boost Switch (A)	Inverter Switch (A)	Package
ADP5070	1.0	0.6	20-lead LFCSP (4 mm× 4 mm) and 20-lead TSSOP
ADP5071	2.0	1.2	20-lead LFCSP (4 mm × 4 mm) and 20-lead TSSOP
ADP5072	1.0	0.6	20-ball WLCSP (1.61 mm × 2.18 mm)
ADP5073	Not applicable	1.2	16-lead LFCSP (3 mm × 3 mm)
ADP5074	Not applicable	2.4	16-lead LFCSP (3 mm × 3 mm)
ADP5075	Not applicable	0.8	12-ball WLCSP (1.61 mm × 2.18 mm)
ADP5076	2.0	1.2	20-ball WLCSP (1.61 mm × 2.18 mm)

Rev. A Document Feedback

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1/2019—Revision 0: Initial Version

SPECIFICATIONS

PVIN = AVIN = 2.85 V to 5.5 V, positive output voltage (V_{POS}) = 15 V, negative output voltage (V_{NEG}) = −15 V, f_{SW} = 1200 kHz, T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT SUPPLY VOLTAGE RANGE	V_{IN}	2.85		5.5	V	PVIN, AVIN
QUIESCENT CURRENT						
Operating Quiescent Current						
PVIN, AVIN (Total)	I_Q		3.5	4.0	mA	No switching, EN1 = EN2 = high
Standby Current	I_{STNDBY}		2.05	2.2	mA	No switching, EN1 = EN2 = low
UVLO						
System UVLO Threshold						AVIN
Rising	V_{UVLO_RISING}		2.8	2.85	V	
Falling	$V_{UVLO\_FALLING}$	2.5	2.55		V	
Hysteresis	V_{HYS}		0.25		V	
OSCILLATOR CIRCUIT						
Switching Frequency	f_{SW}	1.130	1.2	1.270	MHz	SYNC = low
		2.240	2.4	2.560	MHz	SYNC = high (connect to AVIN)
SYNC Input						
Input Clock Range	f_{SYNC}	1.0		2.6	MHz	
Input Clock Minimum On Pulse Width	$t_{SYNC\_MIN\_ON}$	100			ns	
Input Clock Minimum Off Pulse Width	$t_{SYNC\_MIN\_OFF}$	100			ns	
Input Clock High Logic	$V_{H\ (SYNC)}$			1.3	V	
Input Clock Low Logic	$V_{L\ (SYNC)}$	0.4			V	
PRECISION ENABLING (EN1, EN2)						
High Level Threshold	V_{TH_H}	1.125	1.15	1.175	V	
Low Level Threshold	V_{TH_L}	1.025	1.05	1.075	V	
Shutdown Mode	V_{TH_S}	0.4			V	Internal circuitry disabled to achieve I_{STNDBY}
Pull-Down Resistance	R_{EN}		1.48		MΩ	
BOOST REGULATOR						
Adjustable Positive Output Voltage	V_{POS}			35	V	
Feedback Voltage	V_{FB1}		0.8		V	
Feedback Voltage Accuracy		−0.5		+0.5	%	T_J = 25°C
		−1.5		+1.5	%	T_J = −40°C to +125°C
Feedback Bias Current	I_{FB1}			0.1	µA	
Overvoltage Protection Threshold	V_{OV1}		0.86		V	At FB1 pin
Load Regulation	$(\Delta V_{FB1}/V_{FB1})/\Delta I_{LOAD1}$		0.0003		%/mA	I_{LOAD1}[1] = 5 mA to 150 mA
Line Regulation	$(\Delta V_{FB1}/V_{FB1})/\Delta V_{PVIN}$		0.002		%/V	I_{LOAD1} = 50 mA
Error Amplifier (EA) Transconductance	g_{M1}	260	300	340	µA/V	
Power FET On Resistance	$R_{DS\ (ON)\ BOOST}$		175		mΩ	
Power FET Maximum Drain Source Voltage	$V_{DS\ (MAX)\ BOOST}$		39		V	
Current-Limit Threshold, Main Switch	$I_{LIM\ (BOOST)}$	1.0	1.1	1.3	A	
Minimum On Time			50		ns	
Minimum Off Time			25		ns	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
INVERTING REGULATOR						
Adjustable Negative Output Voltage	V_{NEG}	−30			V	
Reference Voltage	V_{REF}		1.60		V	
Reference Voltage Accuracy		−0.5		+0.5	%	T_J = 25°C
		−1.5		+1.5	%	T_J = −40°C to +125°C
Feedback Voltage	$V_{REF} - V_{FB2}$		0.8		V	
Feedback Voltage Accuracy		−0.5		+0.5	%	T_J = 25°C
		−1.5		+1.5	%	T_J = −40°C to +125°C
Feedback Bias Current	I_{FB2}			0.1	µA	
Overvoltage Protection Threshold	V_{OV2}		0.74		V	At FB2 pin after soft start has completed
Load Regulation	$(\Delta(V_{REF} - V_{FB2})/(V_{REF} - V_{FB2}))/I_{LOAD2}$		0.0004		%/mA	I_{LOAD2} = 5 mA to 75 mA
Line Regulation	$(\Delta(V_{REF} - V_{FB2})/(V_{REF} - V_{FB2}))/V_{PVIN}$		0.003		%/V	I_{LOAD2} = 25 mA
EA Transconductance	g_{M2}	260	300	340	µA/V	
Power FET On Resistance	$R_{DS\ (ON)\ INVERTER}$		350		mΩ	
Power FET Maximum Drain Source Voltage	$V_{DS\ (MAX)\ INVERTER}$		39		V	
Current-Limit Threshold, Main Switch	$I_{LIM\ (INVERTER)}$	600	660	750	mA	
Minimum On Time			60		ns	
Minimum Off Time			50		ns	
SOFT START						
Soft Start Timer for DC to DC Regulators	t_{SS}		4		ms	SS = open
			32		ms	SS resistor = 50 kΩ to GND
Hiccup Time	t_{HICCUP}		$8 \times t_{SS}$		ms	
THERMAL SHUTDOWN						
Threshold	T_{SHDN}		150		°C	
Hysteresis	T_{HYS}		15		°C	

[1] I_{LOADx} is the current through a resistive load connected across the output capacitor (where x is 1 for the boost regulator load and 2 for the inverting regulator load).

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
PVIN, AVIN	−0.3 V to +6V
SW1	−0.3 V to +40 V
SW2	PVIN − 40 V to PVIN + 0.3 V
PGND, AGND	−0.3 V to +0.3 V
EN1, EN2, FB1, FB2, SYNC	−0.3 V to +6 V
COMP1, COMP2, SLEW, SS, SEQ, VREF	−0.3 V to AVIN + 0.3 V
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance. ψ_{JT} is the junction to case thermal characterization parameter.

θ_{JA} and Ψ_{JT} are based on a 4-layer PCB (two signal and two power planes). θ_{JC} is measured at the top of the package and is independent of the PCB. The Ψ_{JT} value is more appropriate for calculating junction to case temperature in the application.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Ψ_{JT}	Unit
CB-20-14	50	0.54	0.13	C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

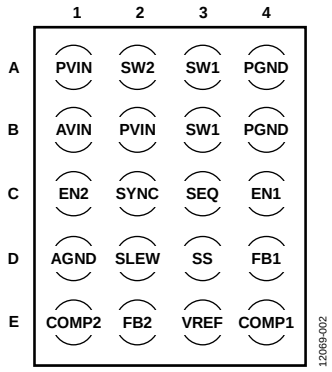

Figure 2. Pin Configuration (Top View)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1, B2	PVIN	Power Input for the Inverter Regulator.
A2	SW2	Switching Node for the Inverting Regulator.
A3, B3	SW1	Switching Node for the Boost Regulator.
A4, B4	PGND	Power Ground for the Boost Regulator.
B1	AVIN	System Power Supply for the ADP5072.
C1	EN2	Inverting Regulator Precision Enable. The EN2 pin is compared to an internal precision reference to enable the inverting regulator output.
C2	SYNC	Frequency Setting and Synchronization Input. To set the switching frequency to 2.4 MHz, pull the SYNC pin high. To set the switching frequency to 1.2 MHz, pull the SYNC pin low. To synchronize the switching frequency, connect the SYNC pin to an external clock.
C3	SEQ	Start-Up Sequence Control. For manual V_{POS}/V_{NEG} startup using an individual precision enabling pin, leave the SEQ pin open. For simultaneous V_{POS}/V_{NEG} startup when the EN2 pin rises, connect the SEQ pin to the AVIN pin. (The EN1 pin can be used to enable the internal references early, if required.) For a sequenced startup, pull the SEQ pin low. Either EN1 or EN2 can be used, and the corresponding supply is the first in sequence. Hold the other enable pin low.
C4	EN1	Boost Regulator Precision Enable. The EN1 pin is compared to an internal precision reference to enable the boost regulator output.
D1	AGND	Analog Ground.
D2	SLEW	Driver Stage Slew Rate Control. The SLEW pin sets the slew rate for the SW1 and SW2 drivers. For the fastest slew rate (best efficiency), leave the SLEW pin open. For normal slew rate, connect the SLEW pin to the AVIN pin. For the slowest slew rate (best noise performance), connect the SLEW pin to the AGND pin.
D3	SS	Soft Start Programming. Leave the SS pin open to obtain the fastest soft start time. To program a slower soft start time, connect a resistor between the SS pin and AGND.
D4	FB1	Feedback Input for the Boost Regulator. Connect a resistor divider between the positive side of the boost regulator output capacitor and AGND to program the output voltage.
E1	COMP2	Error Amplifier Compensation for the Inverting Regulator. Connect the compensation network between this pin and AGND.
E2	FB2	Feedback Input for the Inverting Regulator. Connect a resistor divider between the negative side of the inverting regulator output capacitor and VREF to program the output voltage.
E3	VREF	Inverting Regulator Reference Output. Connect a 1.0 µF ceramic filter capacitor between the VREF pin and AGND.
E4	COMP1	Error Amplifier Compensation for the Boost Regulator. Connect the compensation network between this pin and AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

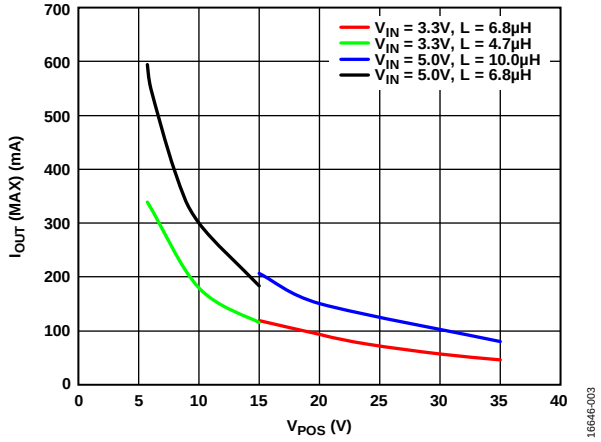

Figure 3. Maximum Output Current (I_{OUT}) vs. V_{POS} for Boost Regulator, f_{SW} = 1.2 MHz, T_A = 25°C, Based on Target of 70% $I_{LIM\ (BOOST)}$

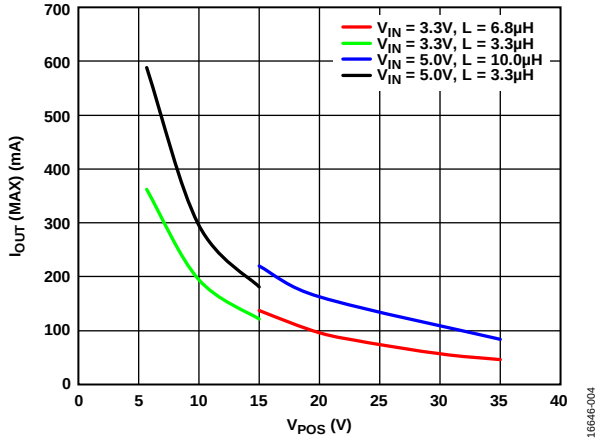

Figure 4. Maximum Output Current (I_{OUT}) vs. V_{POS} for Boost Regulator, f_{SW} = 2.4 MHz, T_A = 25°C, Based on Target of 70% $I_{LIM\ (BOOST)}$

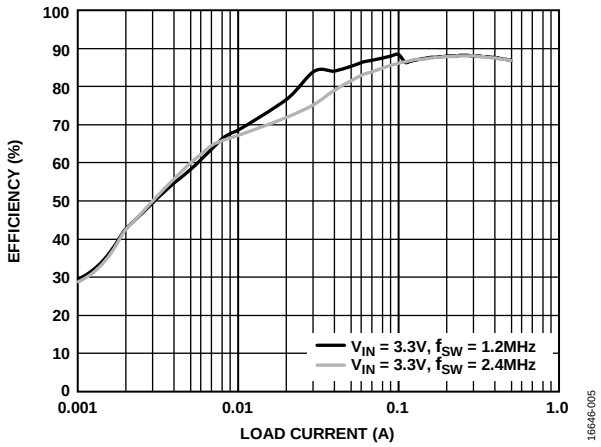

Figure 5. Efficiency vs. Load Current for Boost Regulator, V_{IN} = 3.3 V, V_{POS} = 5 V, T_A = 25°C

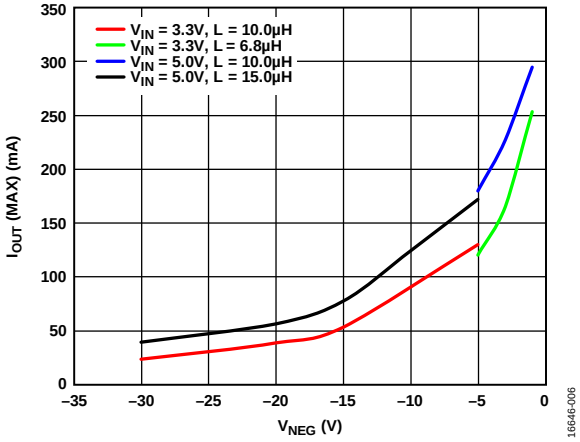

Figure 6. Maximum Output Current (I_{OUT}) vs. V_{NEG} for Inverting Regulator, f_{SW} = 1.2 MHz, T_A = 25°C, Based on Target of 70% $I_{LIM\ (INVERTER)}$

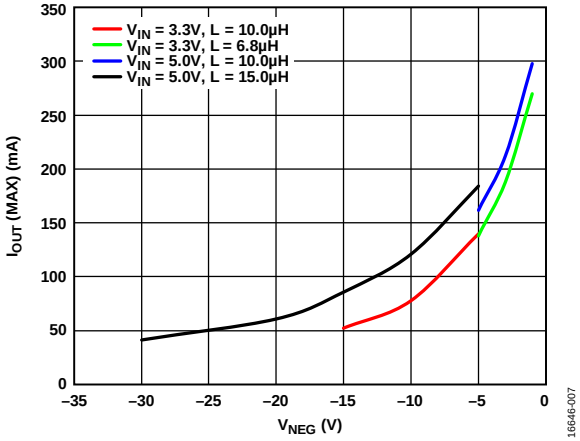

Figure 7. Maximum Output Current (I_{OUT}) vs. V_{NEG} for Inverting Regulator, f_{SW} = 2.4 MHz, T_A = 25°C, Based on Target of 70% $I_{LIM\ (INVERTER)}$

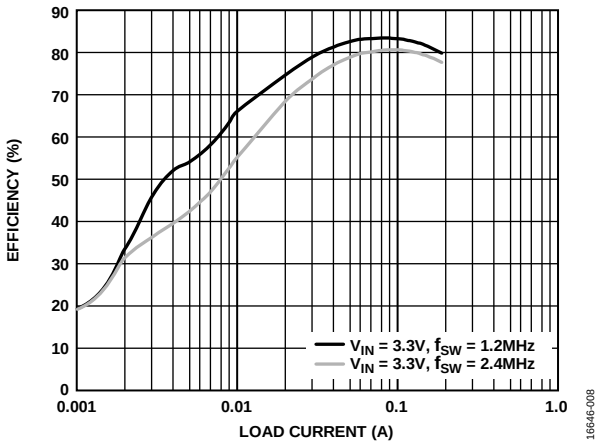

Figure 8. Efficiency vs. Load Current for Inverting Regulator, V_{IN} = 3.3 V, V_{NEG} = −5 V, T_A = 25°C

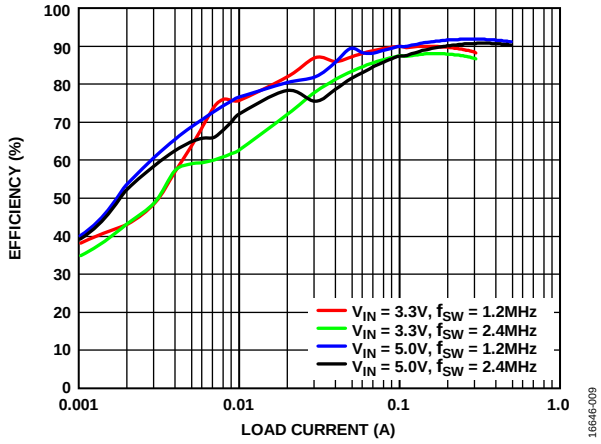

Figure 9. Efficiency vs. Load Current for Boost Regulator, V_{POS} = 9 V, T_A = 25°C

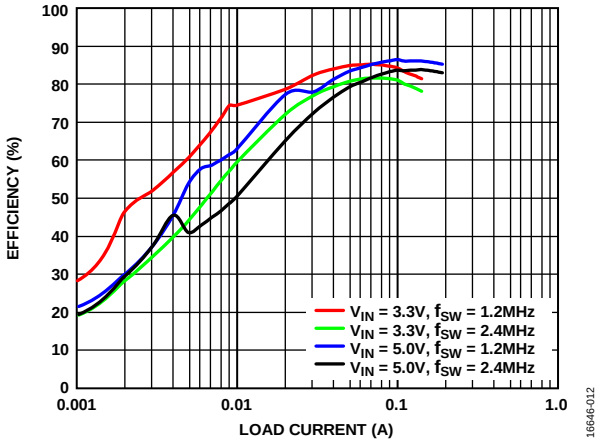

Figure 12. Efficiency vs. Load Current for Inverting Regulator, V_{NEG} = −9 V, T_A = 25°C

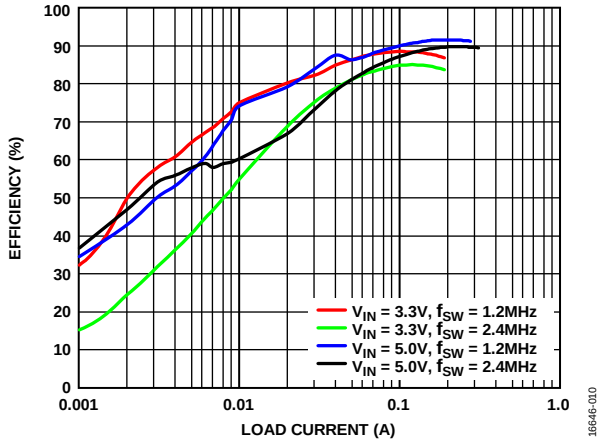

Figure 10. Efficiency vs. Load Current for Boost Regulator, V_{POS} = 15 V, T_A = 25°C

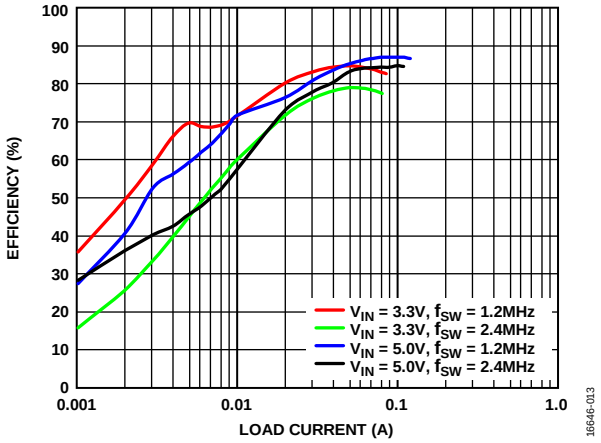

Figure 13. Efficiency vs. Load Current for Inverting Regulator, V_{NEG} = −15 V, T_A = 25°C

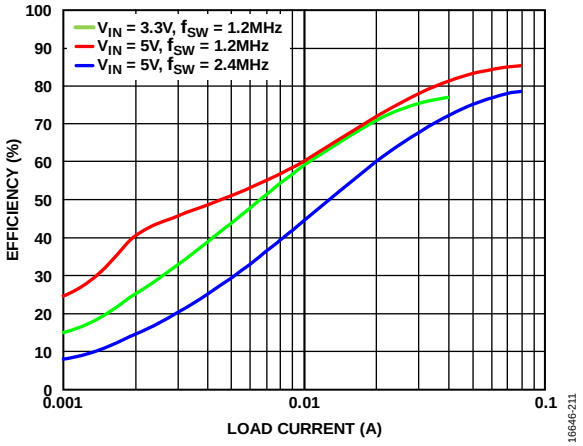

Figure 11. Efficiency vs. Load Current for Boost Regulator, V_{POS} = 35 V, T_A = 25°C

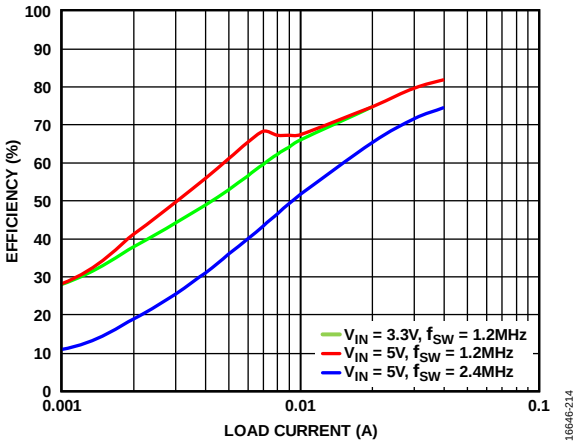

Figure 14. Efficiency vs. Load Current for Inverting Regulator, V_{NEG} = −30 V, T_A = 25°C

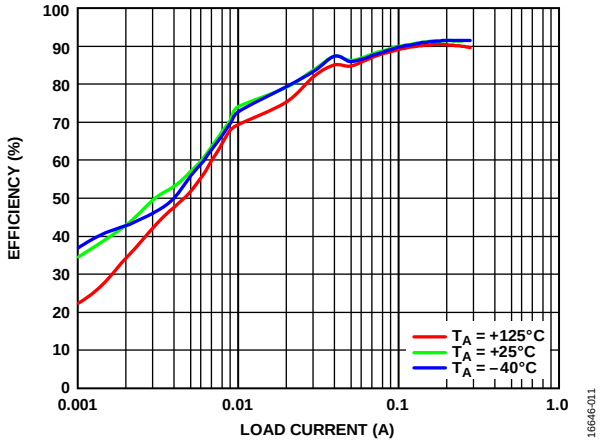

Figure 15. Efficiency vs. Load Current for Boost Regulator over Temperature, V_{IN} = 5 V, V_{POS} = 15 V, f_{SW} = 1.2 MHz

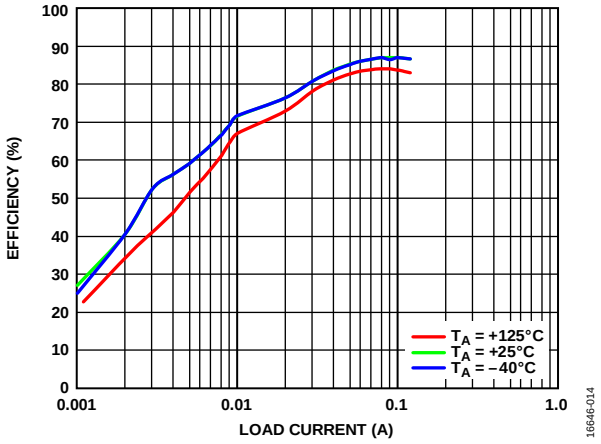

Figure 18. Efficiency vs. Load Current for Inverting Regulator over Temperature, V_{IN} = 5 V, V_{NEG} = −15 V, f_{SW} = 1.2 MHz

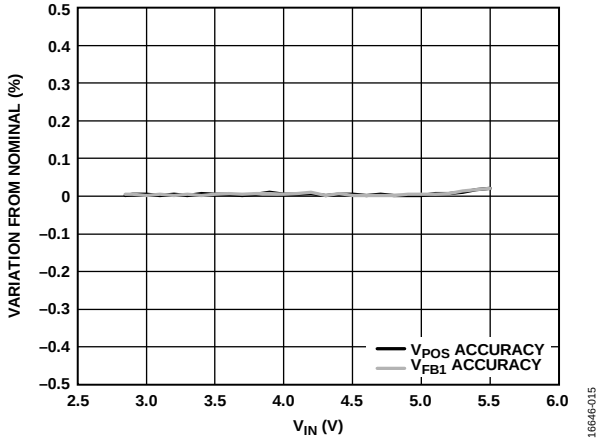

Figure 16. Boost Regulator Line Regulation, V_{POS} = 15 V, f_{SW} = 1.2 MHz, 15 mA Load, T_A = 25°C

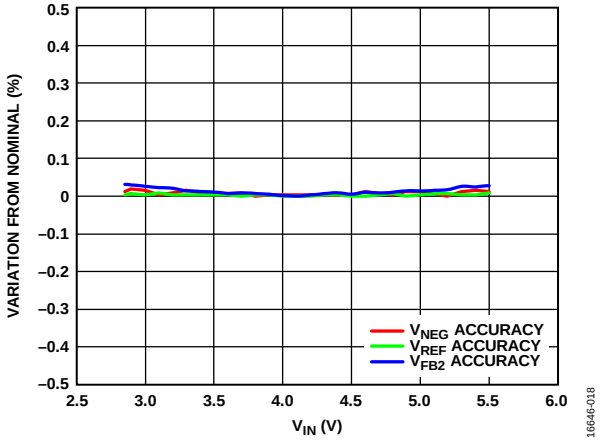

Figure 19. Inverting Regulator Line Regulation, V_{NEG} = −15 V, f_{SW} = 1.2 MHz, 15 mA Load, T_A = 25°C

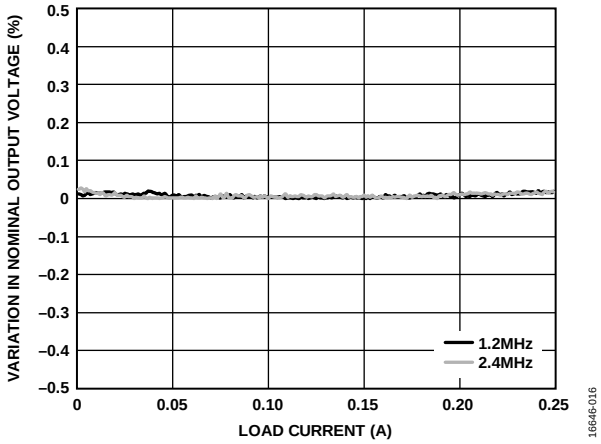

Figure 17. Boost Regulator Load Regulation, V_{IN} = 5 V, V_{POS} = 15 V

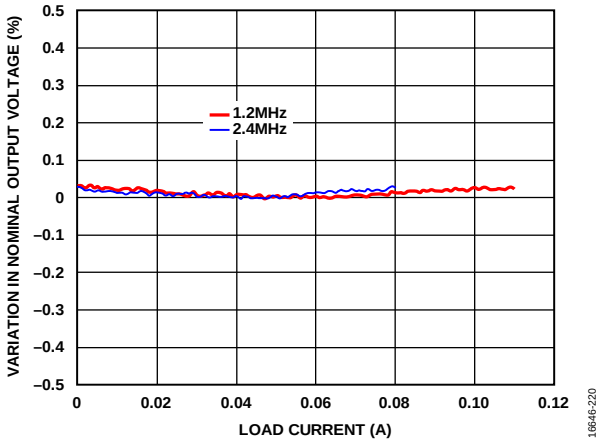

Figure 20. Inverting Regulator Load Regulation, V_{IN} = 5 V, V_{NEG} = −15 V

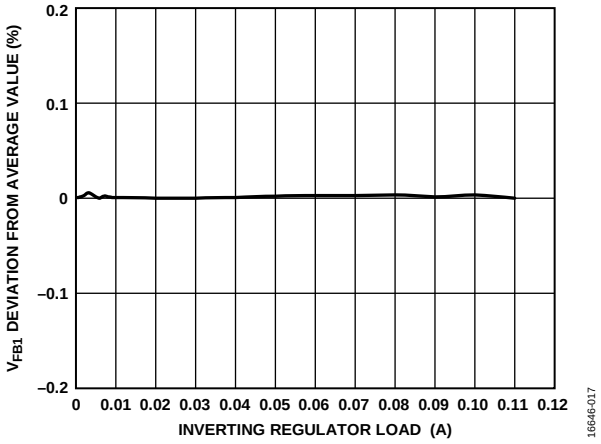

Figure 21. Cross Regulation, Boost Regulator V_{FB1} Regulation, V_{IN} = 5 V, V_{POS} = 15 V, V_{NEG} = −15 V, f_{SW} = 2.4 MHz, T_A = 25°C, Boost Regulator Run in Continuous Conduction Mode with Fixed Load for Test

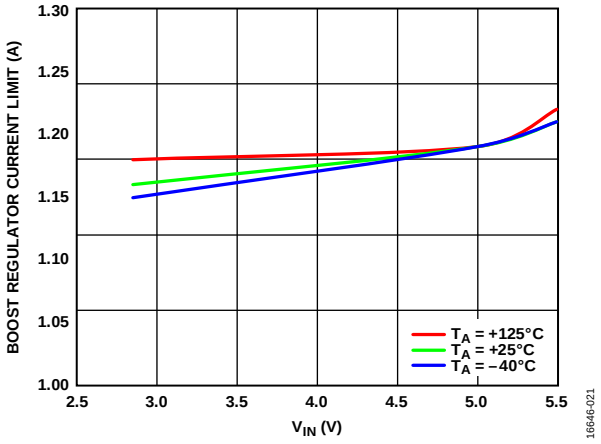

Figure 22. Boost Regulator Current Limit (I_{LIMIT}) vs. Input Voltage (V_{IN}) over Temperature

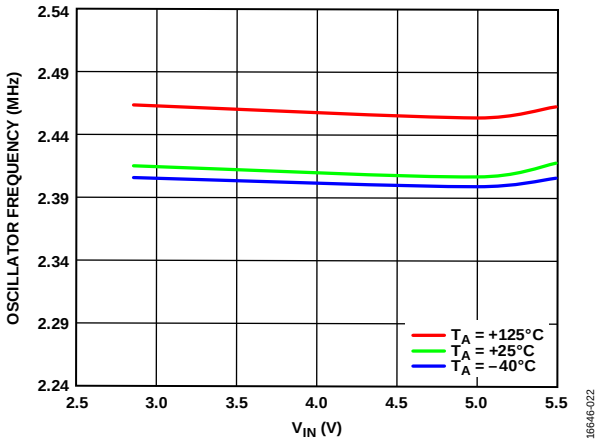

Figure 23. Oscillator Frequency vs. Input Voltage (V_{IN}) over Temperature, SYNC Pin = High

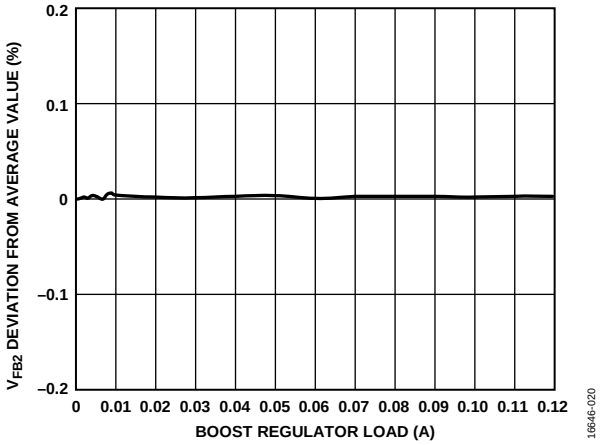

Figure 24. Cross Regulation, Inverting Regulator V_{FB2} Regulation, V_{IN} = 5 V, V_{POS} = 15 V, V_{NEG} = −15 V, f_{SW} = 2.4 MHz, T_A = 25°C, Inverting Regulator Run in Continuous Conduction Mode with Fixed Load for Test

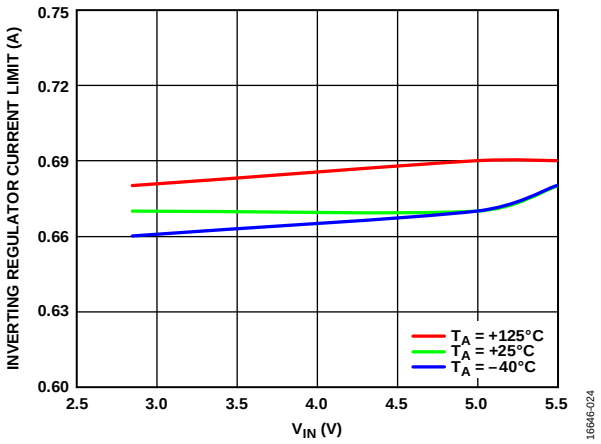

Figure 25. Inverting Regulator Current Limit (I_{LIMIT}) vs. Input Voltage (V_{IN}) over Temperature

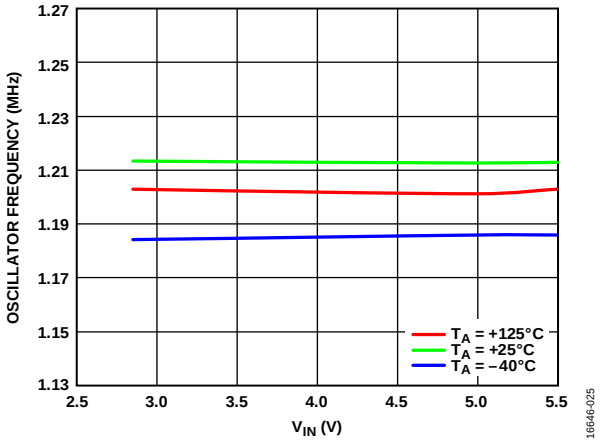

Figure 26. Oscillator Frequency vs. Input Voltage (V_{IN}) over Temperature, SYNC Pin = Low

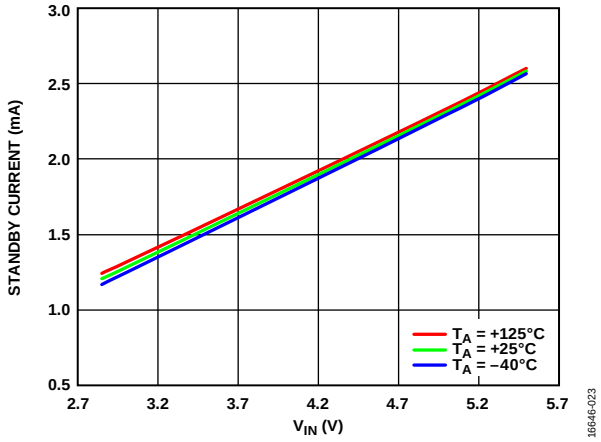

Figure 27. Standby Current vs. Input Voltage (V_{IN}) over Temperature, Both ENx Pins Below Shutdown Threshold

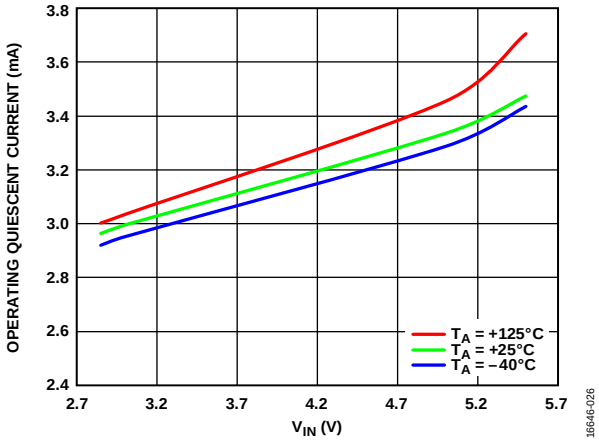

Figure 30. Operating Quiescent Current vs. Input Voltage (V_{IN}) over Temperature, Both ENx Pins On

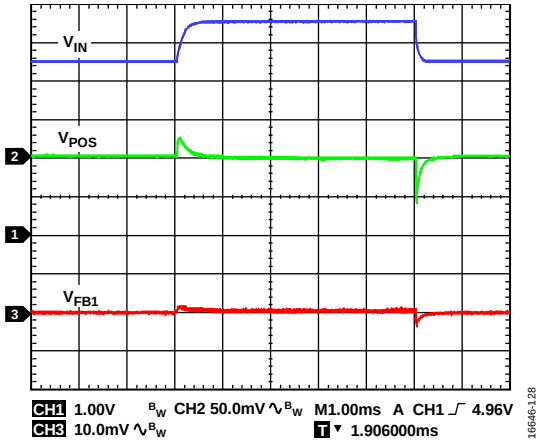

Figure 28. Boost Regulator Line Transient, V_{IN} = 4.5 V to 5.5 V Step, V_{POS} = 15 V, R_{LOAD1} = 300 Ω, f_{SW} = 2.4 MHz, T_A = 25°C

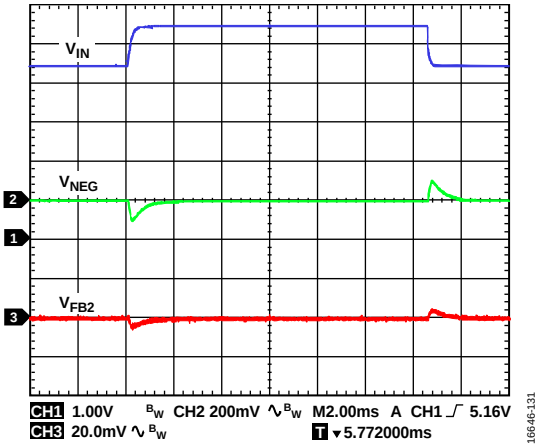

Figure 31. Inverting Regulator Line Transient, V_{IN} = 4.5 V to 5.5 V Step, V_{NEG} = −15 V, R_{LOAD2} = 300 Ω, f_{SW} = 2.4 MHz, T_A = 25°C

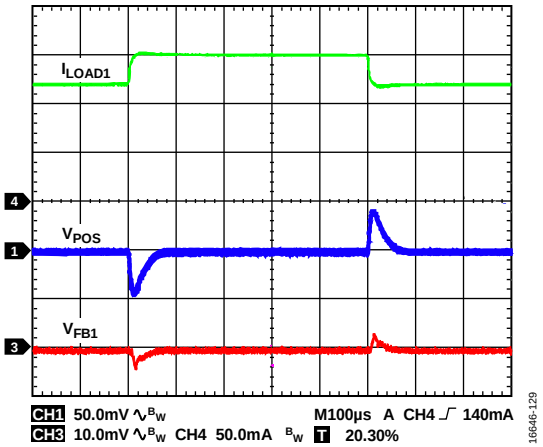

Figure 29. Boost Regulator Load Transient, V_{IN} = 5 V Step, V_{POS} = 15 V, I_{LOAD1} = 120 mA to 150 mA Step, f_{SW} = 2.4 MHz, T_A = 25°C

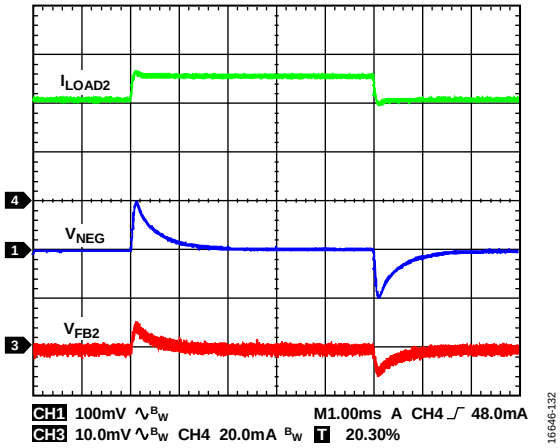

Figure 32. Inverting Regulator Load Transient, V_{IN} = 5 V Step, V_{NEG} = −15 V, I_{LOAD2} = 35 mA to 45 mA Step, f_{SW} = 2.4 MHz, T_A = 25°C

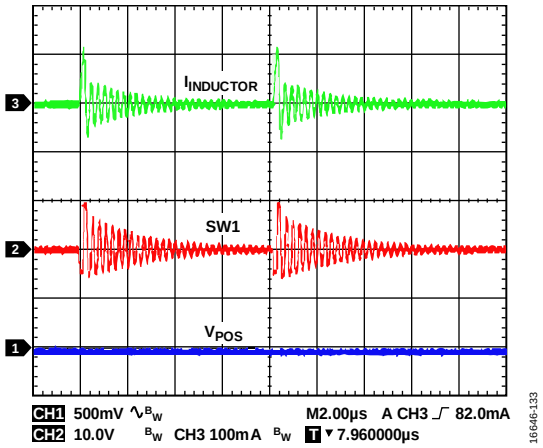

Figure 33. Boost Regulator Skip Mode Operation Showing Inductor Current ($I_{INDUCTOR}$), Switch Node Voltage, and Output Ripple, V_{IN} = 5 V, V_{POS} = 15 V, I_{LOAD1} = 4 mA, f_{SW} = 2.4 MHz, T_A = 25°C

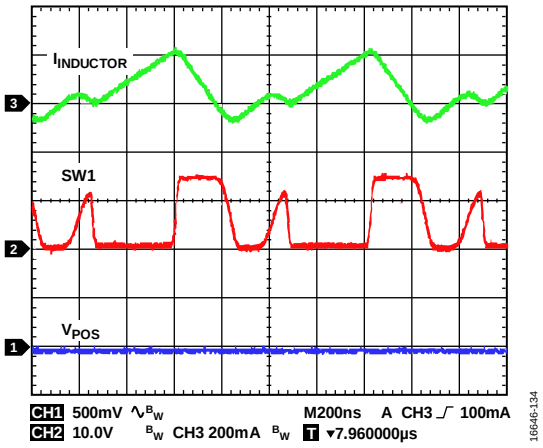

Figure 34. Boost Regulator Discontinuous Conduction Mode Operation Showing Inductor Current ($I_{INDUCTOR}$), Switch Node Voltage, and Output Ripple, V_{IN} = 5 V, V_{POS} = 15 V, I_{LOAD1} = 6 mA, f_{SW} = 2.4 MHz, T_A = 25°C

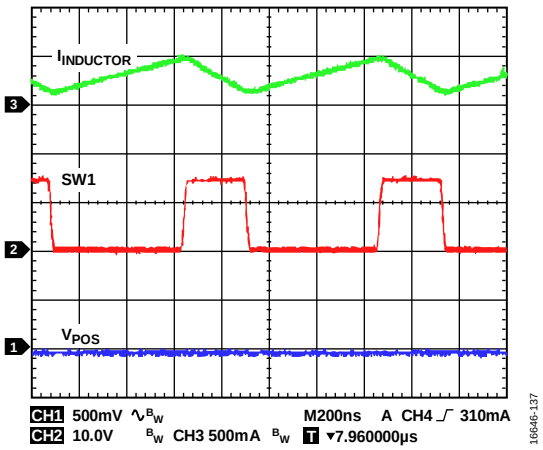

Figure 35. Boost Regulator Continuous Conduction Mode Operation Showing Inductor Current ($I_{INDUCTOR}$), Switch Node Voltage, and Output Ripple, V_{IN} = 5 V, V_{POS} = 15 V, I_{LOAD1} = 90 mA, f_{SW} = 2.4 MHz, T_A = 25°C

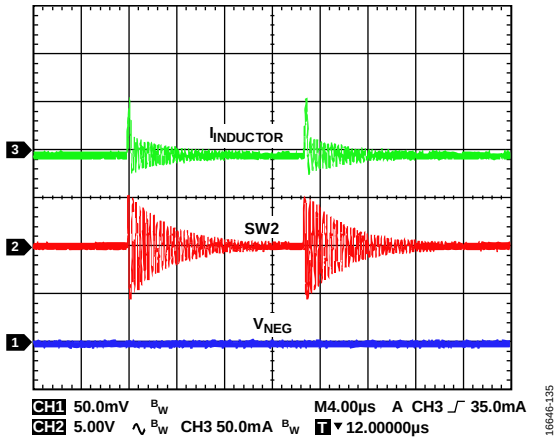

Figure 36. Inverting Regulator Skip Mode Operation Showing Inductor Current ($I_{INDUCTOR}$), Switch Node Voltage, and Output Ripple, V_{IN} = 5 V, V_{NEG} = −5 V, I_{LOAD2} = 0 mA, f_{SW} = 2.4 MHz, T_A = 25°C

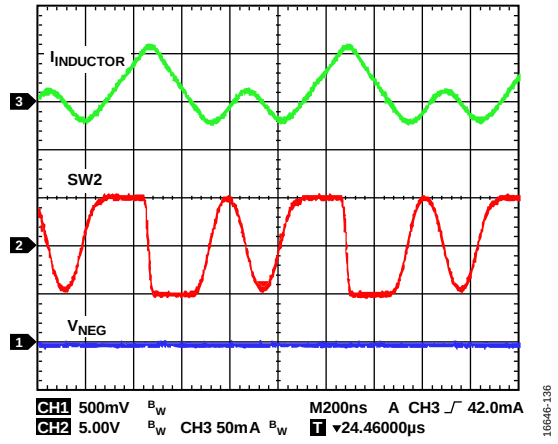

Figure 37. Inverting Regulator Discontinuous Conduction Mode Operation Showing Inductor Current ($I_{INDUCTOR}$), Switch Node Voltage, and Output Ripple, V_{IN} = 5 V, V_{NEG} = −5 V, I_{LOAD2} = 6 mA, f_{SW} = 2.4 MHz, T_A = 25°C

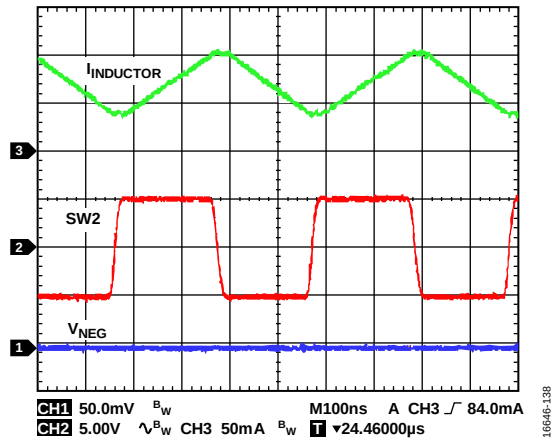

Figure 38. Inverting Regulator Continuous Conduction Mode Operation Showing Inductor Current ($I_{INDUCTOR}$), Switch Node Voltage, and Output Ripple, V_{IN} = 5 V, V_{NEG} = −5 V, I_{LOAD2} = 35 mA, f_{SW} = 2.4 MHz, T_A = 25°C

THEORY OF OPERATION

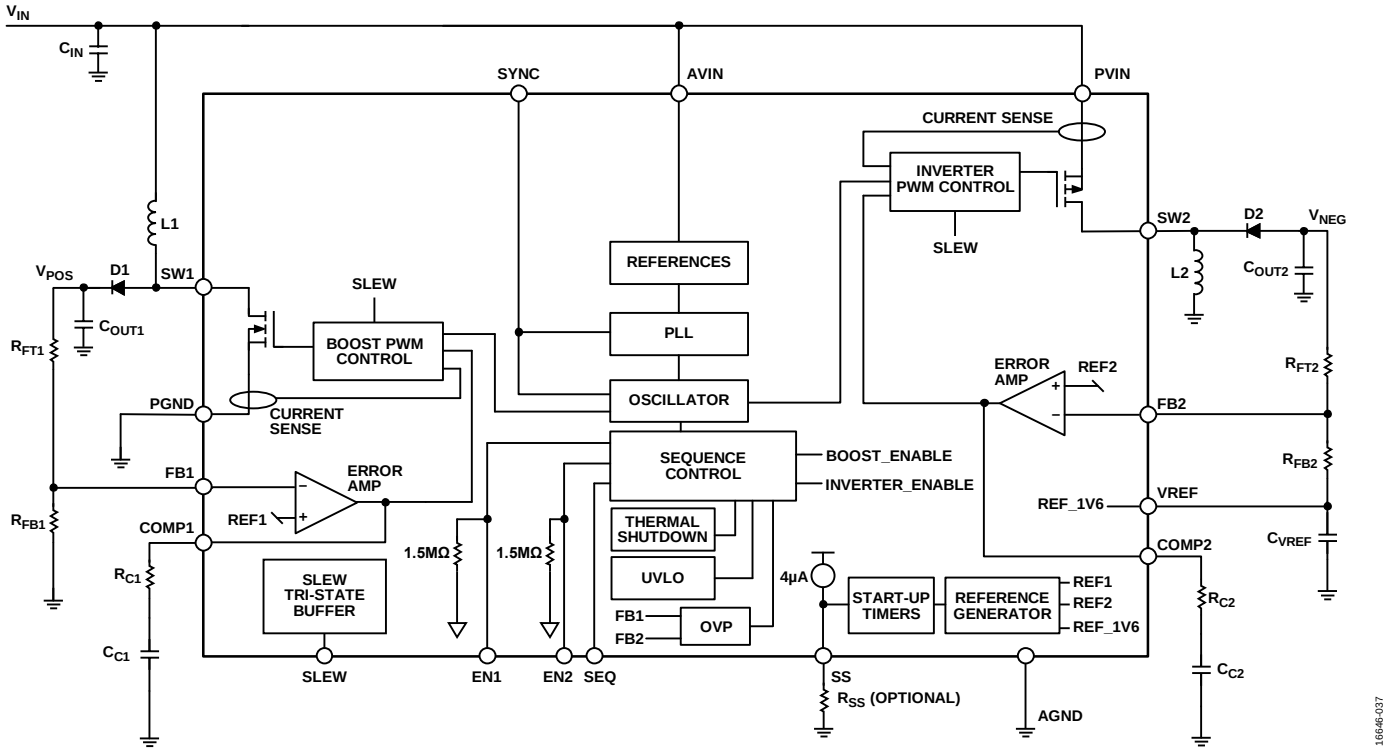

Figure 39. Functional Block Diagram

PULSE WIDTH MODULATION (PWM) MODE

The boost and inverting regulators in the ADP5072 operate at a fixed frequency set by an internal oscillator. At the start of each oscillator cycle, the MOSFET switch turns on, applying a positive voltage across the inductor. The inductor current increases until the current sense signal crosses the peak inductor current threshold that turns off the MOSFET switch; this threshold is set by the error amplifier output. During the MOSFET off time, the inductor current declines through the external diode until the next oscillator clock pulse starts a new cycle. It regulates the output voltage by adjusting the peak inductor current threshold.

PULSE SKIP MODULATION MODE

During light load operation, the regulators can skip pulses to maintain output voltage regulation. Skipping pulses increases the device efficiency.

UNDERVOLTAGE LOCKOUT (UVLO)

The undervoltage lockout circuitry monitors the AVIN pin voltage level. If the input voltage drops below the $V_{UVLO\_FALLING}$ threshold, both regulators turn off. After the AVIN pin voltage rises above the V_{UVLO_RISING} threshold, the soft start period initiates, and the regulators are enabled.

OSCILLATOR AND SYNCHRONIZATION

The ADP5072 initiates the drive of the boost regulator SW1 pin and the inverting regulator SW2 pin 180° out of phase to reduce peak current consumption and noise.

A phase-locked loop (PLL)-based oscillator generates the internal clock and offers a choice of two internally generated frequency options or external clock synchronization. The switching frequency is configured using the SYNC pin options shown in Table 6.

For external synchronization, connect the SYNC pin to a suitable clock source. The PLL locks to an input clock within the range specified by f_{SYNC}.

Table 6. SYNC Pin Options

SYNC Pin	Switching Frequency
High	2.4 MHz
Low	1.2 MHz
External Clock	1 × clock frequency

INTERNAL REGULATOR

The VREF regulator provides a reference voltage for the inverting regulator feedback network to ensure a positive feedback voltage on the FB2 pin.

A current-limit circuit is included for the VREF regulator to protect the circuit from accidental loading.

PRECISION ENABLING

TheADP5072 has an individual enable pin for the boost and inverting regulators: EN1 and EN2. The enable pins feature a precision enable circuit with an accurate reference voltage. This reference allows the ADP5072 to be sequenced easily from other supplies. It can also be used as a programmable UVLO input by using a resistor divider.

The enable pins have an internal pull-down resistor that defaults each regulator to off when the pin is floating.

When the voltage at the enable pins is greater than the V_{TH_H} reference level, the regulator is enabled.

SOFT START

Each regulator in the ADP5072 includes soft start circuitry that ramps the output voltage in a controlled manner during startup, thereby limiting the inrush current. The soft start time is internally set to the fastest rate when the SS pin is open.

Connecting a resistor between SS and AGND allows the adjustment of the soft start delay. The delay length is common to both regulators.

SLEW RATE CONTROL

The ADP5072 employs programmable output driver slew rate control circuitry. This circuitry reduces the slew rate of the switching node as shown in Figure 40, resulting in reduced ringing and lower EMI. To program the slew rate, connect the SLEW pin to the AVIN pin for normal mode, to the AGND pin for slow mode, or leave it open for fast mode. This configuration allows the use of an open-drain output from a noise sensitive device to switch the slew rate from fast to slow, for example, during ADC sampling.

Note that slew rate control causes a trade-off between efficiency and low EMI.

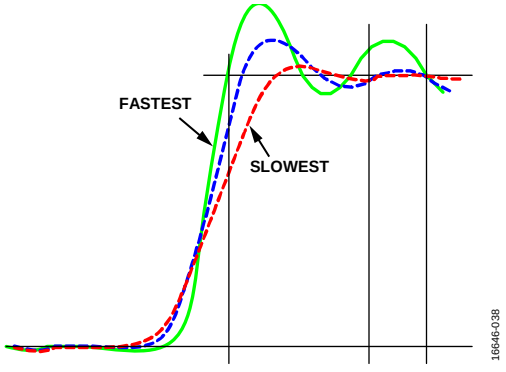

Figure 40. Switching Node at Various Slew Rate Settings

CURRENT-LIMIT PROTECTION

The boost and inverting regulators in the ADP5072 include current-limit protection circuitry to limit the amount of forward current through the MOSFET switch.

When the peak inductor current exceeds the overcurrent limit threshold for a number of clock cycles during an overload or short-circuit condition, the regulator enters hiccup mode. The regulator stops switching and then restarts with a new soft start cycle after t_{HICCUP} and repeats until the overcurrent condition is removed.

OVERVOLTAGE PROTECTION

An overvoltage protection mechanism is present on the FB1 and FB2 pins for the boost and inverting regulators.

On the boost regulator, when the voltage on the FB1 pin exceeds the V_{OV1} threshold, the switching on SW1 stops until the voltage falls below the threshold again. This functionality is permanently enabled on this regulator.

On the inverting regulator, when the voltage on the FB2 pin drops below the V_{OV2} threshold, the switching stops until the voltage rises above the threshold. This functionality is enabled after the soft start period has elapsed.

THERMAL SHUTDOWN

In the event that theADP5072 junction temperature rises above T_{SHDN}, the thermal shutdown circuit turns off the IC. Extreme junction temperatures can be the result of prolonged high current operation, poor circuit board design, and/or high ambient temperature. Hysteresis is included so that when thermal shutdown occurs, the ADP5072 does not return to operation until the on-chip temperature drops below T_{SHDN} minus T_{HYS}. When resuming from thermal shutdown, a soft start is performed on each enabled channel.

START-UP SEQUENCE

The ADP5072 implements a flexible start-up sequence to meet different system requirements. Three different enabling modes can be implemented via the SEQ pin, as explained in Table 7.

Table 7. SEQ Pin Settings

SEQ Pin	Description
Open	Manual enable mode
AVIN	Simultaneous enable mode
Low	Sequential enable mode

To configure the manual enable mode, leave the SEQ pin open. The boost and inverting regulators are controlled separately from their respective precision enable pins.

To configure the simultaneous enable mode, connect the SEQ pin to the AVIN pin. Both regulators power up simultaneously when the EN2 pin is taken high. The EN1 pin enable can be used to enable the internal references ahead of enabling the outputs, if desired. The simultaneous enable mode timing is shown in Figure 41.

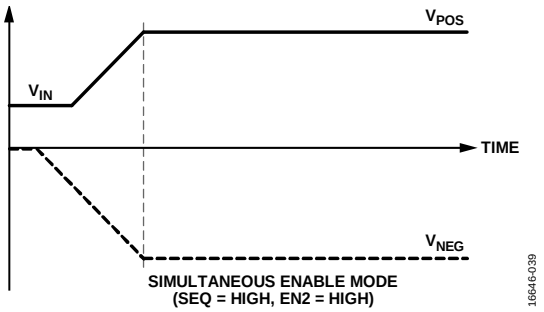

Figure 41. Simultaneous Enable Mode

To configure the sequential enable mode, pull the SEQ pin low. In this mode, either V_{POS} or V_{NEG} can be enabled first by using the EN1 pin or EN2 pin. Keep the other pin low. The secondary supply is enabled when the primary supply completes soft start and its feedback voltage reaches approximately 85% of the target value. The sequential enable mode timing is shown in Figure 42.

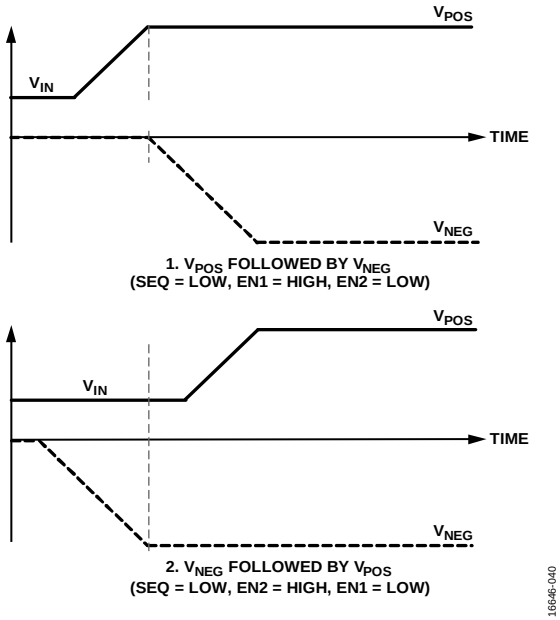

Figure 42. Sequential Enable Mode

APPLICATIONS INFORMATION

COMPONENT SELECTION

Feedback Resistors

The ADP5072 provides an adjustable output voltage for both boost and inverting regulators. An external resistor divider sets the output voltage where the divider output must equal the appropriate feedback reference voltage, V_{FB1} or V_{FB2}. To limit the output voltage accuracy degradation due to feedback bias current, ensure that the current through the divider is at least $10 \times I_{FB1}$ or $10 \times I_{FB2}$.

Set the positive output for the boost regulator by

$$V_{POS} = V_{FB1} \times \left(1 + \frac{R_{FT1}}{R_{FB1}}\right)$$

where:
V_{POS} is the positive output voltage.
V_{FB1} is the FB1 reference voltage.
R_{FT1} is the feedback resistor from V_{POS} to FB1.
R_{FB1} is the feedback resistor from FB1 to AGND.

Set the negative output for the inverting regulator by

$$V_{NEG} = V_{FB2} - \frac{R_{FT2}}{R_{FB2}}(V_{REF} - V_{FB2})$$

where:
V_{NEG} is the negative output voltage.
V_{FB2} is the FB2 reference voltage.
R_{FT2} is the feedback resistor from V_{NEG} to FB2.
R_{FB2} is the feedback resistor from FB2 to VREF.
V_{REF} is the VREF pin reference voltage.

Table 8. Recommended Feedback Resistor Values for Boost Regulator

	Boost Regulator		
Desired Output Voltage (V)	**R_{FT1} (MΩ)**	**R_{FB1} (kΩ)**	**Calculated Output Voltage (V)**
4.2	0.432	102	4.188
5	0.604	115	5.002
9	1.24	121	8.998
12	1.4	100	12.000
13	2.1	137	13.063
15	2.43	137	14.990
18	2.15	100	18.000
20	2.55	107	19.865
24	3.09	107	23.903
30	3.65	100	30.000

Table 9. Recommended Feedback Resistor Values for Inverting Regulator

	Inverting Regulator		
Desired Output Voltage (V)	**R_{FT2} (MΩ)**	**R_{FB2} (kΩ)**	**Calculated Output Voltage (V)**
−1.8	0.332	102	−1.804
−3	0.475	100	−3.000
−3.3	0.523	102	−3.302
−4.2	0.715	115	−4.174
−5	1.15	158	−5.023
−9	1.62	133	−8.944
−12	1.15	71.5	−12.067
−13	2.8	162	−13.027
−15	2.32	118	−14.929
−18	2.67	113	−18.103
−20	2.94	113	−20.014
−24	3.16	102	−23.984
−30	4.12	107	−30.004

OUTPUT CAPACITORS

Higher output capacitor values reduce the output voltage ripple and improve load transient response. When choosing this value, it is also important to account for the loss of capacitance due to the output voltage dc bias.

Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 25 V or 50 V (depending on output) are recommended for optimal performance. Y5V and Z5U dielectrics are not recommended for use with any dc-to-dc converter because of their poor temperature and dc bias characteristics.

Calculate the worst case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage using the following equation:

$$C_{EFFECTIVE} = C_{NOMINAL} \times (1 - TEMPCO) \times (1 - DCBIASCO) \times (1 - Tolerance)$$

where:
$C_{EFFECTIVE}$ is the effective capacitance at the operating voltage.
$C_{NOMINAL}$ is the nominal data sheet capacitance.
TEMPCO is the worst case capacitor temperature coefficient.
DCBIASCO is the dc bias derating at the output voltage.
Tolerance is the worst case component tolerance.

To guarantee the performance of the device, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

Capacitors with lower effective series resistance (ESR) and effective series inductance (ESL) are preferred to minimize output voltage ripple.

The use of large output capacitors may require a slower soft start to prevent current limit during startup. A 10 µF capacitor is suggested as a good balance between performance and size.

Input Capacitor

Higher value input capacitors help to reduce the input voltage ripple and improve transient response.

To minimize supply noise, place the input capacitor as close as possible to the AVIN pin and PVIN pin. A low ESR capacitor is recommended.

The effective capacitance needed for stability is a minimum of 10 µF. If the power pins are individually decoupled, it is recommended to use a minimum of a 5.6 µF capacitor on the PVIN pin and a 3.3 µF capacitor on the AVIN pin to prevent reaching the current limit. The minimum values specified exclude dc bias, temperature, and tolerance effects that are application dependent and must be taken into consideration.

VREF Capacitor

A 1.0 µF ceramic capacitor (C_{VREF}) is required between the VREF pin and AGND.

Soft Start Resistor

A resistor can be connected between the SS pin and the AGND pin to increase the soft start time. The soft start time can be set by the resistor between 4 ms (268 kΩ) and 32 ms (50 kΩ). Leaving the SS pin open selects the fastest time of 4 ms. Figure 43 shows the behavior of this operation. Calculate the soft start time using the following formula:

$$t_{SS} = 38.4 \times 10^{-3} - 1.28 \times 10^{-7} \times R_{SS}\ (\Omega)$$

where 50 kΩ ≤ R_{SS} ≤ 268 kΩ.

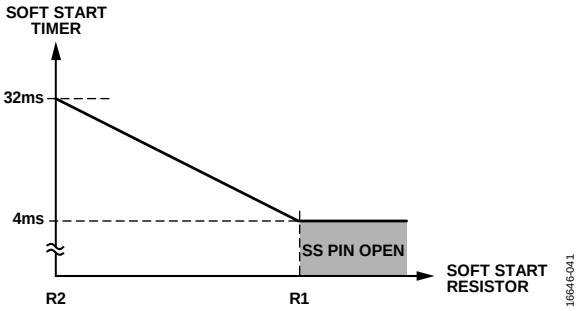

Figure 43. Soft Start Behavior

Diodes

Use a Schottky diode with low junction capacitance for Diode 1 (D1) and Diode 2 (D2). At higher output voltages and especially at higher switching frequencies, the junction capacitance is a significant contributor to efficiency. Higher capacitance diodes also generate more switching noise. As a guide, a diode with less than 40 pF junction capacitance is preferred when the output voltage is above 5 V.

Inductor Selection for the Boost Regulator

The inductor stores energy during the on time of the power switch, and transfers that energy to the output through the output rectifier during the off time. To balance the tradeoffs between small inductor current ripple and efficiency, inductance values in the range of 1 µH to 22 µH are recommended. In general, lower inductance values have higher saturation current and lower series resistance for a given physical size. However, lower inductance results in a higher peak current that can lead to reduced efficiency and greater input and/or output ripple and noise. A peak-to-peak inductor ripple current that is close to 30% of the maximum dc input current for the application typically yields an optimal compromise.

For the inductor ripple current in continuous conduction mode (CCM) operation, the V_{IN} and output voltage (V_{POS}) determine the switch duty cycle ($DUTY_1$) using the following equation:

$$DUTY_1 = \left(\frac{V_{POS} - V_{IN} + V_{DIODE1}}{V_{POS} + V_{DIODE1}} \right)$$

where V_{DIODE1} is the forward voltage drop of D1.

The dc input current in CCM (I_{IN}) can be determined using the following equation:

$$I_{IN} = \frac{I_{OUT1}}{(1 - DUTY_1)}$$

Using the $DUTY_1$ and f_{SW}, determine the on time (t_{ON1}) using the following equation:

$$t_{ON1} = \frac{DUTY_1}{f_{SW}}$$

The inductor ripple current (ΔI_{L1}) in steady state is calculated using the following equation:

$$\Delta I_{L1} = \frac{V_{IN} \times t_{ON1}}{L1}$$

Solve for the inductance value (L1) using the following equation:

$$L1 = \frac{V_{IN} \times t_{ON1}}{\Delta I_{L1}}$$

Assuming an inductor ripple current of 30% of the maximum dc input current, solve for L1 using the following equation:

$$L1 = \frac{V_{IN} \times t_{ON1} \times (1 - DUTY_1)}{0.3 \times I_{OUT1}}$$

Ensure that the peak inductor current (the maximum input current plus half the inductor ripple current) is below the rated saturation current of the inductor. Likewise, ensure that the maximum rated rms current of the inductor is greater than the maximum dc input current to the regulator.

When the ADP5072 boost regulator is operated in CCM at duty cycles greater than 50%, slope compensation is required to stabilize the current mode loop. This slope compensation is built in to the ADP5072. For stable current mode operation, ensure that the selected inductance is equal to or greater than the minimum calculated inductance, L_{MIN1}, for the application parameters in the following equation:

$$L1 > L_{MIN1} = V_{IN} \times \left(\frac{0.13}{(1 - DUTY_1)} - 0.16 \right) \text{ (µH)}$$

Table 11 suggests a series of inductors to use with the ADP5072 boost regulator.

Inductor Selection for the Inverting Regulator

The inductor stores energy during the on time of the power switch and transfers that energy to the output through the output rectifier during the off time. To balance the tradeoffs between small inductor current ripple and efficiency, inductance values in the range of 1 µH to 22 µH are recommended. In general, lower inductance values have higher saturation current and lower series resistance for a given physical size. However, lower inductance results in a higher peak current that can lead to reduced efficiency and greater input and/or output ripple and noise. A peak-to-peak inductor ripple current that is close to 30% of the maximum dc current in the inductor typically yields an optimal compromise.

For the inductor ripple current in continuous conduction mode (CCM) operation, the input (V_{IN}) and output (V_{NEG}) voltages determine the switch duty cycle ($DUTY_2$) by the following equation:

$$DUTY_2 = \left(\frac{|V_{NEG}| + V_{DIODE2}}{V_{IN} + |V_{NEG}| + V_{DIODE2}} \right)$$

where V_{DIODE2} is the forward voltage drop of D2.

The dc current in the inductor in CCM (I_{L2}) can be determined using the following equation:

$$I_{L2} = \frac{I_{OUT2}}{(1 - DUTY_2)}$$

Using the $DUTY_2$ and f_{SW}, determine the on time (t_{ON2}) using the following equation:

$$t_{ON2} = \frac{DUTY_2}{f_{SW}}$$

The inductor ripple current (ΔI_{L2}) in steady state is calculated using the following equation:

$$\Delta I_{L2} = \frac{V_{IN} \times t_{ON2}}{L2}$$

Solve for the inductance value (L2) by the following equation:

$$L2 = \frac{V_{IN} \times t_{ON2}}{\Delta I_{L2}}$$

Assuming an inductor ripple current of 30% of the maximum dc current in the inductor, solve for L2 using the following equation:

$$L2 = \frac{V_{IN} \times t_{ON2} \times (1 - DUTY_2)}{0.3 \times I_{OUT2}}$$

Ensure that the peak inductor current (the maximum input current plus half the inductor ripple current) is less than the rated saturation current of the inductor. Likewise, ensure that the maximum rated rms current of the inductor is greater than the maximum dc input current to the regulator.

When the ADP5072 inverting regulator is operated in CCM at duty cycles greater than 50%, slope compensation is required to stabilize the current mode loop. For stable current mode operation, ensure that the selected inductance is equal to or greater than the minimum calculated inductance, L_{MIN2}, for the application parameters in the following equation:

$$L2 > L_{MIN2} = V_{IN} \times \left(\frac{0.13}{(1 - DUTY_2)} - 0.16 \right) \text{ (µH)}$$

Table 12 suggests a series of inductors to use with the ADP5072 inverting regulator.

LOOP COMPENSATION

The ADP5072 uses external components to compensate the regulator loop, allowing the optimization of the loop dynamics for a given application.

Boost Regulator

The boost converter produces an undesirable right half plane zero in the regulation feedback loop. This feedback loop requires compensating the regulator such that the crossover frequency occurs well below the frequency of the right half plane zero. The right half plane zero is determined by the following equation:

$$f_{Z1}(RHP) = \frac{R_{LOAD1}(1 - DUTY_1)^2}{2\pi \times L1}$$

where:
$f_{Z1}(RHP)$ is the right half plane zero frequency.
R_{LOAD1} is the equivalent resistor load for the boost regulator, which is also equal to the output voltage divided by the load current.

To stabilize the regulator, ensure that the regulator crossover frequency is less than or equal to one-tenth of the right half plane zero frequency.

The boost regulator loop gain is

$$A_{VL1} = \frac{V_{FB1}}{V_{POS}} \times \frac{V_{IN}}{V_{POS}} \times g_{M1} \times \left| R_{OUT1} \| Z_{COMP1} \right| \times g_{CS1} \times \left| Z_{OUT1} \right|$$

where:
A_{VL1} is the loop gain.
V_{FB1} is the feedback regulation voltage
V_{POS} is the regulated positive output voltage.
V_{IN} is the input voltage.
g_{M1} is the error amplifier transconductance gain.
R_{OUT1} is the output impedance of the error amplifier and is 33 MΩ.
Z_{COMP1} is the impedance of the series resistor/capacitor (RC) network from COMP1 to AGND.
g_{CS1} is the current sense transconductance gain (the inductor current divided by the voltage at COMP1), which is internally set by the ADP5072 and is 6.25 A/V.
Z_{OUT1} is the impedance of the load in parallel with the output capacitor.

At the crossover frequency (f_{C1}), the Z_{COMP1} is dominated by a resistor (R_{C1}), and Z_{OUT1} is dominated by the impedance of an output capacitor (C_{OUT1}). Therefore, when solving for f_{C1}, the equation (by definition of the crossover frequency) is simplified to

$$\left| A_{VL1} \right| = \frac{V_{FB1}}{V_{POS}} \times \frac{V_{IN}}{V_{POS}} \times g_{M1} \times R_{C1} \times g_{CS1} \times \frac{1}{2\pi \times f_{C1} \times C_{OUT1}} = 1$$

To solve for R_{C1}, use the following equation:

$$R_{C1} = \frac{2\pi \times f_{C1} \times C_{OUT1} \times (V_{POS})^2}{V_{FB1} \times V_{IN} \times g_{M1} \times g_{CS1}}$$

where g_{CS1} = 6.25 A/V.

Using typical values for V_{FB1} and G_{M1} (see the Specifications section) results in

$$R_{C1} = \frac{4188 \times f_{C1} \times C_{OUT1} \times (V_{POS})^2}{V_{IN}}$$

For better accuracy, it is recommended to use the C_{OUT1} value expected under the dc bias conditions that the C_{OUT1} value operates under in the calculation for R_{C1}.

After the compensation resistor is known, set the zero formed by the compensation capacitor and resistor to one-fourth of the crossover frequency, or

$$C_{C1} = \frac{2}{\pi \times f_{C1} \times R_{C1}}$$

where C_{C1} is the compensation capacitor value.

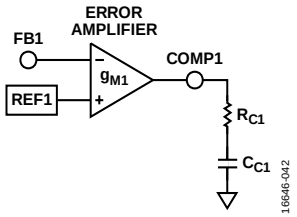

Figure 44. Compensation Components

Inverting Regulator

The inverting converter, like the boost converter, produces an undesirable right half plane zero in the regulation feedback loop. This feedback loop requires compensating the regulator so that the crossover frequency is less than the frequency of the right half plane zero. The right half plane zero frequency is determined by the following equation:

$$f_{Z2}(RHP) = \frac{R_{LOAD2}(1 - DUTY_2)^2}{2\pi \times L2 \times DUTY_2}$$

where:
$f_{Z2}(RHP)$ is the right half plane zero frequency.
R_{LOAD2} is the equivalent resistor load for inverting regulator, which is also equal to the output voltage divided by the load current.

To stabilize the regulator, ensure that the regulator crossover frequency is less than or equal to one-tenth of the right half plane zero frequency.

The inverting regulator loop gain is

$$A_{VL2} = \frac{V_{FB2}}{|V_{NEG}|} \times \frac{V_{IN}}{(V_{IN} + 2 \times |V_{NEG}|)} \times g_{M2} \times \left| R_{OUT2} \| Z_{COMP2} \right| \times g_{CS2} \times \left| Z_{OUT2} \right|$$

where:
A_{VL2} is the loop gain.
V_{FB2} is the feedback regulation voltage.
V_{NEG} is the regulated negative output voltage.

V_{IN} is the input voltage.
g_{M2} is the error amplifier transconductance gain.
R_{OUT2} is the output impedance of the error amplifier and is 33 MΩ.
Z_{COMP2} is the impedance of the series RC network from COMP2 to AGND.
g_{CS2} is the current sense transconductance gain (the inductor current divided by the voltage at COMP2), which is internally set by the ADP5072 and is 6.25 A/V.
Z_{OUT2} is the impedance of the load in parallel with the output capacitor.

At crossover frequency (f_{C2}), the Z_{COMP2} is dominated by a resistor (R_{C2}), and the Z_{OUT2} is dominated by the impedance of the output capacitor (C_{OUT2}). Therefore, when solving for the f_{C2}, the equation (by definition of the crossover frequency) is simplified to

$$|A_{VL2}| = \frac{V_{FB2}}{|V_{NEG}|} \times \frac{V_{IN}}{(V_{IN} + 2 \times |V_{NEG}|)} \times g_{M2} \times R_{C2} \times g_{CS2} \times \frac{1}{2\pi \times f_{C2} \times C_{OUT2}} = 1$$

To solve for R_{C2}, use the following equation:

$$R_{C2} = \frac{2\pi \times f_{C2} \times C_{OUT2} \times |V_{NEG}| \times (V_{IN} + (2 \times |V_{NEG}|))}{V_{FB2} \times V_{IN} \times g_{M2} \times g_{CS2}}$$

where G_{CS2} = 6.25 A/V.

Using typical values for V_{FB2} and G_{M2} results in

$$R_{C2} = \frac{4188 \times f_{C2} \times C_{OUT2} \times |V_{NEG}| \times (V_{IN} + (2 \times |V_{NEG}|))}{V_{IN}}$$

See the Specifications section for the typical values for V_{FB2} and G_{M2}. The typical value for V_{FB2} can be obtained by subtracting (V_{REF} − V_{FB2}) from V_{REF}.

For better accuracy, it is recommended to use the C_{OUT2} value expected under the dc bias conditions that the C_{OUT2} value operates under in the calculation for R_{C2}.

After the compensation resistor is known, set the zero formed by the C_{C2} and R_{C2} to one-fourth of the crossover frequency, or

$$C_{C2} = \frac{2}{\pi \times f_{C2} \times R_{C2}}$$

where C_{C2} is the compensation capacitor.

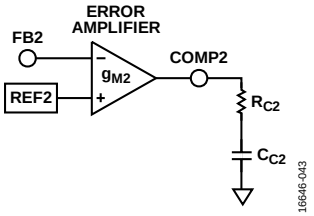

Figure 45. Compensation Component

COMMON APPLICATIONS

Table 10 through Table 12 list a number of common component selections for typical V_{IN}, V_{POS}, and V_{NEG} conditions. These selections are bench tested and provide an off the shelf solution. When pairing a boost and inverting regulator bill of materials, choose the same V_{IN} and f_{SW}.

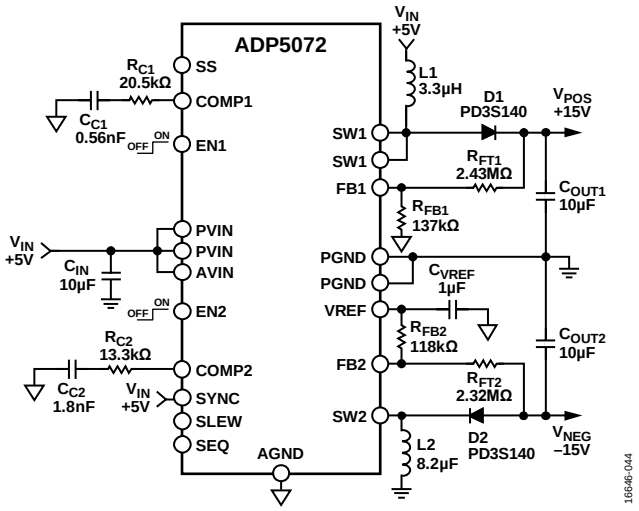

Figure 46. Typical +5 V to ±15 V Application

Figure 46 shows the schematic referenced by

Table 10 through Table 12 with example component values for 5 V input voltage to ±15 V output voltage generation.

Table 10 shows the components common to all of the V_{IN}, V_{POS}, and V_{NEG} conditions.

Table 10. Recommended Common Components Selections

Reference	Value	Part Number	Manufacturer
C_{IN}	10 µF	GRM21BZ71C106KE15L	Murata
C_{VREF}	1 µF	GRM188R71C105KA12C	Murata

Figure 47 shows the efficiency curves for the boost and inverting regulator using the recommended, small size components described in

Table 10, Table 11, and Table 12 display data for V_{POS} = 15 V and V_{NEG} = −15 V at V_{IN} = 5 V.

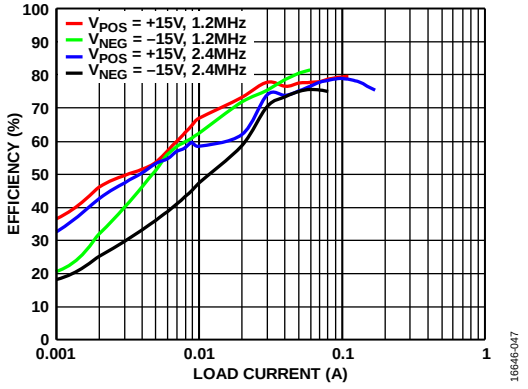

Figure 47. Efficiency vs. Load Current for Boost Regulator and Inverting Regulator, T_A = 25°C

Table 11 and Table 12 are based on the smallest sized components. The maximum output current is limited by the I_{SAT} rating of the 2 mm × 2 mm inductor. A higher output current is possible by using larger inductors with higher I_{SAT} ratings, as long as the inductor peak current remains below the appropriate current limit specifications.

It is important to verify the thermal performance of the small sized inductor at higher ambient temperature in actual application.

Table 11. Recommended Boost Regulator Small Sized Components

V_{IN} (V)	V_{POS} (V)	$I_{LOAD1\ (MAX)}$ (mA)	Frequency (MHz)	L1 (µH)	L1 Manufacturer Part No. (Coilcraft)	C_{OUT1}, Murata Part No.	D1	R_{FT1} (MΩ)	R_{FB1} (kΩ)	C_{C1} (nF)	R_{C1} (kΩ)
3.3	5	340	1.2	3.3	EPL2014-332ML_	GRM21BR71A106KA73L	PMEG2005AELD	0.604	115	0.82	15.8
3.3	5	360	2.4	2.2	EPL2014-222ML_	GRM21BR71A106KA73L	PMEG2005AELD	0.604	115	0.47	29.4
3.3	9	180	1.2	4.7	EPL2014-472ML_	GRM21BZ71C106KE15L	PMEG2005AELD	1.24	121	1.2	26.1
3.3	9	200	2.4	3.3	EPL2014-332ML_	GRM21BZ71C106KE15L	PMEG2005AELD	1.24	121	0.82	17.4
3.3	15	100	1.2	4.7	EPL2014-472ML_	GRM31CR71E106MA12L	PD3S140	2.43	137	1.5	14.3
3.3	15	110	2.4	4.7	EPL2014-472ML_	GRM31CR71E106MA12L	PD3S140	2.43	137	1.2	16.9
3.3	24	50	1.2	6.8	EPL2014-682ML_	GRM32ER7YA106MA12L	PD3S140	3.09	107	1.8	28.7
3.3	24	55	2.4	6.8	EPL2014-682ML_	GRM32ER7YA106MA12L	PD3S140	3.09	107	1.8	16.2
5	9	140	1.2	3.3	EPL2014-332ML_	GRM21BZ71C106KE15L	PMEG2005AELD	1.24	121	0.56	16.9
5	9	280	2.4	2.2	EPL2014-222ML_	GRM21BZ71C106KE15L	PMEG2005AELD	1.24	121	0.39	18.7
5	15	110	1.2	4.7	EPL2014-472ML_	GRM31CR71E106MA12L	PD3S140	2.43	137	1	18.2
5	15	170	2.4	3.3	EPL2014-332ML_	GRM31CR71E106MA12L	PD3S140	2.43	137	0.56	20.5
5	24	50	1.2	10	EPL2014-103ML_	GRM32ER7YA106MA12L	PD3S140	3.09	107	1.8	15.8
5	24	80	2.4	6.8	EPL2014-682ML_	GRM32ER7YA106MA12L	PD3S140	3.09	107	1.2	10
5	34	40	1.2	10	EPL2014-103ML_	GRM32ER71H106KA12L	PD3S140	4.22	102	1.5	25.5
5	34	45	2.4	8.2	EPL2014-822ML_	GRM32ER71H106KA12L	PD3S140	4.22	102	1.2	18.2

Table 12. Recommended Inverting Regulator Small Sized Components

V_{IN} (V)	V_{NEG} (V)	$I_{LOAD2\ (MAX)}$ (mA)	Frequency (MHz)	L2 (µH)	L2 Manufacturer Part No. (Coilcraft)	C_{OUT2}, Murata Part No.	D2	R_{FT2} (MΩ)	R_{FB2} (kΩ)	C_{C2} (nF)	R_{C2} (kΩ)
3.3	−5	120	1.2	6.8	EPL2014-682ML_	GRM21BR71A106KA73L	PMEG2005AELD	1.15	158	8.2	7.5
3.3	−5	130	2.4	4.7	EPL2014-472ML_	GRM21BR71A106KA73L	PMEG2005AELD	1.15	158	3.3	10.5
3.3	−9	70	1.2	4.7	EPL2014-472ML_	GRM21BZ71C106KE15L	PMEG2005AELD	1.62	133	3.9	8.06
3.3	−9	90	2.4	4.7	EPL2014-472ML_	GRM21BZ71C106KE15L	PMEG2005AELD	1.62	133	1.8	8.06
3.3	−15	50	1.2	8.2	EPL2014-822ML_	GRM31CR71E106MA12L	PD3S140	2.32	118	3.3	10.5
3.3	−15	55	2.4	6.8	EPL2014-682ML_	GRM31CR71E106MA12L	PD3S140	2.32	118	2.2	8.25
3.3	−24	30	1.2	10	EPL2014-103ML_	GRM32ER7YA106MA12L	PD3S140	3.16	102	3.3	10.5
3.3	−24	30	2.4	6.8	EPL2014-682ML_	GRM32ER7YA106MA12L	PD3S140	3.16	102	1.5	14.3
5	−9	90	1.2	8.2	EPL2014-822ML_	GRM21BZ71C106KE15L	PMEG2005AELD	1.62	133	5.6	4.87
5	−9	120	2.4	6.8	EPL2014-682ML_	GRM21BZ71C106KE15L	PMEG2005AELD	1.62	133	2.2	10
5	−15	60	1.2	8.2	EPL3015-822ML_	GRM31CR71E106MA12L	PD3S140	2.32	118	4.7	10
5	−15	80	2.4	8.2	EPL2014-822ML_	GRM31CR71E106MA12L	PD3S140	2.32	118	1.8	13.3
5	−24	40	1.2	10	EPL3015-103ML_	GRM32ER7YA106MA12L	PD3S140	3.16	102	4.7	10
5	−24	50	2.4	10	EPL2014-103ML_	GRM32ER7YA106MA12L	PD3S140	3.16	102	2.2	7.15
5	−30	30	1.2	10	EPL3015-103ML_	GRM32ER71H106KA12L	PD3S140	4.99	75	3.9	15.8
5	−30	35	2.4	8.2	EPL2014-822ML_	GRM32ER71H106KA12L	PD3S140	4.99	75	1.2	1.2

LAYOUT CONSIDERATIONS

Layout is important for all switching regulators but is particularly important for regulators with high switching frequencies. To achieve high efficiency, good regulation, good stability, and low noise, a well designed PCB layout is required. Follow these guidelines when designing PCBs:

- Keep the input bypass capacitor (C_{IN}) near the PVIN pin and the AVIN pin.
- Keep the high current paths as short as possible. These paths include the connections between C_{IN}, L1, D1, C_{OUT1}, and the PGND pin for the boost regulator, and L2, D2, C_{OUT2}, and the PGND pin for the inverting regulator and the connections to the ADP5072.
- Keep the AGND pin and the PGND pin separate on the top layer of the board. This separation avoids pollution of the AGND pin with switching noise. Connect both the AGND and PGND pins to the board ground plane with vias. Ideally, connect the PGND pin to the plane at a point between the input and output capacitors.
- Keep high current traces as short and wide as possible to minimize parasitic series inductance, which causes spiking and EMI.
- Avoid routing high impedance traces near any node connected to the SW1 and SW2 pins or near inductors L1 and L2 to prevent radiated switching noise injection.
- Place the feedback resistors (R_{FT1}, R_{FB1}, R_{FT2}, and R_{FB2}) as close as possible to the FB1 and FB2 pins to prevent high frequency switching noise injection.
- Place the tops of the upper feedback resistors (R_{FT1} and R_{FT2}) or route traces to them from as close as possible to the tops of C_{OUT1} and C_{OUT2} for optimum output voltage sensing.
- Place the compensation components (R_{C1}, C_{C1}, R_{C2}, and C_{C2}) as close as possible to the COMP1 and COMP2 pins. Do not share vias to the ground plane with the feedback resistors to avoid coupling high frequency noise into the sensitive COMP1 and COMP2 pins.
- Place the C_{VREF} capacitor as close to the VREF pin as possible. Ensure that short traces are used between the VREF pin and R_{FB2}.

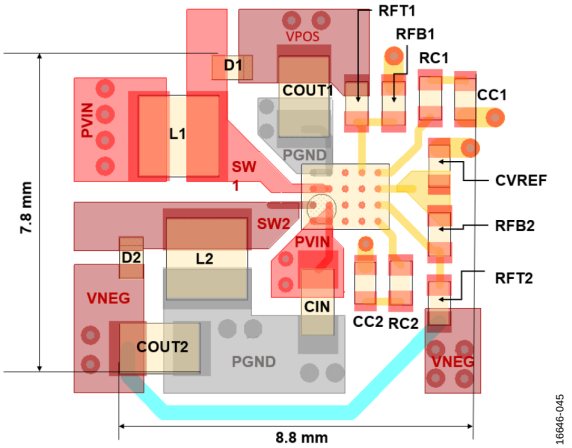

Figure 48. Suggested Layout for V_{IN} = 3.3 V, V_{POS} = 12 V, I_{LOAD1} = 100 mA and V_{NEG} = −3.2 V, I_{LOAD2} = 60 mA; Not to Scale

OUTLINE DIMENSIONS

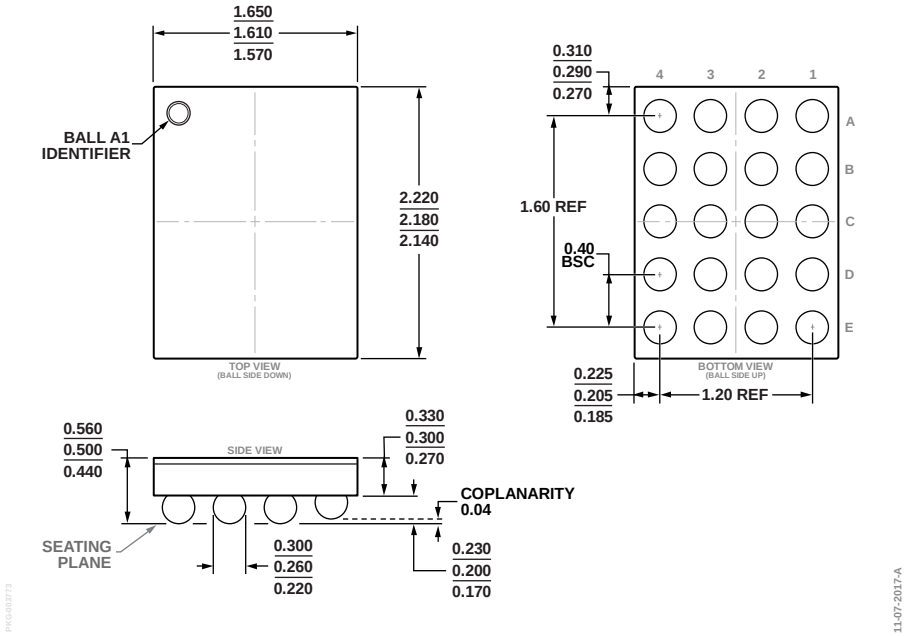

Figure 49. 20-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-20-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP5072ACBZ-R7	−40°C to +125°C	20-Ball Wafer Level Chip Scale Package [WLCSP]	CB-20-14
ADP5072CB-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.