MP3414A

3A, 1MHz, 22µA Iq, 5.5V Synchronous Step-Up Converter with Output Disconnect

The Future of Analog IC Technology

DESCRIPTION

The MP3414A is a high-efficiency, synchronous current mode, step-up converter with output disconnect.

The MP3414A can start up from an input voltage as low as 1.8V while providing inrush current limiting and output short-circuit protection (SCP). The integrated P-channel synchronous rectifier improves efficiency and eliminates the need for an external Schottky diode. The PMOS disconnects the output from the input when the MP3414A shuts down. The output disconnect feature allows the output to be discharged completely, allowing the MP3414A to draw a supply current of under 1µA in shutdown mode.

The 1MHz switching frequency allows small external components while the internal compensation and soft start minimize the external component count. These features produce a compact solution for a wide current load range.

The MP3414A features an integrated power MOSFET that supports an output of up to 5.5V and a peak switching current above 3A.

The MP3414A is available in a small 8-pin TSOT23 package.

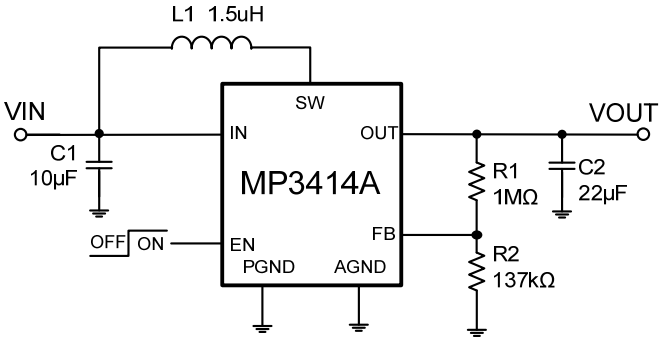
FEATURES

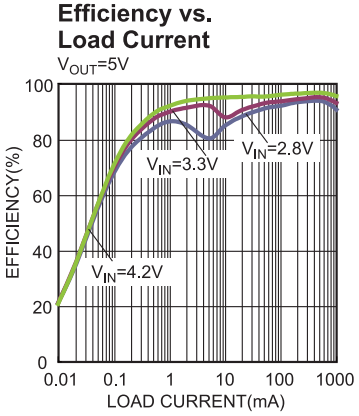
- Supports 5V/1A Output at 2.8V Input
- 1.8V to 5.5V Input Voltage Range
- Up to 5.5V Output Voltage
- Internal Synchronous Rectifier
- 1MHz Fixed Switching Frequency
- 22µA Quiescent Current
- <1µA Shutdown Current
- True Output Disconnect from Input
- Up to 97% Efficiency
- Internal Compensation, Inrush Current Limiting, and Internal Soft Start
- Tiny External Components
- OVP, SCP, and OTP
- TSOT23-8 Package

APPLICATIONS

- Two-Cell and Three-Cell Alkaline, NiCd or NiMH, or Single-Cell Li Battery-Power Products
- Personal Medical Devices
- Portable Media Players
- Wireless Peripherals
- Gaming Accessories

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP3414AGJ	TSOT23-8	*See Below*

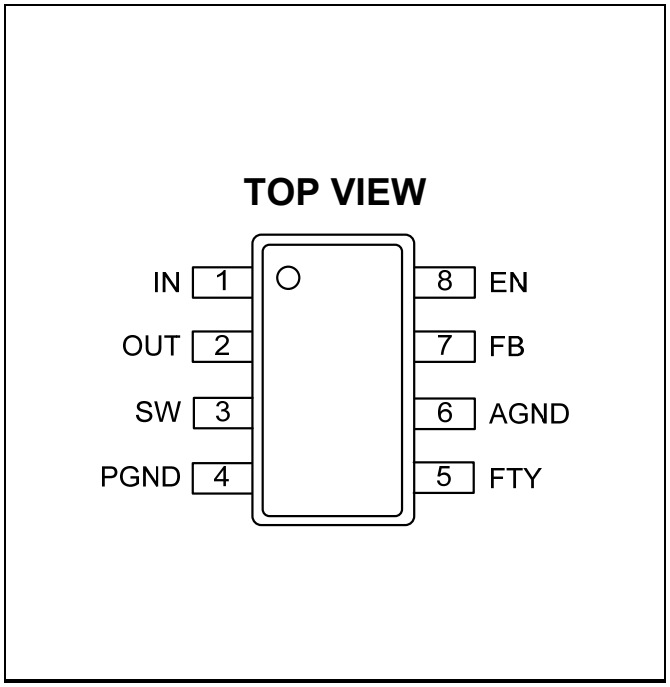
* For Tape & Reel, add suffix –Z (e.g. MP3414AGJ–Z)

TOP MARKING

|AKTY

AKT: Product code of MP3414AGJ
Y: Year code

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

SW, OUT .....-0.3V to +6.5V
SW (<5ns) .....-1V to +9V
All other pins .....-0.3V to +6.5V
Continuous power dissipation (T_A = +25°C) (2) 1.25W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....1.8V to 5.5V
V_{OUT}..... V_{IN-MAX} x 106% to 5.5V(4)
Operating junction temp. (T_J)... -40°C to +125°C

Thermal Resistance (5)

	θ_{JA}	θ_{JC}	
TSOT23-8	100	55	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) If V_{IN} is close to V_{OUT}, the boost converter may trigger minimum on-time. When V_{IN} is higher than V_{OUT}, the boost converter will switch between boost mode and linear charge mode. Both conditions will result in a $V_{OUT-RIPPLE}$ that is too high. Therefore, this is not suggested.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 5V, T_J = -40°C to 125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Voltage Range						
Quiescent current	I_Q	V_{EN} = V_{IN} = 3.3V, V_{OUT} = 5V, no load, V_{FB} = 0.65V, measured on OUT, T_J = 25°C		22	30	μA
		V_{EN} = V_{IN} = 3.3V, V_{OUT} = 5V, no load, V_{FB} = 0.65V, measured on IN, T_J=25°C		8	12	μA
Shutdown current	I_{SD}	V_{EN} = V_{OUT} = 0V, measured on IN T_J = 25°C		0.1	1	μA
IN under-voltage lockout	$V_{IN\ UVLO}$	V_{IN} rising, T_J = 25°C.		1.65	1.7	V
IN under-voltage lockout hysteresis				100		mV
Step-Up Converter						
Operation frequency	F_{SW}		0.8	1.0	1.2	MHz
Feedback voltage reference	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to 125°C	591	600	609	mV
Feedback input current	I_{FB}	V_{FB} = 0.63V		1	50	nA
NMOS on resistance	$R_{NDS\ ON}$			70		mΩ
NMOS leakage current	$I_{N\ LK}$	V_{SW} = 6.5V, T_J = 25°C.		0.1	1	μA
PMOS on resistance	$R_{PDS\ ON}$			80		mΩ
PMOS leakage current	$I_{P\ LK}$	V_{SW} = 6.5V, V_{OUT} = 0V, T_J = 25°C.		0.1	1	μA
Maximum duty cycle	D_{MAX}		85	95		%
Start-up current limit	I_{ST_LIMIT}	V_{IN} = 4V, Vo = 0V		0.3		A
		V_{IN} = 4V, Vo setting = 3.6V, pull Vo to 3.3V		0.8		A
NMOS current limit	$I_{SW\ LIMIT}$	Duty = 40%	3	3.6		A
Logic Interface						
EN input high-level voltage	$V_{EN\ H}$		1.2			V
EN input low-level voltage	$V_{EN\ L}$				0.4	V
EN input current	I_{EN}	Connect to V_{IN}		10		nA
Protection						
Thermal shutdown(6)				155		°C
Over-temperature hysteresis(6)				25		°C

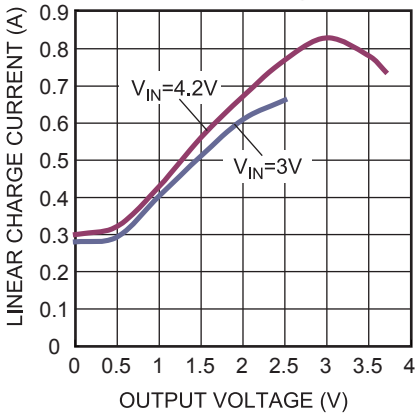
NOTE:

6) Guaranteed by characterization, not production tested.

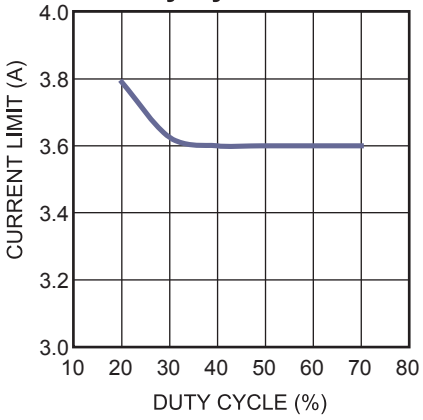
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

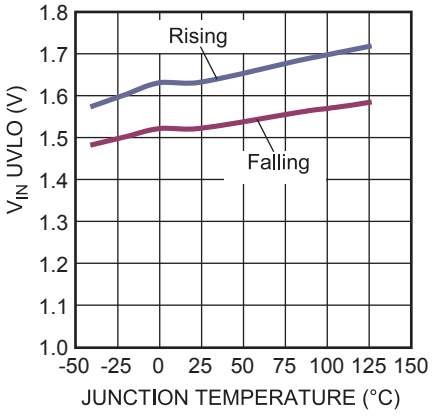
Linear Charge Current vs. Output Voltage



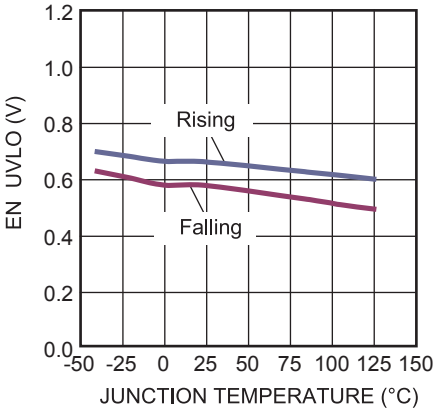
Boost Current Limit vs. Duty Cycle



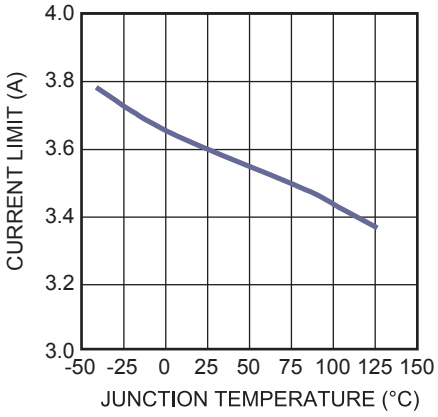
V_{IN} UVLO vs. Junction Temperature



EN UVLO vs. Junction Temperature

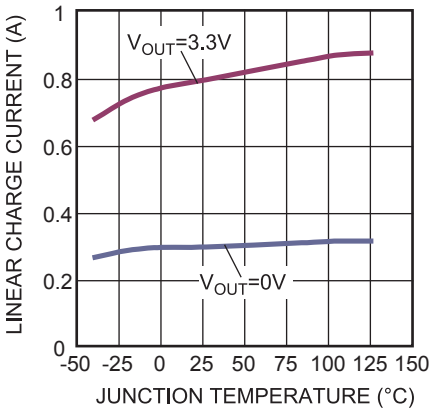


Boost Current Limit vs. Junction Temperature

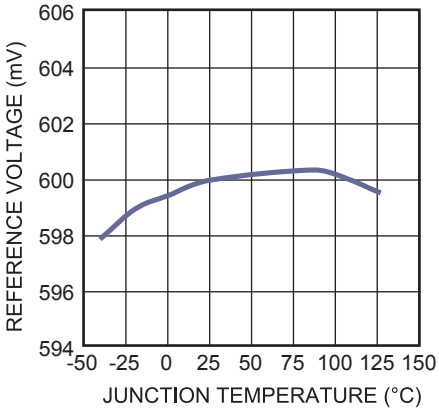


Linear Charge Current vs. Junction Temperature

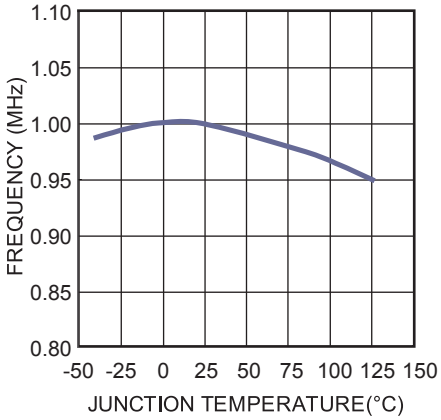
V_{IN}=4V



Reference Voltage vs. Junction Temperature

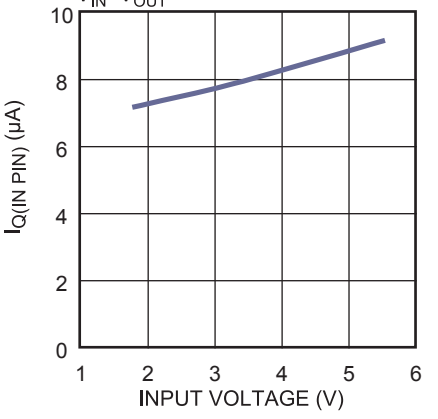


Frequency vs. Junction Temperature



$I_{Q(IN\ PIN)}$ vs. Input Voltage

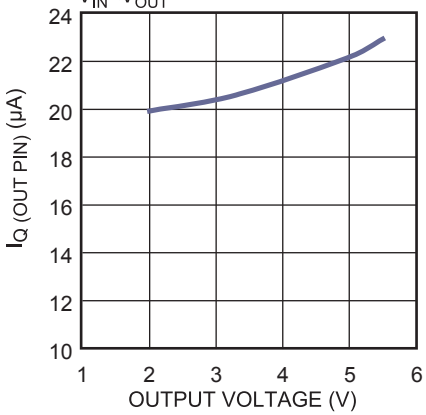
V_{IN}<V_{OUT}



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

$I_{Q(OUT\ PIN)}$ vs. Output Voltage

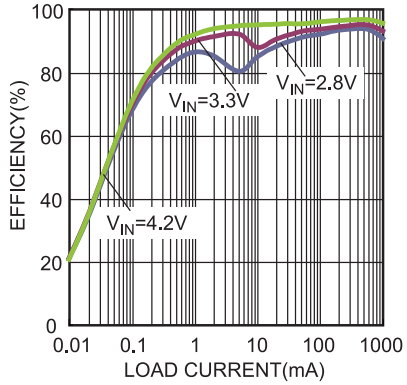


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

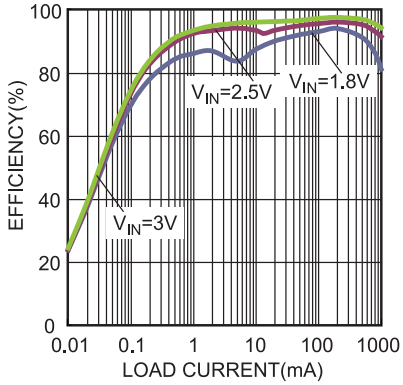
Efficiency vs. Load Current

V_{OUT}=5V



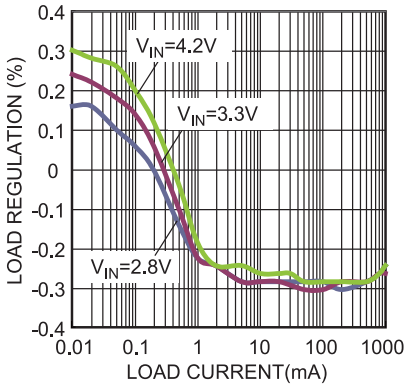
Efficiency vs. Load Current

V_{OUT}=3.3V



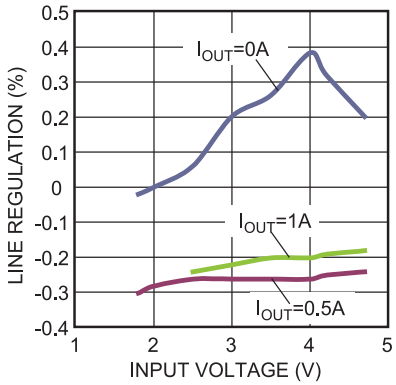
Load Regulation

V_{OUT}=5V



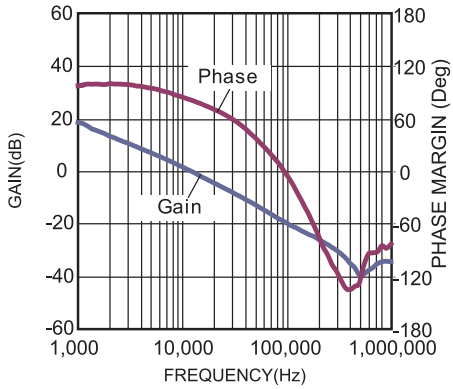
Line Regulation

V_{OUT}=5V

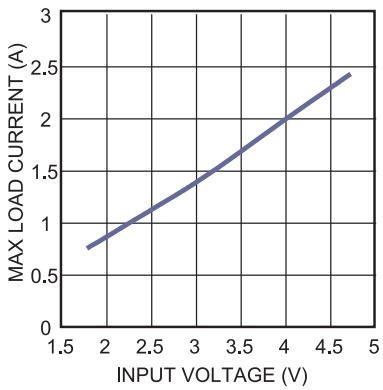


Bode Plot

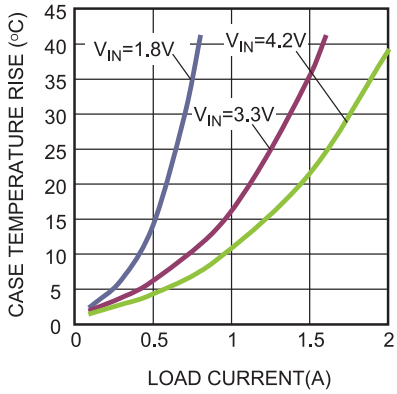
V_{IN}=3.3V, V_{OUT}=5V, I_{OUT}=1A



Load Capability vs. Input Voltage (7)



Case Temperature Rise



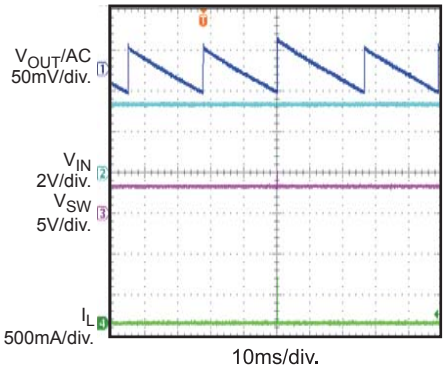
NOTE:

7) Tested with a 3A inductor peak current with the schematic in Figure 3. The maximum load current may decrease if the temperature rising is limited on the real application board.

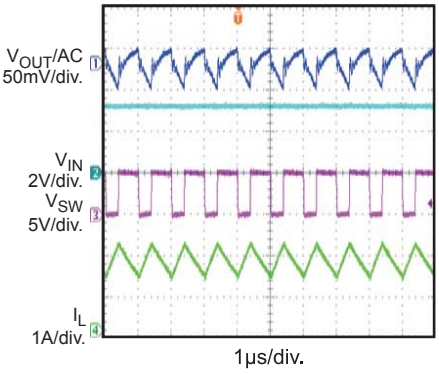
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

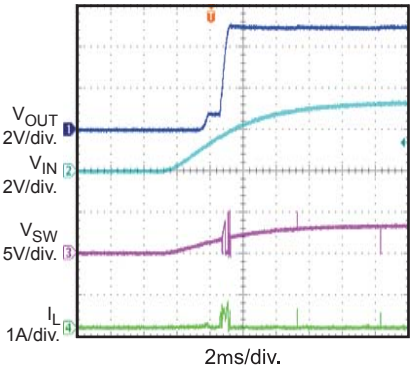
Steady State
I_{OUT} = 0A



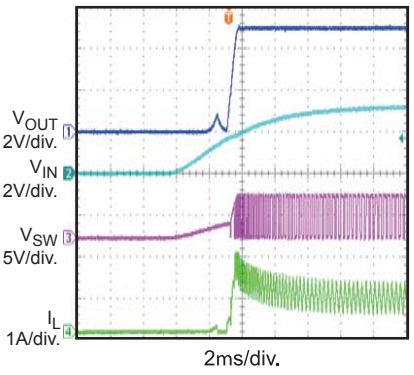
Steady State
I_{OUT} = 1A



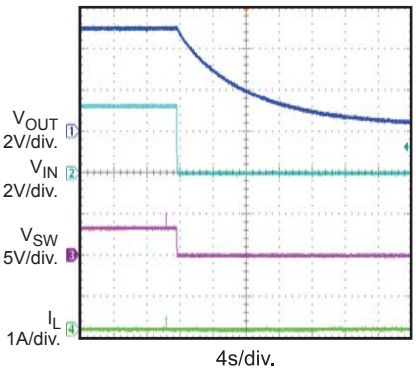
V_{IN} Start-Up
I_{OUT} = 0A



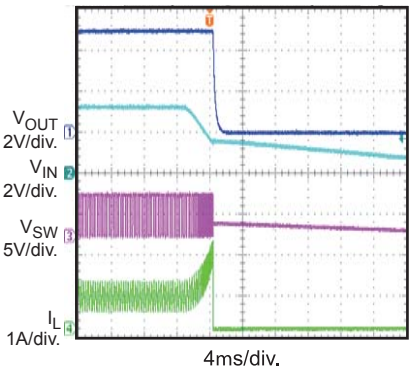
V_{IN} Start-Up
R_{LOAD} = 10Ω



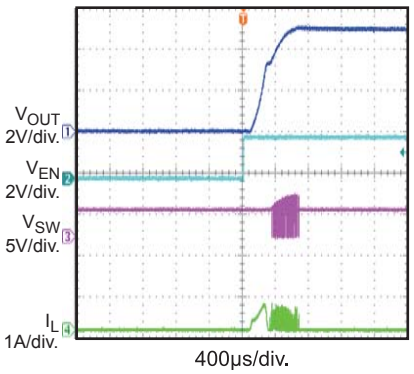
V_{IN} Shutdown
I_{OUT} = 0A



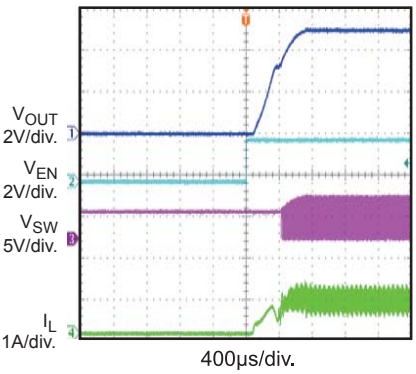
V_{IN} Shutdown
R_{LOAD} = 10Ω



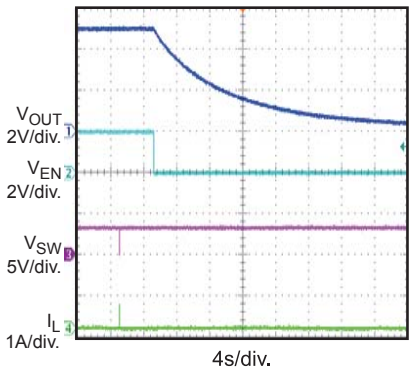
EN Start-Up
I_{OUT} = 0A



EN Start-Up
R_{LOAD} = 10Ω



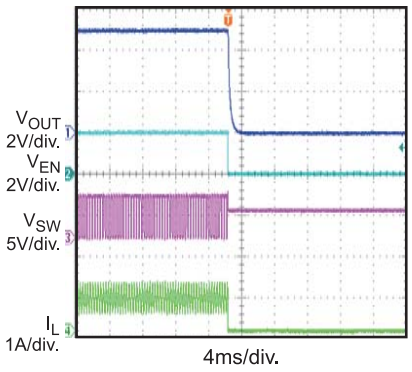
EN Shutdown
I_{OUT} = 0A



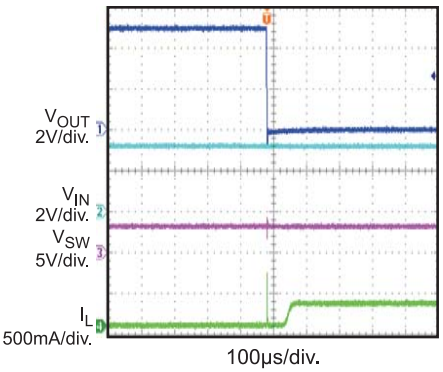
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

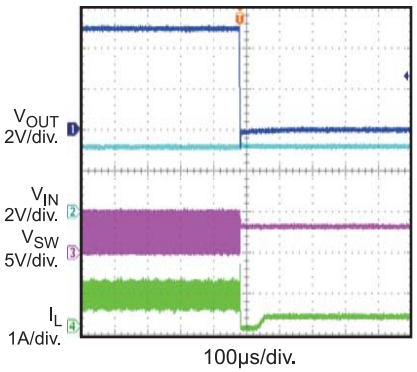
EN Shutdown
R_{LOAD} = 10Ω



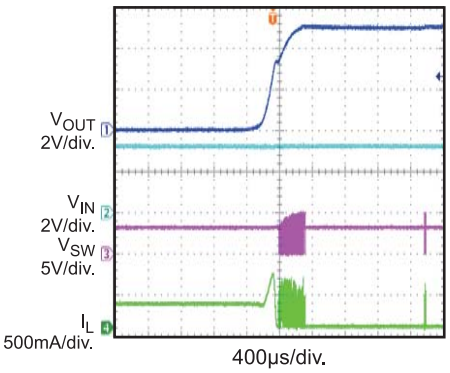
SCP Entry
I_{OUT} = 0A to Short



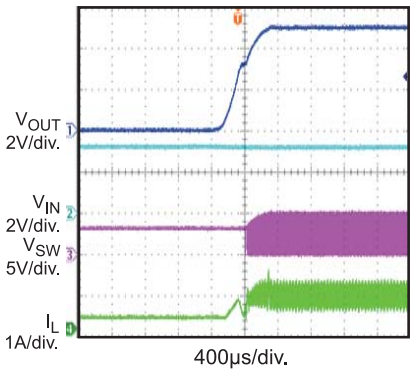
SCP Entry
R_{LOAD} = 10Ω to Short



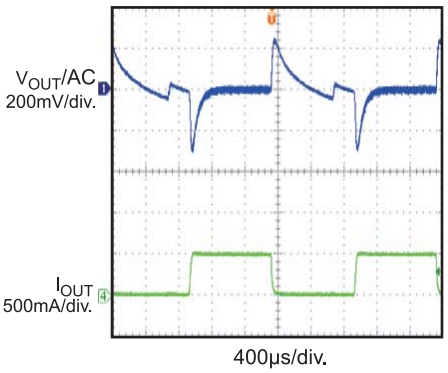
SCP Recovery
I_{OUT} = Short to 0A



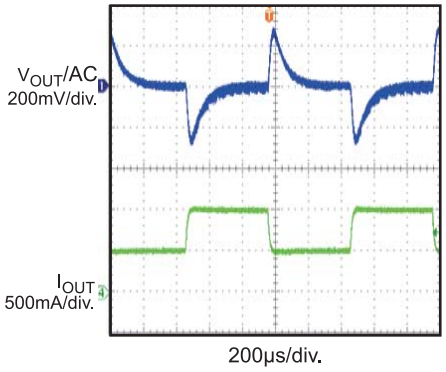
SCP Recovery
R_{LOAD} = Short to 10Ω



Load Transient
I_{OUT} = 0A to 0.5A



Load Transient
I_{OUT} = 0.5A to 1A



PIN FUNCTIONS

Pin #	Name	Pin Function
1	IN	**Power supply input.** The start-up bias is derived from IN and must be bypassed locally. Once the OUT voltage exceeds the IN voltage, the bias power comes from OUT.
2	OUT	**Output.** OUT is the drain of the internal synchronous rectifier MOSFET. Bias power is derived from OUT when V_{OUT} is higher than V_{IN}. The PCB trace length from OUT to the output filter capacitor(s) should be as short and wide as possible. The output disconnect feature allows OUT to be disconnected completely from IN when EN is low.
3	SW	**Power switch output.** SW is the connection node of the internal low-side MOSFET and synchronous MOSFET. Connect the power inductor between SW and the input power. Keep the PCB trace length as short and wide as possible to reduce EMI and voltage spikes.
4	PGND	**Power ground.**
5	FTY	**Factory use only.** Leave FTY floating or connect it to ground in application.
6	AGND	**Analog ground.**
7	FB	**Feedback.** Connect to the tap of an external resistive voltage divider from the output to FB to set the output voltage.
8	EN	**Chip enable control input.** Set EN higher than 1.2V to turn on the regulator. Set EN lower than 0.4V to turn off the regulator.

FUNCTION DIAGRAM

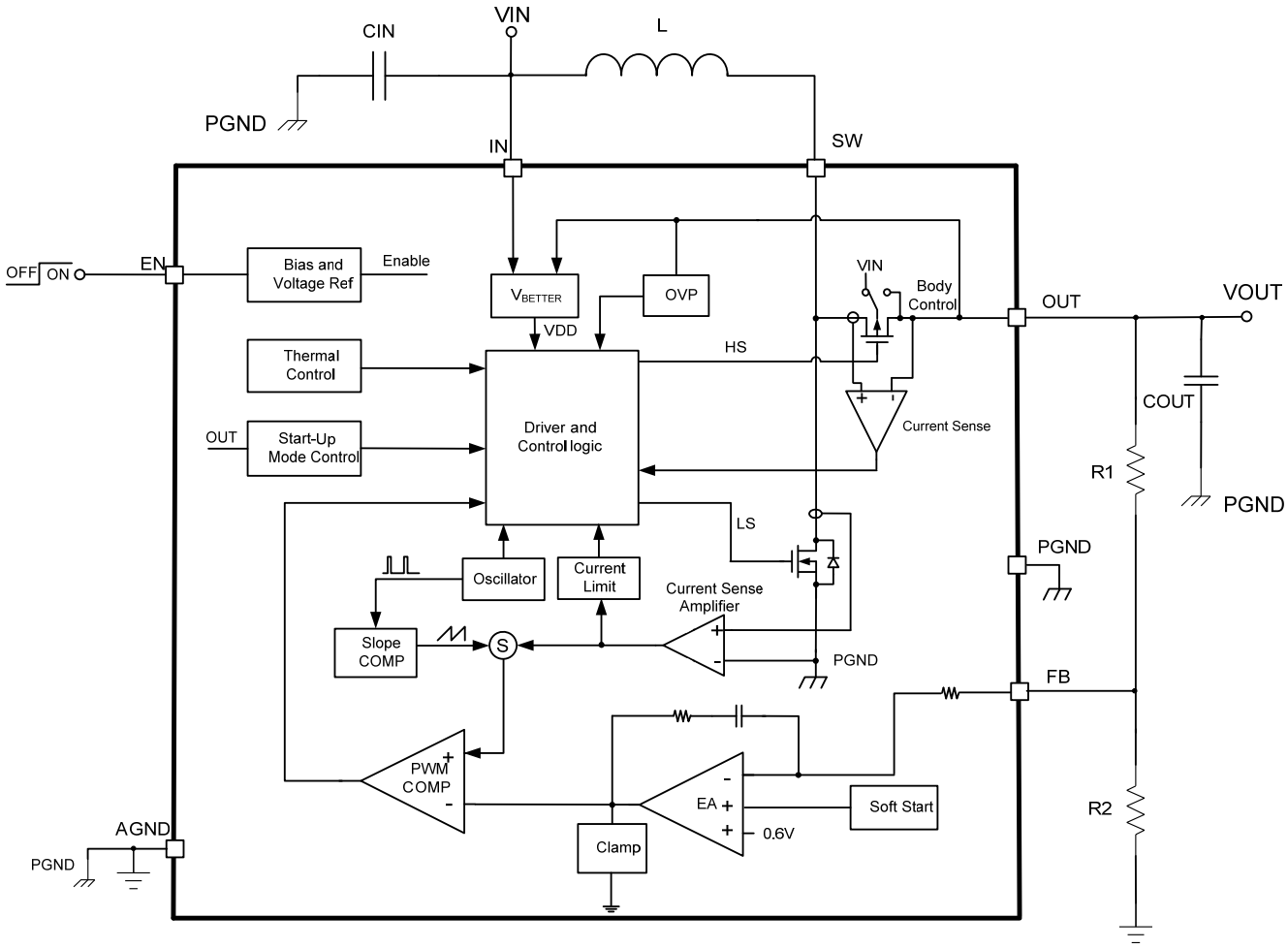


Figure 1: Functional Block Diagram

OPERATION

The MP3414A is a 1MHz synchronous step-up converter in a compact TSOT23 package with true output disconnect. The device features a fixed-frequency, current-mode PWM control for good line and load regulation. Internal soft start and loop compensation simplify the design process and minimize external components. The combined internal low $R_{DS\ (ON)}$ MOSFETs and frequency stretching allow the MP3414A to maintain high efficiency over a wide current load range.

Start-Up

When enabled, the MP3414A starts up in linear charge mode. During the linear charge, the rectified PMOS turns on until the output voltage is charged close to V_{IN}. To avoid inrush current, the PMOS current is limited to about 0.3A (when V_{OUT} is 0V). The PMOS linear charge current limit is increased to about 0.8A while V_{OUT} rises to 3.3V (if V_{IN} is higher than 3.3V). This circuit helps limit the output current under short-circuit conditions. Once the output voltage reaches V_{IN}, the linear charging period elapses, and the device starts switching. V_{OUT} starts to rise under the control of the internal soft start (SS). In boost switching conditions, the current limit is 3.6A, typically.

When the output voltage is higher than V_{IN}, the MP3414A powers its internal circuits from V_{OUT} instead of V_{IN}. This allows strong driving capabilities and high efficiency, even if V_{IN} drops as low as 1.8V.

Soft Start (SS)

The MP3414A provides a soft start (SS) by charging an internal capacitor with a current source. During the linear charge period, the SS signal keeps rising, following FB. Once the linear charge elapses, the voltage on the SS capacitor is charged and ramps up the reference voltage based on the internal fixed slew-rate. The SS capacitor is discharged completely during a commanded shutdown, thermal shutdown, or short circuit at the output.

Device Enable (EN)

The device begins operating if EN is set higher than 1.2V. It enters shutdown mode if EN is lower than 0.4V. In shutdown mode, the regulator stops switching, all internal control circuits switch off, and the output disconnects from the input completely.

Power-Save Mode (PSM)

The MP3414A enters power-save mode (PSM) automatically when the load decreases. It switches back to PWM mode when the load increases. In PSM, the converter stretches the frequency down to save switching and driver losses. In addition, the switch frequency is stretched down too when the input voltage is close to the output voltage (which triggers the minimum on-time if kept at a 1MHz frequency). This helps decrease the output ripple by avoiding group-pulse mode. Under a very light-load condition, the MP3414A continues to run in group-pulse mode to regulate the output voltage and save more power.

Error Amplifier (EA)

The error amplifier (EA) is an internally compensated amplifier. The EA compares the internal 0.6V reference voltage against V_{FB} to generate an EA signal, which in turn controls V_{OUT}. The output voltage of the MP3414A is adjusted via FB by an external resistor divider. See Equation (1):

$$V_{OUT} = 0.6V \times (1 + \frac{R1}{R2}) \quad (1)$$

Setting a high value for R1 and R2 achieves a low quiescent current. However, a resistance set too high will be sensitive to noise and lead to a low loop bandwidth. Set the R1 value between 499kΩ to 1MΩ for good leakage, stability and transient balance.

Current Sensing

In a linear charge condition, the high-side PMOS current is sensed and compared with the current limit threshold. The compared output manages the linear charge current.

In a boost switching condition, lossless current sensing converts the NMOS switch current signal to a voltage that is summed with the internal slope compensation. The summed signal is compared with the EA output to provide a peak current control command for the PWM. The peak switch current is limited to approximately 3.6A. The switch current signal is

blanked for 60ns internally to enhance noise immunity.

Output Disconnect

The MP3414A is designed to allow a true output disconnect by eliminating body diode conduction of the internal PMOS rectifier. This allows V_{OUT} to reach 0V during shutdown, drawing zero current from the input source.

This also allows for inrush current limiting at start-up, which minimizes the surge current seen by the input supply. To obtain the advantages of the output disconnect, there must NOT be an external Schottky diode connected between SW and V_{OUT}.

Overload (OLP) and Short-Circuit Protection (SCP)

When an overload or a short circuit occurs, the output voltage drops. If V_{OUT} drops below V_{IN} (0.3V), the MP3414A stops for about 50μs and then runs in a linear charge mode at start-up. If the overload or short circuit is removed, the MP3414A restarts automatically under SS control.

Over-Voltage Protection (OVP)

If the voltage on V_{OUT} is higher than the typical 6V threshold, the boost switching stops. After the output drops to about 5.7V, the switching recovers automatically. This protects the internal power MOSFET from over-voltage stress.

Thermal Shutdown (TSD)

The device has an internal temperature monitor. If the die temperature exceeds 155°C, the converter turns off. Once the temperature drops below 130°C, the converter restarts.

APPLICATION INFORMATION

COMPONENT SELECTION

Input Capacitor Selection

Low equivalent series resistance (ESR) input capacitors reduce input switching noise and reduce the peak current drawn from the battery. Ceramic capacitors are recommended for input decoupling and should be placed as close to the device as possible. A ceramic capacitor larger than 10µF is recommended to limit the V_{IN} ripple.

Output Capacitor Selection

To ensure stability over the full operating range, the output capacitor requires a minimum capacitance value of 22µF at the programmed output voltage. A higher capacitance value may be required to lower the output and transient ripple. Low ESR capacitors such as X5R or X7R type are recommended. Supposing the ESR is zero, use Equation 2 to calculate the minimum output capacitor to support the ripple in the PWM mode:

$$C_O \geq \frac{I_O \times (V_{OUT(MAX)} - V_{IN(MIN)})}{f_S \times V_{OUT(MAX)} \times \Delta V} \quad (2)$$

$V_{OUT(MAX)}$ = Maximum output voltage
$V_{IN(MIN)}$ = Minimum input voltage
I_O = Output current
f_S = Switching frequency
ΔV = Acceptable output ripple

A 1µF ceramic capacitor is recommended between V_{OUT} and PGND with a short loop. This reduces spikes on the SW node and improves EMI performance.

Inductor Selection

The MP3414A utilizes small surface mounted chip inductors due to its 1MHz switching frequency. Inductor values between 1µH and 2.2µH are suitable for most applications. Larger values of inductance allow for slightly greater output current capabilities by reducing the inductor ripple current. However, larger value inductances will increase the component size. The minimum inductance value is given using Equation (3):

$$L \geq \frac{V_{IN(MIN)} \times (V_{OUT(MAX)} - V_{IN(MIN)})}{V_{OUT(MAX)} \times \Delta I_L \times f_S} \quad (3)$$

ΔI_L = Acceptable inductor current ripple

Typically, the inductor current ripple is set to 30% to 50% of the maximum inductor current. Maintain a low DCR (series resistance of the inductor) to reduce resistive power loss. The saturated current (I_{SAT}) should be large enough to support the peak current.

PCB Layout Guidelines

Efficient PCB layout is critical for high-frequency switching power supplies. Poor layout can result in reduced performance, excessive EMI, resistive loss, system instability, and even over-voltage stress.

For best results, refer to Figure 2 and follow the guidelines below:

1. Place the output capacitor as close as possible to OUT with minimal distance to PGND. A small decoupling capacitor should be in parallel with the bulk output capacitor.
2. Place the small decoupling capacitor as close as possible to OUT and PGND. This is very important to reduce the spikes on SW and improve EMI performance.
3. Place the input capacitor and inductor as close as possible to IN and SW. The trace between the inductor and SW should be as wide and short as possible.
4. Place the feedback loop far away from all noise sources (such as SW). The feedback divider resistors should be as close as possible to FB and AGND.
5. Tie the ground return of the input/output capacitors as close as possible to PGND using a large copper GND area. Vias around GND are recommended to lower the die temperature.

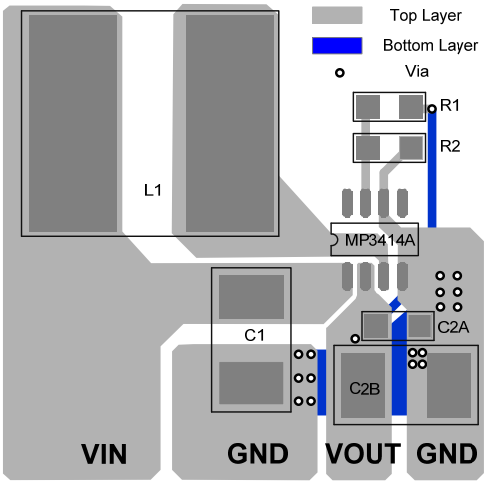


Figure 2: Recommended PCB Layout

Design Example

See Table 1 below for a design example following the application guidelines for the specifications below:

Table 1: Design Example

V_{IN}	2.8V-4.2V
V_{OUT}	5V
I_{OUT}	0A-1A

The typical application circuit for V_{OUT} = 5V in Figure 3 shows the detailed application schematic and the basis for the typical performance waveforms. For additional detailed device applications, please refer to the related evaluation board datasheet (EVB).

TYPICAL APPLICATION CIRCUITS

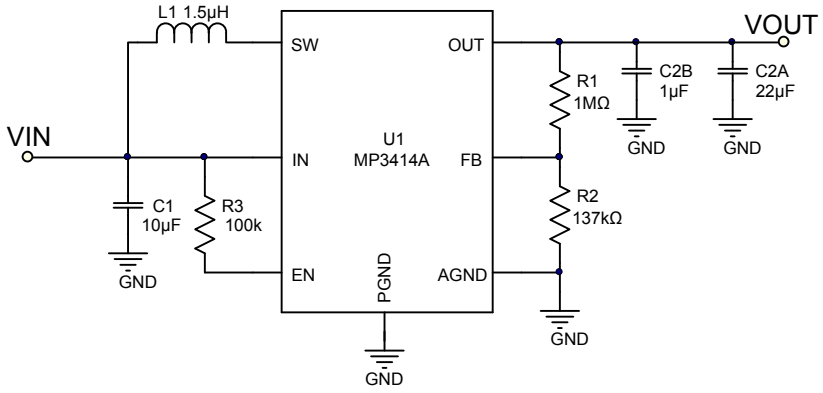


Figure 3: Typical Boost Application Circuit, V_{IN} = 2.8V to 4.2V, V_{OUT} = 5V, I_{OUT} = 0A-1A

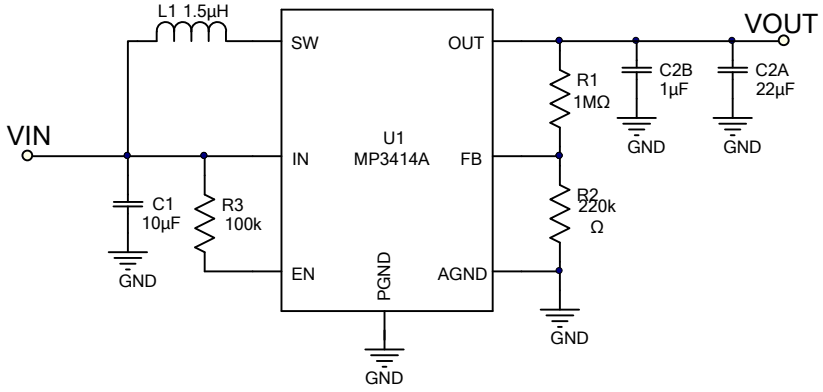
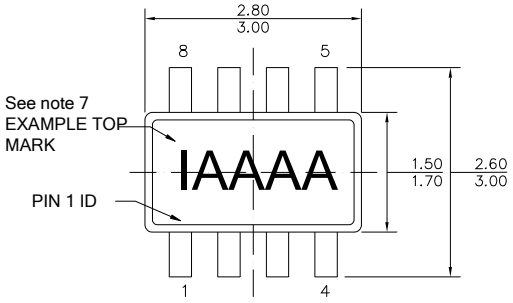


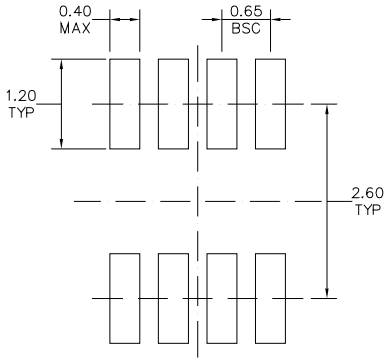
Figure 4: Typical Boost Application Circuit, V_{IN} = 1.8V to 3V, V_{OUT} = 3.3V, I_{OUT} = 0A-1A

PACKAGE INFORMATION

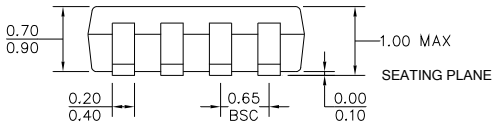
TSOT23-8



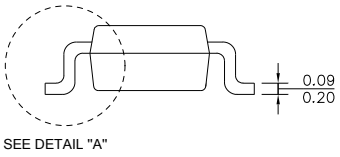
TOP VIEW



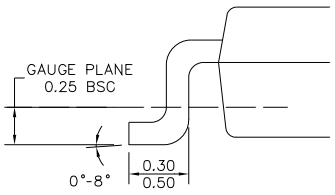
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK).