3.3 VOLT CMOS CLOCKED FIFO WITH BUS-MATCHING AND BYTE SWAPPING 64 x 36

IDT72V3613

OBSOLETE PART

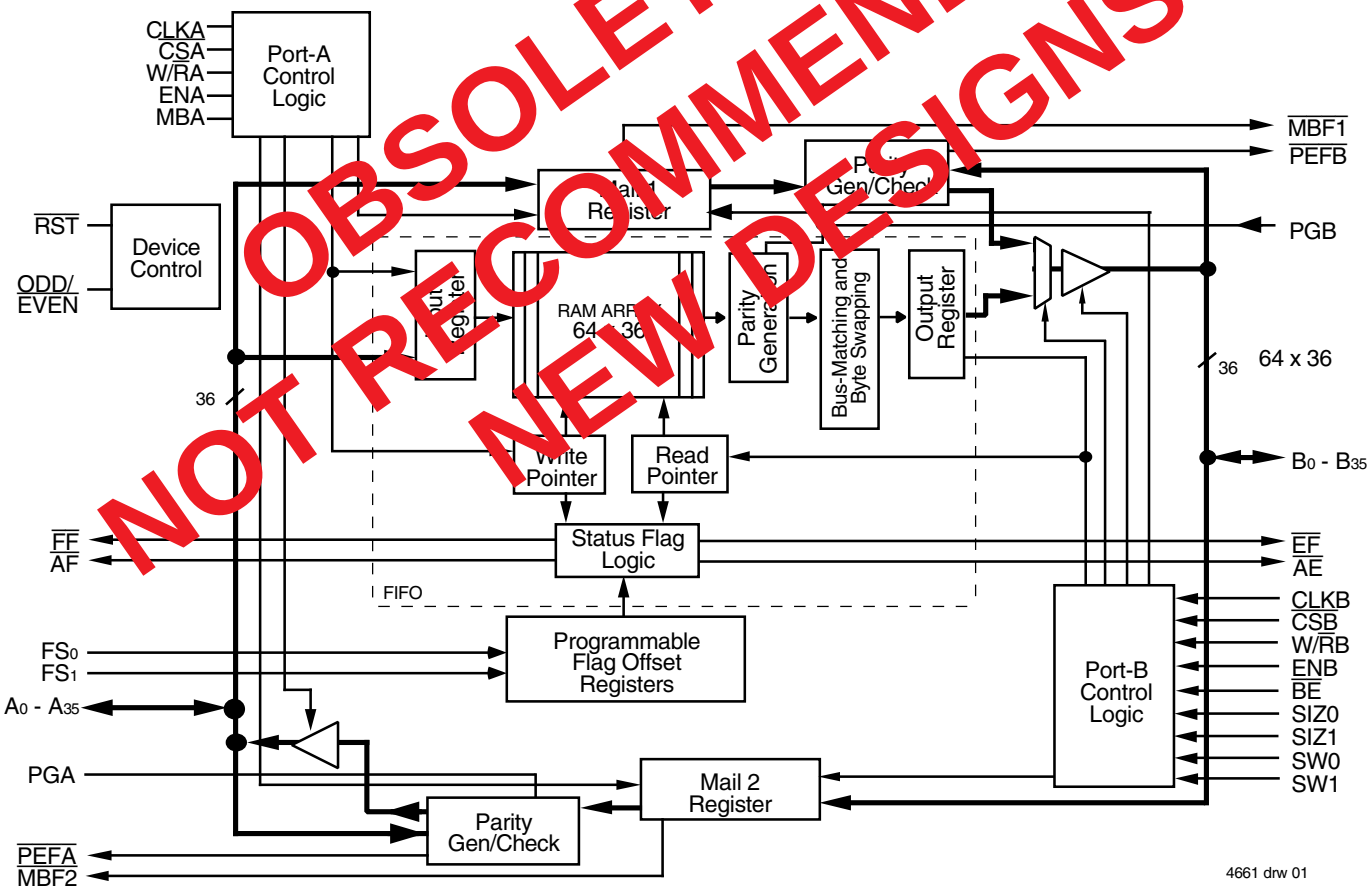
FEATURES:

- 64 x 36 storage capacity FIFO buffering data from Port A to Port B
- Supports clock frequencies up to 67MHz
- Fast access times of 10ns
- Free-running CLKA and CLKB may be asynchronous or coincident (permits simultaneous reading and writing of data on a single clock edge)
- Mailbox bypass registers in each direction
- Dynamic Port B bus sizing of 36 bits (long word), 18 bits (word), and 9 bits (byte)
- Selection of Big- or Little-Endian format for word and byte bus sizes
- Three modes of byte-order swapping on Port B
- Programmable Almost-Full and Almost-Empty flags
- Microprocessor interface control logic
- $\overline{FF}$, $\overline{AF}$ flags synchronized by CLKA
- $\overline{EF}$, $\overline{AE}$ flags synchronized by CLKB
- Passive parity checking on each Port
- Parity Generation can be selected for each Port
- Available in space saving 120-pin thin quad flat package (TQFP)
- Green parts available, see ordering information

DESCRIPTION:

The IDT72V3613 is designed to run off a 3.3V supply for exceptionally low-power consumption. This device is a monolithic, high-speed, low-power, CMOS synchronous (clocked) FIFO memory which supports clock frequencies up to 67 MHz and has read-access times as fast as 10 ns. The 64 x 36 dual-port SRAM FIFO buffers data from port A to port B. The FIFO operates in IDT Standard mode and has flags to indicate empty and full conditions, and two programmable flags, Almost-Full (AF) and Almost-Empty (AE), to indicate when a selected number of words is stored in memory. FIFO data on port B can be output in 36-bit, 18-bit, and 9-bit formats with a choice of Big- or Little-Endian configurations. Three modes of byte-order swapping are possible with any bus-size selection. Communication between each port can bypass the FIFO via two

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION (CONTINUED)

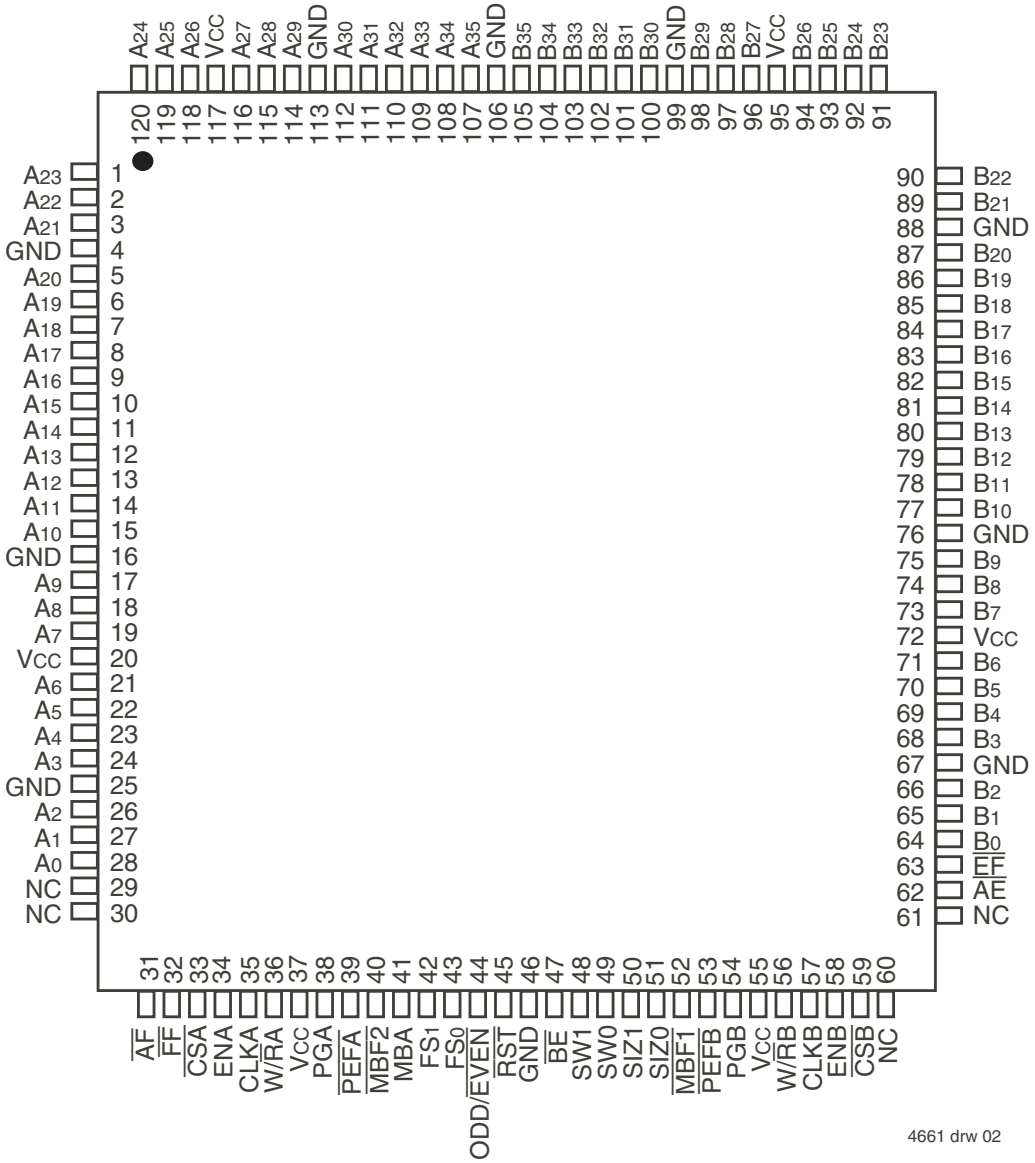
36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Parity is checked passively on each port and may be ignored if not desired. Parity generation can be selected for data read from each port. Two or more devices may be used in parallel to create wider data paths.

The IDT72V3613 is a synchronous (clocked) FIFO, meaning each port employs a synchronous interface. All data transfers through a port are gated to the LOW-to-HIGH transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple interface between microprocessors and/or buses with synchronous interfaces.

The Full Flag ($\overline{FF}$) and Almost-Full ($\overline{AF}$) flag of the FIFO are two-stage synchronized to the port clock (CLKA) that writes data into its array. The Empty Flag ($\overline{EF}$) and Almost-Empty ($\overline{AE}$) flag of the FIFO are two-stage synchronized to the port clock (CLKB) that reads data from its array.

The IDT72V3613 is characterized for operation from 0°C to 70°C. This device is fabricated using high speed, submicron CMOS technology.

PIN CONFIGURATION



4661 drw 02

NOTES:
1. Pin 1 idenifier in corner.
2. NC = No internal connection

TQFP (PNG120, order code: PF)
TOP VIEW

PIN DESCRIPTION

Symbol	Name	I/O	Description
A0-A35	Port A Data	I/O	36-bit bidirectional data port for side A.
$\overline{AE}$	Almost-Empty Flag	O Port B	Programmable Almost-Empty flag synchronized to CLKB. It is LOW when Port B the number of 36-bit words in the FIFO is less than or equal to the value in the offset register, X.
$\overline{AF}$	Almost-Full Flag	O Port A	Programmable Almost-Full flag synchronized to CLKA. It is LOW when the number of 36-bit empty empty locations in the FIFO is less than or equal to the value in the offset register, X.
B0-B35	Port B Data	I/O	36-bit bidirectional data port for side B
$\overline{BE}$	Big-Endian Select	I	Selects the bytes on port B used during byte or word FIFO reads. A LOW on $\overline{BE}$ selects the most significant bytes on B0-B35 for use, and a HIGH selects the least significant bytes.
CLKA	Port A Clock	I	CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. $\overline{FF}$ and $\overline{AF}$ are synchronized to the LOW-to-HIGH transition of CLKA.
CLKB	Port B Clock	I	CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. Port-B byte swapping and data port sizing operations are also synchronous to the LOW-to-HIGH transition of CLKB. $\overline{EF}$ and $\overline{AE}$ are synchronized to the LOW-to-HIGH transition of CLKB.
$\overline{CSA}$	Port A Chip Select	I	$\overline{CSA}$ must be LOW to enable a LOW-to-HIGH transition of CLKA to read or write data on port A. The A0-A35 outputs are in the high-impedance state when $\overline{CSA}$ is HIGH.
$\overline{CSB}$	Port B Chip Select	I	$\overline{CSB}$ must be LOW to enable a LOW-to-HIGH transition of CLKB to read or write data on port B. The B0-B35 outputs are in the high-impedance state when $\overline{CSB}$ is HIGH.
$\overline{EF}$	Empty Flag	O Port B	$\overline{EF}$ is synchronized to the LOW-to-HIGH transition of CLKB. When $\overline{EF}$ is LOW, the FIFO is empty, and reads from its memory are disabled. Data can be read from the FIFO to its output register when $\overline{EF}$ is HIGH. $\overline{EF}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKB after data is loaded into empty FIFO memory.
ENA	Port A Enable	I	ENA must be HIGH to enable a LOW-to-HIGH transition of CLKA to read or write data on port A.
ENB	Port B Enable	I	ENB must be HIGH to enable a LOW-to-HIGH transition of CLKB to read or write data on port B.
$\overline{FF}$	Full Flag	O Port A	$\overline{FF}$ is synchronized to the LOW-to-HIGH transition of CLKA. When $\overline{FF}$ is LOW, the FIFO is full, and writes to its memory are disabled. $\overline{FF}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKA after reset.
FS1, FS0	Flag Offset Selects	I	The LOW-to-HIGH transition of $\overline{RST}$ latches the values of FS0 and FS1, which loads one of four preset values into the Almost-Full flag and Almost-Empty flag offsets.
MBA	Port A Mailbox Select	I	A high level on MBA chooses a mailbox register for a port A read or write operation. When the A0-A35 outputs are active, mail2 register data is output.
$\overline{MBF1}$	Mail1 Register Flag	O	$\overline{MBF1}$ is set LOW by a LOW-to-HIGH transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is set LOW. $\overline{MBF1}$ is set HIGH by a LOW-to-HIGH transition of CLKB when a port B read is selected and both SIZ1 and SIZ0 are HIGH. $\overline{MBF1}$ is set HIGH when the device is reset.
$\overline{MBF2}$	Mail2 Register Flag	O	$\overline{MBF2}$ is set LOW by a LOW-to-HIGH transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is set LOW. $\overline{MBF2}$ is set HIGH by a LOW-to-HIGH transition of CLKA when a port A read is selected and MBA is HIGH. $\overline{MBF2}$ is set HIGH when the device is reset.
ODD/ $\overline{EVEN}$	Odd/Even Parity Select	I	Odd parity is checked on each port when ODD/$\overline{EVEN}$ is HIGH, and even parity is checked when ODD/$\overline{EVEN}$ is LOW. ODD/$\overline{EVEN}$ also selects the type of parity generated for each port if parity generation is enabled for a read operation.
$\overline{PEFA}$	Port A Parity Error Flag	O	When any valid byte applied to terminals A0-A35 fails parity, $\overline{PEFA}$ is LOW. Bytes (Port A) are organized as A0-A8, A9-A17, A18-A26, and A27-A35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/$\overline{EVEN}$ input. The parity trees used to check the A0-A35 inputs are shared by the mail2 register to generate parity if parity generation is selected by PGA. Therefore, if a mail2 read with parity generation is set up by having $\overline{CSA}$ LOW, ENA HIGH, W/$\overline{RA}$ LOW, MBA HIGH and PGA HIGH, the $\overline{PEFA}$ flag is forced HIGH regardless of the state of the A0-A35 inputs.

PIN DESCRIPTION (CONTINUED)

Symbol	Name	I/O	Description
$\overline{PEFB}$	Port B Parity Error Flag	O (Port B)	When any valid byte applied to terminals B0-B35 fails parity, $\overline{PEFB}$ is LOW. Bytes are organized as B0-B8, B9-B17, B-18-B26, and B27-B35, with the most significant bit of each byte serving as the parity bit. A byte is valid when it is used by the bus size selected for port B. The type of parity checked is determined by the state of the ODD/$\overline{EVEN}$ input. The parity trees used to check the B0-B35 inputs are shared by the mail1 register to generate parity if parity generation is selected by PGB. Therefore, if a mail1 read with parity generation is set up by having $\overline{CSB}$ LOW, ENB HIGH, W/$\overline{RB}$ LOW, SIZ1 and SIZ0 HIGH and PGB HIGH, the $\overline{PEFB}$ flag is forced HIGH regardless of the state of the B0-B35 inputs.
PGA	Port A Parity Generation	I	Parity is generated for data reads from the mail2 register when PGA is HIGH. The type of parity generated is selected by the state of the ODD/$\overline{EVEN}$ input. Bytes are organized at A0-A8, A9-A17, A18-A26, and A27-A35. The generated parity bits are output in the most significant bit of each byte.
PGB	Port B Parity Generation	I	Parity is generated for data reads from port B when PGB is HIGH. The type of parity generated is selected by the state of the ODD/$\overline{EVEN}$ input. Bytes are organized as B0-B8, B9-B17, B18-B26, and B27-B35. The generated parity bits are output in the most significant bit of each byte.
$\overline{RST}$	Reset	I	To reset the device, four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while $\overline{RST}$ is LOW. This sets the $\overline{AF}$, $\overline{MBF1}$, and $\overline{MBF2}$ flags HIGH and the $\overline{EF}$, $\overline{AE}$, and $\overline{FF}$ flags LOW. The LOW-to-HIGH transition of $\overline{RST}$ latches the status of the FS1 and FS0 inputs to select Almost-Full flag and Almost-Empty flag offset.
SIZ0, SIZ1	Port B Bus Size Selects	I (Port B)	A LOW-to-HIGH transition of CLKB latches the states of SIZ0, SIZ1, and $\overline{BE}$, and the following LOW-to-HIGH transition of CLKB implements the latched states as a port B bus size. Port B bus sizes can be long word, word, or byte. A HIGH on both SIZ0 and SIZ1 chooses a mailbox register for a port B 36-bit write or read.
SW0, SW1	Port B Byte Swap Selects	I (Port B)	At the beginning of each long word FIFO read, one of four modes of byte-order swapping is selected by SW0 and SW1. The four modes are no swap, byte swap, word swap, and byte-word swap. Byte-order swapping is possible with any bus-size selection.
W/$\overline{RA}$	Port A Write/Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on port A for a LOW-to-HIGH transition of CLKA. The A0-A35 outputs are in the high-impedance state when W/$\overline{RA}$ is HIGH.
W/$\overline{RB}$	Port B Write/Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on port B for a LOW-to-HIGH transition of CLKB. The B0-B35 outputs are in the high-impedance state when W/$\overline{RB}$ is HIGH.

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (unless otherwise noted)(1)

Symbol	Rating	Commercial	Unit
V_{CC}	Supply Voltage Range	–0.5 to +4.6	V
V_I(2)	Input Voltage Range	–0.5 to V_{CC}+0.5	V
V_O(2)	Output Voltage Range	–0.5 to V_{CC}+0.5	V
I_{IK}	Input Clamp Current, (V_I < 0 or V_I > V_{CC})	±20	mA
I_{OK}	Output Clamp Current, (V_O < 0 or V_O > V_{CC})	±50	mA
I_{OUT}	Continuous Output Current, (V_O = 0 to V_{CC})	±50	mA
I_{CC}	Continuous Current Through V_{CC} or GND	±500	mA
T_{STG}	Storage Temperature Range	–65 to 150	°C

NOTES:
1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	HIGH Level Input Voltage	2	—	V_{CC}+0.5	V
V_{IL}	LOW-Level Input Voltage	—	—	0.8	V
I_{OH}	HIGH-Level Output Current	—	—	–4	mA
I_{OL}	LOW-Level Output Current	—	—	8	mA
T_A	Operating Free-air Temperature	0	—	70	°C

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (unless otherwise noted)

Symbol	Parameter	Test Conditions		IDT72V3613 Commercial t_{CLK} = 15 ns			Unit
				Min.	Typ.(1)	Max.	
V_{OH}	Output Logic "1" Voltage	V_{CC} = 3.0V,	I_{OH} = –4 mA	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage	V_{CC} = 3.0V,	I_{OL} = 8 mA	—	—	0.5	V
I_{LI}	Input Leakage Current (Any Input)	V_{CC} = 3.6V,	V_I = V_{CC} or 0	—	—	±5	µA
I_{LO}	Output Leakage Current	V_{CC} = 3.6V,	V_O = V_{CC} or 0	—	—	±5	µA
I_{CC}(2)	Standby Current	V_{CC} = 3.6V,	V_I = V_{CC} - 0.2V or 0	—	—	500	µA
C_{IN}	Input Capacitance	V_I = 0,	f = 1 MHz	—	4	—	pF
C_{OUT}	Output Capacitance	V_O = 0,	f = 1 MHZ	—	8	—	pF

NOTES:
1. All typical values are at V_{CC} = 3.3V, T_A = 25°C.
2. For additional I_{CC} information, see Figure 1, *Typical Characteristics: Supply Current (I_{CC}) vs. Clock Frequency (fs)*.

DETERMINING ACTIVE CURRENT CONSUMPTION AND POWER DISSIPATION

The ICC(f) current for the graph in Figure 1 was taken while simultaneously reading and writing the FIFO on the IDT72V3613 with CLKA and CLKB set to fs. All date inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero-capacitance load. Once the capacitive lead per data-output channel is known, the power dissipation can be calculated with the equation below.

CALCULATING POWER DISSIPATION

With $I_{CC(f)}$ taken from Figure 1, the maximum power dissipation (P_T) of the IDT72V3613 may be calculated by:

$$P_T = V_{CC} \times I_{CC(f)} + \sum_{N} (C_L \times (V_{OH} - V_{OL})^2 \times f_o)$$

where:

N	=	number of used outputs (36-bit (long word), 18-bit (word) or 9-bit (byte) bus-size)
C_L	=	output capacitance load
f_o	=	switching frequency of an output
V_{OH}	=	output high-level voltage
V_{OL}	=	output high-level voltage

When no reads or writes are occurring on the IDT72V3613, the power dissipated by a single clock (CLKA or CLKB) input running at frequency fs is calculated by:

$$P_T = V_{CC} \times f_S \times 0.025 mA/MHz$$

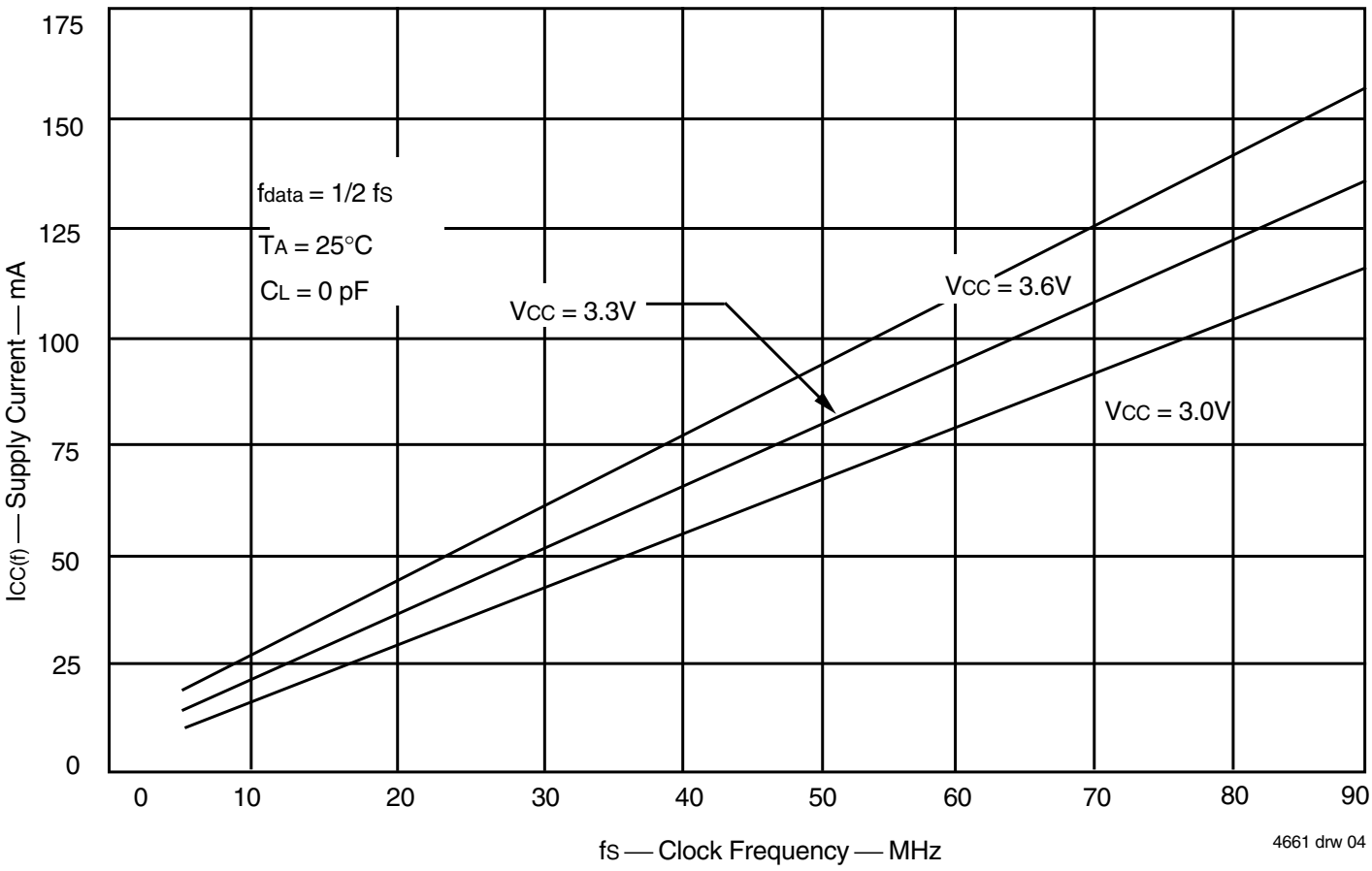


Figure 1. Typical Characteristics: Supply Current (Icc) vs Clock Frequency (fs)

AC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE

Commercial: Vcc=3.3V± 0.30V; T_A = 0°C to +70°C; JEDEC JESD8-A compliant

Symbol	Parameter	IDT72V3613L15		Unit
		Min.	Max.	
f_S	Clock Frequency, CLKA or CLKB	–	66.7	MHz
t_{CLK}	Clock Cycle Time, CLKA or CLKB	15	–	ns
t_{CLKH}	Pulse Duration, CLKA and CLKB HIGH	6	–	ns
t_{CLKL}	Pulse Duration, CLKA and CLKB LOW	6	–	ns
t_{DS}	Setup Time, A0-A35 before CLKA↑ and B0-B35 before CLKB↑	4	–	ns
t_{ENS}	Setup Time, $\overline{CSA}$, W/$\overline{R}$A, ENA, and MBA before CLKA↑; $\overline{CSB}$, W/$\overline{R}$B, and ENB before CLKB↑	5	–	ns
t_{SZS}	Setup Time, SIZ0, SIZ1, and $\overline{BE}$ before CLKB↑	4	–	ns
t_{SWS}	Setup Time, SW0 and SW1 before CLKB↑	6	–	ns
t_{PGS}	Setup Time, ODD/$\overline{EVEN}$ and PGB before CLKB↑(1)	4	–	ns
t_{RSTS}	Setup Time, $\overline{RST}$ LOW before CLKA↑ or CLKB↑(2)	5	–	ns
t_{FSS}	Setup Time, FS0 and FS1 before $\overline{RST}$ HIGH	5	–	ns
t_{DH}	Hold Time, A0-A35 after CLKA↑ and B0-B35 after CLKB↑	1	–	ns
t_{ENH}	Hold Time, $\overline{CSA}$ W/$\overline{R}$A, ENA and MBA after CLKA↑; $\overline{CSB}$, W/$\overline{R}$B, and ENB after CLKB↑	1	–	ns
t_{SZH}	Hold Time, SIZ0, SIZ1, and $\overline{BE}$ after CLKB↑	2	–	ns
t_{SWH}	Hold Time, SW0 and SW1 after CLKB↑	2	–	ns
t_{PGH}	Hold Time, ODD/$\overline{EVEN}$ and PGB after CLKB↑(1)	0	–	ns
t_{RSTH}	Hold Time, $\overline{RST}$ LOW after CLKA↑ or CLKB↑(2)	5	–	ns
t_{FSH}	Hold Time, FS0 and FS1 after $\overline{RST}$ HIGH	4	–	ns
t_{SKEW1}(3)	Skew Time, between CLKA↑ and CLKB↑ for $\overline{EF}$ and $\overline{FF}$	8	–	ns
t_{SKEW2}(3,4)	Skew Time, between CLKA↑ and CLKB↑ for $\overline{AE}$ and $\overline{AF}$	14	–	ns

NOTES:
1. Only applies for a clock edge that does a FIFO read.
2. Requirement to count the clock edge as one of at least four needed to reset a FIFO.
3. Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.
4. Design simulated, not tested.

SWITCHING CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, C_L = 30pF

Commercial: Vcc=3.3V± 0.30V; T_A = 0°C to +70°C; JEDEC JESD8-A compliant

Symbol	Parameter	IDT72V3613L15		Unit
		Min.	Max.	
t_A	Access Time, CLKA↑ to A0-A35 and CLKB↑ to B0-B35	2	10	ns
t_{WFF}	Propagation Delay Time, CLKA↑ to $\overline{FF}$	2	10	ns
t_{REF}	Propagation Delay Time, CLKB↑ to $\overline{EF}$	2	10	ns
t_{PAE}	Propagation Delay Time, CLKB↑ to $\overline{AE}$	2	10	ns
t_{PAF}	Propagation Delay Time, CLKA↑ to $\overline{AF}$	2	10	ns
t_{PMF}	Propagation Delay Time, CLKA↑ to $\overline{MBF1}$ LOW or $\overline{MBF2}$ HIGH and CLKB↑ to $\overline{MBF2}$ LOW or $\overline{MBF1}$ HIGH	1	9	ns
t_{PMR}	Propagation Delay Time, CLKA↑ to B0-B35[1] and CLKB↑ to A0-A35[2]	2	10	ns
t_{PPE}[3]	Propagation delay time, CLKB↑ to $\overline{PEFB}$	2	10	ns
t_{MDV}	Propagation Delay Time, SIZ1, SIZ0 to B0-B35 valid	1	10	ns
t_{PDPE}	Propagation Delay Time, A0-A35 valid to $\overline{PEFA}$ valid; B0-B35 valid to $\overline{PEFB}$ valid	2	10	ns
t_{POPE}	Propagation Delay Time, ODD/$\overline{EVEN}$ to $\overline{PEFA}$ and $\overline{PEFB}$	2	10	ns
t_{POPB}[4]	Propagation Delay Time, ODD/$\overline{EVEN}$ to parity bits (A8, A17, A26, A35) and (B8, B17, B26, B35)	2	10	ns
t_{PEPE}	Propagation Delay Time, $\overline{CSA}$, ENA, W/$\overline{R}$A, MBA, or PGA to $\overline{PEFA}$; $\overline{CSB}$, ENB, W/$\overline{R}$B, SIZ1, SIZ0, or PGB to $\overline{PEFB}$	1	10	ns
t_{PEPB}[4]	Propagation Delay Time, $\overline{CSA}$, ENA, W/$\overline{R}$A, MBA, or PGA to parity bits (A8, A17, A26, A35); $\overline{CSB}$, ENB, W/$\overline{R}$B, SIZ1, SIZ0, or PGB to parity bits (B8, B17, B26, B35)	2	10	ns
t_{RSF}	Propagation Delay Time, $\overline{RST}$ to $\overline{AE}$, $\overline{EF}$ LOW and $\overline{AF}$, $\overline{MBF1}$, $\overline{MBF2}$ HIGH	1	15	ns
t_{EN}	Enable Time, $\overline{CSA}$ and W/$\overline{R}$A LOW to A0-A35 active and $\overline{CSB}$ LOW and W/$\overline{R}$B HIGH to B0-B35 active	2	10	ns
t_{DIS}	Disable Time, $\overline{CSA}$ or W/$\overline{R}$A HIGH to A0-A35 at high-impedance and $\overline{CSB}$ HIGH or W/$\overline{R}$B LOW to B0-B35 at high-impedance	1	8	ns

NOTES:
1. Writing data to the mail1 register when the B0-B35 outputs are active and SIZ1 and SIZ0 are HIGH.
2. Writing data to the mail2 register when the A0-A35 outputs are active.
3. Only applies when a new port-B bus size is implemented by the rising CLKB edge.
4. Only applies when reading data from a mail register.

FUNCTIONAL DESCRIPTION

RESET ($\overline{RST}$)

The IDT72V3613 is reset by taking the Reset ($\overline{RST}$) input LOW for at least four port A Clock (CLKA) and four port B Clock (CLKB) LOW-to-HIGH transitions. The Reset input can switch asynchronously to the clocks. A device reset initializes the internal read and write pointers of the FIFO and forces the Full Flag ($\overline{FF}$) LOW, the Empty Flag ($\overline{EF}$) LOW, the Almost-Empty flag ($\overline{AE}$) LOW, and the Almost-Full flag ($\overline{AF}$) HIGH. A reset also forces the Mailbox Flags ($\overline{MBF1}$, $\overline{MBF2}$) HIGH. After a reset, $\overline{FF}$ is set HIGH after two LOW-to-HIGH transitions of CLKA. The device must be reset after power up before data is written to its memory.

A LOW-to-HIGH transition on the $\overline{RST}$ input loads the Almost-Full and Almost-Empty Offset register (X) with the value selected by the Flag Select (FS0, FS1) inputs. The values that can be loaded into the register are shown in Table 1. See Figure 5 for relevant FIFO Reset and preset value loading timing diagram.

FIFO WRITE/READ OPERATION

The state of the port A data (A0-A35) outputs is controlled by the port-A Chip Select ($\overline{CSA}$) and the port-A Write/Read select (W/$\overline{RA}$). The A0-A35 outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is HIGH. The A0-A35 outputs are active when both $\overline{CSA}$ and W/$\overline{RA}$ are LOW.

TABLE 1 – FLAG PROGRAMMING

FS1	FS0	$\overline{RST}$	ALMOST-FULL AND ALMOST-EMPTY FLAG OFFSET REGISTER (X)
H	H	↑	16
H	L	↑	12
L	H	↑	8
L	L	↑	4

Data is loaded into the FIFO from the A0-A35 inputs on a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, W/$\overline{RA}$ is HIGH, ENA is HIGH, MBA is LOW, and $\overline{FF}$ is HIGH (see Table 2). The relevant FIFO write timing diagram can found in Figure 6.

The state of the port B data (B0-B35) outputs is controlled by the port B Chip Select ($\overline{CSB}$) and the port B Write/Read select (W/$\overline{RB}$). The B0-B35 outputs are in the high-impedance state when either $\overline{CSB}$ or W/$\overline{RB}$ is HIGH. The B0-B35 outputs are active when both $\overline{CSB}$ and W/$\overline{RB}$ are LOW. Data is read from the FIFO to the B0-B35 outputs by a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ is LOW, W/$\overline{RB}$ is LOW, ENB is HIGH, $\overline{EFB}$ is HIGH, and either SIZ0 or SIZ1 is LOW (see Table 3). Relevant FIFO read timing diagrams together with Bus-Matching, Endian select and Byte-swapping operation can be found in Figures 7, 8 and 9.

The setup and hold-time constraints to the port clocks for the port Chip Selects ($\overline{CSA}$, $\overline{CSB}$) and Write/Read selects (W/$\overline{RA}$, W/$\overline{RB}$) are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is LOW during a clock cycle, the port's Chip Select and Write/Read select can change states during the setup and hold time window of the cycle.

SYNCHRONIZED FIFO FLAGS

Each FIFO flag is synchronized to its port clock through two flip-flop stages. This is done to improve the flags' reliability by reducing the probability of metastable events on their outputs when CLKA and CLKB operate asynchronously to one another. $\overline{FF}$ and $\overline{AF}$ are synchronized to CLKA. $\overline{EF}$ and $\overline{AE}$ are synchronized to CLKB. Table 4 shows the relationship of each port flag to the level of FIFO fill.

EMPTY FLAG ($\overline{EF}$)

The FIFO Empty Flag is synchronized to the port clock that reads data from its array (CLKB). When the $\overline{EF}$ is HIGH, new data can be read to the FIFO output register. When the $\overline{EF}$ is LOW, the FIFO is empty and attempted FIFO reads

TABLE 2 – PORT A ENABLE FUNCTION TABLE

$\overline{CSA}$	W/$\overline{RA}$	ENA	MBA	CLKA	Data A (A0-A35) I/O	Port Function
H	X	X	X	X	Input	None
L	H	L	X	X	Input	None
L	H	H	L	↑	Input	FIFO write
L	H	H	H	↑	Input	Mail1 write
L	L	L	L	X	Output	None
L	L	H	L	↑	Output	None
L	L	L	H	X	Output	None
L	L	H	H	↑	Output	Mail2 read (set $\overline{MBF2}$ HIGH)

TABLE 3 – PORT B ENABLE FUNCTION TABLE

$\overline{CSB}$	W/$\overline{RB}$	ENB	SIZ1, SIZ0	CLKB	Data B (B0-B35) I/O	Port Function
H	X	X	X	X	Input	None
L	H	L	X	X	Input	None
L	H	H	One, both LOW	↑	Input	None
L	H	H	Both HIGH	↑	Input	Mail2 write
L	L	L	One, both LOW	X	Output	None
L	L	H	One, both LOW	↑	Output	FIFO read
L	L	L	Both HIGH	X	Output	None
L	L	H	Both HIGH	↑	Output	Mail1 read (set $\overline{MBF1}$ HIGH)

are ignored. When reading the FIFO with a byte or word size on port B, $\overline{EF}$ is set LOW when the fourth byte or second word of the last long word is read.

The FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls the $\overline{EF}$ monitors a write-pointer and read-pointer comparator that indicates when the FIFO memory status is empty, empty+1, or empty+2. A word written to the FIFO can be read to the FIFO output register in a minimum of three port B clock (CLKB) cycles. Therefore, an $\overline{EF}$ is LOW if a word in memory is the next data to be sent to the FIFO output register and two CLKB cycles have not elapsed since the time the word was written. The $\overline{EF}$ of the FIFO is set HIGH by the second LOW-to-HIGH transition of CLKB, and the new data word can be read to the FIFO output register in the following cycle.

A LOW-to-HIGH transition on CLKB begins the first synchronization cycle of a write if the clock transition occurs at time t_{SKEW1} or greater after the write. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 10).

FULL FLAG ($\overline{FF}$)

The FIFO Full Flag is synchronized to the port clock that writes data to its array (CLKA). When the $\overline{FF}$ is HIGH, a FIFO memory location is free to receive new data. No memory locations are free when the $\overline{FF}$ is LOW and attempted writes to the FIFO are ignored.

Each time a word is written to the FIFO, its write-pointer is incremented. The state machine that controls the $\overline{FF}$ monitors a write-pointer and read-pointer comparator that indicates when the FIFO memory status is full, full-1, or full-2. From the time a word is read from the FIFO, its previous memory location is ready to be written in a minimum of three CLKA cycles. Therefore, a $\overline{FF}$ is LOW if less than two CLKA cycles have elapsed since the next memory write location has been read. The second LOW-to-HIGH transition on the $\overline{FF}$ synchronizing clock after the read sets the $\overline{FF}$ HIGH and data can be written in the following clock cycle.

A LOW-to-HIGH transition on CLKA begins the first synchronization cycle of a read if the clock transition occurs at time t_{SKEW1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figure 11).

ALMOST-EMPTY FLAG ($\overline{AE}$)

The FIFO Almost-Empty flag is synchronized to the port clock that reads data from its array (CLKB). The state machine that controls the $\overline{AE}$ flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO memory status is almost-empty, almost-empty+1, or almost-empty+2. The almost-empty state is defined by the value of the Almost-Full and Almost-Empty Offset register (X). This register is loaded with one of four preset values during a device reset (see reset above). The $\overline{AE}$ flag is LOW when the FIFO contains X or less long words in memory and is HIGH when the FIFO contains (X+1) or more long words.

Two LOW-to-HIGH transitions on the port B Clock (CLKB) are required after a FIFO write for the $\overline{AE}$ flag to reflect the new level of fill. Therefore, the $\overline{AE}$ flag of a FIFO containing (X+1) or more long words remains LOW if two CLKB cycles have not elapsed since the write that filled the memory to the (X+1) level. The $\overline{AE}$ flag is set HIGH by the second CLKB LOW-to-HIGH transition after the FIFO write that fills memory to the (X+1) level. A LOW-to-HIGH transition of CLKB begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the write that fills the FIFO to (X+1) long words. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 12).

TABLE 4 – FIFO FLAG OPERATION

NUMBER OF 36-BIT WORDS IN THE FIFO[1]	SYNCHRONIZED TO CLKB		SYNCHRONIZED TO CLKA	
	$\overline{EF}$	$\overline{AE}$	$\overline{AF}$	$\overline{FF}$
0	L	L	H	H
1 to X	H	L	H	H
(X+ 1) to [64 - (X + 1)]	H	H	H	H
(64 - X) to 63	H	H	L	H
64	H	H	L	L

NOTE:
1. X is the value in the Almost-Empty flag and Almost-Full flag Offset register

ALMOST FULL FLAG ($\overline{AF}$)

The FIFO Almost-Full flag is synchronized to the port clock that writes data to its array (CLKA). The state machine that controls an $\overline{AF}$ flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO memory status is almost-full, almost-full-1, or almost-full-2. The almost-full state is defined by the value of the Almost-Full and Almost-Empty Offset register (X). This register is loaded with one of four preset values during a device reset (see Reset section). The $\overline{AF}$ flag is LOW when the FIFO contains (64-X) or more long words in memory and is HIGH when the FIFO contains [64-(X+1)] or less long words.

Two LOW-to-HIGH transitions on the port A Clock (CLKA) are required after a FIFO read for the $\overline{AF}$ flag to reflect the new level of fill. Therefore, the $\overline{AF}$ flag of a FIFO containing [64-(X+1)] or less words remains LOW if two CLKA cycles have not elapsed since the read that reduced the number of long words in memory to [64-(X+1)]. The $\overline{AF}$ flag is set HIGH by the second CLKA LOW-to-HIGH transition after the FIFO read that reduces the number of long words in memory to [64-(X+1)]. A LOW-to-HIGH transition on CLKA begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the read that reduces the number of long words in memory to [64-(X+1)]. Otherwise, the subsequent CLKA cycle can be the first synchronization cycle (see Figure 13).

MAILBOX REGISTERS

Two 36-bit bypass registers (mail1, mail2) are on the IDT72V3613 to pass command and control information between port A and port B without putting it in queue. A LOW-to-HIGH transition on CLKA writes A0-A35 data to the mail1 register when a port A write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA with MBA HIGH. A LOW-to-HIGH transition on CLKB writes B0-B35 data to the mail2 register when a port B write is selected by $\overline{CSB}$, W/$\overline{RB}$ and ENB, and both SIZ0 and SIZ1 are HIGH. Writing data to a mail register sets its corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) LOW. Attempted writes to a mail register are ignored while its mail flag is LOW.

When the port B data (B0-B35) outputs are active, the data on the bus comes from the FIFO output register when either one or both SIZ1 and SIZ0 are LOW and from the mail1 register when both SIZ1 and SIZ0 are HIGH. The Mail1 Register Flag ($\overline{MBF1}$) is set HIGH by a rising CLKB edge when a port B read is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB, and both SIZ1 and SIZ0 HIGH. The Mail2 Register Flag ($\overline{MBF2}$) is set HIGH by a rising CLKA edge when a port A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA with MBA HIGH. The data in a mail register remains intact after it is read and changes only when new data is written to the register. See Figure 14 and 15 for relevant mail register and mail register flag timing diagrams.

DYNAMIC BUS SIZING

The port B bus can be configured in a 36-bit long word, 18-bit word, or 9-bit byte format for data read from the FIFO. Word- and byte-size bus selections can utilize the most significant bytes of the bus (Big-Endian) or least significant bytes of the bus (Little-Endian). Port B bus-size can be changed dynamically and synchronous to CLKB to communicate with peripherals of various bus widths.

The levels applied to the port B bus-size select (SIZ0, SIZ1) inputs and the Big-Endian select ($\overline{BE}$) input are stored on each CLKB LOW-to-HIGH transition. The stored port B bus-size selection is implemented by the next rising edge on CLKB according to Figure 2.

Only 36-bit long-word data is written to or read from the FIFO memory on the IDT72V3613. Bus-matching operations are done after data is read from the FIFO RAM. Port B bus sizing does not apply to mail register operations.

BUS-MATCHING FIFO READS

Data is read from the FIFO RAM in 36-bit long-word increments. If a long-word bus-size is implemented, the entire long word immediately shifts to the FIFO output register upon a read. If byte or word size is implemented on port B, only the first one or two bytes appear on the selected portion of the FIFO output register, with the rest of the long word stored in auxiliary registers. In this case, subsequent FIFO reads with the same bus-size implementation output the rest of the long word to the FIFO output register in the order shown by Figure 2.

Each FIFO read with a new bus-size implementation automatically unloads data from the FIFO RAM to its output register and auxiliary registers. Therefore, implementing a new port B bus-size and performing a FIFO read before all bytes or words stored in the auxiliary registers have been read results in a loss of the unread data in these registers.

When reading data from FIFO in byte or word format, the unused B0-B35 outputs are indeterminate.

BYTE SWAPPING

The byte-order arrangement of data read from the FIFO can be changed synchronous to the rising edge of CLKB. Byte-order swapping is not available for mail register data. Four modes of byte-order swapping (including no swap) can be done with any data port size selection. The order of the bytes are rearranged within the long word, but the bit order within the bytes remains constant.

Byte arrangement is chosen by the port B Swap select (SW0, SW1) inputs on a CLKB rising edge that reads a new long word from the FIFO. The byte order chosen on the first byte or first word of a new long word read from the FIFO is maintained until the entire long word is transferred, regardless of the SW0 and SW1 states during subsequent reads. Figure 4 is an example of the byte-order swapping available for long word reads. Performing a byte swap and bus-size simultaneously for a FIFO read first rearranges the bytes as shown in Figure 4, then outputs the bytes as shown in Figure 2.

PORT-B MAIL REGISTER ACCESS

In addition to selecting port B bus sizes for FIFO reads, the port B bus Size select (SIZ0, SIZ1) inputs also access the mail registers. When both SIZ0 and SIZ1 are HIGH, the mail1 register is accessed for a port B long-word read and the mail2 register is accessed for a port B long-word write. The mail register is accessed immediately and any bus-sizing operation that can be underway is unaffected by the mail register access. After the mail register access is complete, the previous FIFO access can resume in the next CLKB cycle. The logic diagram in Figure 3 shows the previous bus-size selection is preserved when the mail registers are accessed from port B. A port B bus-size is implemented on each rising CLKB edge according to the states of SIZ0_Q, SIZ1_Q, and $\overline{BE}$_Q.

PARITY CHECKING

The port A data inputs (A0-A35) and port B data inputs (B0-B35) each have four parity trees to check the parity of incoming (or outgoing) data. A parity failure on one or more bytes of the port A data bus is reported by a low level on the port A Parity Error Flag ($\overline{PEFA}$). A parity failure on one or more bytes of the port B data inputs that are valid for the bus-size implementation is reported by a low level on the port B Parity Error Flag ($\overline{PEFB}$). Odd or Even parity checking can be selected, and the Parity Error Flags can be ignored if this feature is not desired.

Parity status is checked on each input bus according to the level of the Odd/Even parity (ODD/$\overline{EVEN}$) select input. A parity error on one or more valid bytes of a port is reported by a LOW level on the corresponding port Parity Error Flag ($\overline{PEFA}$, $\overline{PEFB}$) output. Port A bytes are arranged as A0-A8, A9-A17, A18-A26, and A27-A35, and port B bytes are arranged as B0-B8, B9-B17, B18-B26, and B27-B35, and its valid bytes are those used in a port B bus size implementation. When Odd/Even parity is selected, a port Parity Error Flag ($\overline{PEFA}$, $\overline{PEFB}$) is LOW if any byte on the port has an odd/even number of LOW levels applied to its bits.

The four parity trees used to check the A0-A35 inputs are shared by the mail2 register when parity generation is selected for port-A reads (PGA = HIGH). When a port A read from the mail2 register with parity generation is selected with $\overline{CSA}$ LOW, ENA HIGH, W/$\overline{R}$A LOW, MBA HIGH, and PGA HIGH, the port A Parity Error Flag ($\overline{PEFA}$) is held HIGH regardless of the levels applied to the A0-A35 inputs. Likewise, the parity trees used to check the B0-B35 inputs are shared by the mail1 register when parity generation is selected for port B reads (PGB = HIGH). When a port B read from the mail1 register with parity generation is selected with $\overline{CSB}$ LOW, ENB HIGH, W/$\overline{R}$B LOW, both SIZ0 and SIZ1 HIGH, and PGB HIGH, the port B Parity Error Flag ($\overline{PEFB}$) is held HIGH regardless of the levels applied to the B0-B35 inputs.

PARITY GENERATION

A HIGH level on the port A Parity Generate select (PGA) or port B Parity Generate select (PGB) enables the IDT72V3613 to generate parity bits for port reads from a FIFO or mailbox register. Port A bytes are arranged as A0-A8, A9-A17, A18-A26, and A27-A35, with the most significant bit of each byte used as the parity bit. Port B bytes are arranged as B0-B8, B9-B17, B18-B26, and B27-B35, with the most significant bit of each byte used as the parity bit. A write to a FIFO or mail register stores the levels applied to all nine inputs of a byte regardless of the state of the Parity Generate select (PGA, PGB) inputs. When data is read from a port with parity generation selected, the lower eight bits of each byte are used to generate a parity bit according to the level on the ODD/$\overline{EVEN}$ select. The generated parity bits are substituted for the levels originally written to the most significant bits of each byte as the word is read to the data outputs.

Parity bits for FIFO data are generated after the data is read from the FIFO memory and before the data is written to the output register. Therefore, the port A Parity Generate select (PGA) and Odd/Even parity select (ODD/$\overline{EVEN}$) have setup and hold time constraints to the port A Clock (CLKA) and the port B Parity Generate select (PGB) and ODD/$\overline{EVEN}$ select have setup and hold time constraints to the port B Clock (CLKB). These timing constraints only apply for a rising clock edge used to read a new long word to the FIFO output register (see Figure 16 and 17).

The circuit used to generate parity for the mail1 data is shared by the port B bus (B0-B35) to check parity and the circuit used to generate parity for the mail2 data is shared by the port A bus (A0-A35) to check parity. The shared parity trees of a port are used to generate parity bits for the data in a mail register when the port Chip Select ($\overline{CSA}$, $\overline{CSB}$) is LOW, Enable (ENA, ENB) is HIGH, and Write/Read select (W/$\overline{R}$A, W/$\overline{R}$B) input is LOW, the mail register is selected (MBA HIGH for port A; both SIZ0 and SIZ1 are HIGH for port B), and port Parity Generate select (PGA, PGB) is HIGH. Generating parity for mail register data does not change the contents of the register. Parity Generation timing, when reading from a mail register, can be found in Figure 18 and 19.

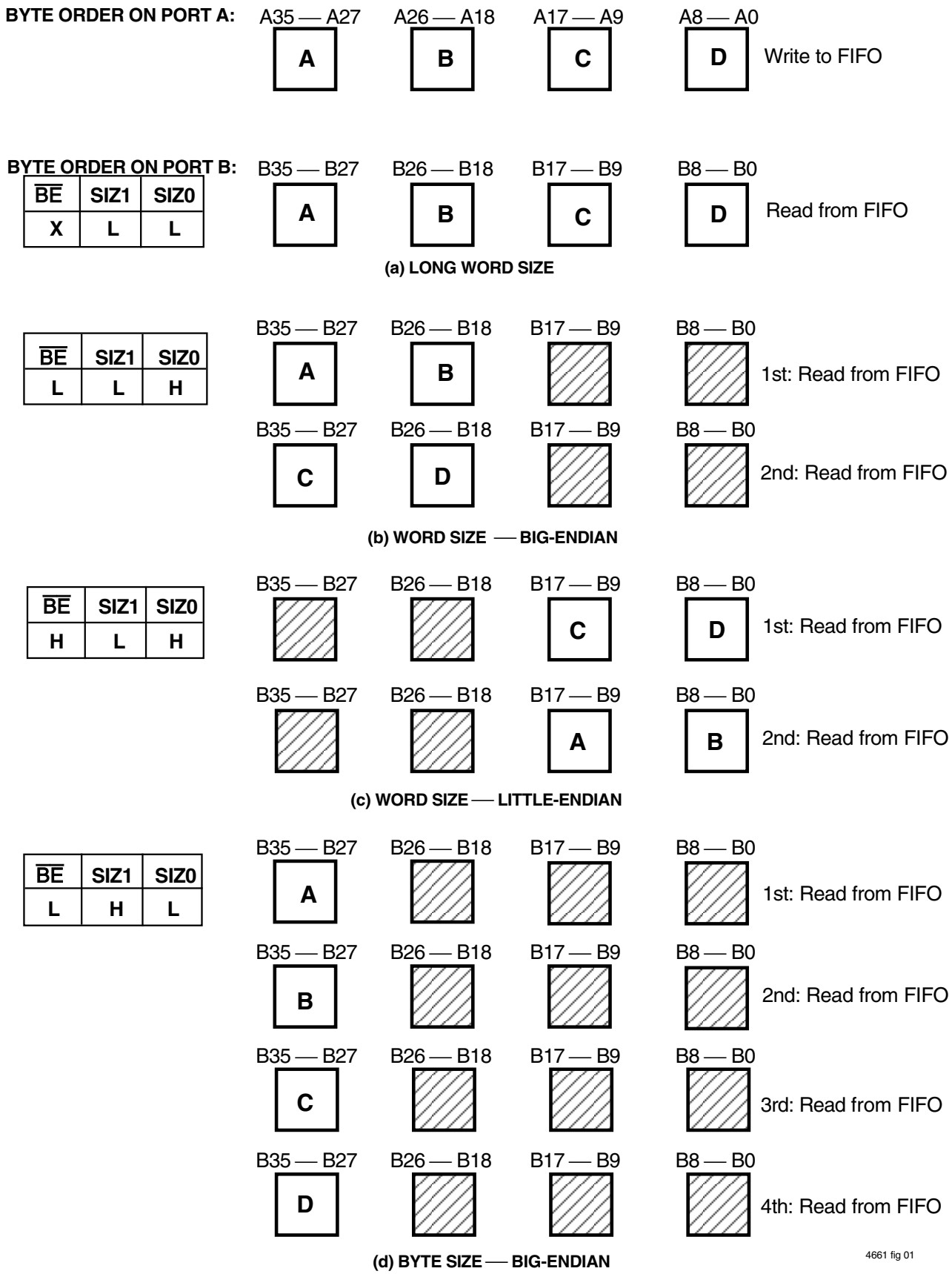
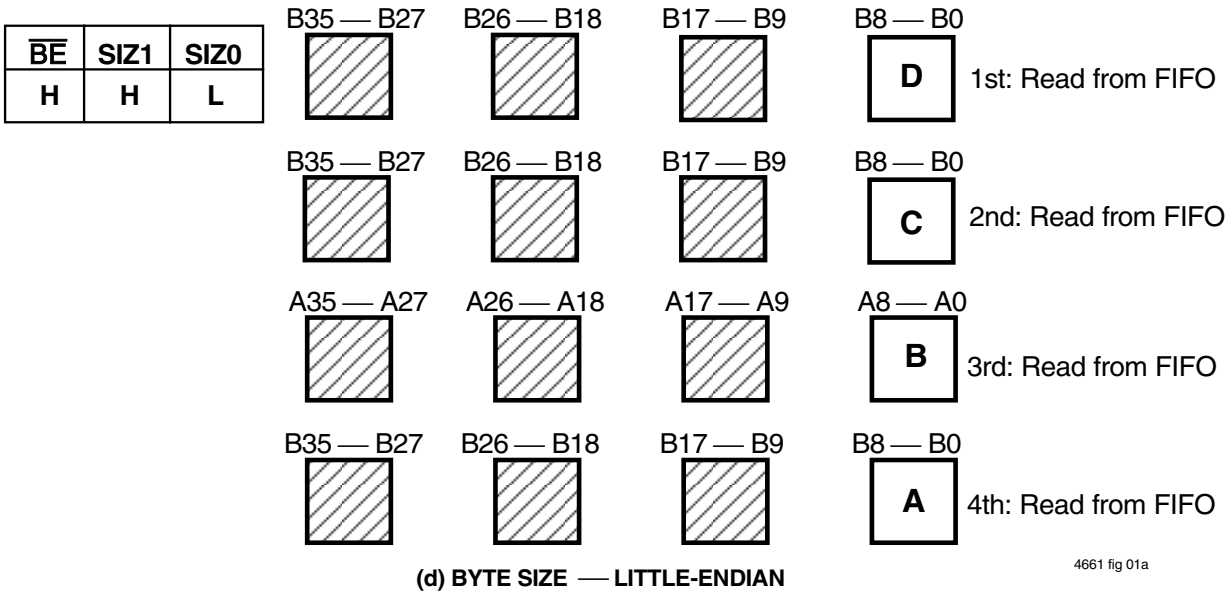


Figure 2. Dynamic Bus Sizing



(d) BYTE SIZE — LITTLE-ENDIAN

Figure 2. Dynamic Bus Sizing (Continued)

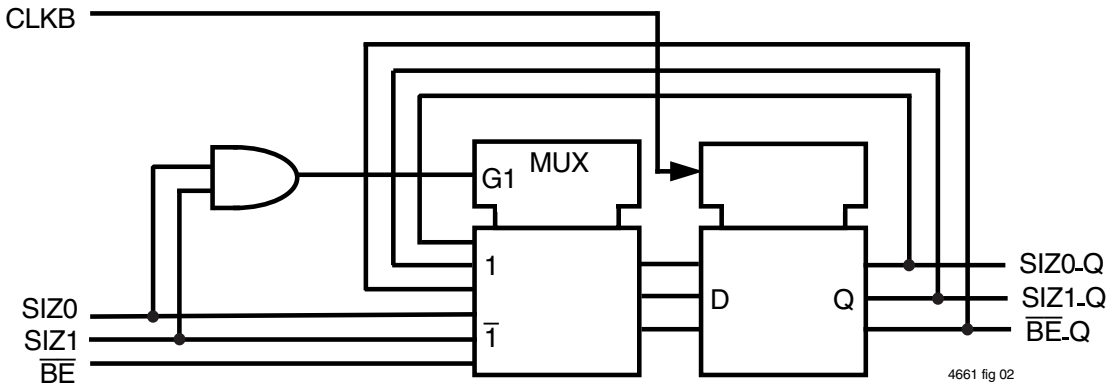


Figure 3. Logic Diagram for SIZ0, SIZ1, and BE Register

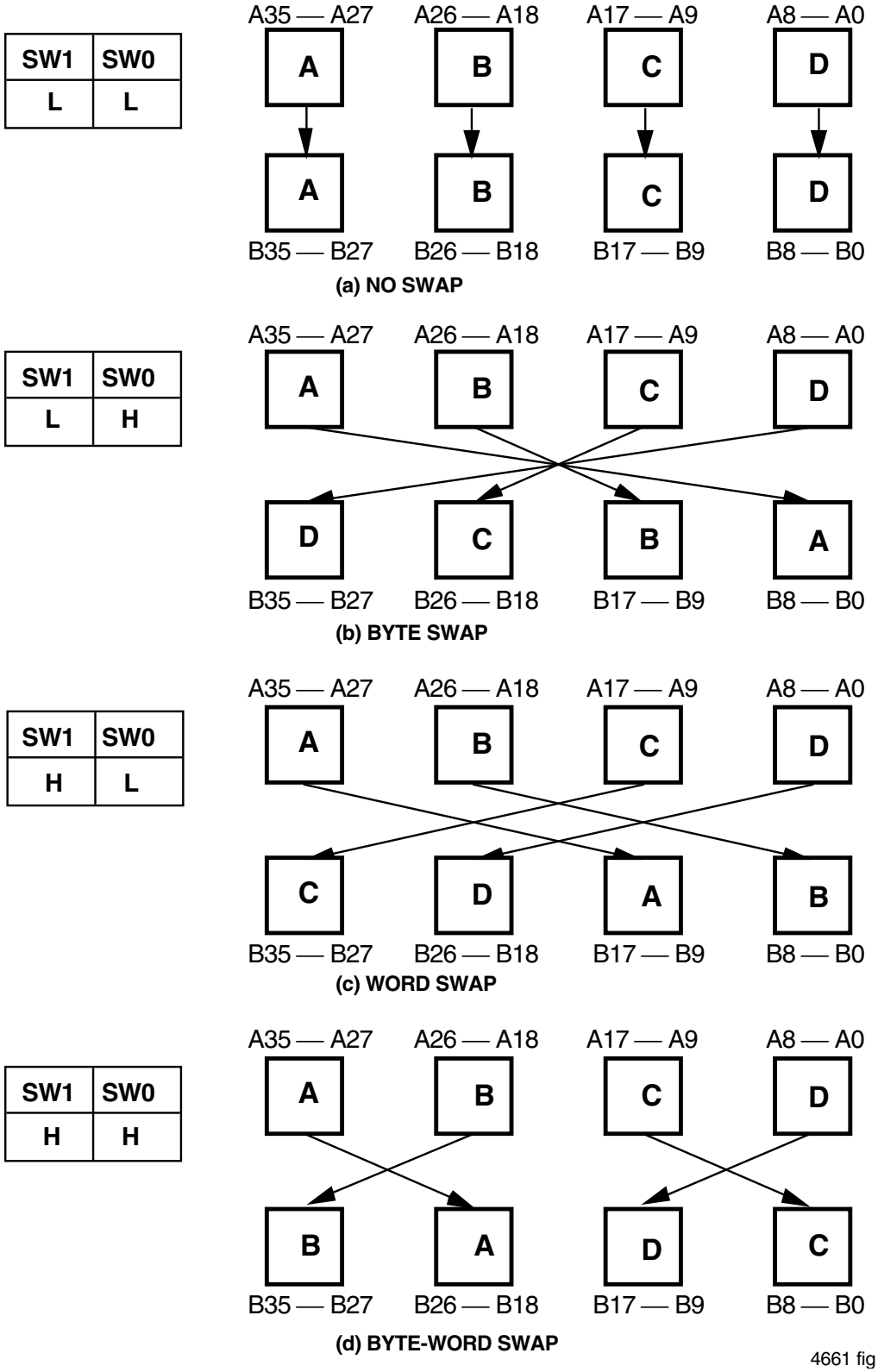


Figure 4. Byte Swapping for FIFO Reads (Long-Word Size Example)

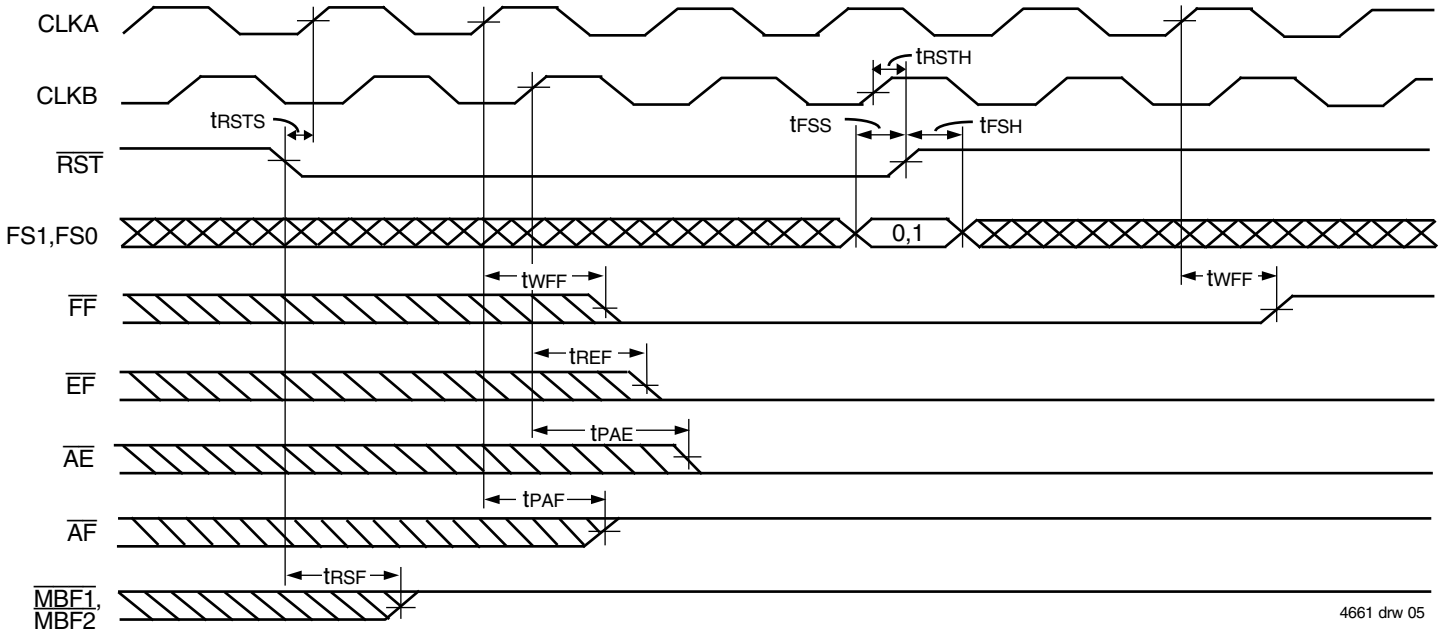
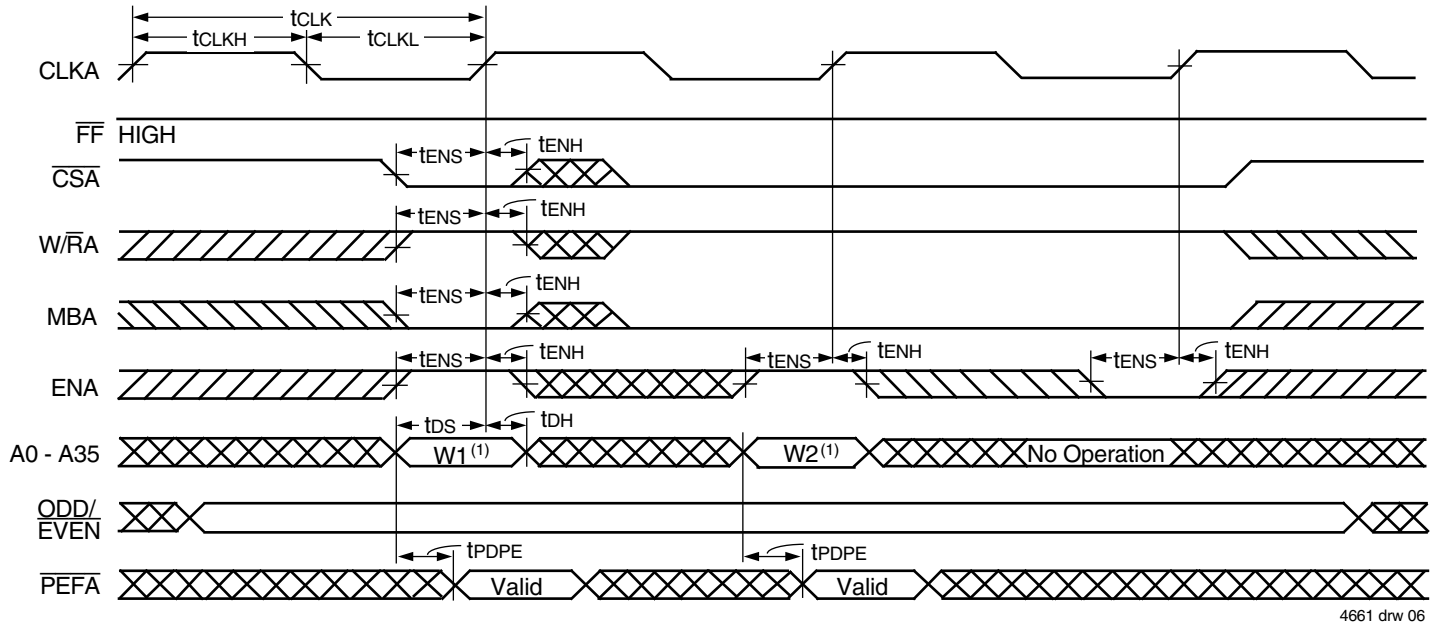
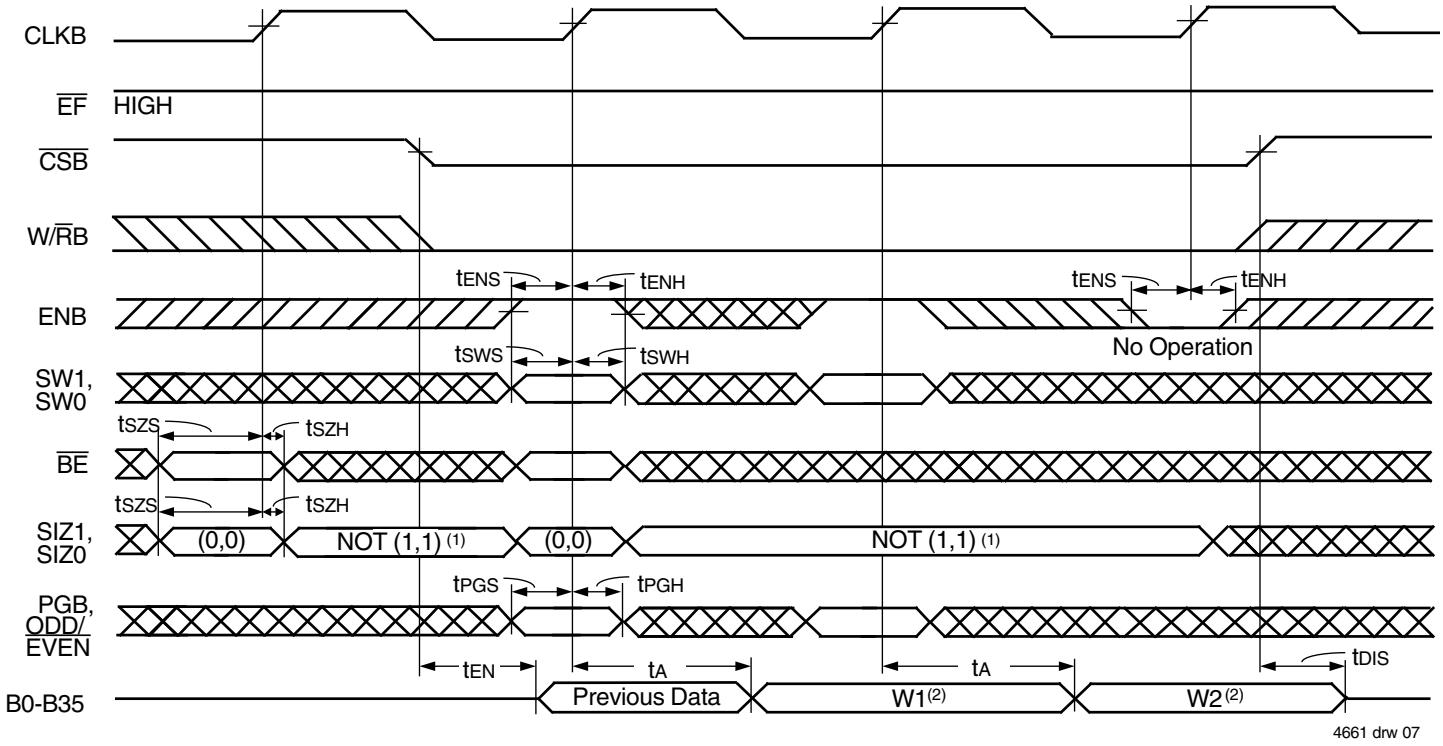


Figure 5. FIFO Reset and Loading the X Register with the Value of Eight



NOTE:
1. Written to the FIFO.

Figure 6. Port A Write Cycle Timing

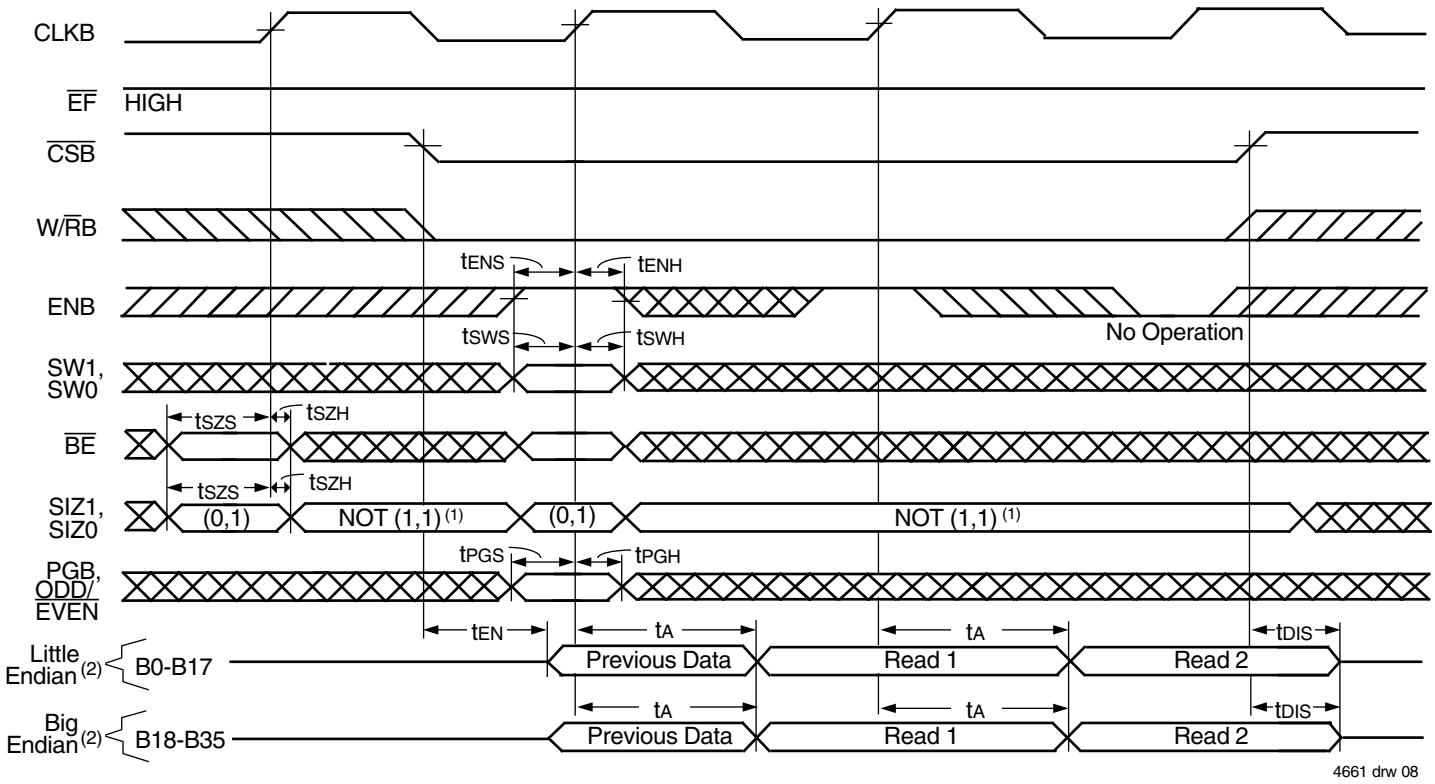


NOTES:
1. SIZ0 = HIGH and SIZ1 = HIGH selects the mail1 register for output on B0-B35.
2. Data read from FIFO1.

DATA SWAP TABLE FOR FIFO LONG-WORD READS

FIFO DATA WRITE				SWAP MODE		FIFO DATA READ			
A35-A27	A26-A18	A17-A9	A8-A0	SW1	SW0	B35-B27	B26-B18	B17-B9	B8-B0
A	B	C	D	L	L	A	B	C	D
A	B	C	D	L	H	D	C	B	A
A	B	C	D	H	L	C	D	A	B
A	B	C	D	H	H	B	A	D	C

Figure 7. Port B Long-Word Read Cycle Timing

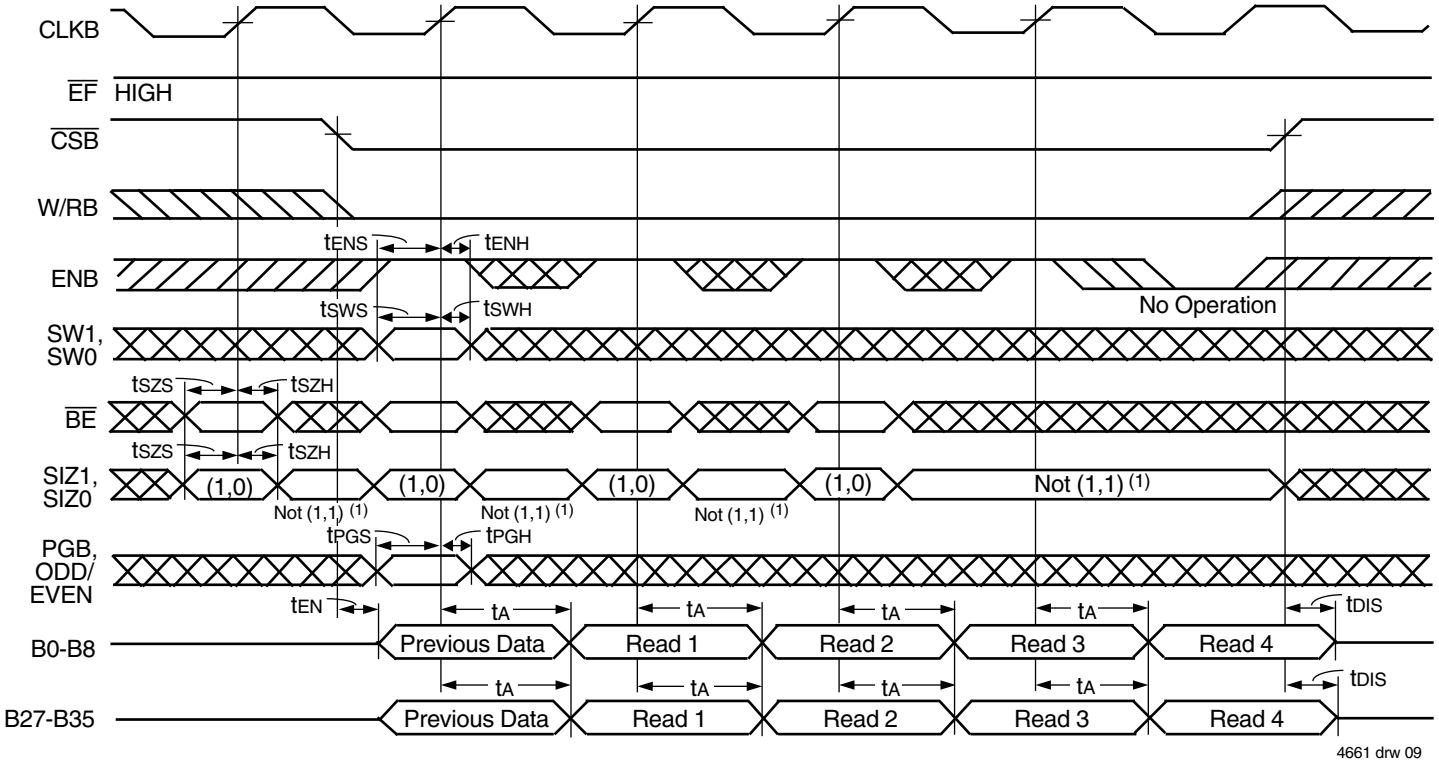


NOTES;
1. SIZ0 = HIGH and SIZ1 = HIGH selects the mail1 register for output on B0-B35.
2. Unused word B0-B17 or B18-B35 are indeterminate.

DATA SWAP TABLE FOR FIFO WORD READS

FIFO DATA WRITE				SWAP MODE		READ NO.	FIFO DATA READ			
							BIG-ENDIAN		LITTLE-ENDIAN	
A35-A27	A26-A18	A17-A9	A8-A0	SW1	SW0		B35-B27	B26-B18	B17-B9	B8-B0
A	B	C	D	L	L	1 2	A C	B D	C A	D B
A	B	C	D	L	H	1 2	D B	C A	B D	A C
A	B	C	D	H	L	1 2	C A	D B	A C	B D
A	B	C	D	H	H	1 2	B D	A C	D B	C A

Figure 8. Port B Word Read-Cycle Timing

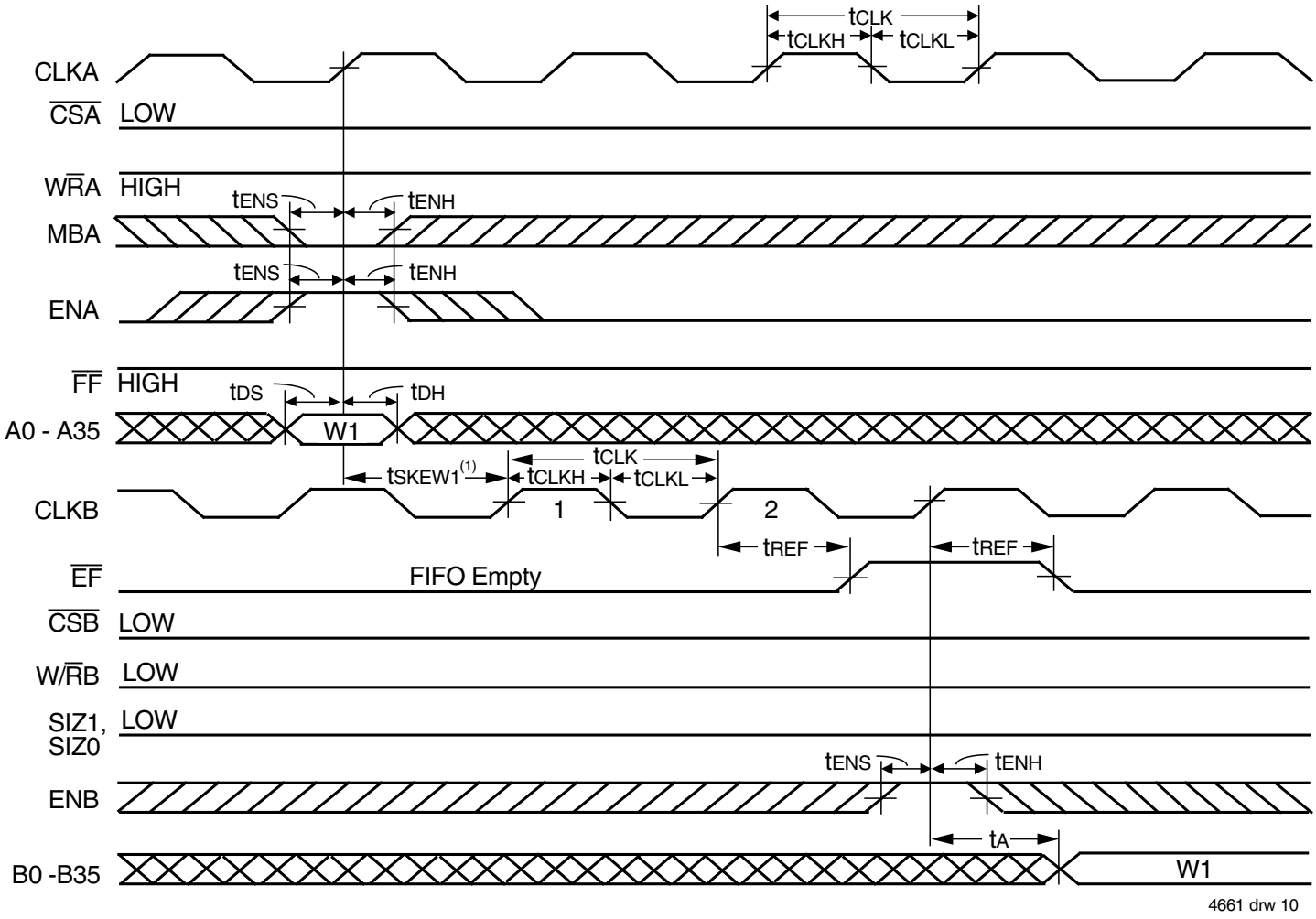


NOTES:
1. SIZ0 = HIGH and SIZ1 = HIGH selects the mail1 register for output on B0-B35.
2. Unused bytes B0-B26 or B9-B35 are indeterminate.

DATA SWAP TABLE FOR FIFO BYTE READS

FIFO DATA WRITE				SWAP MODE		READ NO.	FIFO DATA READ	
							BIG-ENDIAN	LITTLE-ENDIAN
A35-A27	A26-A18	A17-A9	A8-A0	SW1	SW0		B35-B27	B8-B0
A	B	C	D	L	L	1 2 3 4	A B C D	D C B A
A	B	C	D	L	H	1 2 3 4	D C B A	A B C D
A	B	C	D	H	L	1 2 3 4	C D A B	B A D C
A	B	C	D	H	H	1 2 3 4	B A D C	C D A B

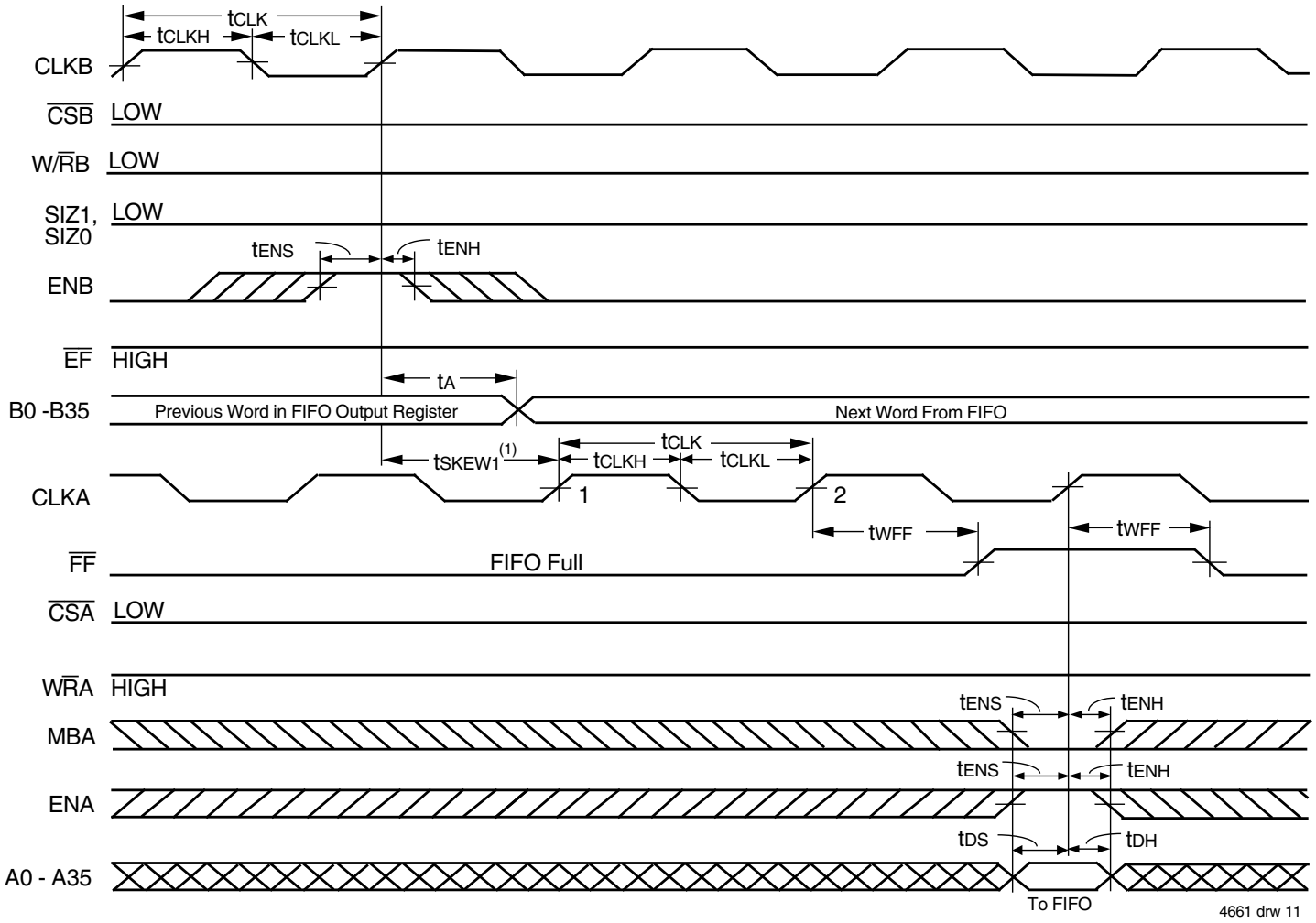
Figure 9. Port B Byte Read-Cycle Timing



NOTES:

1. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EF}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of $\overline{EF}$ HIGH may occur one CLKB cycle later than shown.
2. Port B size of long word is selected for the FIFO read by SIZ1 = LOW, SIZ0 = LOW. If port-B size is word or byte, $\overline{EF}$ is set LOW by the last word or byte read from the FIFO, respectively.

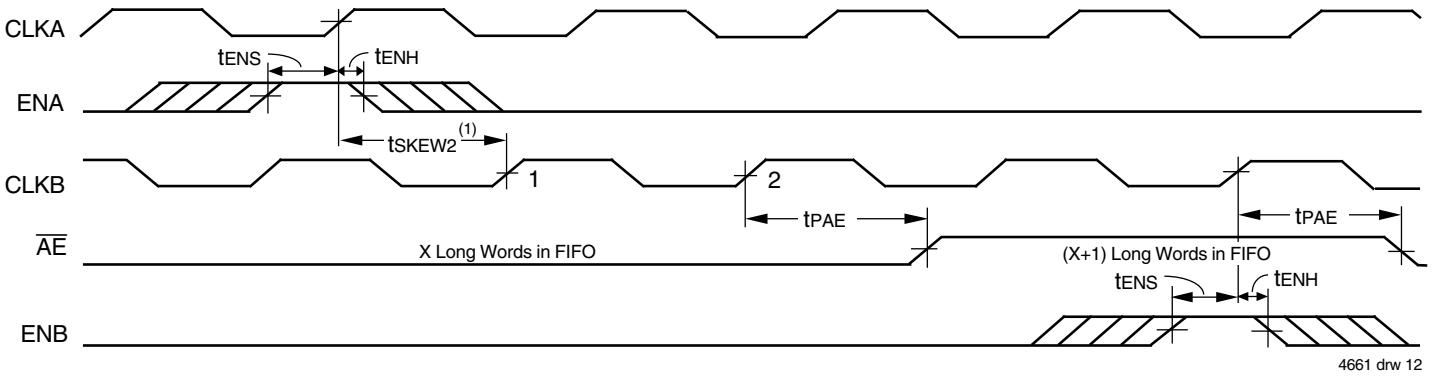
Figure 10. $\overline{EF}$ Flag Timing and First Data Read when the FIFO is Empty



NOTES:

1. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{EF}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then the transition of $\overline{EF}$ HIGH may occur one CLKA cycle later than shown.
2. Port B size of long word is selected for the FIFO read by SIZ1 = LOW, SIZ0 = LOW. If port B size is word or byte, t_{SKEW1} is referenced from the rising CLKB edge that reads the last word or byte of the long word, respectively.

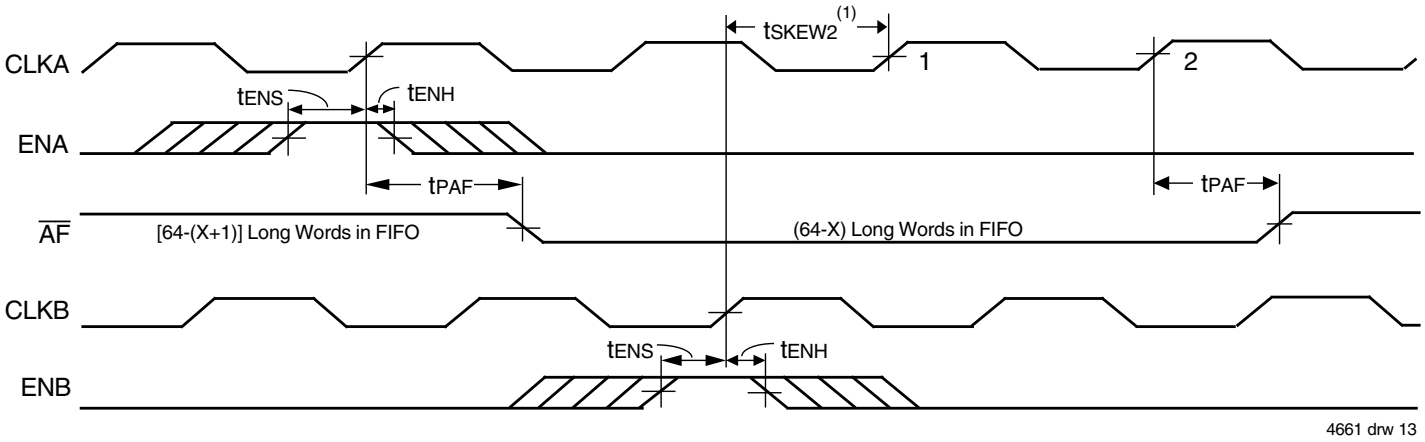
Figure 11. $\overline{FF}$ Flag Timing and First Available Write when the FIFO is Full



NOTES:

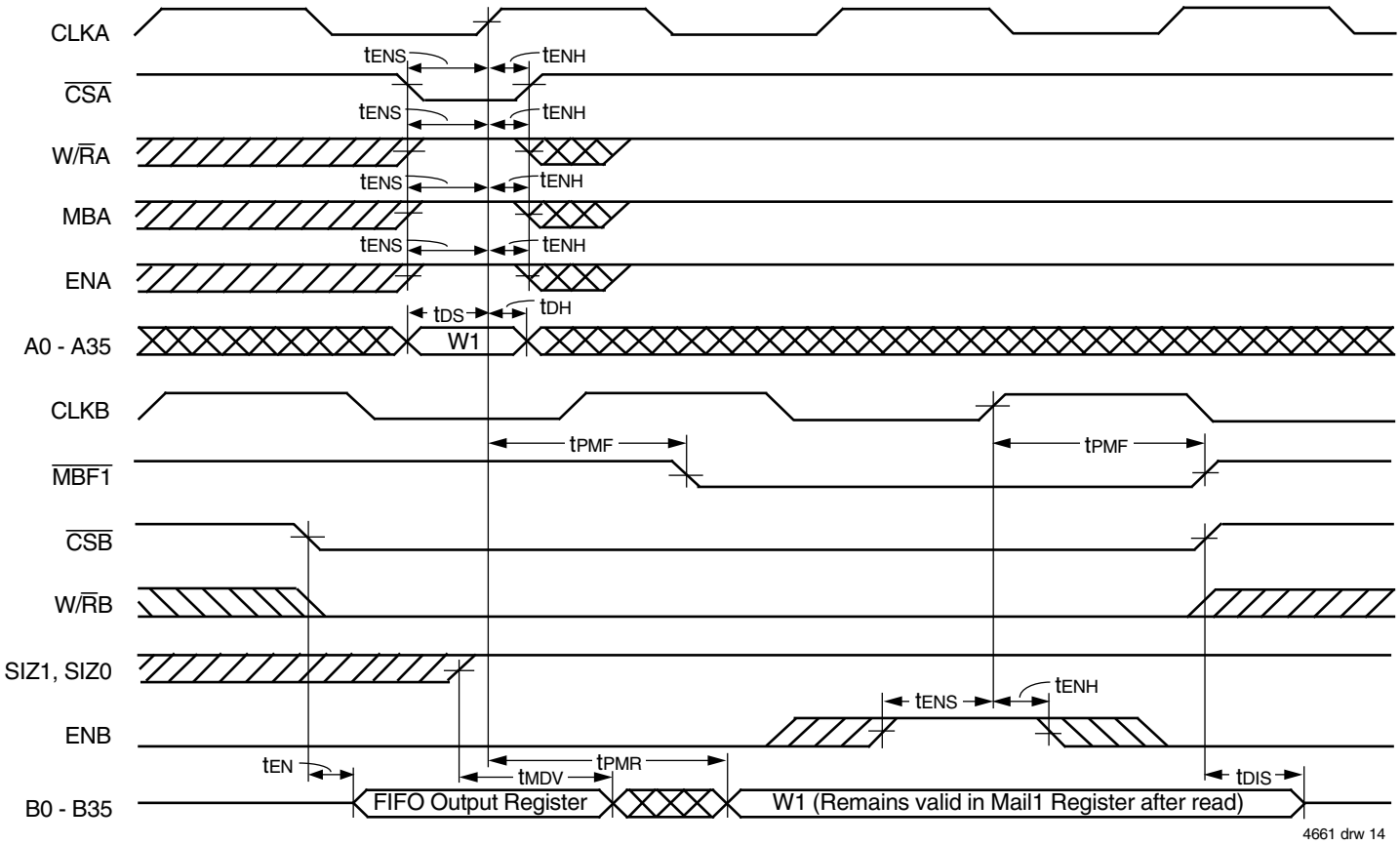
1. t_{SKEW2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AE}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW2}, then $\overline{AE}$ may transition HIGH one CLKB cycle later than shown.
2. FIFO write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW), FIFO read ($\overline{CSB}$ = LOW, W/$\overline{RB}$ = LOW, either SIZ0 = LOW or SIZ1 = LOW).
3. Port B size of long word is selected for the FIFO read by SIZ1 = LOW, SIZ0 = LOW. If port B size is word or byte, t_{SKEW2} is referenced to the last word or byte of the long word, respectively.

Figure 12. Timing for $\overline{AE}$ when the FIFO is Almost-Empty



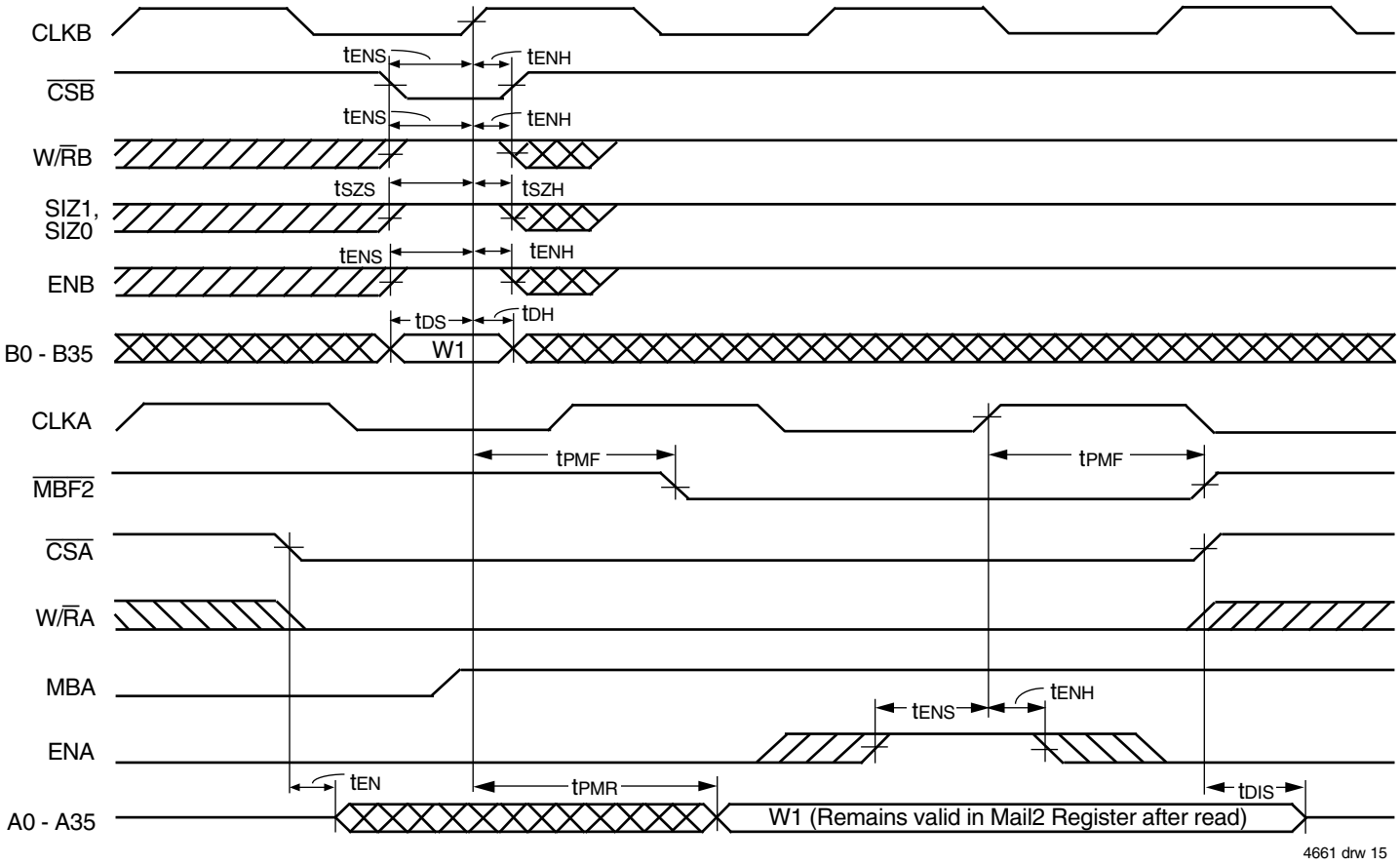
NOTES:
1. t_{SKEW2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AF}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW2}, then $\overline{AF}$ may transition HIGH one CLKA cycle later than shown.
2. FIFO write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW), FIFO read ($\overline{CSB}$ = LOW, W/$\overline{RB}$ = LOW, either SIZ0 = LOW or SIZ1 = LOW).
3. Port-B size of long word is selected for FIFO read by SIZ1 = LOW, SIZ0 = LOW. If port B size is word or byte, t_{SKEW2} is referenced from the last word or byte read of the long word, respectively.

Figure 13. Timing for $\overline{AF}$ when the FIFO is Almost-Full



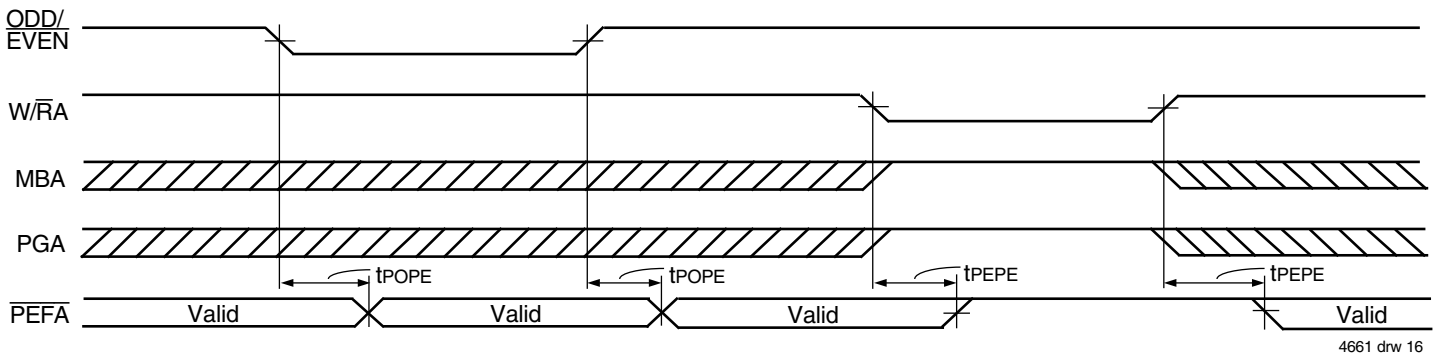
NOTE:
1. Port-B parity generation off (PGB = LOW).

Figure 14. Timing for Mail1 Register and $\overline{MBF1}$ Flag



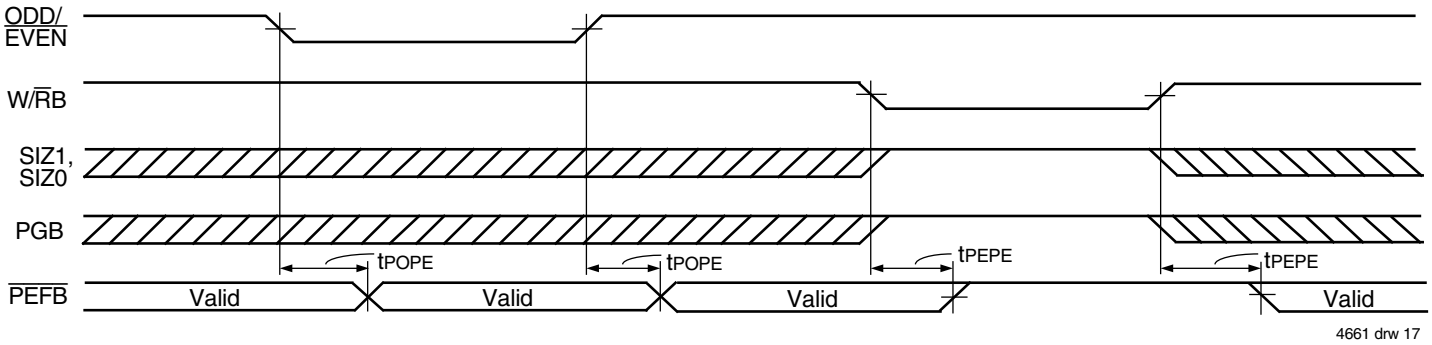
NOTE:
1. Port-A parity generation off (PGA = LOW).

Figure 15. Timing for Mail2 Register and $\overline{\text{MBF2}}$ Flag



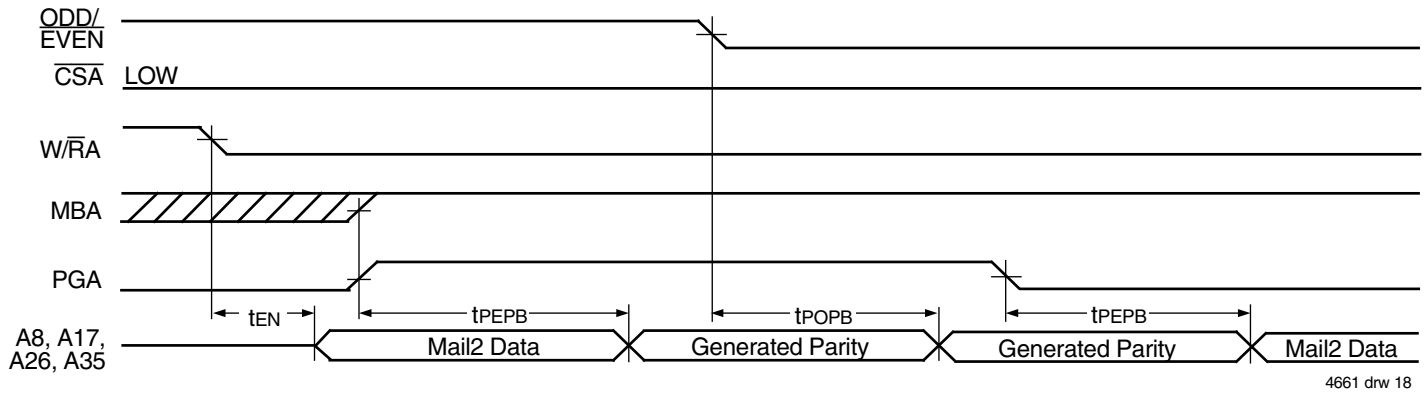
NOTE:
1. $\overline{\text{CSA}}$ = LOW and ENA = HIGH.

Figure 16. ODD/$\overline{\text{EVEN}}$, W/$\overline{\text{RA}}$, MBA, and PGA to $\overline{\text{PEFA}}$ Timing



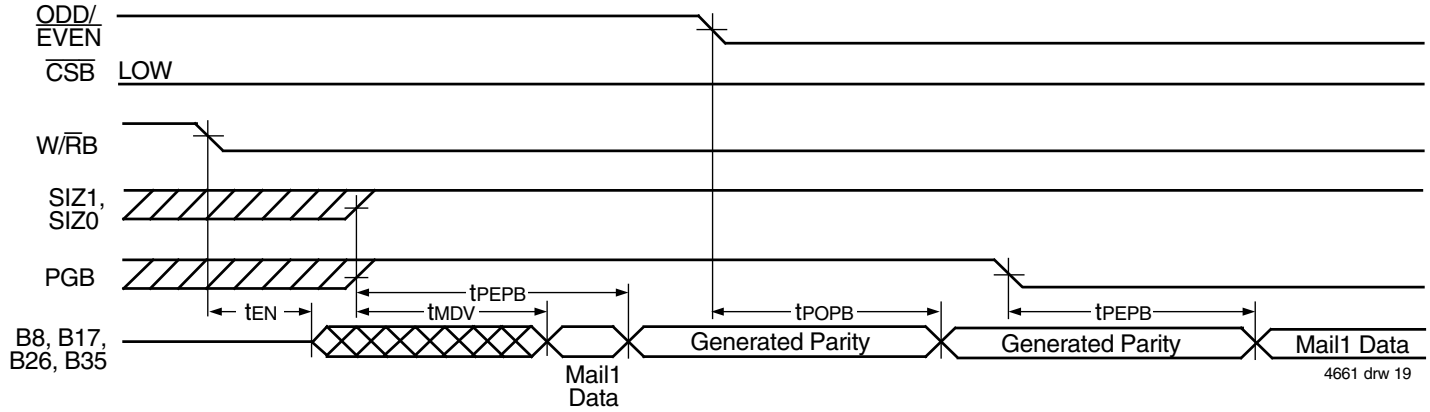
NOTE:
1. $\overline{CSB}$ = LOW and ENB = HIGH.

Figure 17. ODD/$\overline{EVEN}$, W/$\overline{R}$B, SIZ1, SIZ0, and PGB to $\overline{PEFB}$ Timing



NOTE:
1. ENA = HIGH.

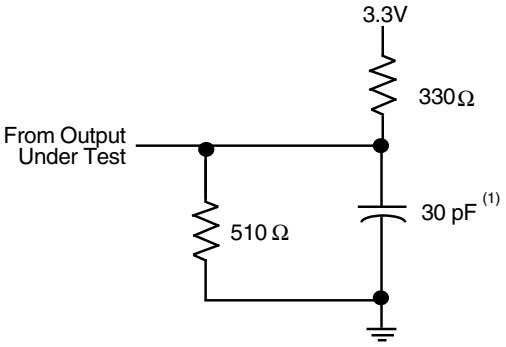
Figure 18. Parity Generation Timing when Reading from the Mail2 Register



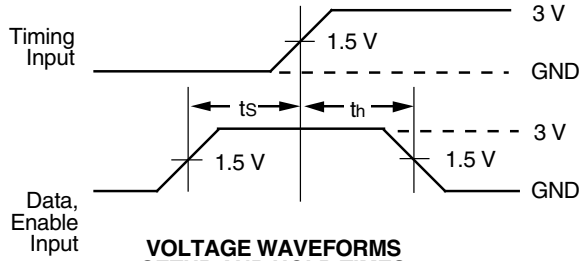
NOTE:
1. ENB = HIGH.

Figure 19. Parity Generation Timing when Reading from the Mail1 Register

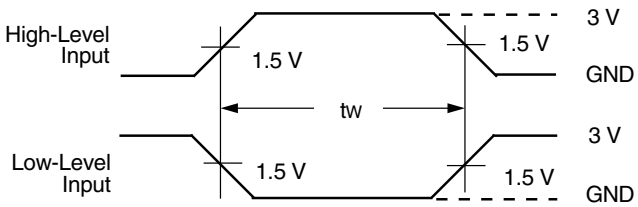
PARAMETER MEASUREMENT INFORMATION



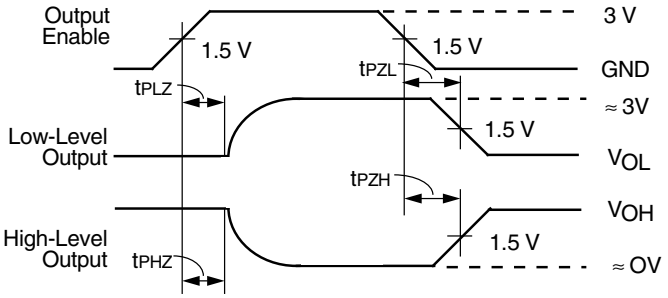
**PROPAGATION DELAY
LOAD CIRCUIT**



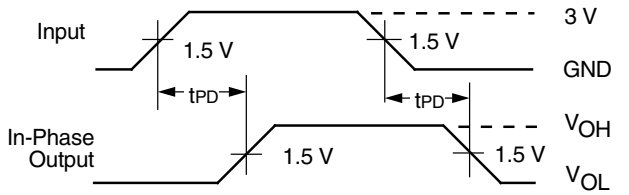
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATIONS**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**



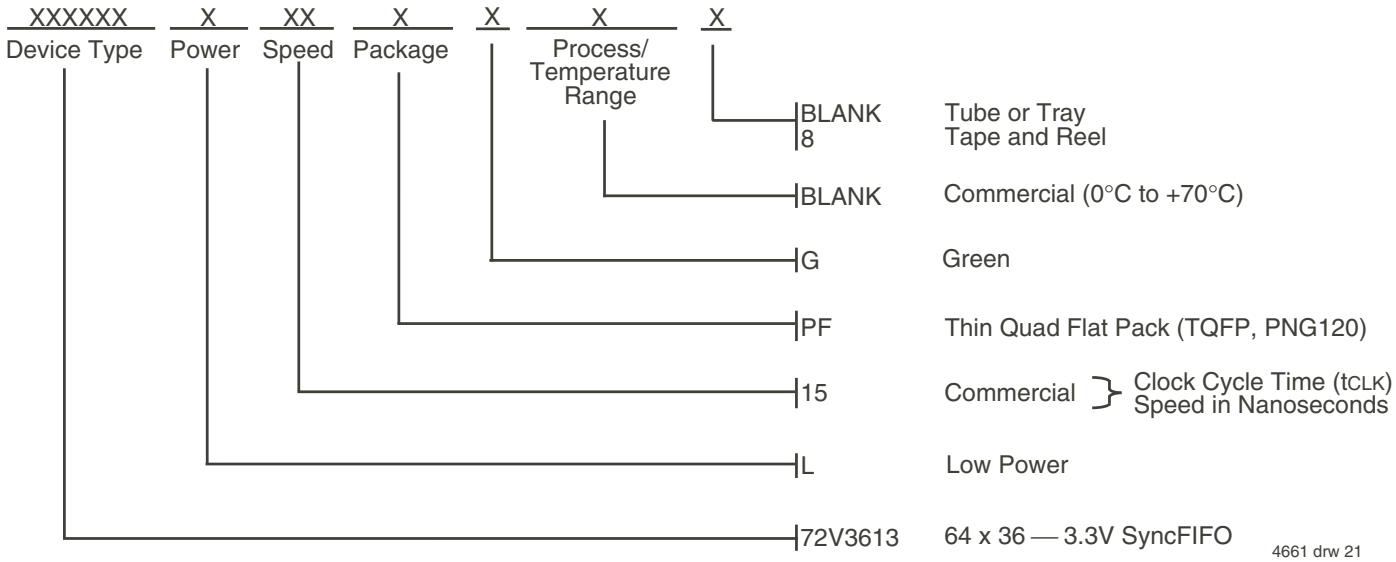
**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

4661 drw 20

NOTE:
1. Includes probe and jig capacitance.

Figure 20. Load Circuit and Voltage Waveforms

ORDERING INFORMATION



DATASHEET DOCUMENT HISTORY

07/10/2000	pg. 1.
05/27/2003	pg. 6.
06/09/2005	pgs. 1, 2, 3 and 26.
02/12/2009	pg. 26.
11/11/2013	pgs. 1, 2, 5, 7, 8, 20, 21 and 25.
01/09/2014	pg. 2.
07/23/2019	Datasheet changed to Obsolete Status.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use o any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.