EVBUM2283/D

KLI-4104 Image Sensor Evaluation Timing Specification

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EVAL BOARD USER'S MANUAL

Altera Code Version Description

The Altera code (Firmware version 2.5) described in this document is intended for use in the AD984X Timing Board. The code is written specifically for use with the following system configuration:

Table 1. SYSTEM CONFIGURATION

Evaluation Board Kit	PN 4H0349
Timing Generator Board	3E8180 (AD9845A 12-bit 30 MHz)
KLI−4104 Imager Board	3E8218
Framegrabber Board	National Instruments Model PCI−1424

ALTERA CODE FEATURES/FUNCTIONS

The Altera Programmable Logic Device (PLD) has four major functions:

Timing Generator

The PLD serves as a state machine based timing generator whose outputs interface to the KLI−4104, the AD9845A Analog Front End (AFE), and the PCI−1424 Framegrabber. When powered on, the video outputs are always in free-running mode.

The behavior of these output signals is dependent upon the current state of the state machine. External digital inputs, as well as jumpers on the board can be used to set the conditions of certain state transitions (See Table 2). In this manner, the board may be run using any of the following features:

- Optical Black Clamp Mode
- Programmable Electronic Exposure Control
- Programmable Multi-line Integration

Delay Line Initialization

Upon power-up, or when the BOARD_RESET button is depressed, the PLD programs the 10 silicon delay IC's on the Timing Generator Board to their default delay settings via a 3-wire serial interface. See Table 11 for details.

AFE Register Initialization

Upon power up, or when the BOARD_RESET button is depressed, the PLD programs the registers of the two AFE chips on the Timing Generator Board to their default settings via a 3 wire serial interface. See Table 12 for details.

Programmable Register Initialization

Upon power up, or when the BOARD_RESET button is depressed, the PLD initializes the programmable registers within the Altera PLD to their default settings. See Table 13 for details.

ALTERA CODE I/O

Inputs

Table 2. ALTERA INPUTS

Symbol	Description
POWER_ON_DELAY	The Rising Edge of This Signal Clears and Re-initializes the PLD
SYSTEM_CLK	60 MHz Clock, 2X the Pixel Clock Rate
INTEGRATE_CLK	Integration Clock – 1 ms Asynchronous Clock used for Power-up Delay.
JMP0	(Not Used for KLI−4104 Operation)
JMP1	Optical Black Mode Select (CLPOB)
	HIGH = Disable (CLPOB)
	LOW = Enable (CLPOB)
JMP2	(Not Used for KLI−4104 Operation)
JMP3	(Not Used for KLI−4104 Operation)
DIO[2..0]	Address Control Lines
DIO[10..3]	Data Control Lines
DIO11	Write Strobe – Rising Edge Latches New Data
DIO[13..12]	(Not Used for KLI−4104 Operation)
DIO[19..14]	(Not Used for KLI−4104 Operation)

Outputs

Table 3. ALTERA OUTPUTS

Symbol	Description
TG1_CLK	KLI−4104 CCD TG1 Clock
TG2_CLK	KLI−4104 CCD TG2C Clock
H1_CLK	KLI−4104 CCD H1A Clock
H2_CLK	KLI−4104 CCD H2A Clock
R_CLK	KLI−4104 CCD Reset Clock
VID_TEST	(Not Used for KLI−4104 Operation)
LOG_GREEN	LOG Green Clock
LOG_BLUE	LOG Blue Clock
LOG_RED	LOG Red Clock
LOG_LUMA	LOG Luma Clock
SHP	AD9845A Clamp CCD Reset Level
SHD	AD9845A Sample CCD Data Level
DATACLK	AD9845A A/D Convert Clock
PBLK	AD9845A Pixel Blanking
CLPOB	AD9845A Black Level Clamp
CLPDM	AD9845A DC Restore Input Clamp
VD	(Not Used for KLI−4104 Operation)
HD	(Not Used for KLI−4104 Operation)
PIX	PCI−1424 Frame Grabber Pixel Rate Synchronization
FRAME	PCI−1424 Frame Grabber Frame Rate Synchronization
LINE	PCI−1424 Frame Grabber Line Rate Synchronization

Table 3. ALTERA OUTPUTS (continued)

Symbol	Description
CH1_SLOAD	Serial Load Enable, Ch1 AD9845A AFE
CH2_SLOAD	Serial Load Enable, Ch2 AD9845A AFE
SLOAD	Serial Load Enable, Delay Line IC's
SCLOCK	Serial Clock (AD9845A, Delay Line IC's)
SERIAL_ENA	Enable Serial Programming of AD9845A, Delay Line IC's
H2BR_CLK	KLI−4104 CCD TG2L Clock
INTEGRATE	(Not Used for KLI−4104 Operation)

KLI−4104 TIMING CONDITIONS

System Timing Conditions

Table 4. SYSTEM TIMING

Description	Symbol	Time	Notes
System Clock Period	Tsys	16.67 ns	60 MHz System Clock
Unit Integration Time	Uint	1 ms	
Power Stable Delay	Tpwr	30 ms	Typical
Default Serial Load Time	Tsload	112.5 μs	Typical
Integration Time	Tint		Operating Mode Dependent

CCD Timing Conditions

Table 5. CCD TIMING

Description	Symbol	Pixel Counts	Time (30 MHz)	Notes
H1, H1L, H2, RESET Period	Tpix	1	0.033 μs	30 MHz Clocking of H1, H2, RESET
TGCCD Delay	Ttgd	2	0.07 μs	#NAME?
TGCCD Transfer Time	Tpd	17	0.57 μs	#NAME?
TG1 Clear	ttg1	1	0.033 μs	#NAME?
HCCD Delay (TG2 Clear)	Thd/ ttg2	5	0.17 μs	#NAME?
Vertical Transfer Period	TGperiod	21	0.80 μs	TGperiod = Ttgd + Tpd +Thd = Thd_STOP
LOGx Pulse Time	Tdr	0	0.00 μs	Default; Programmable in 16-pixel Increments
Pix per Line Single Output	Tline	4300	143.32 μs	CCD Pixels plus Overclock
Lines per Frame	TF	32		
RESET Clock Pulse Width	Tr		5.0 ns	Tr is Set by Hardware on Imager Board
TG2L_MIDLINE_START		2068	68.93 μs	Beginning of TGL_MIDLINE State

AFE Timing Conditions

Table 6. AFE TIMING

Description	Symbol	Pixel Counts	Time (30 MHz)	Notes
SHP, SHD, DATACLK Period	Tpix	1	0.033 μs	30 MHz Clocking of SHP, SHD, DATACLK
SHP Pulse Width	Tshp		7.5 ns	Tshp is Set by Hardware on Timing Board
SHD Pulse Width	Tshd		7.5 ns	Tshd is Set by Hardware on Timing Board
CLPOB Line Start	CLPOB_ls	4190		Line Transfer Counter, CLPOB Mode 1 Only
CLPOB Line End	CLPOB_le	4210		Line Transfer Counter, CLPOB Mode 1 Only
CLPDM Start Pixel	CLPDM_ps	4160		Horizontal Transfer Counter
CLPDM End Pixel	CLPDM_pe	4180		Horizontal Transfer Counter
PBLK Start Pixel	PBLK_ps	1		Vertical Transfer Counter
PBLK End Pixel	PBLK_pe	62		Vertical Transfer Counter

PCI−1424 Timing Conditions

Table 7. PCI−1424 TIMING

Description	Symbol	Pixel Counts	Time (30 MHz)	Notes
PIX Period	Tpix	1	0.033 μs	30 MHz Clocking of PIX Sync Signal
LINE Time	Tline	4324	144.10 μs	Single Line Integration Mode
FRAME Time	Tframe	139,112	4.64 ms	Tframe = TLine * TF + TGperiod * (TF − 1)

MODES OF OPERATION

The 3E8218 Imager Board has seven video output channels to accommodate the Red, Green, Blue, LAO, LAE, LBO, and LBE outputs of the KLI−4104. Any two of these outputs may be connected to the 3E8180 Timing Generator Board at one time, using the supplied coaxial cables.

Black Clamp Mode

One of the features of the AD9845A AFE chip is an optical black clamp. The black clamp (CLPOB) is asserted during the CCD's dark pixels and is used to remove residual offsets in the signal chain, and to track low frequency variations in the CCD's black level. This feature may be enabled or disabled by setting JMP1 (See Table 8).

Table 8. OUTPUT MODE JUMPER SETTINGS

JMP1	Operating Mode
LOW	CLPOB Mode Enabled
HIGH	CLPOB Mode Disabled

Programmable Operational Modes

Several operational modes are selected by programming registers in the Altera PLD, using the Discrete Input bits DIO[11..0]. DIO11 is the WRITE strobe to the registers; its rising edge latches data from DIO[10..3] to the register address in DIO[2..0]. The WRITE strobe timing requirements are summarized in Figure 1.

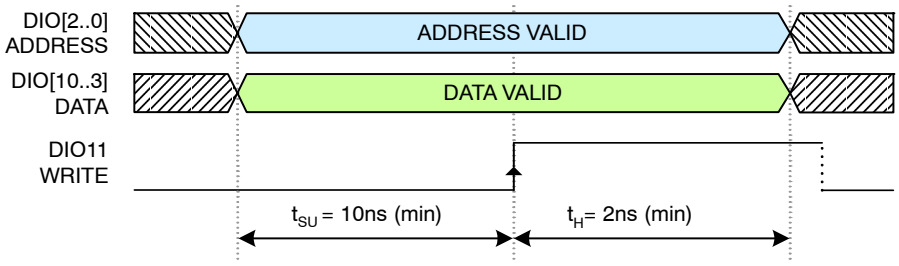

Figure 1. Programmable Register Timing

Exposure Control Mode

The LOGx inputs to the CCD allow independent exposure control of each Chroma channel. If a non-zero value is programmed into a LOGx_STOP register, the LOGx pulse will go HIGH on the falling edge of TG2C. In Multi-Line Integration Mode, the LOGx pulse will remain HIGH for 6 pixel periods before the Hclks begin, plus 16 pixel periods for each count in the register. The range of the 8-bit register data is 0 to 255, so the LOGx pulsewidth can be from 0 to 4086 pixel periods. See Figure 5, Table 9, and Table 13. If Multi-Line integration is off, the Horizontal clocks are suspended during the Luma mid-line transfer, and the LOGx pulse will therefore be lengthened by the same amount (TGperiod) if the LOGx register value is greater than 129. See Figure 6 and Table 10.

Multi-Line Integration Mode

The Multi-Line Integration mode is controlled by programming a value greater than 1 into the INT_LINES register. Each count in this register represents one line of integration time, with a minimum of 1 line time of integration. Values of 0 and 1 are equivalent, except that a value of 0 enables the Luma midline transfer, thereby increasing the total line length by TGperiod. The range of the 8-bit register is 0 to 255, so integration may be programmed up to 255 line times. See Figure 8, Figure 9 and Table 13.

Table 9. LOGX PULSEWIDTHS (SELECTED VALUES) – MULTI-LINE INTEGRATION MODE

LOGx_STOP Register Value	Puslewidth (Pixels)	Exposure (Percent)	LOGx_STOP Register Value	Puslewidth (Pixels)	Exposure (Percent)
0	0	100.00%	120	1926	55.30%
1	22	99.50%	128	2054	52.20%
2	38	99.10%	129	2070	51.90%
3	54	98.70%	130	2086	51.60%
4	70	98.40%	140	2246	47.90%
5	86	98.00%	150	2406	44.10%
10	166	96.10%	160	2566	40.40%
20	326	92.40%	170	2726	36.70%
30	486	88.70%	180	2886	33.00%
40	646	85.00%	190	3046	29.30%
50	806	81.30%	200	3206	25.60%
60	966	77.60%	210	3366	21.80%
70	1126	73.90%	220	3526	18.10%
80	1286	70.10%	230	3686	14.40%
90	1446	66.40%	240	3846	10.70%
100	1606	62.70%	250	4006	7.00%
110	1766	59.00%	255	4086	5.10%

Table 10. LOGX PULSEWIDTHS (SELECTED VALUES) – SINGLE LINE INTEGRATION MODE

LOGx_STOP Register Value	Puslewidth (Pixels)	Exposure (Percent)	LOGx_STOP Register Value	Puslewidth (Pixels)	Exposure (Percent)
0	0	100.00%	120	1926	55.30%
1	22	99.50%	128	2054	52.20%
2	38	99.10%	129	2070	51.90%
3	54	98.70%	130	2111	50.90%
4	70	98.40%	140	2271	47.20%
5	86	98.00%	150	2431	43.50%
10	166	96.10%	160	2591	39.70%
20	326	92.40%	170	2751	36.00%
30	486	88.70%	180	2911	32.30%
40	646	85.00%	190	3071	28.60%
50	806	81.30%	200	3231	24.90%
60	966	77.60%	210	3391	21.10%
70	1126	73.90%	220	3551	17.40%
80	1286	70.10%	230	3711	13.70%
90	1446	66.40%	240	3871	10.00%
100	1606	62.70%	250	4031	6.30%
110	1766	59.00%	255	4111	4.40%

PIXEL RATE CLOCKS GENERATION

The pixel rate clocks are derived from the System Clock. For 30 MHz operation, they operate at 1/2 the frequency of the 60 MHz System Clock. The PIXEL_CLK signal is generated from the rising edge of the system clock. The DELAYED_PIX_CLK signal is generated from the falling edge of the System Clock. By utilizing both edges of the System Clock, four start positions for the pixel rate clocks are achieved:

1. The PIXEL_CLK signal
2. The DELAYED_PIX_CLK signal occurs 25 percent later than the PIXEL_CLK signal
3. The inverse of the PIXEL_CLK signal occurs 50 percent later than the PIXEL_CLK signal
4. The inverse of the DELAYED_PIX_CLK signal occurs 75 percent later than the PIXEL_CLK signal

One of these four signals is chosen to be the input signal source for a particular pixel rate signal, and then the position of the signal is optimized using a programmable delay line IC.

For 30 MHz operation, the pixel rate clocks are derived as shown in Figure 2.

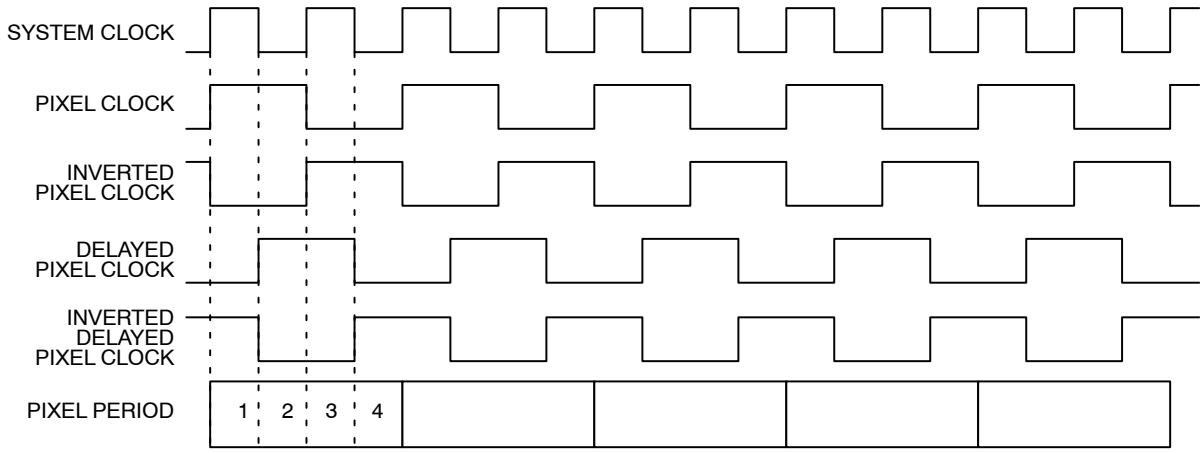

Figure 2. 30 MHz Pixel Clock Generation Timing

TIMING GENERATOR STATE MACHINE DESCRIPTION

The Timing Generator State Machine is Free-Running at all times. The sequence of states is shown in Figure 3.

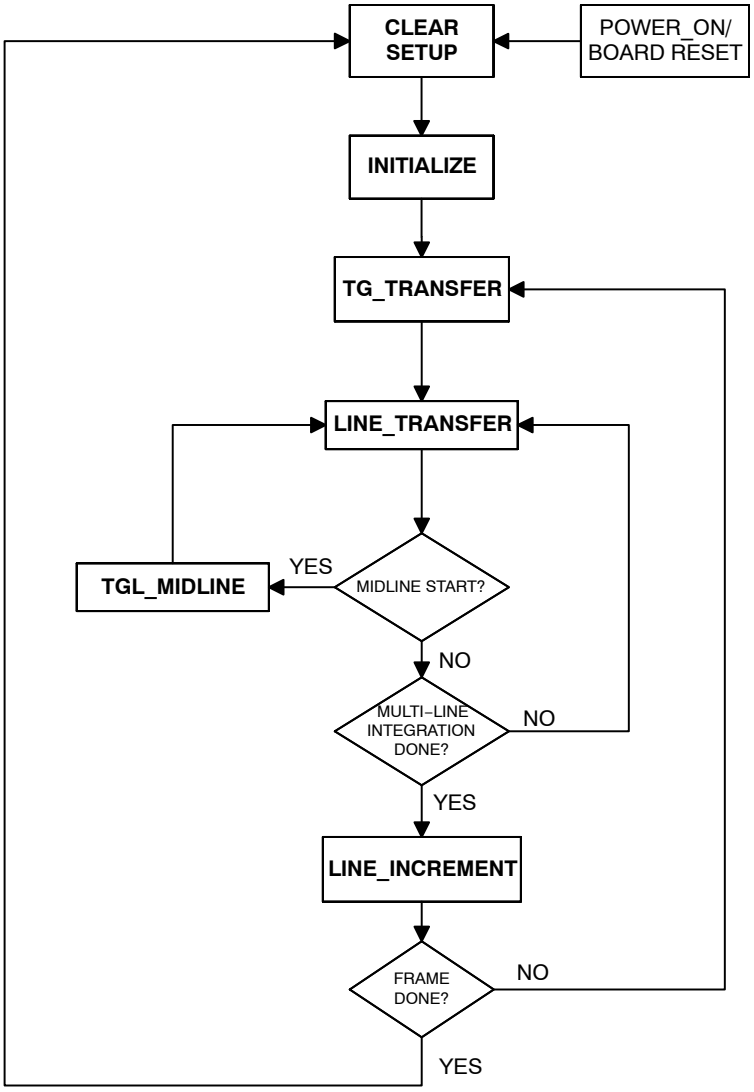

Figure 3. Timing Generator State Machine

Power-On/Board Reset State

When the board is powered up or the Board Reset button is pressed, the Altera PLD is internally reset. When this occurs, state machines in the PLD will first serially load the initial default values into the ten delay line IC's on the board, and then serially load the initial default values into the AFE registers. Upon completion of the serial load of the AFE, the board will be ready to proceed according to the output mode selected.

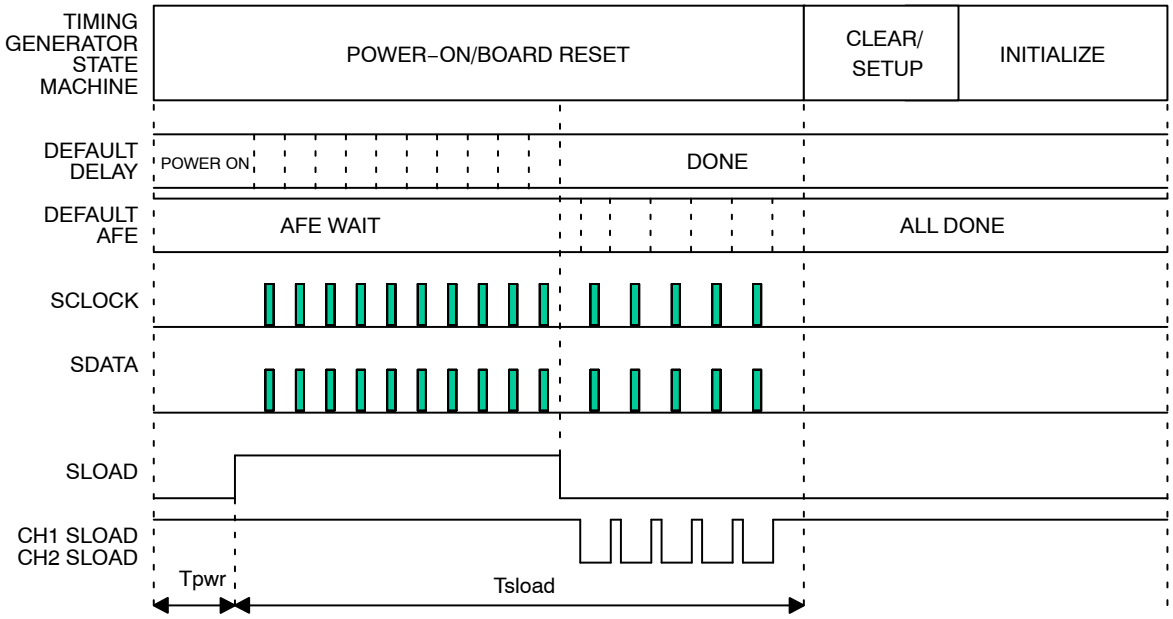

Figure 4. Power-On Initialization Timing

Delay Register Initialization

The DS1020 Programmable Silicon Delay Lines allow the Horizontal Clocks, Reset Clock, Clamp, Sample, and Data Clock signals to be adjusted within the sub-pixel timing. On Power-Up or Board Reset, the delay lines are programmed with values stored in the Altera device. These values are chosen to comply with the timing requirements of the CCD image sensor (See References for details). The delay values shown in Table 11 are typical values, and may vary on an individual Evaluation Board set.

For programming purposes, the silicon delay lines are cascaded, i.e., the serial output pin of device 1 is tied to the serial input pin of device 2 and so on. Therefore, when making an adjustment to one or more delay lines, all the delay lines must be reprogrammed. The total number of serial bits must be eight times the number of units daisy-chained and each group of 8 bits must be sent in MSB-to-LSB order. The total delay on each output signal is calculated as:

$$\text{Delay} = 10.0 + 0.25 \cdot [\text{Delay Code}] \text{ (ns)} \qquad \text{(eq. 1)}$$

Refer to the Dallas Semiconductor DS1020 Programmable Silicon Delay Line Specification Sheet (References) for details.

Table 11. DEFAULT DALEY IC PROGRAMMING

Programming Order	Delay IC Output Signal	Delay IC Input Signal Source	Delay Code (Typical)	Delay (ns) (Typical)
1	AD9845A DATACLK	PIXEL CLK	42	20.50
2	CH2 AD9845A SHP	PIXEL CLK	28	17.00
3	CH1 AD9845A SHP	PIXEL CLK	24	16.00
4	CH2 AD9845A SHD	INVERTED PIXEL CLK	16	14.00
5	CH1 AD9845A SHD	INVERTED PIXEL CLK	22	15.50
6	H1 CLOCK	PIXEL CLK	34	18.50
7	(Not Used)	PIXEL CLK	16	14.00
8	H2 CLOCK	PIXEL CLK	28	17.00
9	(Not Used)	PIXEL CLK	8	12.00
10	RESET CLOCK	INVERTED PIXEL CLK	4	11.00

AFE Register Initialization

On power up or board-reset, the AFE registers are programmed to the default levels shown in Table 12. See the AD9845A specifications sheet (References) for details.

Table 12. DEFAULT AD9845A AFE REGISTER PROGRAMMING

Register Address	Description	Value (Decimal)	Notes
0	Operation	128	
1	VGA Gain	164	Corresponds to a VGA Stage Gain of 6.0 dB
2	Clamp	96	The Output of the AD9845A will be Clamped to Code 96 during the CLPOB Period
3	Control	10	CDS Gain Enabled
4	CDS Gain	43	Corresponds to a CDS Stage Gain of 0.0 dB

Programmable Register Initialization

There are five 8-bit programmable registers used to control the Multi-line integration mode, and the electronic exposure control (LOG). These registers are programmed in parallel through the DIO interface. DIO[2..0] specify the register address, DIO[10..3] specify the 8 bits of data, and DIO11 is the WRITE strobe used to latch the data. The data values range from 0 to 255 (decimal).

At the end of the AFE Register Initialization, the registers are automatically initialized to the default values listed in Table 13. The LOGx_STOP registers adjust the Electronic Exposure controls in 16-pixel increments. The INT_LINES register adjusts the Multi-line Integration in 1-line increments.

Table 13. DEFAULT PROGRAMMABLE REGISTER PROGRAMMING

Register Address DIO[2..0]	Description	Value (Decimal) DIO[10..3]	Notes
3	LOGL_STOP	0	16 Pixels per Count plus 6
4	LOGR_STOP	0	16 Pixels per Count plus 6
5	LOGG_STOP	0	16 Pixels per Count plus 6
6	LOGB_STOP	0	16 Pixels per Count plus 6
7	INT_LINES	0	1 Line per Count

CLEAR/SETUP and INITIALIZE States

The timing generator state machine is free-running at all times. It cycles through the states depending on the jumper settings and DIO inputs, and then returns back to the clear/setup state to begin the next frame. The clear/setup state is used to reset the internal PLD counters at the beginning of each frame.

The INITIALIZE state is used to determine the selected operating modes, and to synchronize with the INTEGRATE_CLK as needed. The values of the JMP[3..0] jumpers and the programmable registers are read, and are used to determine the timing signals for the subsequent frame.

TG_TRANSFER State

During the TG_TRANSFER state, the TG1C, TG2C, and TG2L clocks are brought to the high level and charge is transported from the photodiodes to the Horizontal CCDs. If Exposure Control Mode is selected for any channel, LOGx (where x = L, R, G, or B) will go HIGH as TG2 goes LOW. Integration begins on the falling edge of TG2, or the falling edge of LOGx if Exposure Control is being used. See Figure 5.

LINE_TRANSFER and LINE_INCREMENT States

During the LINE_TRANSFER state, charge is transported to the CCD output structure pixel by pixel. A line transfer counter in the PLD is used to keep track of how many pixels have been transported, and to synchronize the AD9845A timing signals and the PCI−1424 timing signals with the appropriate pixels (dark pixels for black clamping, for example).

At the end of each line transfer, the Multi-Line counter is checked. If Multi-Line Integration Mode has been selected by entering a value greater than 1 in the INT_LINES register, the CCD will be integrated for that number of line times, without clocking TG1C and TG2x. See Figure 9.

When the desired integration time has been achieved, the state machine will enter the LINE_INCREMENT state, in which the Line Counter is incremented. If TF lines have been clocked out of the CCD (See Table 5), the state machine proceeds to the CLEAR/SETUP state; if not,

the state machine returns to the TG_TRANSFER state, and transfers another line of charge into the horizontal register.

TGL_MIDLINE State

The entire KLI−4104 Luma photodiode array contains twice the number of active pixels in each Chroma array, but because there are four Luma output channels, each of the Luma channels has half the number of active pixels of a Chroma channel. Therefore, two lines may be read from the Luma channels for every line read from the Chroma channels, thus achieving twice the resolution in both the vertical and horizontal dimensions. See the KLI−4104 Device Performance Specifications (References) for details.

In Single Line Integration Mode, the charge in the Luma photodiodes is transferred during the TG_TRANSFER state, and again during the TGL_MIDLINE state. When the horizontal counter reaches TG2L_MIDLINE_START (See Table 5), the Horizontal clocks are suspended, and the TG2L clock is activated to transport charge to the Luma Horizontal CCDs. The timing of this state is identical to the TG_TRANSFER state, except that TG1C and TG2C are not clocked.

Following the TGL_MIDLINE state, the LINE_TRANSFER state resumes, and a new Luma line is read out along with the remaining Chroma line. See Figure 6.

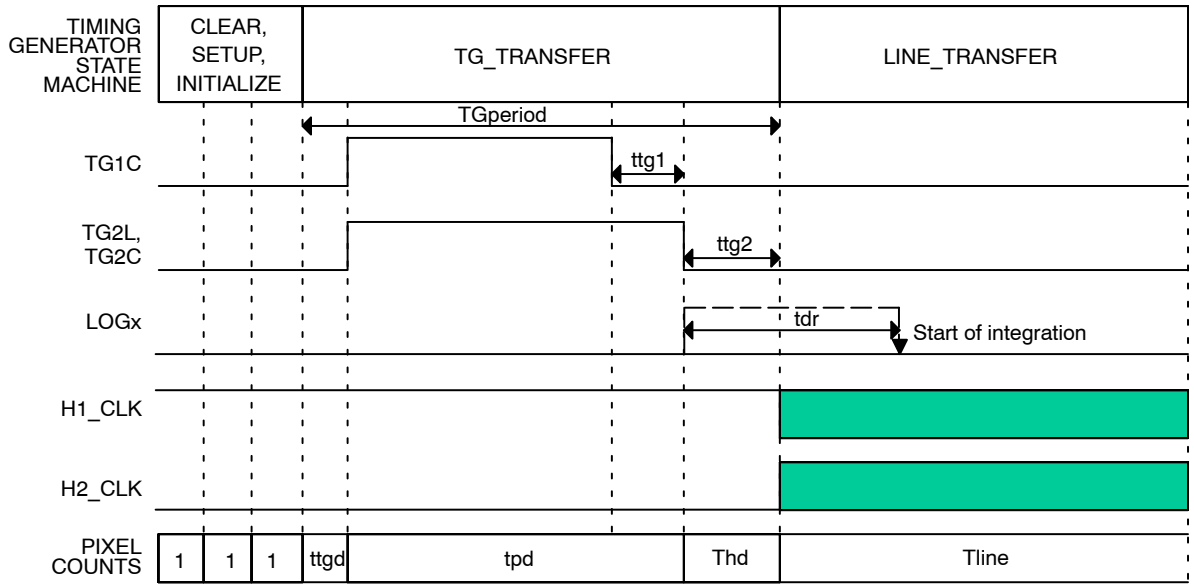

Figure 5. Transfer Gate Transfer Timing

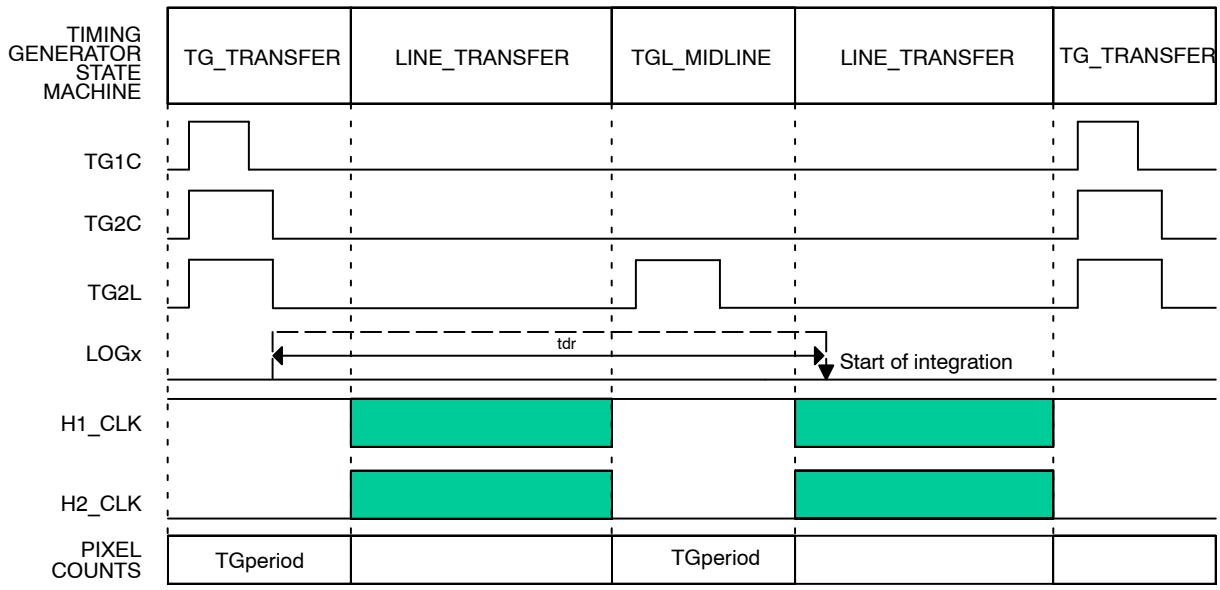

Figure 6. Line Timing − Single Line Integration Mode

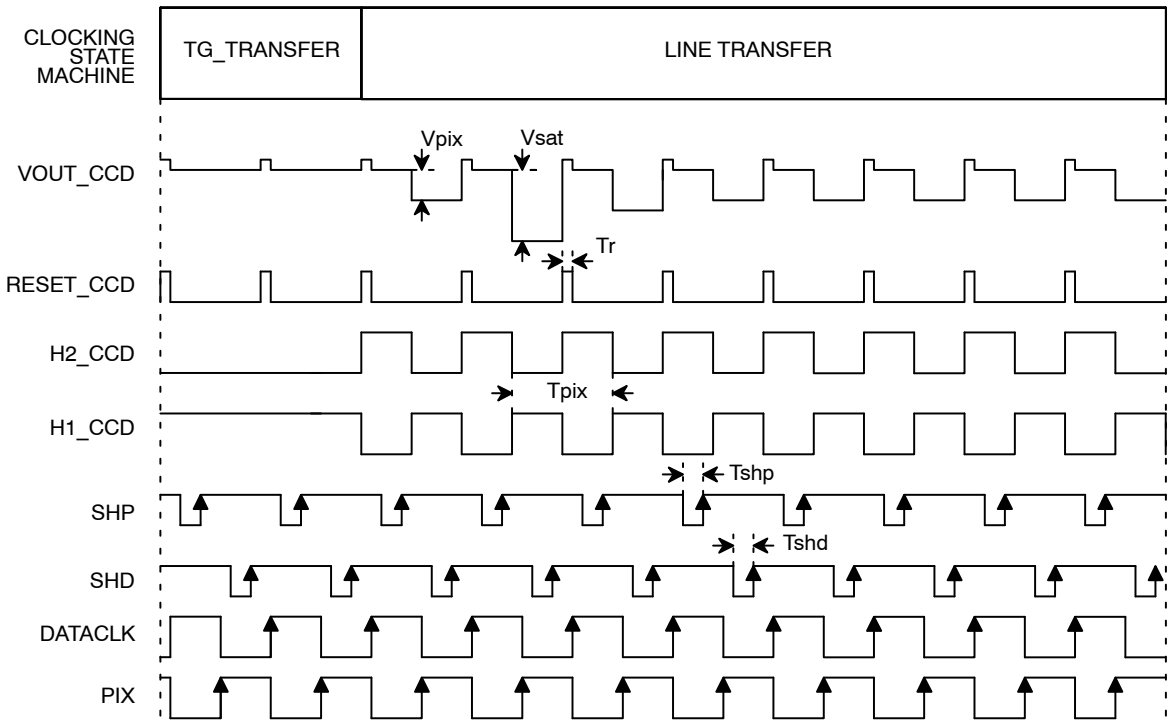

Figure 7. Horizontal Timing − Line Transfer

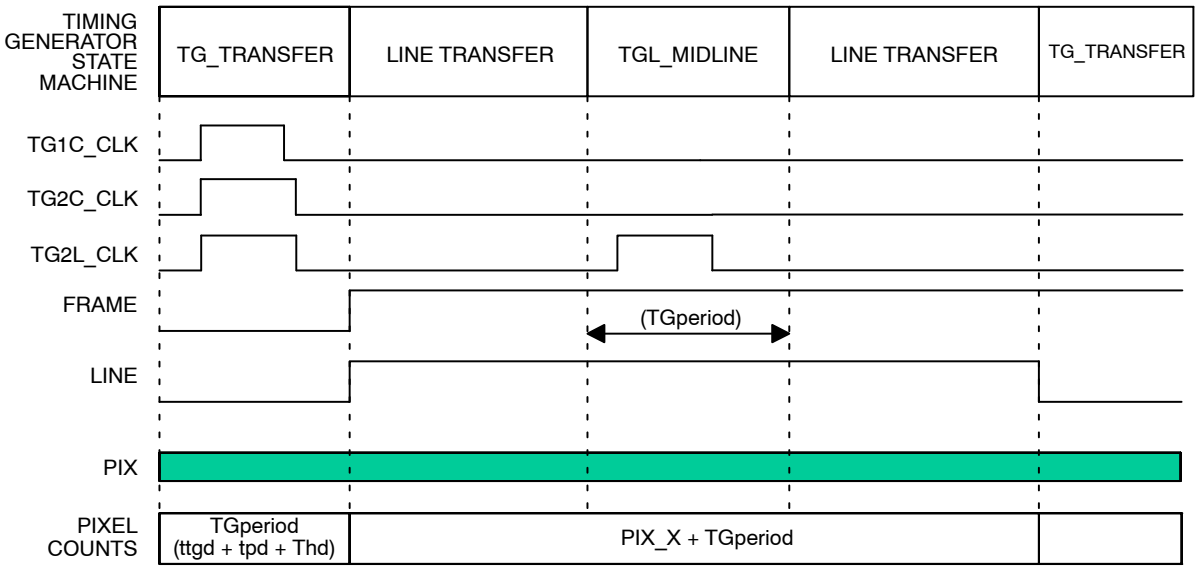

Figure 8. PCI−1424 Frame Grabber Timing − Single Line Integration Mode

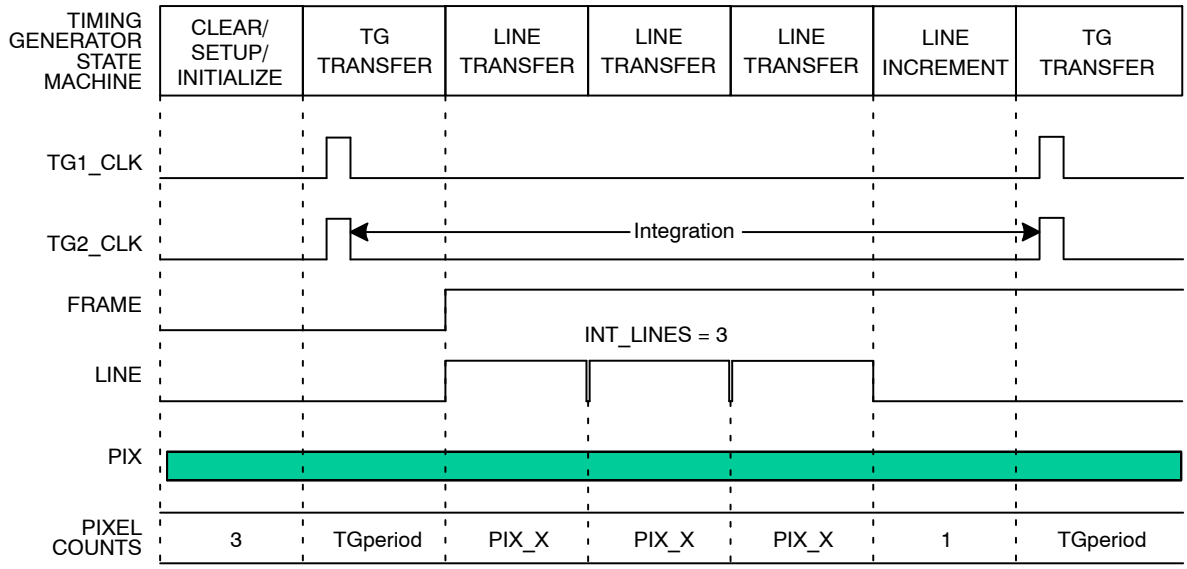

Figure 9. PCI−1424 Frame Grabber Timing − Multi-Line Integration Mode

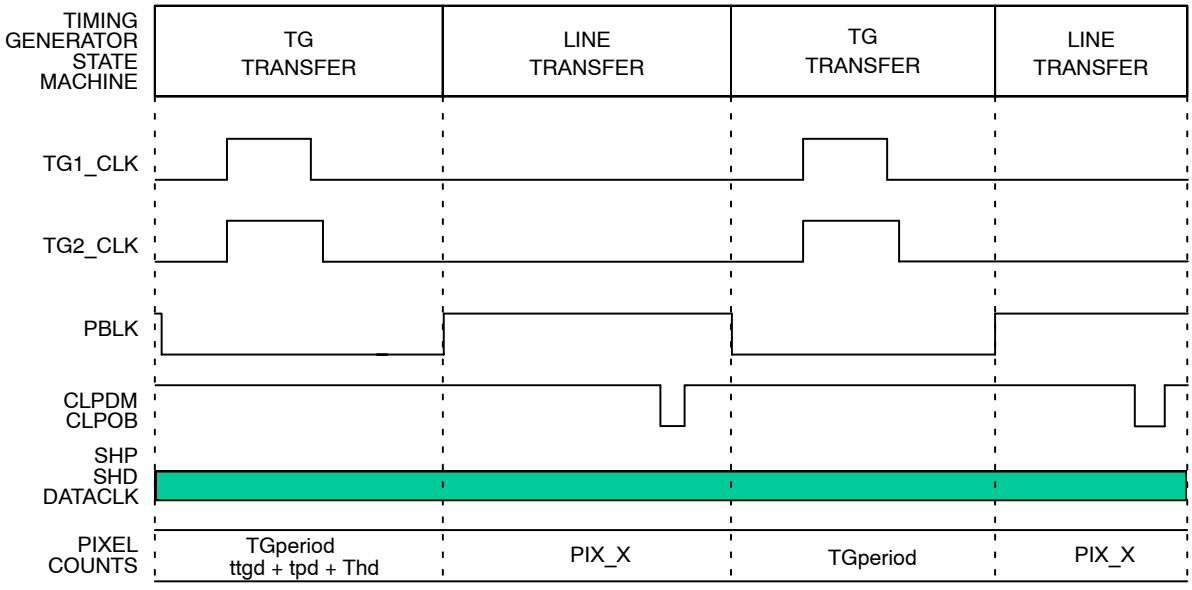

Figure 10. AD9845 Timing

WARNINGS AND ADVISORIES

When programming the Timing Board, the Imager Board must be disconnected from the Timing Board before power is applied. If the Imager Board is connected to the Timing Board during the reprogramming of the Altera PLD, damage to the Imager Board will occur.

Purchasers of a Truesense Imaging Evaluation Board Kit may, at their discretion, make changes to the Timing Generator Board firmware. ON Semiconductor can only support firmware developed by, and supplied by, Truesense Imaging. Changes to the firmware are at the risk of the customer.

ORDERING INFORMATION

Please address all inquiries and purchase orders to:

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E-mail: info@truesenseimaging.com

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

REFERENCES

[1] KLI−4104 Device Specification
[2] KLI−4104 Imager Board User Manual
[3] KLI−4104 Imager Board Schematic
[4] AD984X Timing Generator Board User Manual
[5] AD984X Timing Generator Board Schematic
[6] Analog Devices AD9845 Product Data Sheet (28 and 30 MHz operation)

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
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