

LTC4316

Single I²C/SMBus Address Translator

DESCRIPTION

Demonstration circuit 2217A features the **LTC[®]4316** single I²C/SMBus address translator. The LTC4316 enables one or more I²C or SMBus slave devices to translate their hardwired address to a different address. This allows slaves with the same address to coexist on the same bus. Only discrete resistors are needed to select the new address and no software programming is required. Up to 127 different translations are available.

The LTC4316 has a rich set of features including:

- Allowing Multiple Slaves with the Same Address to Coexist on the Same Bus.
- Resistor Configurable Address Translating
- Compatibility with SMBus, I²C and I²C Fast Mode
- Pass-Through Mode for General Call Addressing
- Level Translation for 2.5V, 3.3V, and 5V Buses
- Stuck Bus Timeout
- Prevention of SDA and SCL Corruption During Live Board Insertion and Removal

- Support for Bus Hot Swap™
- 10-Lead MSOP or DFN 3mm × 3mm Package

The LTC4316 incorporates a pass-through mode which disables the address translating and allows general call addressing by the master. The LTC4316 is designed to automatically recover from abnormal bus conditions like bus stuck low or premature stop bits. There are three LTC parts in this family with different numbers of inputs and outputs. The part numbers are as follows:

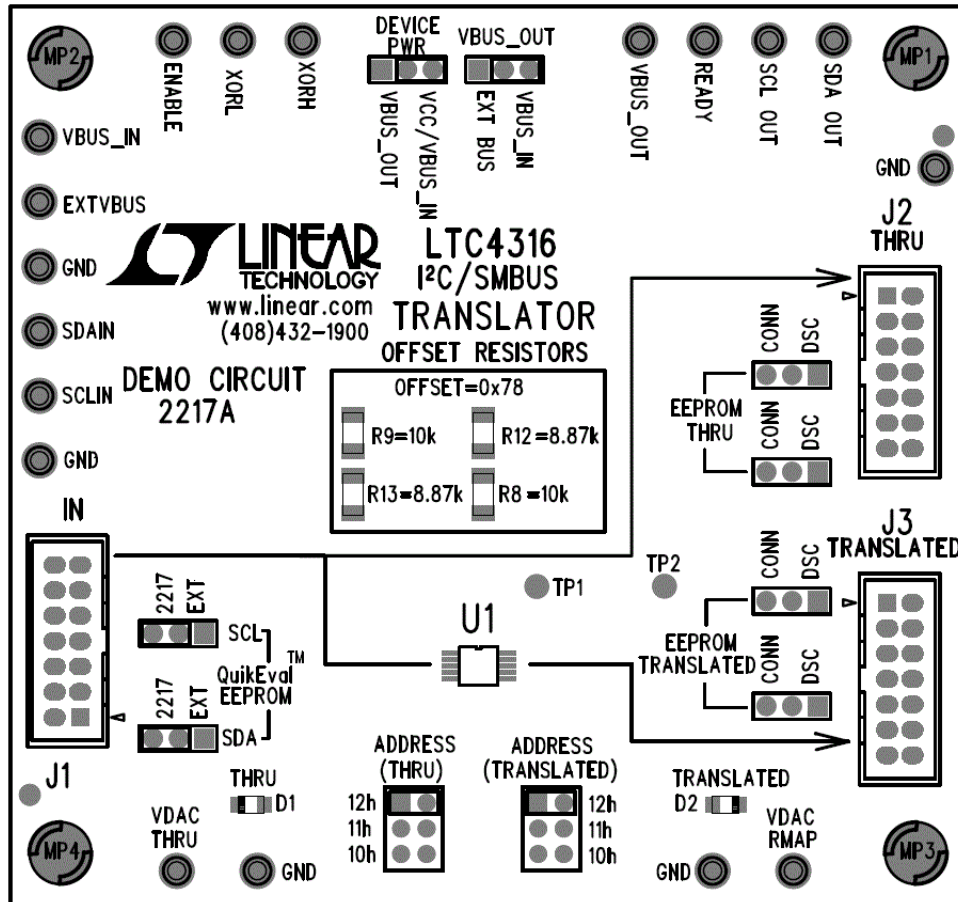
PART NUMBER	NUMBER OF INPUT CHANNELS	NUMBER OF OUTPUT CHANNELS
LTC4316	1	1
LTC4317	1	2
LTC4318	2	2

DC2217A demonstrates only the LTC4316. The other parts provide similar functions with differences listed in their respective data sheets.

Design files for this circuit board are available at <http://www.linear.com/demo/DC2217A>

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QUICK START PROCEDURE



QUICK START PROCEDURE

OVERVIEW

The DC2217A is designed to demonstrate the ability of the LTC4316 to offset an incoming I²C address field on the SDAIN pin to any other I²C address on the SDAOUT pin. The I²C data input to the card is generated from the DC590 in conjunction with a PC.

This is implemented by EXCLUSIVE ORing the input address with a fixed offset that is determined by resistors R8, R9, R12, and R13, located on the OFFSET RESISTORS section on the top center of the board. These resistor values are selected by using values shown in Table 3 and Table 4 of the LTC4316 data sheet.

Input I²C serial data (SDAIN) and serial clock (SCLIN) are applied to the DC2217A via a connecting cable between a DC590 USB SERIAL CONTROLLER and IN jack J1 of the DC2217A. These incoming signals are connected to SCLIN and SDAIN of the LTC4316 (U1), as well as to the SCL and SDA pins of U2, an LTC2631 DAC. Another LTC2631 DAC, U3, has its SCL and SDA connected to SDAOUT and SCLOUT of the LTC4316 TRANSLATOR. Both DACs can be programmed to one of three addresses by use of their CA0 inputs. These addresses are selected by jumper pins ADDRESS (THRU) and ADDRESS (TRANSLATED). For the purposes of testing the board, both are selected to respond to address 0x12h.

If both DACs were connected to SDAIN and SCLIN, they would both respond at the same time when address 0x12h is received. However, since DAC U3 is connected to SDAOUT and SCLOUT of U1, and U1 is set for a 0x78h offset by the OFFSET RESISTORS, it will respond to the address 0x6Ah. The data bits are set to full-scale for the DACs.

The net result is that when address field 0x12h is sent from the DC590 with data bits set to full-scale, the LED designated THRU will be illuminated. When address field 0x6Ah is sent, the LED designated TRANSLATED will be illuminated. This shows that an address translation has occurred because of the offset programmed into address translator U1, the LTC4316.

Jumper options VBUS_OUT and DEVICE POWER allow operation of the LTC4316 at different V_{CC} and I²C bus levels than the 5V supplied from the DC590. With VBUS_OUT in the VBUS_IN position, and DEVICE PWR in the VCC/VBUS_IN position, all power for V_{CC} of U1 and SCLIN, SDAIN, SCLOUT, and SDAOUT bus pull-up voltages will be sourced by the DC590. With EXT BUS selected by the VBUS_OUT jumper and VCC/VBUS_IN selected by the DEVICE PWR jumper, V_{CC} of U1 will be sourced by the 5V from the DC590 along with SCLIN, SDAIN bus pull up resistors while SCLOUT and SDAOUT will be sourced from the EXTVBUS turret. With VBUS_OUT jumper in the EXT BUS position and DEVICE PWR in the VBUS_OUT position, V_{CC} for U1 as well as SCLOUT and SDAOUT will be sourced from the EXTVBUS turret. This gives maximum flexibility of input and output I²C bus levels for use with external bus structures.

Optional connections allow selection and control of other QuikEval™ demonstration circuits using the THRU and TRANSLATED connectors. The EESCL and EESDA lines from J1 may be configured to address either the onboard EEPROM U4, or EEPROMs located on other QuikEval demonstration circuits by using the QuikEval EEPROM SCL and SDA jumpers. For normal operation, the SCL and SDA jumpers should be in the 2217 position.

DEMO MANUAL DC2217A

QUICK START PROCEDURE

PROCEDURE

Connect the DC2217A and DC590 as shown in Figure 1. Insert the USB cable into a USB port on the PC.

QuikEval Interface

The DC2217A can be connected to a DC590 and used with QuikEval software. The DC590 connects to a PC through USB. QuikEval automatically detects the demo

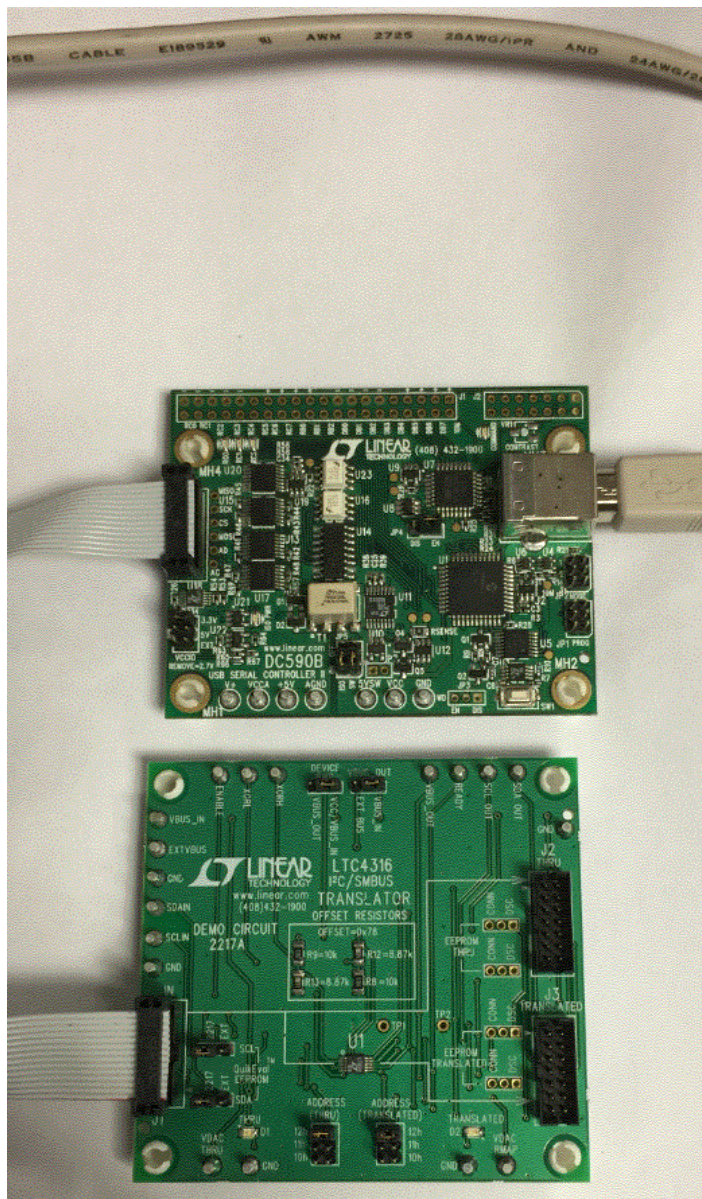


Figure 1. Connection of DC2217A to DC590

QUICK START PROCEDURE

board and brings up the LTC4316 Evaluation Software Interface (Figure 2). The QuikEval software is available at: <http://www.linear.com/QuikEval>

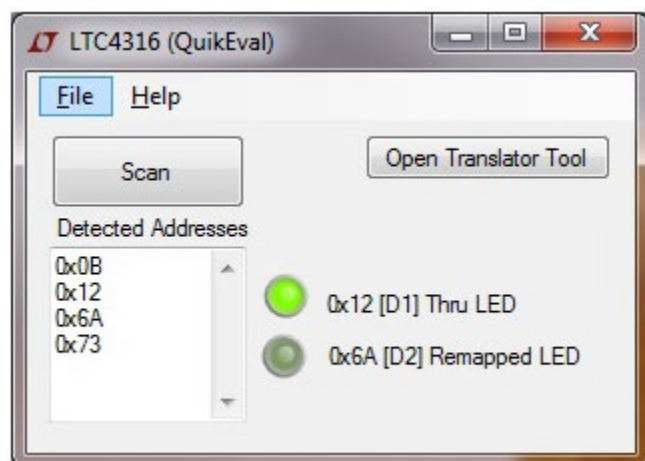


Figure 2. Evaluation Software Interface

Interface Design

The QuikEval interface consists of a Scan button which, when pressed, causes the software to poll every I²C address one at a time and listen for an acknowledge. Every address that acknowledges is then listed in the Detected Address list box directly beneath the Scan button. Once the addresses are detected, the software determines which ones correspond to the LEDs on the demo board. At this point, clicking on the DAC Thru or DAC Translated light-up control will cause the corresponding LED on the demo board to illuminate. The Open Translator Tool button opens a tool that allows users to design an I²C bus using LTC4316 I²C devices in an easy to use graphical format. Figure 2 shows the results of selecting the Scan button on a DC22117A with a standard configuration. The Detected addresses show the All Call address, the address of the DAC on the incoming I²C bus, the address

of the translated output I²C bus, and the address of the on board EEPROM. The 0x12 [D1] Thru LED button has been selected and corresponds to the THRU LED on the DC2217A being illuminated.

Table 1. Input and Output Connections

NOMENCLATURE	CONNECTOR	DESCRIPTION
IN	J1	Connection to DC590
THRU	J2	Optional Output for Customer Use
TRANSLATED	J3	Optional Output for Customer Use

Table 2. Turrets

NOMENCLATURE	DESCRIPTION
VDAC THRU	Analog Output of Thru Address DAC U2
VDAC RMAP	Analog Output of Translated Address DAC U3
GND	Ground
SCL OUT	Serial Clock on Output Side of U1
SDA OUT	Serial Data on Output Side of U1
READY	READY Pin of U1
VBUS_OUT	V _{CC} Bus Voltage Selected by VBUS_OUT Jumper for SCLOUT and SDAOUT
SCL IN	U1 SCLIN Pin
SDAIN	U1 SDAIN Pin
XORL	U1 XORL Pin
XORH	U1 XORH Pin
ENABLE	U1 ENABLE Pin
EXTVBUS	Input for External V _{CC} for U1 and Input Pull Up Supply
VBUS_IN	Internal V _{CC} Bus Supplied by DC590

QUICK START PROCEDURE

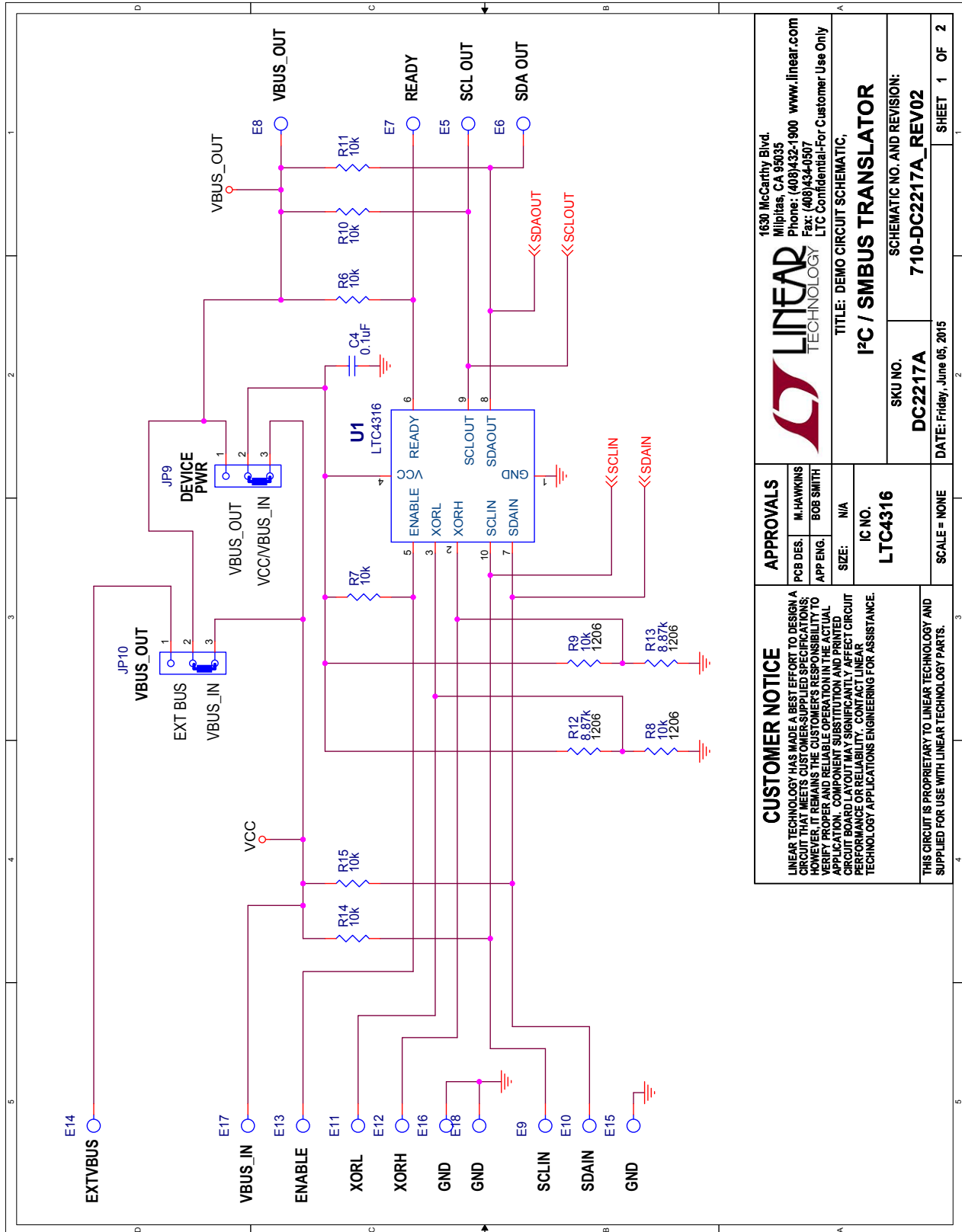
Table 3. Jumpers

NOMENCLATURE	DESCRIPTION	DEFAULT POSITION
ADDRESS (THRU)	Selects Address of D/A U2	12h
ADDRESS (Translated)	Selects Address of D/A U3	12h
QuikEval EEPROM SCL	Selects SCL Source of EEPROM	2217
QuikEval EEPROM SDA	Selects SDA Source of EEPROM	2217
EEPROM THRU	Optional EEPROM J2 Select	Optional
EEPROM THRU	Optional EEPROM J2 Select	Optional
EEPROM TRANSLATED	Optional EEPROM J3 Select	Optional
EEPROM TRANSLATED	Optional EEPROM J3 Select	Optional
DEVICE PWR	Selects Power Source of V _{CC} from Either DC590 or VBUS_OUT	VCC/VBUS_IN
VBUS_OUT	Selects VBUS_OUT from Either DC590 or External Power Source (EXTVBUS)	VBUS_IN

Table 4. LEDs

NOMENCLATURE	LED	DESCRIPTION
THRU (Green)	D1	Illuminates When DAC U2 is Addressed and Data FF is Received
TRANSLATED (Green)	D2	Illuminates When DAC U3 is Addressed and Data FF is Received

SCHEMATIC DIAGRAM



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<p>IC NO. LTC4316</p>		<p>SKU NO. DC2217A</p>							
<p>TITLE: DEMO CIRCUIT SCHEMATIC,</p>		<p>SCHEMATIC NO. AND REVISION: 710-DC2217A_REV02</p>							
<p>THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.</p>		<p>DATE: Friday, June 05, 2015</p>							
<p>SCALE = NONE</p>		<p>SHEET 1 OF 2</p>							

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DEMO MANUAL DC2217A

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