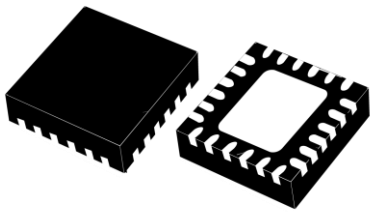
LNBH25S

LNB supply and control IC with step-up and I²C interface

Datasheet - production data



QFN24 (4x4 mm)

Features

- Complete interface between LNB and I²C bus
- Built-in DC-DC converter for single 12 V supply operation and high efficiency (typ. 93% @ 0.5 A)
- Selectable output current limit by external resistor
- Compliant with main satellite receiver output voltage specifications (15 programmable levels)
- Accurate built-in 22 kHz tone generator suits widely accepted standards
- 22 kHz tone waveform integrity guaranteed at no-load condition
- Low drop post regulator and high efficiency step-up PWM with integrated power NMOS allowing low power losses
- LPM function (low power mode) to reduce dissipation
- Overload and overtemperature internal protections with I²C diagnostic bits
- LNB short-circuit dynamic protection
- +/- 4 kV ESD tolerant on output power pins

Applications

- STB satellite receivers
- TV satellite receivers
- PC card satellite receivers

Description

Intended for analog and digital satellite receivers/Sat-TV and Sat-PC cards, the LNBH25S is a monolithic voltage regulator and interface IC, assembled in QFN24L (4x4 mm) specifically designed to provide 13/18 V power supply and 22 kHz tone signaling to the LNB down-converter in the antenna dish or to the multi-switch box. In this application field, it offers a complete solution with extremely low component count and low power dissipation together with a simple design and I²C standard interface.

Table 1: Device summary

Order code	Package	Packing
LNBH25SPQR	QFN24L (4x4)	Tape and reel

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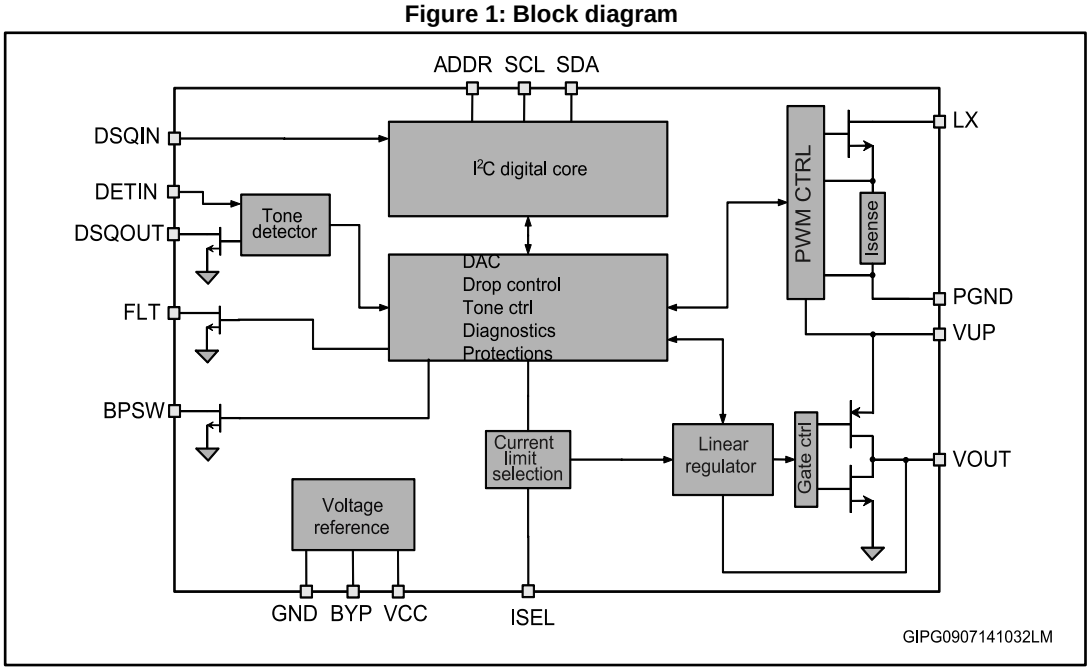
1 Block diagram

Figure 1: Block diagram



2 Application information

This IC has a built-in DC-DC step-up converter that, from a single source (8 V to 16 V), generates voltages (V_{UP}) which let the integrated LDO post-regulator (generating13 V/18 V LNB output voltages plus 22 kHz DiSEqC™ tone) work with a minimum dissipated power of 0.5 W typ. @ 500 mA load (the LDO drop voltage is internally kept at V_{UP}-V_{OUT} = 1 V typ.). The LDO power dissipation can be reduced when 22 kHz tone output is disabled by setting the LPM bit to “1” see *Section 2.4: "LPM (low power mode)"*. The IC is also provided with an undervoltage lockout circuit that disables the whole circuit when the supplied V_{CC} drops below a fixed threshold (4.7 V typ.). The step-up converter soft-start function reduces the inrush current during startup. SS time is internally fixed at 4 ms typ. to switch from 0 to 13 V and 6 ms typ. switch from 0 to 18 V.

2.1 DiSEqC data encoding (DSQIN pin)

The internal 22 kHz tone generator is factory trimmed in accordance with DiSEqC standards, and can be active in 3 different ways:

1. By an external 22 kHz source DiSEqC data connected to the DSQIN logic pin (TTL compatible). In this case I²C tone control bits have to be set: EXTM = TEN = 1.
2. By an external DiSEqC data envelope source connected to the DSQIN logic pin. In this case I²C tone control bits must be set: EXTM = 0 and TEN = 1.
3. Through TEN I²C bit if the 22 kHz presence is requested in continuous mode. In this case the DSQIN TTL pin must be pulled high and EXTM bit is set to “0”.

Each of the above solutions requires that during the 22 kHz tone activation and/or DiSEqC data transmission, the LPM bit has to be set to “0” see *Section 2.4: "LPM (low power mode)"*.

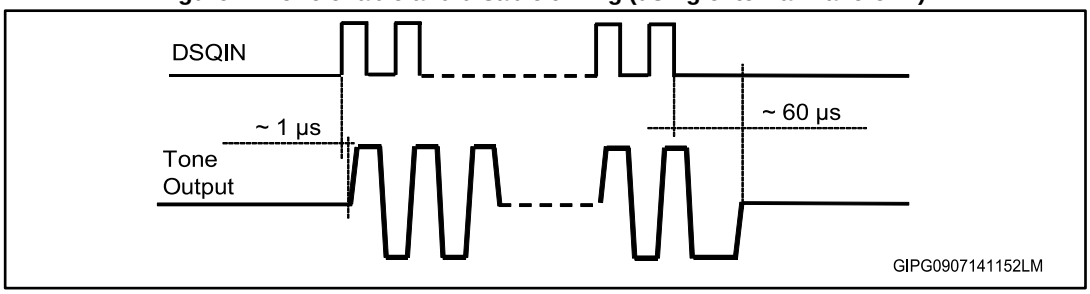
2.2 Data encoding by external 22 kHz tone TTL signal

In order to improve design flexibility, an external tone signal can be input to the DSQIN pin by setting the EXTM bit to “1”.

The DSQIN is a logic input pin, which activates the 22 kHz tone to the VOUT pin, by using the LNBH25S integrated tone generator.

The output tone waveforms are internally controlled by the LNBH25S tone generator in terms of rise/fall time and tone amplitude, while, the external 22 kHz signal on the DSQIN pin is used to define the frequency and the duty cycle of the output tone. A TTL compatible 22 kHz signal is required for the proper control of the DSQIN pin function. Before sending the TTL signal to the DSQIN pin, the EXTM and TEN bits have to be previously set to “1”. As soon as the DSQIN internal circuit detects the 22 kHz TTL external signal code, the LNBH25S activates the 22 kHz tone on the V_{OUT} output with about 1 µs delay from TTL signal activation, and it stops with about 60 µs delay after the 22 kHz TTL signal on DSQIN has expired, refer to *Figure 2: "Tone enable and disable timing (using external waveform)"*.

Figure 2: Tone enable and disable timing (using external waveform)

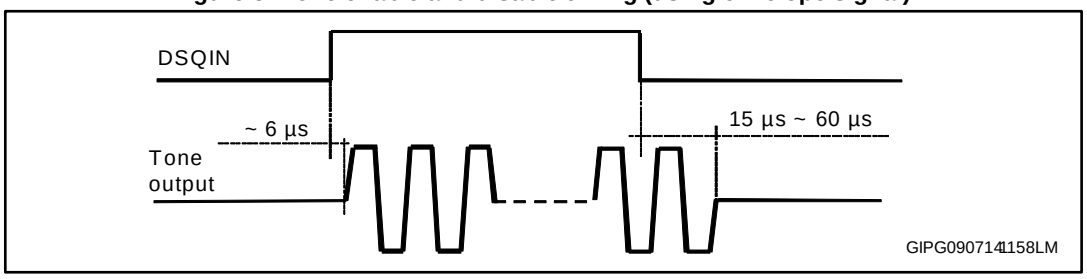


2.3 Data encoding by external DiSEqC envelope control through the DSQIN pin

If an external DiSEqC envelope source is available, the internal 22 kHz generator can be activated during the tone transmission by connecting the DiSEqC envelope source to the DSQIN pin. In this case the I²C tone control bits must be set: EXTM = 0 and TEN = 1. In this manner, the internal 22 kHz signal is superimposed to the V_{OUT} DC voltage to generate the LNB output 22 kHz tone. During the period in which the DSQIN is kept high, the internal control circuit activates the 22 kHz tone output.

The 22 kHz tone on the VOUT pin is active with about 6 µs delay from the DSQIN TTL signal rising edge, and it stops with a delay time in the range from 15 µs to 60 µs after the 22 kHz TTL signal on DSQIN has expired, refer to *Figure 3: "Tone enable and disable timing (using envelope signal)"*.

Figure 3: Tone enable and disable timing (using envelope signal)



2.4 LPM (low power mode)

In order to reduce the total power loss, the LNBH25S is provided with the LPM I²C bit that can be activated (LPM=1) in applications where the 22 kHz tone can be disabled for long time periods. The LPM bit can be set to “1” when the DiSEqC data transmission is not requested (no 22 kHz tone output is present); the drop voltage across the integrated LDO regulator (V_{UP}-V_{OUT}) is reduced to 0.6 V typ. and, consequently, the power loss inside the LNBH25S linear regulator is reduced as well. For example: at 500 mA load, LPM=1 allowing a minimum LDO dissipated power of 0.3 W typ. It is recommended to set the LPM bit to “0” before starting the 22 kHz DiSEqC data transmission; at this condition the drop voltage across the LDO is kept to 1 V typ. LPM=0 if the LPM function is not used.

2.5 DiSEqC 2.0 implementation

The built-in 22 kHz tone detector completes the fully bi-directional DiSEqC 2.0 interfacing. The input pin (DETIN) has to be AC coupled to the DiSEqC bus, and extracted PWK data is available on the DSQOUT pin. To comply with the bi-directional DiSEqC 2.0 bus hardware requirements, an output RL filter is needed. In order to avoid 22 kHz waveform

distortion during tone transmission, the LNBH25S is provided with the BPSW pin to be connected to an external transistor, which allows the output RL filter to be bypassed in DiSEqC 2.x applications while in transmission mode. Before starting tone transmission, TEN bit has to be set to “1” and after ending tone transmission, TEN bit has to be set to “0”.

2.6 Output current limit selection

The linear regulator current limit threshold can be set by an external resistor connected to the ISEL pin. The resistor value defines the output current limit by the equation:

$$I_{LIM}\ (typ.) = \frac{13915}{RSEL^{1.111}}$$

with ISET=0

$$I_{LIM}\ (typ.) = \frac{6808}{RSEL^{1.068}}$$

with ISET=1

see ISET bit description in *Table 9: "Data 3 (read/write register. Register address = 0X4)"*, where RSEL is the resistor connected between ISEL and GND expressed in kΩ and I_{LIM}(typ.) is the typical current limit threshold expressed in mA. I_{LIM} can be set up to 1 A.

2.7 Output voltage selection

The linear regulator output voltage level can be easily programmed in order to accomplish application specific requirements, using 4 bits of an internal data 1 register, see *Section 7.3: "Data registers"* for exact programmable values. Register writing is accessible via I²C bus.

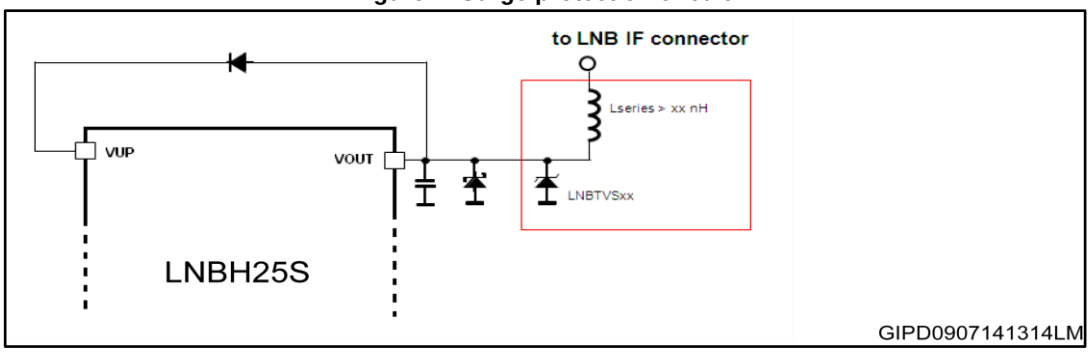
2.8 Diagnostic and protection functions

The LNBH25S has 8 diagnostic internal functions provided by I²C bus, by reading 8 bits on two status registers (in read mode). All the diagnostic bits are, in normal operation (that is no failure detected), set to low. Two diagnostic bits are dedicated to the overtemperature and overload protection status (OTF and OLF) while the remaining 6 bits are dedicated to the output voltage level (VMON), to 22 kHz tone characteristics (TMON), to the minimum load current (IMON), to external voltage source presence on the VOUT pin (PDO), to the input voltage power not good function (PNG) and to the 22 kHz tone presence on the DETIN pin (TDET). Once the OLF (or OTF or PNG) bit has been activated (set to “1”), it is latched to “1” until relevant cause is removed and a new register reading operation is performed.

2.9 Surge protections and TVS diodes

The LNBH25S device is directly connected to the antenna cable in a set-top box. Atmospheric phenomenon can cause high voltage discharges on the antenna cable causing damage to the attached devices. Surge pulses occur due to direct or indirect lightning strikes to an external (outdoor) circuit. This leads to currents or electromagnetic fields causing high voltage or current transients. Transient voltage suppressor (TVS) devices are usually placed, as shown in the following schematic, to protect the STB output circuits where the LNBH25S and other devices are electrically connected to the antenna cable.

Figure 4: Surge protection circuit



For this purpose, the use of the LNBTVSxx surge protection diodes specifically designed by ST is recommended. The selection of the LNBTVSxx diodes should be based on the maximum peak power dissipation supported by the diode (see the LNBTVS datasheet for further details).

2.10 FLT (fault flag)

In order to get an immediate feedback on diagnostic status, the LNBH25S is equipped with a dedicated fault flag pin (FLT). In case of overload (OLF bit=1) or overheating (OTF bit=1) or if “power no good” (PNG bit=1) condition is detected, the FLT pin (open drain output) is set to low and is kept low until the relevant activating diagnostic bit is cleared. Diagnostic bits: OLF, OTF and PNG, once activated, are kept latched to “1” until the root cause is removed and a new register reading operation is performed by the microprocessor. The FLT pin has to be connected to a positive voltage (5 V max.) by a pull-up resistor.

2.11 VMON (output voltage diagnostic)

When the device output voltage is activated (VOUT pin), its value is internally monitored and, as long as the output voltage level is below the guaranteed limits, VMON I²C bit is set to “1”. See *Table 17: "Output voltage diagnostic (VMON bit, status 1 register) characteristics"* for more details.

2.12 TMON (22 kHz tone diagnostic)

The 22 kHz tone can be internally detected and monitored if DETIN pin is connected to the LNB output bus, see typical application circuit in *Figure 7: "DiSEqC 2.x application circuit"*, through a decoupling capacitor. The tone diagnostic function is provided with TMON I²C bit. If the 22 kHz tone amplitude and/or the tone frequency is out of the guaranteed limits, see *Table 19: "22 kHz tone diagnostic (TMON bit, status 2 register) characteristics"*, TMON I²C bit is set to “1”.

2.13 TDET (22 kHz tone detection)

When a 22 kHz tone presence is detected on DETIN pin, TDET I²C bit is set to “1”.

2.14 IMON (minimum output current diagnostic)

In order to detect the output load absence (no LNB connected on the bus or cable not connected to the IRD) the LNBH25S is provided with a minimum output current flag by the IMON I²C bit, accessible in read mode, which is set to “1” if the output current is lower than 12 mA (typ.). IMON function should be used with the 22 kHz tone transmission deactivated, otherwise the IMON bit could be set to “0” even if the output current is below the minimum current threshold. To activate IMON diagnostic function, set to “1” the EN_IMON I²C bit in

the data 4 register. As soon as the IMON function is active by EN_IMON = 1, V_{OUT} rises 21 V (typ.) on the VSEL bit setting. This operation is applied to be sure that the LNBH25S output has the higher voltage in the LNB bus. Do not use this function in an application environment where 21 V voltage level is not supported by other peripherals connected to the LNB bus.

2.15 PDO (overcurrent detection on output pull-down stage)

When an overcurrent occurs on the pull-down output stage due to an external voltage source greater than the LNBH25S nominal V_{OUT} and for a time longer than $I_{SINK\_TIME-OUT}$ (10 ms typ.), PDO I²C bit is set to “1”. This may happen due to an external voltage source on the LNB output (VOUT pin).

For current threshold and deglitch time details, see *Table 13: "Electrical characteristics"*.

2.16 Power-on I²C interface reset and undervoltage lockout

The I²C interface, built into the LNBH25S, is automatically reset at power-on. As long as the V_{CC} is below the undervoltage lockout (UVLO) threshold (4.7 V typ.), the interface does not respond to any I²C command and all data register bits are initialized to zero, therefore the power blocks are disabled. Once V_{CC} rises above 4.8 V typ. the I²C interface becomes operative and data registers can be configured by the main microprocessor.

2.17 PNG (input voltage minimum detection)

When input voltage (VCC pin) is lower than LPD (low power diagnostic) minimum thresholds, the PNG I²C bit is set to “1” and the FLT pin is set low. See *Table 13: "Electrical characteristics"* for threshold details.

2.18 ISW (inductor switching current limit)

In order to allow low saturation current inductors to be used, the maximum DC-DC inductor switching current limit threshold can be set by one I²C bit (ISW). Two values are available: 2.5 A typ. (with ISW = 1) and 4 A typ. (with ISW = 0).

2.19 COMP (boost capacitors and inductor)

The DC-DC converter compensation loop can be optimized to properly work with both ceramic and electrolytic capacitors (VUP pin). For this purpose, one I²C bit in the data 4 register, see table 10, where COMP can be set to “1” or “0” as follows:

- COMP = 0 for electrolytic capacitors
- COMP = 1 for ceramic capacitors

For recommended DC-DC capacitor and inductor values see *Section 5: "Typical application circuits"* and the BOM in and *Table 6: "DiSEqC 2.x bill of material"*.

2.20 OLF (overcurrent and short-circuit protection and diagnostic)

To reduce the total power dissipation during an overload or a short-circuit condition, the device is provided with a dynamic short-circuit protection. It is possible to set the short-circuit current protection either statically (simple current clamp) or dynamically by the PCL bit of I²C data 3 register. When the PCL (pulsed current limiting) bit is set low, the overcurrent protection circuit works dynamically: as soon as an overload is detected, the output current is provided for T_{ON} time (90 ms or 180 ms typ., according to the TIMER bit programmed in the data 3 register) and after that, the output is set in shutdown for T_{OFF} time of typically 900 ms. Simultaneously, the diagnostic OLF I²C bit of the system register is set to “1” and the FLT pin is set to low level. After this time has elapsed, the output is resumed for a time T_{ON}. At the end of T_{ON}, if the overload is still detected, the protection circuit cycles again through T_{OFF} and T_{ON}. At the end of a full T_{ON} in which no overload is detected, normal operation is resumed and the OLF diagnostic bit is reset to low after a register reading. Typical T_{ON} +T_{OFF} time is 990 ms (if TIMER=0) or 1080 ms (if TIMER=1) and it is determined by an internal timer. This dynamic operation can reduce the power dissipation in short-circuit condition, assuring excellent power-on startup in most conditions. However, there may be some cases in which a highly capacitive load on the output may cause a difficult startup when the dynamic protection is chosen. This can be solved by initiating any power startup in static mode (PCL=1) and, then, switching to the dynamic mode (PCL=0) after a specified period of time depending on the output capacitance. Also in static mode, the diagnostic OLF bit goes to “1” (and the FLT pin is set to low) when the current clamp limit is reached and returns low when the overload condition is cleared and register reading is performed.

After the overload condition is removed, normal operation can be resumed in two ways, according to the OLR I²C bit on the data 4 register.

If OLR=1, all VSEL 1..4 bits are reset to “0” and LNB output (VOUT pin) is disabled. To re-enable the output stage, VSEL bits have to be set again by the microprocessor, and the OLF bit is reset to “0” after a register reading operation.

If OLR=0, output is automatically re-enabled as soon as the overload condition is removed, and the OLF bit is reset to “0” after a register reading operation.

2.21 OTF (thermal protection and diagnostic)

The LNBH25S is also protected against overheating: when the junction temperature exceeds 150 °C (typ.), the step-up converter and the linear regulator shut off, the diagnostic OTF bit in the status 1 register is set to “1” and the FLT pin is set to low level. After the overtemperature condition is removed, normal operation can be resumed in two ways, according to the THERM I²C bit on the data 4 register.

If THERM=1, all VSEL 1..4 bits are reset to “0” and LNB output (VOUT pin) is disabled. To re-enable the output stage, VSEL bits must be set again by the microprocessor, while the OTF bit is reset to “0” after a register reading operation.

If THERM=0, output is automatically re-enabled as soon as the overtemperature condition is removed, while the OTF bit is reset to “0” after a register reading operation.

3 Pin configuration

Figure 5: Pin connection (top view)

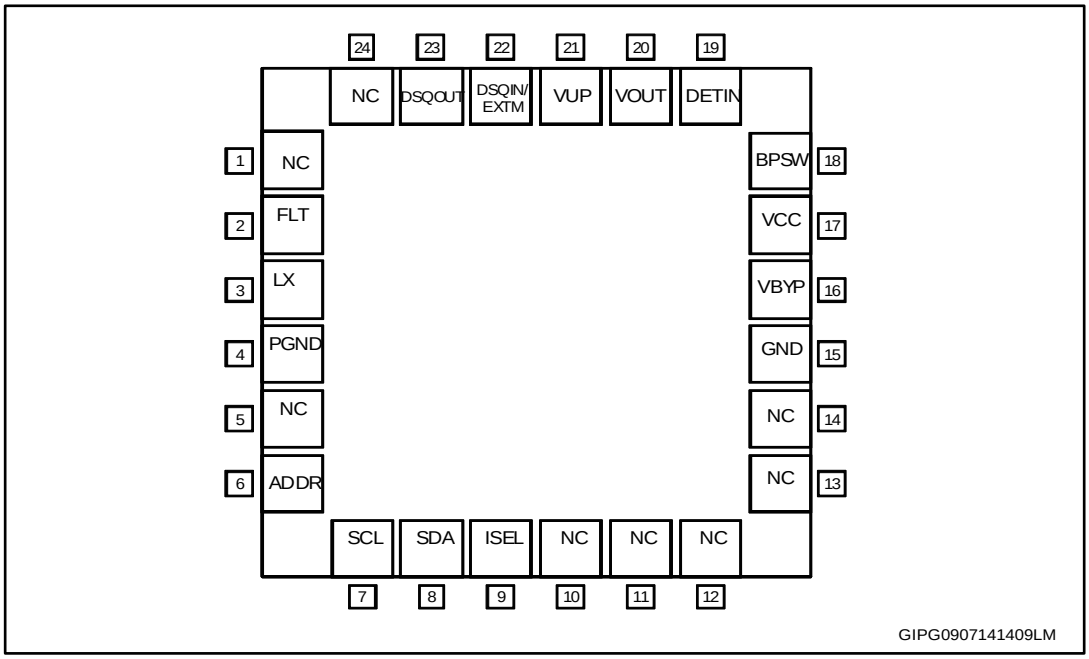


Table 2: Pin description

Pin	Symbol	Name	Pin function
2	FLT	FLT	Open drain output for IC fault conditions. It is set low in case of overload (OLF bit) or overheating status (OTF bit) or power not good (PNG) is detected. To be connected to pull-up resistor (5 V max.)
3	LX	NMOS drain	Integrated N-channel power MOSFET drain
4	PGND	Power ground	DC-DC converter power ground. To be connected directly to exposed pad
6	ADDR	Address setting	Two I²C bus addresses available by setting the address pin level voltage.
7	SCL	Serial clock	Clock from I²C bus
8	SDA	Serial data	Bi-directional data from/to I²C bus
9	ISEL	Current selection	The resistor “RSEL” connected between ISEL and GND defines the linear regulator current limit threshold. Refer to *Section 2.6: "Output current limit selection"* and ISET bit description in *Table 9: "Data 3 (read/write register. Register address = 0X4)"*
15	GND	Analog ground	Analog circuit ground. To be connected directly to the exposed pad
16	VBYP	Bypass capacitor	Needed for internal pre-regulator filtering. The VBYP pin connects an external ceramic capacitor. Any connection of this pin to external current or voltage sources may cause permanent damage to the device
17	VCC	Supply input	8 to 16 V IC DC-DC power supply

Pin	Symbol	Name	Pin function
18	BPSW	Switch control	To be connected to an external transistor to be used to bypass the output RL filter needed in DiSEqC 2.x applications during DiSEqC transmitting mode, see *Section 5: "Typical application circuits"*. Set to ground if it is not used. Open drain pin
19	DETIN	Tone detector input	22 kHz tone decoder input open drain pin has to be AC coupled to the DiSEqC 2.0 bus. Set to ground if it is not used
20	VOUT	LNB output port	Output of the integrated very low drop linear regulator.
21	VUP	Step-up voltage	Input of the linear post-regulator. The voltage on this pin is monitored by the internal step-up controller to keep a minimum dropout across the linear pass transistor
22	DSQIN	DSQIN for DiSEqC envelope input or external 22 kHz TTL input	It can be used as DiSEqC envelope input or external 22 kHz TTL input depending on EXTM I²C bit setting as follows: EXTM=0, TEN=1. It accepts the DiSEqC envelope code from the main microcontroller. The LNBH25S uses this code to modulate the internally generated 22 kHz carrier. If EXTM=TEN=1. It accepts external 22 kHz logic signals which activate the 22 kHz tone output, refer to *Section 2.3: "Data encoding by external DiSEqC envelope control through the DSQIN pin"*. Pull-up high if the tone output is activated by the TEN I²C bit only
23	DSQOUT	DiSEqC output	Open drain output of the tone detector to the main microcontroller for DiSEqC 2.0 data decoding. It is low when tone is detected to the DETIN input pin. Set to ground if it is not used
Epad	Epad	Exposed pad	To be connected with power ground and to the ground layer through vias to dissipate heat
1, 5, 10, 11, 12, 13, 14, 24	NC	Not internally connected	Not internally connected. These pins can be connected to GND to improve thermal performance

4 Maximum ratings

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC power supply input voltage pins	-0.3 to 20	V
V_{UP}	DC input voltage	-0.3 to 40	V
I_{OUT}	Output current	Internally limited	mA
V_{OUT}	DC output pin voltage	-0.3 to 40	V
V_I	Logic input pin voltage (SDA, SCL, DSQIN, ADDR pins)	-0.3 to 7	V
V_O	Logic output pin voltage (FLT, DSQOUT)	-0.3 to 7	V
V_{BPSW}	BPSW pin voltage	-0.3 to 40	V
V_{DETIN}	Detector input signal amplitude	-0.6 to 2	V
I_O	Logic output pin current (FLT, DSQOUT, BPSW)	10	mA
LX	LX input voltage	-0.3 to 30	V
V_{BYP}	Internal reference pin voltage	-0.3 to 4.6	V
ISEL	Current selection pin voltage	-0.3 to 3.5	V
T_{STG}	Storage temperature range	-50 to 150	°C
T_J	Operating junction temperature range	-25 to 125	°C
ESD	ESD rating with human body model (HBM) all pins, unless power output pins	2	kV
	ESD rating with human body model (HBM) for power output pins	4	

Table 4: Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case	2	°C/W
R_{thJA}	Thermal resistance junction-ambient with the device soldered on 2s2p 4-layer PCB provided with thermal vias below exposed pad	40	°C/W

Absolute maximum ratings are those values beyond which damage to the device may occur. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect the device reliability. All voltage values are referred to network ground terminal.

5 Typical application circuits

Figure 6: DiSEqC 1.x application circuit

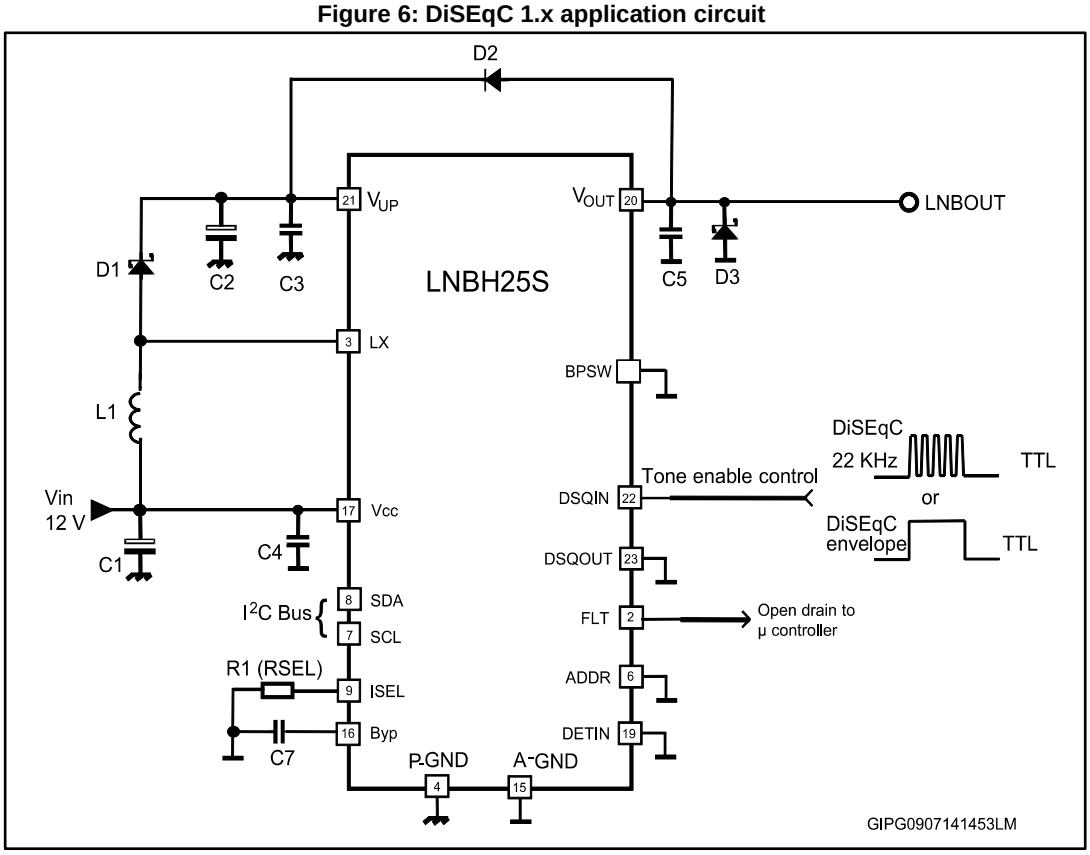


Table 5: DiSEqC 1.x bill of material

Component	Notes
R1 (RSEL)	SMD resistor. Refer to *Table 13: "Electrical characteristics"* and ISEL pin description in *Table 2: "Pin description"*
C1	> 25 V electrolytic capacitor, 100 µF or higher is suitable or > 25 V ceramic capacitor, 10 µF or higher is suitable
C2	With COMP = 0, > 25 V electrolytic capacitor, 100 µF or higher is suitable or with COMP = 1, > 35 V ceramic capacitor, 22 µF (or 2 x 10 µF) or higher is suitable
C3	From 470 nF to 2.2 µF ceramic capacitor placed as closer as possible to VUP pins. Higher values allow lower DC-DC noise
C5	From 100 nF to 220 nF ceramic capacitor placed as close as possible to VOUT pins. Higher values allow lower DC-DC noise
C4, C7	220 nF ceramic capacitors. To be placed as close as possible to VOUT pin
D1	STPS130A or similar Schottky diode
D2	1N4001-07, S1A-S1M, or any similar general purpose rectifier

Component	Notes
D3	BAT54, BAT43, 1N5818, or any low power Schottky diode with $I_F(AV) > 0.2$ A, $V_{RRM} > 25$ V, $V_F < 0.5$ V. To be placed as close as possible to VOUT pin
L1	With COMP=0, use 10 µH inductor with $I_{SAT} > I_{PEAK}$ where I_{PEAK} is the boost converter peak current, or with COMP=1 and C2 = 22 µF, use 6.8 µH inductor with $I_{SAT} > I_{PEAK}$ where I_{PEAK} is the boost converter peak current

Figure 7: DiSEqC 2.x application circuit

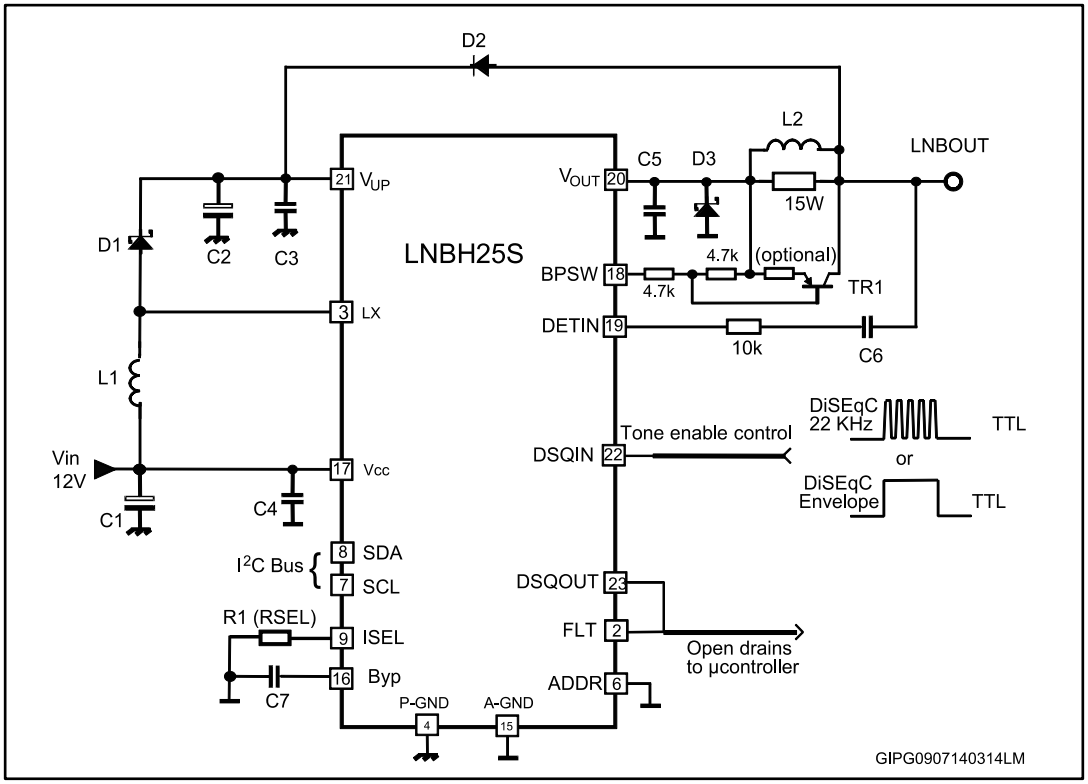


Table 6: DiSEqC 2.x bill of material

Component	Notes
R1 (RSEL)	SMD resistor. Refer to *Table 13: "Electrical characteristics"* and ISEL pin description in *Table 2: "Pin description"*
C1	> 25 V electrolytic capacitor, 100 µF or higher is suitable or > 25 V ceramic capacitor, 10 µF or higher is suitable
C2	With COMP = 0, > 25 V electrolytic capacitor, 100 µF or higher is suitable or with COMP = 1, > 35 V ceramic capacitor, 22 µF (or 2 x10 µF) or higher is suitable
C3	From 470 nF to 2.2 µF ceramic capacitor placed as closer as possible to VUP pin. Higher values allow lower DC-DC noise
C5	From 100 nF to 220 nF ceramic capacitor placed as closer as possible to VOUT pin. Higher values allow lower DC-DC noise
C4, C7	220 nF ceramic capacitors. To be placed as closer as possible to VOUT pin
C6	10 nF ceramic capacitors
D1	STPS130A or similar Schottky diode
D2	1N4001-07, S1A-S1M, or any similar general purpose rectifier
D3	BAT54, BAT43, 1N5818, or any low power Schottky diode with $I_F(AV)$ > 0.2 A, V_{RRM} > 25 V, V_F < 0.5 V. To be placed as closer as possible to VOUT pin
L1	With COMP = 0, use 10 µH inductor with $I_{SAT} > I_{PEAK}$ where I_{PEAK} is the boost converter peak current or with COMP=1 and C2 = 22 µF, use 6.8 µH inductor with $I_{SAT} > I_{PEAK}$ where I_{PEAK} is the boost converter peak current
L2	220 µH - 270 µH inductor as per DiSEqC 2.x specification
TR1	MMBTA92, 2STR2160 or any low power PNP with I_C > 250 mA, V_{CE} > 30 V, can be used. Also any small power PMOS with I_D > 250 mA, $R_{DS(on)}$ < 0.5 W, V_{DS} > 20 V, can be used

6 I²C bus interface

Data transmission from the main microprocessor to the LNBH25S and vice versa takes place through the 2-wire I²C bus interface, consisting of the 2-line SDA and SCL (pull-up resistors to positive supply voltage must be externally connected).

6.1 Data validity

As shown in *Figure 8: "Data validity on the I²C bus"*, the data on the SDA line must be stable during the high semi-period of the clock. The high and low state of the data line can only change when the clock signal on the SCL line is low.

6.2 Start and stop condition

As shown in *Figure 9: "Timing diagram of I²C bus"*, a start condition is a transition from high to low of the SDA line while SCL is high. The stop condition is a transition from low to high of the SDA line while SCL is high. A stop condition must be sent before each start condition.

6.3 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is the first to be transferred.

6.4 Acknowledge

The master (microprocessor) puts a resistive high level on the SDA line during the acknowledge clock pulse, see *Figure 10: "Acknowledge on the I²C bus"*. The peripheral (LNBH25S), which acknowledges, must pull down (low) the SDA line during the acknowledge clock pulse, so that the SDA line is stable low during this clock pulse. The peripheral, which has been addressed, has to generate acknowledge after the reception of each byte, otherwise the SDA line remains at high level during the nin^{th} clock pulse time. In this case, the master transmitter can generate the stop information in order to abort the transfer. The LNBH25S doesn't generate acknowledge if the V_{CC} supply is below the undervoltage lockout threshold (4.7 V typ.).

6.5 Transmission without acknowledge

If the detection of the LNBH25S acknowledges is not necessary, the microprocessor can use a simpler transmission: it simply waits for one clock without checking the slave acknowledging, and sends the new data. This approach is less protected from misworking and decreases noise immunity.

Figure 8: Data validity on the I²C bus

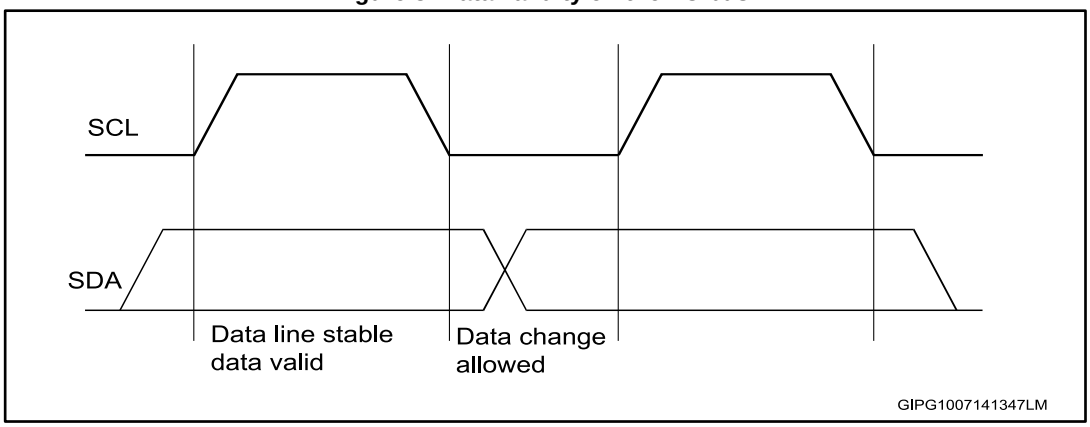


Figure 9: Timing diagram of I²C bus

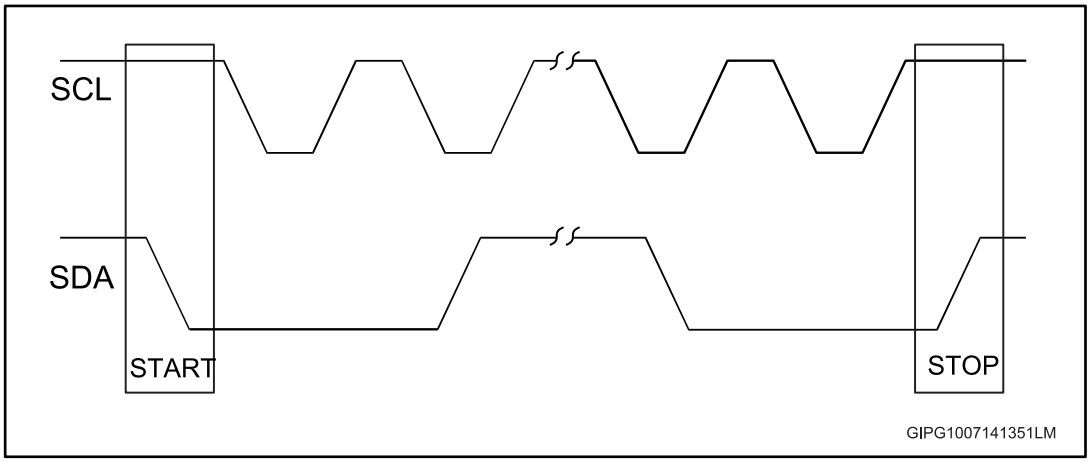
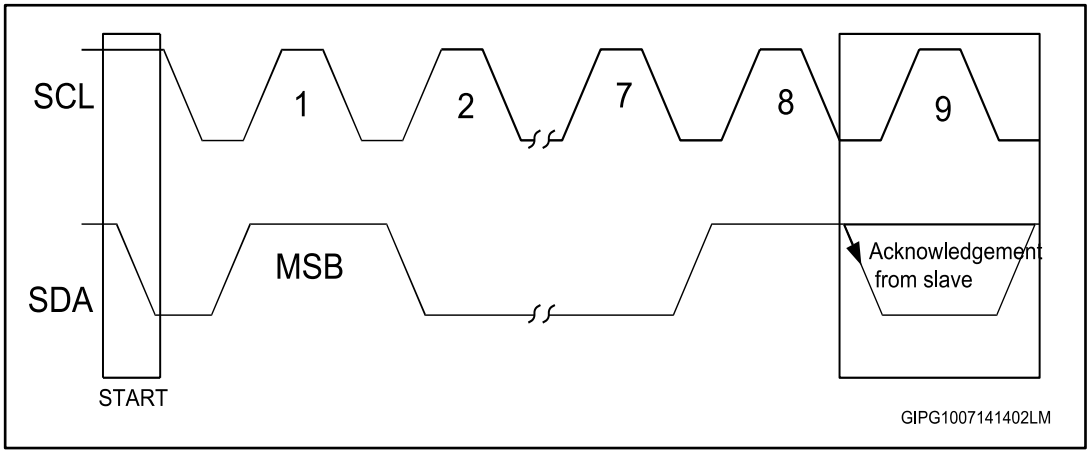


Figure 10: Acknowledge on the I²C bus



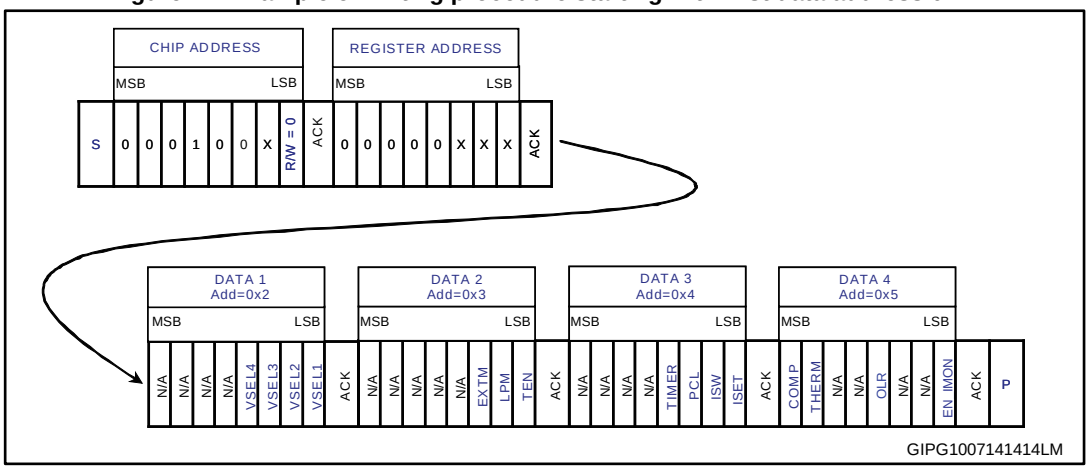
7 I²C interface protocol

7.1 Write mode transmission

The LNBH25S interface protocol is made up of:

- A start condition (S)
- A chip address byte with the LSB bit R/W = 0
- A register address (internal address of the first register to be accessed)
- A sequence of data (byte to write to the addressed internal register + acknowledge)
- The following bytes, if any, to be written to successive internal registers
- A stop condition (P). The transfer lasts until a stop bit is encountered
- The LNBH25S, as slave, acknowledges every byte transfer

Figure 11: Example of writing procedure starting with first data address 0X2



ACK = acknowledge

S = start

P = stop

R/W = 1/0, read/write bit

X = 0/1, set the values to select the chip address for pin selection and to select the register address, see *Table 7: "Data 1 (read/write register. Register address = 0X2)"*.

The writing procedure can start from any register address by simply setting X values in the register address byte (after the chip address). It can be also stopped by the master by sending a stop condition after any acknowledge bit.

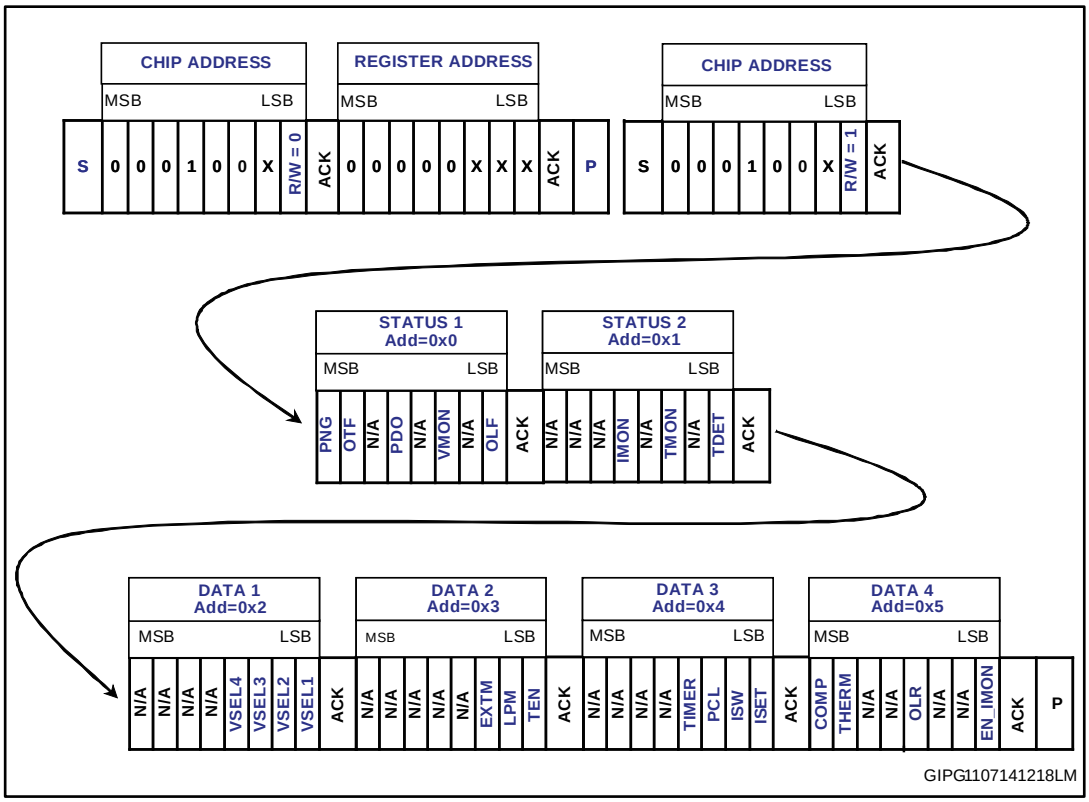
7.2 Read mode transmission

In read mode the byte sequence as follows:

- A start condition (S)
- A chip address byte with the LSB bit R/W=0
- The register address byte of the internal first register to be accessed
- A stop condition (P)
- A new master transmission with the chip address byte and the LSB bit R/W=1

- After the acknowledge, the LNBH25S starts to send the addressed register content. As long as the master keeps the acknowledge low, the LNBH25S transmits the next address register byte content
- The transmission is terminated when the master sets the acknowledge high with the following stop bit

Figure 12: Example of reading procedure starting with first status address 0X0



ACK = acknowledge

S = start

P = stop

R/W = 1/0, read/write bit

X = 0/1, set the values to select the chip address, see *Table 16: "Address pin characteristics"* for pin selection and to select the register address see *Table 7: "Data 1 (read/write register. Register address = 0X2)"*.

The writing procedure can start from any register address (status 1,2 or data 1..4) by simply setting X values in the register address byte (after the chip address). It can be also stopped by the master by sending a stop condition after any acknowledge bit.

7.3 Data registers

The data 1..4 registers can be addressed both to write and read mode. In read mode they return the last writing byte status received in the previous write transmission.

The following tables provide the register address values of data 1..4 and a function description of each bit.

Table 7: Data 1 (read/write register. Register address = 0X2)

Bit	Name	Value	Description
Bit 0 (LSB)	VSEL1	0/1	Output voltage selection bits
Bit 1	VSEL2	0/1	
Bit 2	VSEL3	0/1	
Bit 3	VSEL4	0/1	
Bit 4	N/A	0	Reserved. Keep to “0”
Bit 5	N/A	0	Reserved. Keep to “0”
Bit 6	N/A	0	Reserved. Keep to “0”
Bit 7 (MSB)	N/A	0	Reserved. Keep to “0”

N/A = reserved bit

All bits reset to “0” at power-on

Table 8: Data 2 (read/write register. Register address = 0X3)

Bit	Name	Value	Description
Bit 0 (LSB)	TEN	1	22 kHz tone enabled. Tone output controlled by DSQIN pin
		0	22 kHz tone output disabled
Bit 1	LPM	1	Low power mode active (used with 22 kHz tone output disabled only)
		0	Low power mode deactivated (keep always LPM = 0 during 22 kHz tone transmission)
Bit 2	EXTM	1	DSQIN input pin is set to receive external 22 kHz TTL signal source
		0	DSQIN input pin is set to receive external DiSEqC envelope TTL signal
Bit 3	N/A	0	Reserved. Keep to “0”
Bit 4	N/A	0	Reserved. Keep to “0”
Bit 5	N/A	0	Reserved. Keep to “0”
Bit 6	N/A	0	Reserved. Keep to “0”
Bit 7(MSB)	N/A	0	Reserved. Keep to “0”

N/A = reserved bit

All bits reset to 0 at power-on

Table 9: Data 3 (read/write register. Register address = 0X4)

Bit	Name	Value	Description
Bit 0 (LSB)	ISET	1	Current limit of LNB output (VOUT pin) set to lower current range (see *Section 2.6: "Output current limit selection"*)
		0	Current limit of LNB output (VOUT pin) set to default range (see *Section 2.6: "Output current limit selection"*)
Bit 1	ISW	1	DC-DC, inductor switching current limit set to 2.5 A typ.
		0	DC-DC, inductor switching current limit set to 4 A typ.
Bit 2	PCL	1	Pulsed (dynamic) LNB output current limiting is deactivated
		0	Pulsed (dynamic) LNB output current limiting is active
Bit 3	TIMER	1	Pulsed (dynamic) LNB output current T_{ON} time set to 180 ms typ.
		0	Pulsed (dynamic) LNB output current T_{ON} time set to 90 ms typ.
Bit 4	N/A	0	Reserved. Keep to “0”
Bit 5	N/A	0	Reserved. Keep to “0”
Bit 6	N/A	0	Reserved. Keep to “0”
Bit 7 (MSB)	N/A	0	Reserved. Keep to “0”

N/A = reserved bit

All bits reset to 0 at power-on

Table 10: Data 4 (read/write register. Register address = 0X5)

Bit	Name	Value	Description
Bit 0 (LSB)	EN_IMON	1	IMON diagnostic function is enabled. (V_{OUT} is set to 21 V typ.)
		0	IMON diagnostic function is disabled, keep always at “0” if IMON is not used
Bit 1	N/A	-	Reserved
Bit 2	N/A	-	Reserved
Bit 3	OLR	1	In case of overload protection activation (OLF=1), all VSEL 1..4 bits are reset to “0” and LNB output (VOUT pin) is disabled. VSEL bits have to be set again by the master after the overcurrent condition is removed (OLF=0)
		0	In case of overload protection activation (OLF=1) the LNB output (VOUT pin) is automatically enabled as soon as the overload condition is removed (OLF=0) with the previous VSEL bits setting
Bit 4	N/A	-	Reserved
Bit 5	N/A	-	Reserved
Bit 6	THERM	1	If thermal protection is active (OTF=1), all VSEL 1..4 bits are reset to “0” and LNB output (VOUT pin) is disabled. VSEL bits have to be set again by the master after the overtemperature condition is removed (OTF=0)
		0	If thermal protection is active (OTF=1) the LNB output (VOUT pin) is automatically enabled as soon as the overtemperature condition is removed (OTF=0) with the previous VSEL bits setting
Bit 7(MSB)	COMP	1	DC-DC converter compensation: set to use very low ESR capacitors or ceramic caps on VUP pin
		0	DC-DC converter compensation: set to use standard electrolytic capacitors on VUP pin

N/A = reserved bit

All bits reset to 0 at power-on

7.4 Status registers

Status 1, 2 registers can be only addressed to read mode and provide the diagnostic functions described in the following tables.

Table 11: Status 1 (read register. Register address = 0X0)

Bit	Name	Value	Description
Bit 0 (LSB)	OLF	1	VOUT pin overload protection has been triggered ($I_{OUT} > I_{LIM}$). Refer to *Table 9: "Data 3 (read/write register. Register address = 0X4)"* for the overload operation settings (ISET, PCL, TIMER bits)
		0	No overload protection has been triggered to the VOUT pin ($I_{OUT} < I_{LIM}$)
Bit 1	N/A	-	Reserved
Bit 2	VMON	1	Output voltage (VOUT pin) lower than VMON specification thresholds. Refer to *Table 17: "Output voltage diagnostic (VMON bit, status 1 register) characteristics"*
		0	Output voltage (VOUT pin) is within the VMON specifications
Bit 3	N/A	-	Reserved
Bit 4	PDO	1	Overcurrent detected on output pull-down stage for a time longer than the deglitch period. This may happen due to an external voltage source present on the LNB output (VOUT pin)
		0	No overcurrent detected on output pull-down stage
Bit 5	N/A	-	Reserved
Bit 6	OTF	1	Junction overtemperature is detected, $T_J > 150$ °C.
		0	Junction overtemperature is not detected, $T_J < 135$ °C. T_J is below thermal protection threshold
Bit 7 (MSB)	PNG	1	Input voltage (VCC pin) lower than LPD minimum thresholds. Refer to *Table 13: "Electrical characteristics"*
		0	Input voltage (VCC pin) higher than LPD thresholds. Refer to *Table 13: "Electrical characteristics"*

N/A = reserved bit

All bits reset to 0 at power-on

Table 12: Status 2 (read register. Register address = 0X1)

Bit	Name	Value	Description
Bit 0 (LSB)	TDET	1	22 kHz tone presence is detected on the DETIN pin
		0	No 22 kHz tone is detected on the DETIN pin
Bit 1	N/A	-	Reserved
Bit 2	TMON	1	22 kHz tone present on the DETIN pin is out of TMON specification threshold: the tone frequency or the A_{TONE} (tone amplitude) is out of the thresholds guaranteed in the TMON electrical characteristics
		0	22 kHz tone present on the DETIN pin is within TMON specification thresholds. Refer to *Table 19: "22 kHz tone diagnostic (TMON bit, status 2 register) characteristics"*
Bit 3	N/A	-	Reserved
Bit 4	IMON	1	Output current (from VOUT pin) is lower than IMON specification thresholds. Refer to *Table 18: "Output current diagnostic (IMON bit, status 2 register) characteristics"*
		0	Output current (from VOUT pin) is higher than IMON specifications. Refer to*Table 18: "Output current diagnostic (IMON bit, status 2 register) characteristics"*
Bit 5	N/A	-	Reserved
Bit 6	N/A	-	Reserved
Bit 7 (MSB)	N/A	-	Reserved

N/A = reserved bit

All bits reset to 0 at power-on

8 Electrical characteristics

See *Section 5: "Typical application circuits"*, T_J from 0 to 85 °C, all data 1..4 register bits set to 0 unless VSEL1 = 1, RSEL = 11.5 kΩ, DSQIN = low, V_{IN} = 12 V, I_{OUT} = 50 mA, unless otherwise stated. Typical values are referred to T_J = 25 °C. V_{OUT} = VOUT pin voltage.

Table 13: Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Supply voltage (1)		8	12	16	V
I_{IN}	Supply current	I_{OUT} = 0 mA		6		mA
		22 kHz tone enabled (TEN=1), DSQIN = high, I_{OUT} = 0 mA		10		mA
		VSEL1=VSEL2=VSEL3= VSEL4=0		1		mA
V_{OUT}	Output voltage total accuracy	Valid at any V_{OUT} selected level	-3.5		+3.5	%
V_{OUT}	Line regulation	V_{IN} = 8 to 16 V			40	mV
V_{OUT}	Load regulation	I_{OUT} from 50 to 750 mA		100		
I_{LIM}	Output current limiting thresholds	RSEL = 11.5 kΩ, ISET = 0	750		1100	mA
		RSEL = 16.2 kΩ, ISET = 0	500		750	
		RSEL = 22 kΩ, ISET = 0	350		550	
I_{LIM}	Output current limiting thresholds	RSEL = 11.5 kΩ, ISET = 1		500		mA
		RSEL = 16.2 kΩ, ISET = 1		350		
		RSEL = 22 kΩ, ISET = 1		250		
I_{SC}	Output short-circuit current	RSEL = 11.5 kΩ, ISET = 0		500		mA
SS	Soft-start time	V_{OUT} from 0 to 13 V		4		ms
SS	Soft-start time	V_{OUT} from 0 to 18 V		6		ms
T13-18	Soft transition rise time	V_{OUT} from 13 to 18 V		1.5		ms
T18-13	Soft transition fall time	V_{OUT} from 18 to 13 V		1.5		ms
T_{OFF}	Dynamic overload protection off-time	PCL = 0, output shorted		900		ms
T_{ON}	Dynamic overload protection on-time	PCL = TIMER = 0, output shorted		T_{OFF}/10		
		PCL = 0, TIMER = 1, output shorted		T_{OFF}/5		
A_{TONE}	Tone amplitude	DSQIN = high, EXTM=0, TEN=1 I_{OUT} from 0 to 750 mA C_{BUS} from 0 to 750 nF	0.55	0.675	0.8	V_{PP}
F_{TONE}	Tone frequency	DSQIN = high, EXTM=0, TEN=1	20	22	24	kHz
D_{TONE}	Tone duty cycle		43	50	57	%
tr, tf	Tone rise or fall time (2)		5	8	15	µs
$Eff_{DC/DC}$	DC-DC converter efficiency	I_{OUT} = 500 mA		93		%
F_{SW}	DC-DC converter switching frequency			440		kHz
UVLO	Undervoltage lockout	UVLO threshold rising		4.8		V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
	thresholds	UVLO threshold falling		4.7		
V_{LP}	Low power diagnostic (LPD) thresholds	V_{LP} threshold rising		7.2		V
		V_{LP} threshold falling		6.7		
V_{IL}	DSQIN, pin logic low				0.8	V
V_{IH}	DSQIN, pin logic high		2			V
I_{IH}	DSQIN, pin input current	V_{IH} = 5 V		15		µA
F_{DETIN}	Tone detector frequency capture range (3)	0.4 V_{PP} sine wave	19	22	25	kHz
V_{DETIN}	Tone detector input amplitude(3)	Sine wave signal, 22 kHz	0.3		1.5	V_{PP}
Z_{DETIN}	Tone detector input impedance			150		kΩ
V_{OL_BPSW}	BPSW pin low voltage	I_{OL_BPSW} = 5 mA, DSQIN = high, EXTM=0, TEN=1		0.7		V
V_{OL}	DSQOUT, FLT pins logic LOW	DETIN tone present, I_{OL}= 2 mA		0.3	0.5	V
I_{OZ}	DSQOUT, FLT pins leakage current	DETIN tone absent, V_{OH} = 6 V			10	µA
I_{OBK}	Output backward current	All VSELx=0, V_{OBK} = 30 V		-3	-6	mA
I_{SINK}	Output low-side sink current	V_{OUT} forced at V_{OUT_NOM} + 0.1 V		70		mA
$I_{SINK\_TIME-OUT}$	Low-side sink current time-out	V_{OUT} forced at V_{OUT_NOM} + 0.1 V PDO I²C bit is set to 1 after this time is elapsed		10		ms
I_{REV}	Max. reverse current	V_{OUT} forced at V_{OUT_NOM} + 0.1 V after PDO bit is set to 1 ($I_{SINK\_TIME-OUT}$ elapsed)		2		mA
T_{SHDN}	Thermal shutdown threshold			150		°C
DT_{SHDN}	Thermal shutdown hysteresis			15		°C

Notes:

(1)In applications where (V_{CC} -V_{OUT}) > 1.3 V the increased power dissipation inside the integrated LDO must be taken into account in the application thermal management design.

(2)Guaranteed by design.

(3)Frequency range in which the DETIN function is guaranteed. The V_{PP} level is intended on the LNB bus (before the C6 capacitor. See typical application circuit for DiSEqC 2.x). I_{OUT} from 0 to 750 mA, C_{BUS} from 0 to 750 nF.

Table 14: Output voltage selection table (data1 register, write mode)

VSEL 4	VSEL 3	VSEL 2	VSEL 1	V_{OUT} min.	V_{OUT} voltage	V_{OUT} max.	Function
0	0	0	0		0.000		V_{OUT} disabled. The LNBH25S is set in standby mode
0	0	0	1	12.545	13.000	13.455	
0	0	1	0	12.867	13.333	13.800	
0	0	1	1	13.188	13.667	14.145	
0	1	0	0	13.51	14.000	14.490	
0	1	0	1	13.832	14.333	14.835	
0	1	1	0	14.153	14.667	15.180	
0	1	1	1	14.475	15.000	15.525	
1	0	0	0	17.515	18.150	18.785	
1	0	0	1	17.836	18.483	19.130	
1	0	1	0	18.158	18.817	19.475	
1	0	1	1	18.48	19.150	19.820	
1	1	0	0	18.801	19.483	20.165	
1	1	0	1	19.123	19.817	20.510	
1	1	1	0	19.445	20.150	20.855	
1	1	1	1	19.766	20.483	21.200	

T_J from 0 to 85 °C, V_I = 12 V

Table 15: I²C electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage	SDA, SCL			0.8	V
V_{IH}	High level input voltage	SDA, SCL	2			V
I_{IN}	Input current	SDA, SCL, V_{IN} = 0.4 to 4.5 V	-10		10	µA
V_{OL}	Low level output voltage [a]	SDA (open drain), I_{OL} = 6 mA			0.6	V
F_{MAX}	Maximum clock frequency	SCL			400	kHz

T_J from 0 to 85 °C, V_I = 12 V

[a] Guaranteed by design.

Table 16: Address pin characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{ADDR-1}	“0001000(R/W)” address pin voltage range	R/W bit determines the transmission mode: read (R/W=1) write (R/W=0)	0		0.8	V
V_{ADDR-2}	“0001001(R/W)” address pin voltage range	R/W bit determines the transmission mode: read (R/W=1) write (R/W=0)	2		5	V

Refer to *Section 5: "Typical application circuits"*, T_J from 0 to 85 °C, all dat 1..4 register bits set to “0”, RSEL = 11.5 kΩ, DSQIN = low, V_{IN} = 12 V, I_{OUT} = 50 mA, unless otherwise stated. Typical values are referred to T_J = 25 °C. V_{OUT} = VOUT pin voltage. See *Section 6: "I²C bus interface"* and *Section 7: "I²C interface protocol"*.

Table 17: Output voltage diagnostic (VMON bit, status 1 register) characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{TH-L}	Diagnostic low threshold at V_{OUT} = 13.0 V	VSEL1 =1, VSEL2 = VSEL3 = VSEL4 = 0	80	90	95	%
V_{TH-L}	Diagnostic low threshold at V_{OUT} = 18.15 V	VSEL4 =1, VSEL1 = VSEL2 = VSEL3 = 0	80	90	95	%

If the output voltage is lower than the min. value, the VMON I²C bit is set to 1.

If VMON=0 then V_{OUT} > 80% of V_{OUT} typical

If VMON=1 then V_{OUT} < 95% of V_{OUT} typical

Refer to *Section 5: "Typical application circuits"*, T_J from 0 to 85 °C, RSEL = 11.5 kΩ, DSQIN = low, V_{IN} = 12 V, unless otherwise stated. Typical values are referred to T_J = 25 °C. V_{OUT} = VOUT pin voltage. See *Section 6: "I²C bus interface"* and *Section 7: "I²C interface protocol"*.

Table 18: Output current diagnostic (IMON bit, status 2 register) characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{TH}	Minimum current diagnostic threshold	EN_IMON = 1 (V_{OUT} is set to 21 V typ.)	5	12	20	mA

If the output current is lower than the min. threshold limit, the IMON I²C bit is set to 1. If the output current is higher than the max. threshold limit, the IMON I²C bit is set to 0.

Refer to *Section 5: "Typical application circuits"*, T_J from 0 to 85 °C, all data 1..4 register bits set to “0” unless VSEL1 = 1, TEN =1, RSEL = 11.5 kΩ, DSQIN = high, V_{IN} = 12 V, I_{OUT} = 50 mA, unless otherwise stated. Typical values are referred to T_J = 25 °C. V_{OUT} = VOUT pin voltage. See *Section 6: "I²C bus interface"* and *Section 7: "I²C interface protocol"*.

Table 19: 22 kHz tone diagnostic (TMON bit, status 2 register) characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
A_{TH-L}	Amplitude diagnostic low threshold	DETIN pin AC coupled	200	300	400	mV
A_{TH-H}	Amplitude diagnostic high threshold	DETIN pin AC coupled	900	1100	1200	mV
F_{TH-L}	Frequency diagnostic low thresholds	DETIN pin AC coupled	13	16.5	20	kHz
F_{TH-H}	Frequency diagnostic high thresholds	DETIN pin AC coupled	24	29.5	38	kHz

If the 22 kHz tone parameters are lower or higher than the above limits, the TMON I²C bit is set to “1”.

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 QFN24L (4x4 mm) package information

Figure 13: QFN24L (4x4 mm) package outline

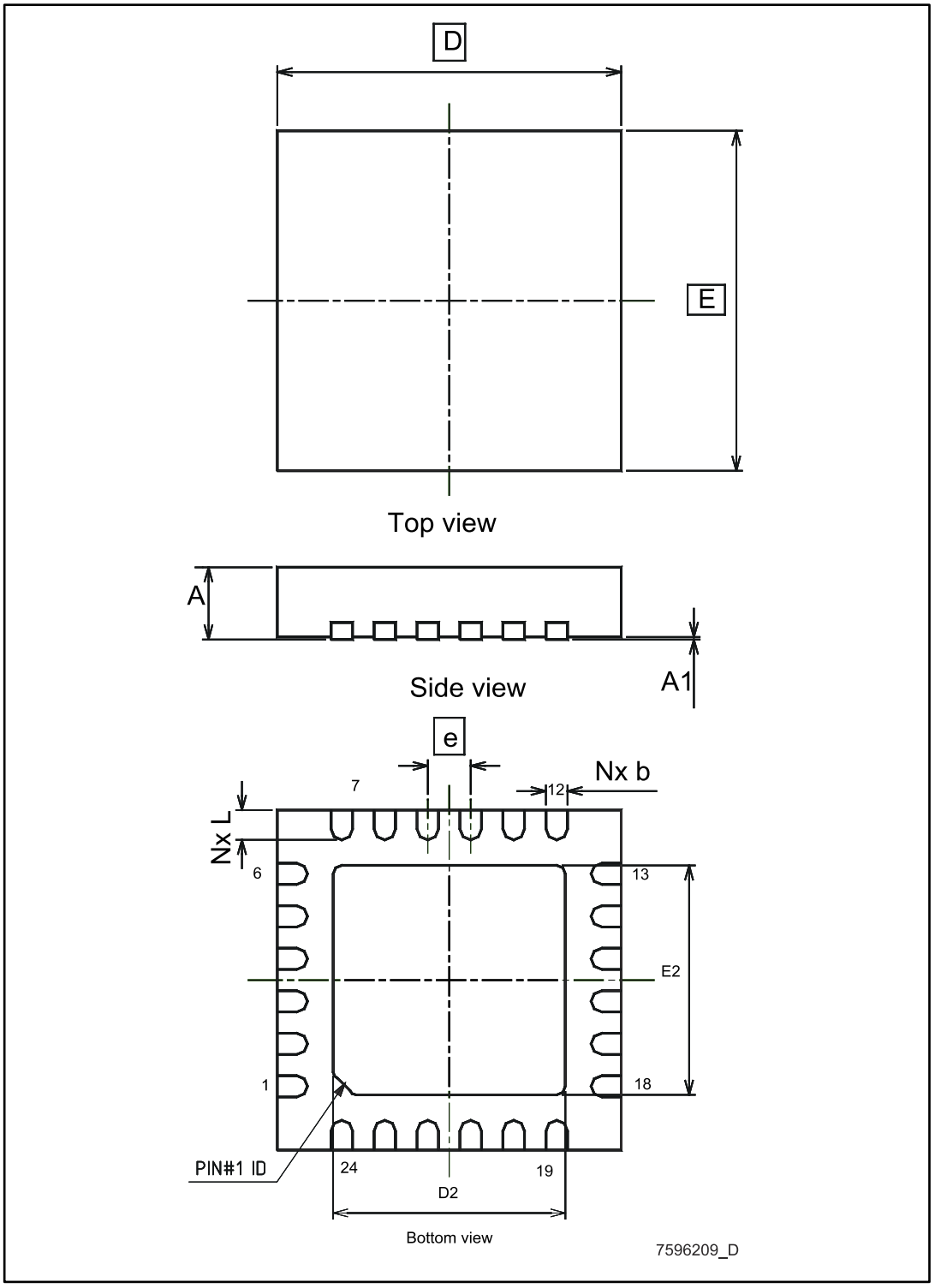
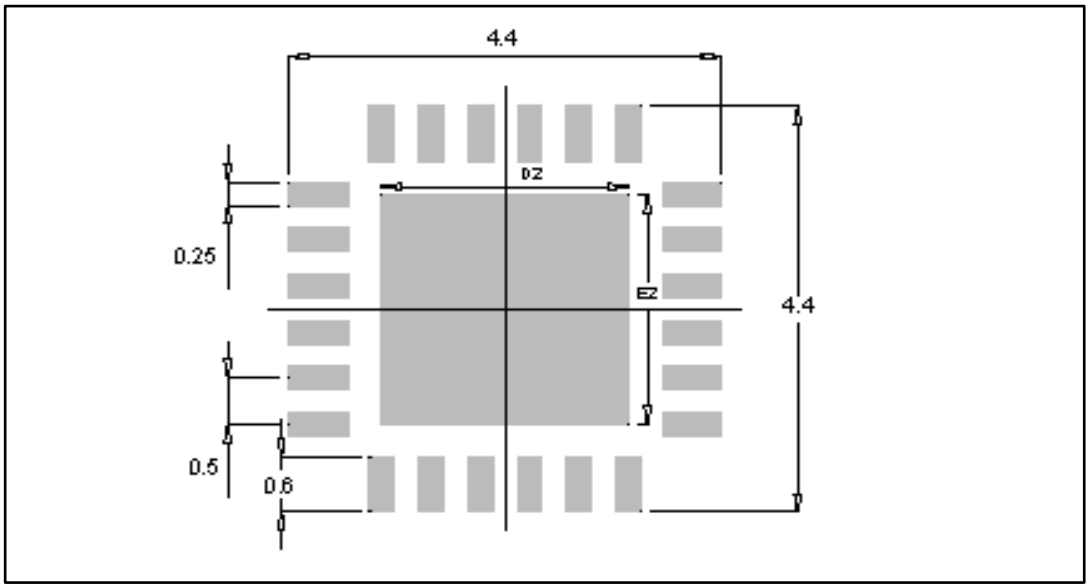


Table 20: QFN24L (4x4 mm) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D2	2.55	2.70	2.80
E	3.90	4.00	4.10
E2	2.55	2.70	2.80
e	0.45	0.50	0.55
L	0.25	0.35	0.40

Figure 14: QFN24L (4x4 mm) recommended footprint



10 Revision history

Table 21: Document revision history

Date	Revision	Changes
23-Jul-2014	1	Initial release.
24-Mar-2015	2	Updated *section 2.6*, *figure 5* and *table 13*.
26-Oct-2016	3	Updated *Figure 6: "DiSEqC 1.x application circuit"*

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