BGT24MTR11

User's Guide to BGT24MTR11

24 GHz Radar

Application Note AN305

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14	Calibration of temperature sensor added

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Table of Content

List of Figures

List of Tables

1 Introduction

This document provides supplementary information on how to use BGT24MTR11 that you may not completely find in the datasheet.

BGT24MTR11 is the lead product of Infineon's BGT24-series of 24 GHz radar transceiver products and serves here as an example for all BGT24 products in this application note. All building blocks of BGT24MTR11 described here can be found on the other two products, BGT24MTR12 and BGT24MR2 as well. The additional information in this application note is valid for these products as well.

2 Overview

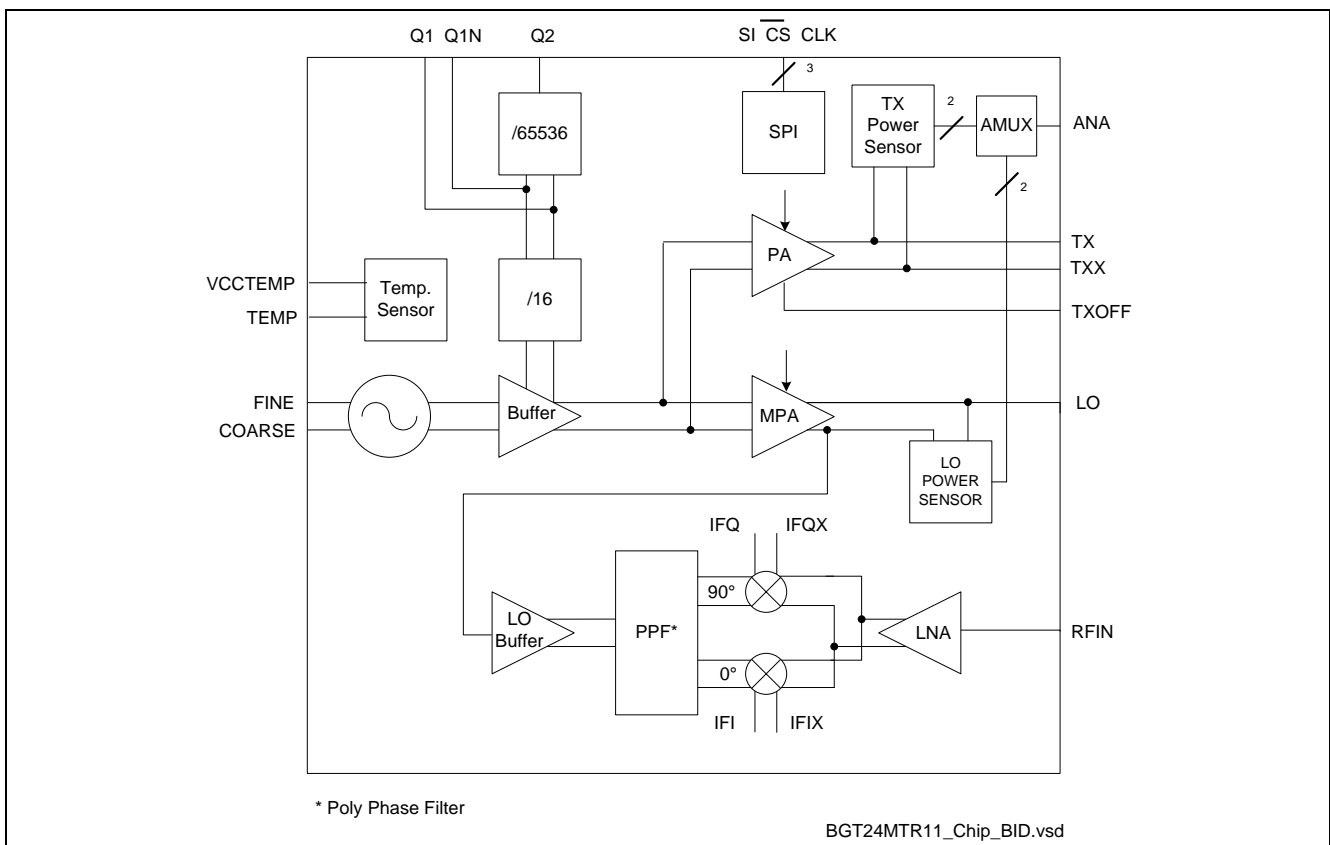The picture below shows the internal block diagram of BGT24MTR11.

Figure 1   BGT24MTR11 block diagram

The following sub-sections of the block diagram will be covered in this application note:
- Voltage controlled oscillator (VCO) and prescalers
- Transmitter chain including both TX and LO outputs
- Reciver chain including LNA and mixer
- On-chip sensors

3 VCO Section

BGT24MTR11's signal generation section consists of a free-running VCO with two separate tuning voltage inputs followed by a buffer amplifer to reduce frequency pulling effects. Two prescalers are available to monitor the frequency of oscillation. The first prescaler devides the transmitted frequency by 16, the second prescaler further reduces the output of the first one by a factor of 65536.

3.1 Tuning Voltage Inputs

BGT24MTR11 has two inputs for tuning the VCO's frequency of oscillation, FINE (pin 4) and COARSE (pin 5).

Both inputs can be used independently of each other to adjust the frequency output. As the pin names imply, COARSE has a steeper tuning slope compared to FINE.

If there is only one voltage available for tuning the VCO it is possible to connect both pins to this single voltage source. The resulting tuning sensitivity will be then the sum of the sensitivities of the respective pins.

Both tuning pins are connected internally via a pull-up resistor to Vcc. This means that when a pin is left open, it will be internally at Vcc. So if both pins are left open the oscillator will be around 26 GHz at room temperature.

Note: It is mandatory for each of the two pins to be at a voltage equal or higher than 0.5 V. If any voltage at the pins drops below that voltage level the oscillator will fail to work. This might lead to problems when starting a control loop and the loop's control output voltage at the start is below 0.5V. In this case some additional DC voltage needs to be present at the tuning inputs.

It is possible to cover the whole 24 GHz ISM band with tuning voltages between 0.5 V and 3.3 V - both over the device's specified temperature range and production related device variations.

Figure 2 shows the temperature behavior of the VCO. The measurement was conducted with both tuning pins, COARSE and FINE, connected together.
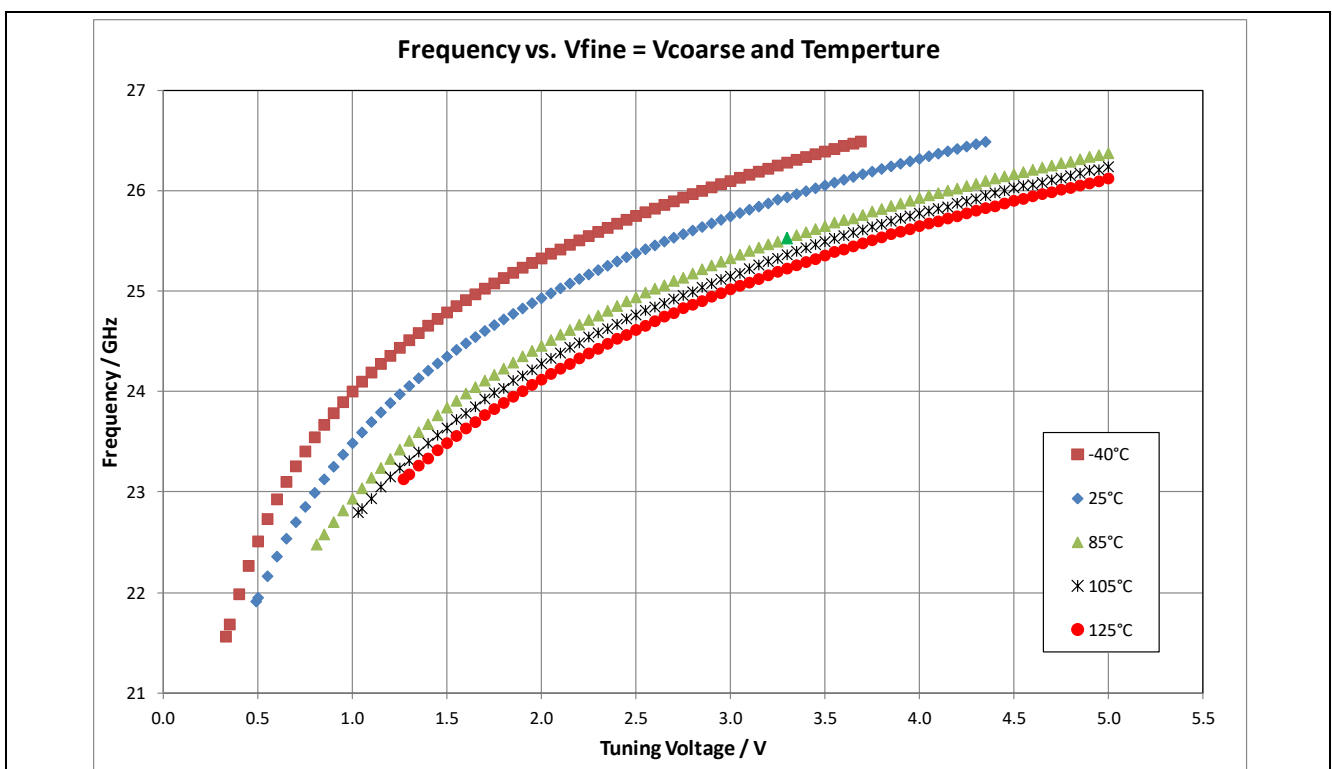

Figure 2 VCO frequency vs. tuning voltage $V_{FINE} = V_{COARSE}$ and temperature

Below are two graphs that show how the the frequency output of the oscillator behaves for different pairs of V_{COARSE} and V_{FINE}.
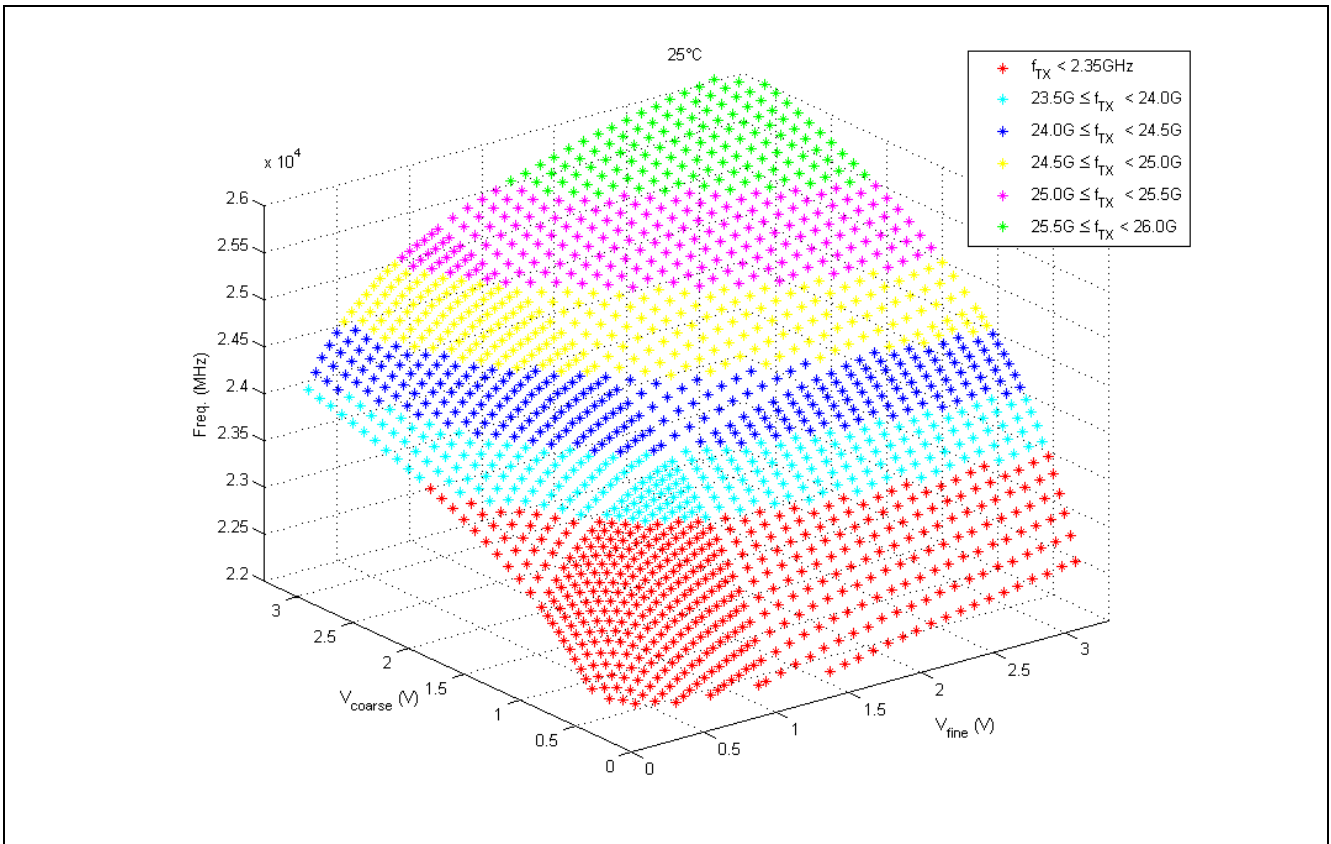
Figure 3   3D plot: Output frequency vs. V_{COARSE} and V_{FINE}
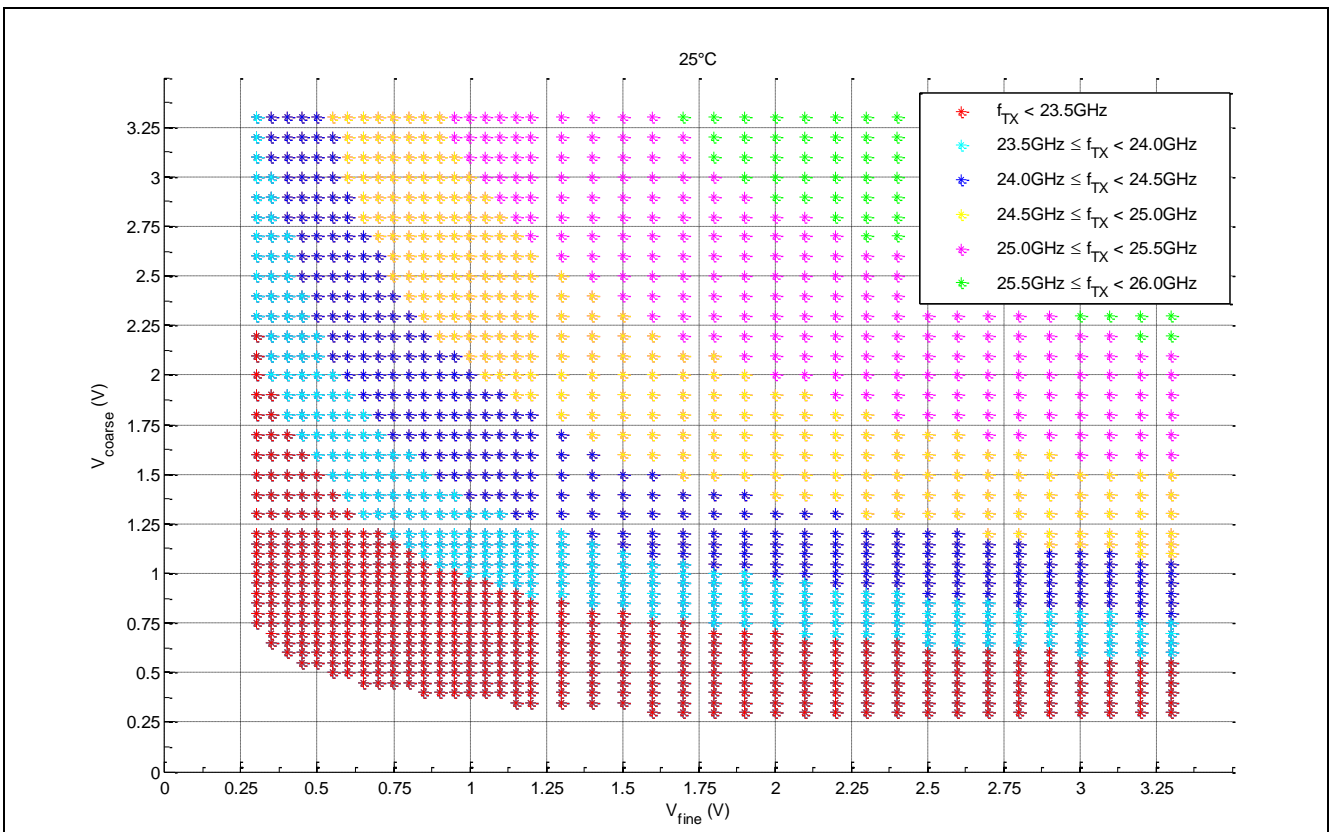

Figure 4   2D plot: Output voltage vs. V_{COARSE} and V_{FINE}

3.2   Prescalers

BGT24MTR11 has two cascaded built-in prescalers. The first prescaler divides the oscillator's frequency by 16, the second reduces the output of the first one by the factor of 65536 – resulting in a total division factor of 1,048,576.

3.2.1   Divide-by-16 Prescaler

This first prescaler divides the VCO's frequency of oscillation by the factor of 16. So at a given VCO frequency of 24 GHz the prescaler's output frequency is 1.5 GHz. This is a convenient frequency to feed into RF-PLLs.

The output frequency is fed differentially to pins 31 and 1 (Q1, Q1N). The differential port impedance is 100 Ω.

Note: For proper operation of the prescaler both output pins need to be terminated by 50 Ω. As there is DC present at the two output pins a coupling capacitor will be necessary if the termination does not have a DC-blocking circuit already implemented, (e.g. a blocking capacitor at a PLL's input).

In case a PLL does not support differential inputs it is possible to use any of the two outputs and terminate the unused one.
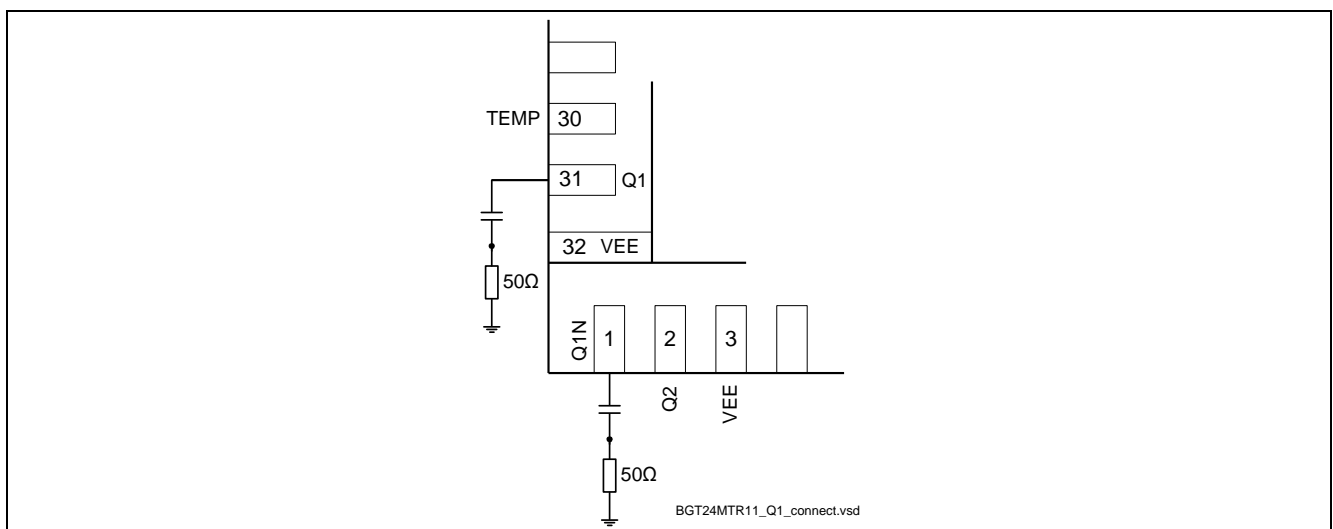
Figure 5   Termination of Div16 outputs

This prescaler may be disabled by setting SPI data bit 5 (DIS_DIV16) to HIGH.

3.2.2   Divide-by-65536 Prescaler

This prescaler is fed by the divide-by-16 prescaler's output frequency and reduces it furtherly by the factor of 65536 resulting in a total reduction factor of 1,048,576. This means a 24 GHz VCO signal will result in an output square wave signal of approximately 23 kHz at pin 2 (Q2).

This 23 kHz output signal can be monitored via a microcontroller's timer input, for example, and then be used together with the microcontrollers DAC or PWM output to create a software loop to control the VCO's output frequency.

Note: For proper operation of this prescaler it is mandatory that the divide-by-16 prescaler is enabled. Otherwise the divide-by-65536 will not get an input signal and will produce false output.

This prescaler may be disabled by setting SPI data bit 6 (DIS_DIV64k) to HIGH.

4 Transmitter Section

This chapter describes the functionalities of the main power amplifier (PA in the block diagram) that provides the ouput for transmitting the actual radar signal at the TX output as well as the medium power amplifier (MPA) that provides the signal at the LO output.

4.1 TX Section

The TX output signal is provided via TX and TXX pins (pin 22 and 23). It is a differential output signal with a load impedance of 100 Ω, given that the off-chip compensation structures, shown in the data sheet, are in place.

Ideally the TX outputs can be used directly with an antenna that has differential 100 Ω inputs. In case of single-ended antennas it will be necessary to use a balun. If the antenna is single-ended 50 Ω then there is also the option to terminate one of the TX outputs with 50 Ω and use the other one directly as a 50 Ω output port. However, this will reduce the available output power by 3 dB.

Note: It is not recommended to create a 100 Ω single-ended output signal by grounding one of the TX pins.

The TX output power level can be adjusted via settings in the SPI data register as shown in the table below.

Table 1   Output power reduction

SPI Data Register			Reduction of output power relative to maximum output power / dB
Bit 2	Bit 1	Bit 0	
0	0	0	0
0	0	1	0.4
0	1	0	0.8
0	1	1	1.4
1	0	0	2.5
1	0	1	4
1	1	0	6
1	1	1	9

To mitigate the roll-off of output power at high temperatures it is possible to set SPI data bit 3 (PC1_BUF, High TX buffer output power) to HIGH. This buffer is not explicitily shown in the block diagram in Figure 1 on page 5. At room temperature there is only an increase of 0.2 dB in the maximum TX output power.

Output power plotted versus frequency for different temperatures can be found in the figure below. The TX buffer was in high output power mode during this measurement.
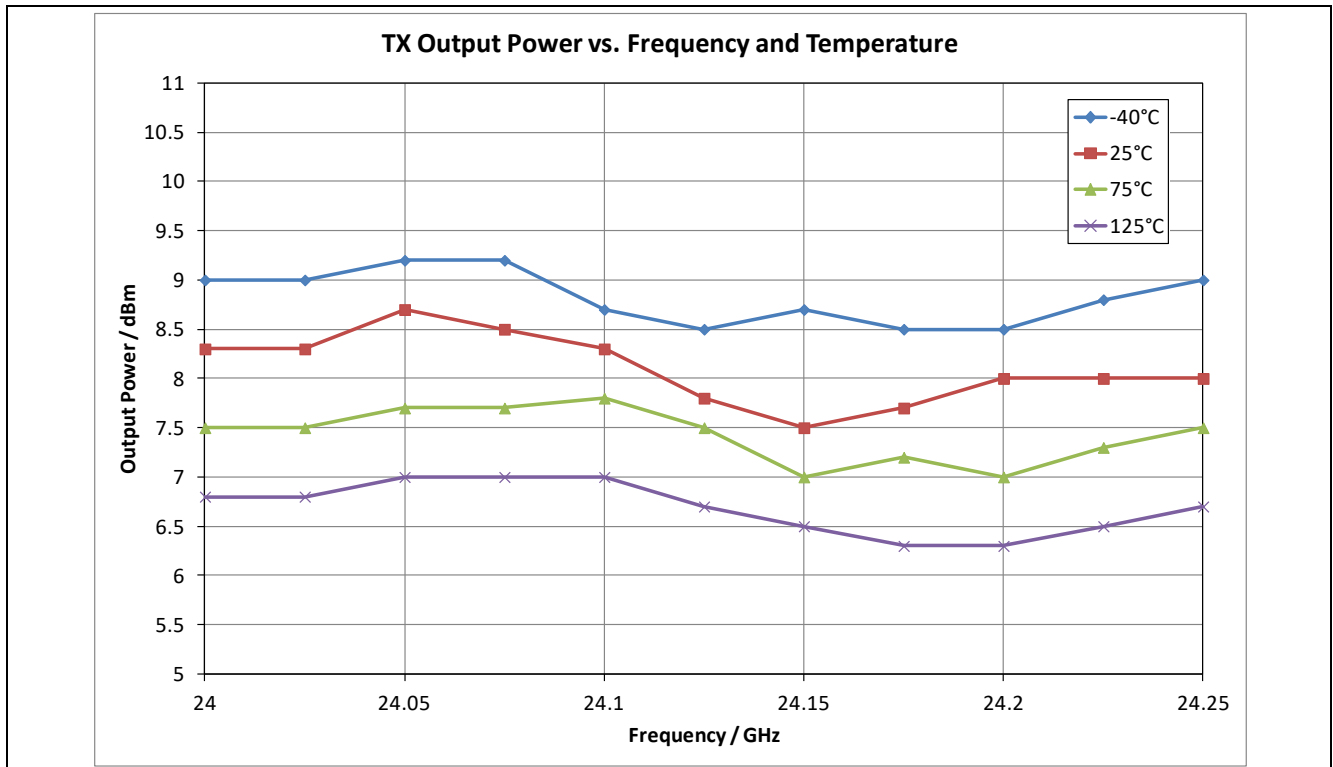
Figure 6   TX output power vs. frequency for different temperatures

4.1.1   Enabling and Disabling of the Output Power

The TX outputs are disabled by default after powering-up the IC. This is to make sure that the output frequency can be stabilized before actually transmitting a signal.

Note: Disabling the TX outputs will not reduce power consumption as all IC-internal blocks will still be running. TX outputs are switched to an internal load when disabled. This keeps the power dissipation at a constant level and therefore keeps the chip temperature constant. Abrupt changes in temperature would cause the VCO's frequency to jump to a different value which might lead to violation of the band limits before the frequency control loop can re-lock the frequency again.

There are two possibilities to turn on and off the TX ouput power. The first is via the SPI bus and the second is using the TXOFF pin.

4.1.1.1   Enabling/disabling via the SPI bus.

To enable the power output SPI data bit 12 (DIS_PA) needs to be set to LOW and to disable the power it needs to be set to HIGH. If you use this method, please connect the TXOFF pin to ground.

4.1.1.2   Enabling/disabling via the TXOFF pin.

Using the TXOFF pin (pin 26) for swiching on/off or generating transmit pulses allow considerably shorter switching times compared to using the SPI bus.

In this mode it is necessary to first set SPI data bit 12 to LOW and thus generally activating the TX outputs. After that applying a voltage below 0.5 V to TXOFF will enable the TX outputs and a voltage higher than 1.5 V will disable the TX outputs.

4.2   LO Section

BGT24MTR11 was designed to be used in monostatic radars. These radars are only capable of detecting a target's distance and speed, but not the angle of the target's position relative to the antenna. It is possible, though, to determine this angle when using additional RX-antennas and receiver chains. In this case the BGT24MR2 offers two additional receiver chains in one package to build a system with three RX-antennas. These external receiver chains need a local oscillator input which can be taken from BGT24MTR11's LO output (LO, pin 28).

In case the system needs one TX channel and two RX channels, Infineon offers BGT24MTR12 as a completely integrated device especially for that application.

The LO pin may also be used as an alternative TX output in case the minimum TX output power is still too high for the intended application. It must be noted, however, that the LO output can not be disabled unlike the TX output.

If the proposed off-chip compensation structures described in the datasheet are implemented, the LO output has a load impedance of 50 Ω.

The typical output power of the LO pin is 0 dBm if the LO buffer is set to high output power mode. This can be done by setting bit 4 (PC2_BUF) of the SPI register to HIGH. In low output power mode the output power is reduced by 3.5 dB.

In case the LO output is not required, this pin can be left open.

5   Receiver Section

BGT24MTR11's receiver section consists of two major blocks, the low noise amplifer (LNA) and the mixer.

5.1   Low Noise Amplifier

The LNA has a single-ended RF input with a port impedance of 50 Ω, provided that the suggested off-chip compensation structures are present on the PCB.

It is possible to reduce the LNA's gain by setting SPI data bit 15 (GS) to high. The gain is then reduced by 6 dB.

5.2   Mixer and IF Output Stages

BGT24MTR11 features a homodyne quadrature downconversion mixer. RF input is provided by the LNA and the LO signal is taken from the VCO's output, isolated by a buffer amplifier. A RC polyphase filter is used for LO quadrature phase generation.

The mixer converts the 24 GHz signals directly down to zero-IF and offers differential in-phase and quadrature IF output signals. Each port has an impedance of 800 Ω. and may be connected directly to loads greater than 10 kΩ . Low ohmic loads need to have a coupling capacitor in place as there is a DC voltage of typically 2.3 V present at each IF-output.

This value can easily be checked by disabling the TX output as the chip internal TX to RX leakage and LO to RX leakage is very small. Once the TX output is enabled self-mixing effects due to TX-RX coupling outside the IC might occur resulting in DC offsets in the range ±0.2 V.

Self-mixing effects are strongly related to the layout of the PCB and are frequency dependend.

6 Sensors

BGT24MTR11 has three built in sensors for measuring TX-power, LO-power and chip temperature

All three sensors offer their readings via analog output voltages, which can be accessed via a multiplexer that connects the single output voltages to the ANA pin (pin 25).

The table below shows which bits in the SPI data register need to be set to select the different sensor readings at ANA.

Table 2 *Truth table for analog multiplexer*

Output signal at ANA	AMUX2 (bit 11)	AMUX1 (bit 8)	AMUX0 (bit 7)
$P_{OUT,TX}$	low	low	low
$P_{REF,TX}$	low	low	high
$P_{OUT,LO}$	low	high	low
$P_{REF,LO}$	low	high	high
V_{TEMP}	high	low	low

6.1 Power Sensors

For output power measurement, peak voltage detectors are connected to the output of the TX power amplifier and to the LO medium power amplifier. To eliminate temperature and supply voltage variations, a reference output voltage V_{REF} is available through the ANA output for the TX and LO power sensor. The compensated detector output voltage is given by the difference between V_{OUT} and V_{REF} for both power sensors. This voltage difference is proportional to the RF voltage swing at the individual amplifier outputs, its characteristic is non-directional.

Note: The actual voltage output of the power sensors is strongly dependant on the terminations of the amplifier outputs since the power sensors are actually peak voltage detectors.
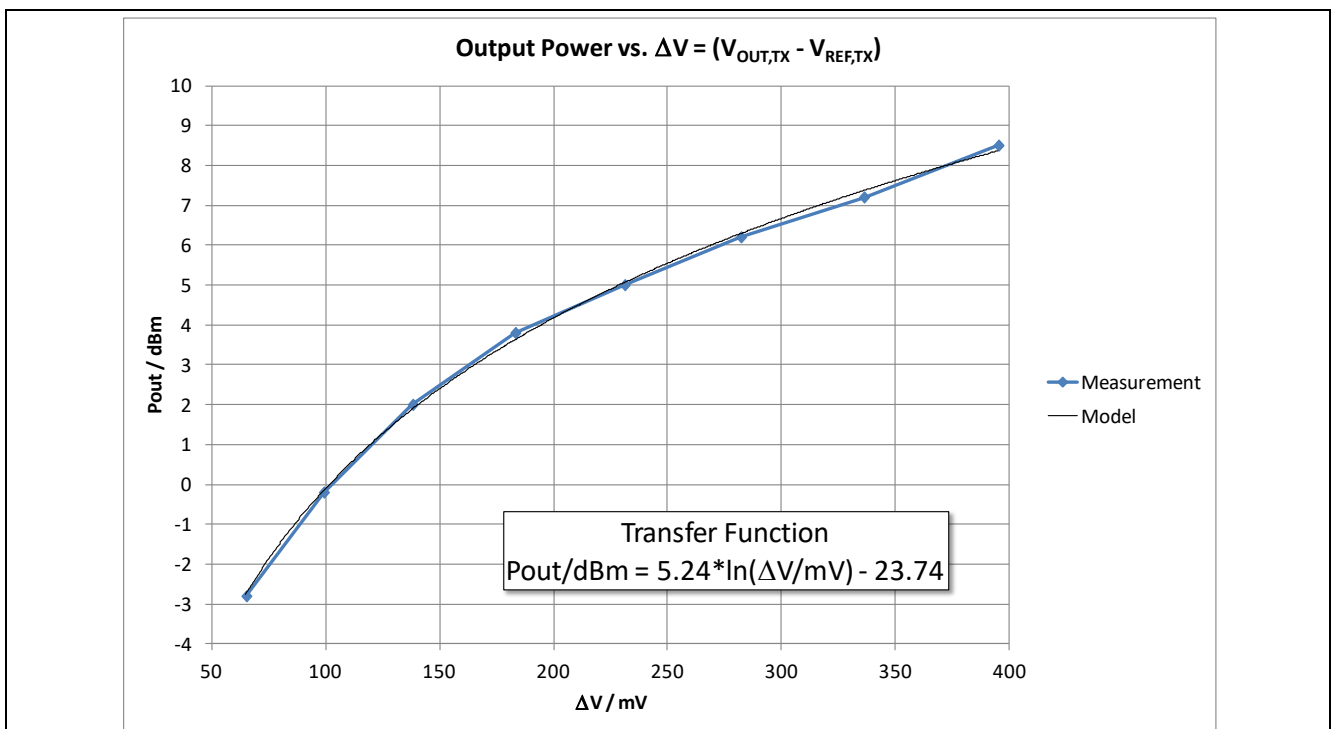
Output Power vs. $\Delta V = (V_{OUT,TX} - V_{REF,TX})$

Transfer Function
Pout/dBm = 5.24*ln(ΔV/mV) - 23.74

Figure 7 **Transfer characteristics of power sensors**

6.2 Temperature Sensor

Monitoring of the chip temperature is provided by the on-chip temperature sensor which delivers a temperature-proportional voltage to the TEMP output pin (pin 30). Alternatively the output voltage can be read out via the analog multiplexer output ANA (pin 25). The temperature sensor can be independently biased through VCCTEMP (pin 29). This makes it possible to measure the chip temperature while the main supply of the transceiver is switched off.
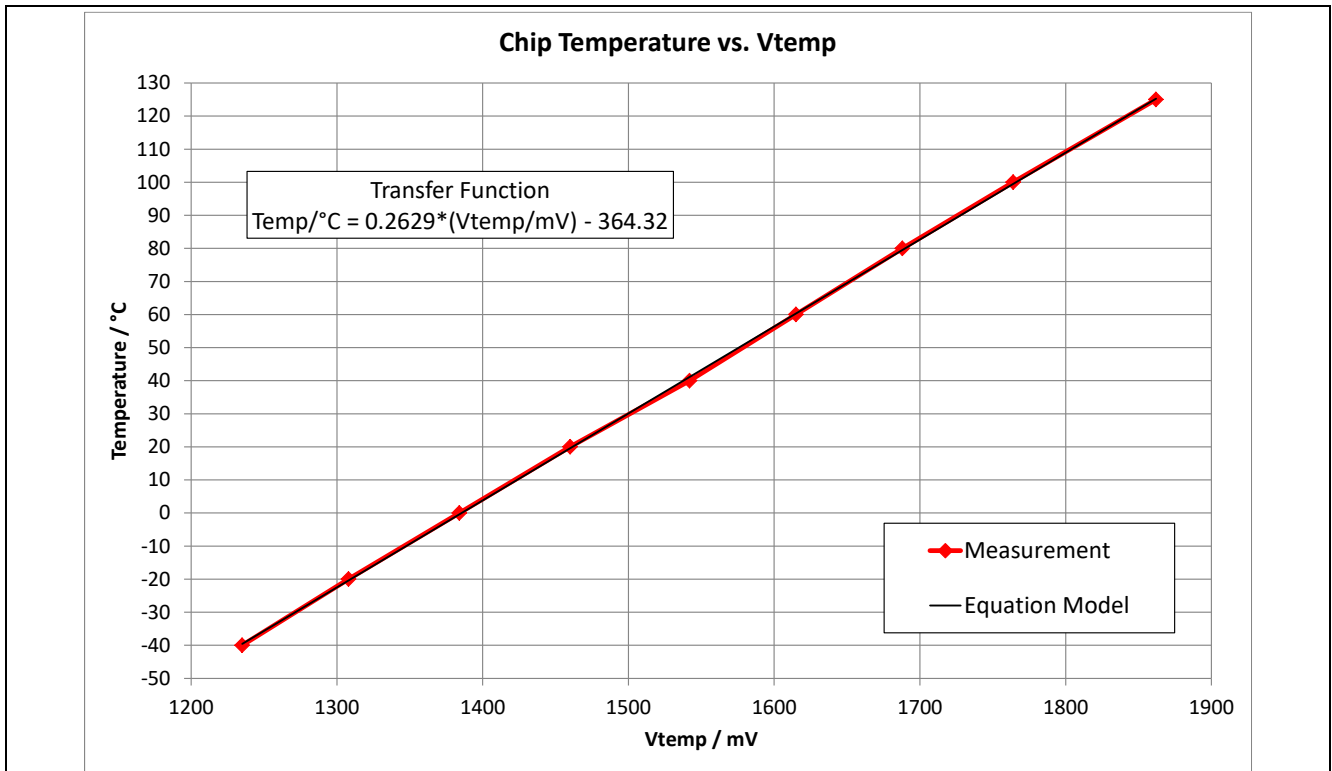

Figure 8 **Uncalibrated transfer characteristic of a random device's temperature sensor**

Figure 8 displays the uncalibrated transfer characteristics of the temperature sensor and a formula to calculate the chip temperature from the measured output voltage. Gradient and offset of the transfer function fit well to the values given in the data sheet.

This measurement was done by biasing only the temperature sensor. As the temperature sensor draws only 2 mA there is very little power dissipation in the chip and the chip temperature may be considered to be the same as the ambient temperature or board temperature can actually be controlled during the measurement.

Under normal operation the chip temperature will be higher compared to the ambient temperature because the chip's power dissipation is considerably higher in this case. The power dissipation is not fixed as the current consumption of the chip is depending on how it was configured to operate. Additionally the ratio chip temperature to ambient temperature is strongly influenced on how PCB was designed.

Note: In order to obtain temperature readings that are within the limits stated in the datasheet, it is necessary to calibrate the temperature sensor. This will remove chip-to-chip offsets, as well as effects due to the PCB design.

6.2.1 Calibrating the temperature sensor

As stated in the section before, it is necessary to perform a calibration of the temperature sensor of every single chip to get the accuracy specified in the datasheet:

- Measure the sensors output V_{cal} at a known temperature T_{cal}
- Use this value pair (V_{cal}, T_{cal}) as a fix point for the voltage-temperature reference curve
- Extrapolate a line through this point with a gradient of 0.22 K/mV to get the final voltage-temperature reference curve
- In order to get the accuracy specified in the datasheet it is necessary that the measurement uncertainty of T_{cal} is below ±6K.
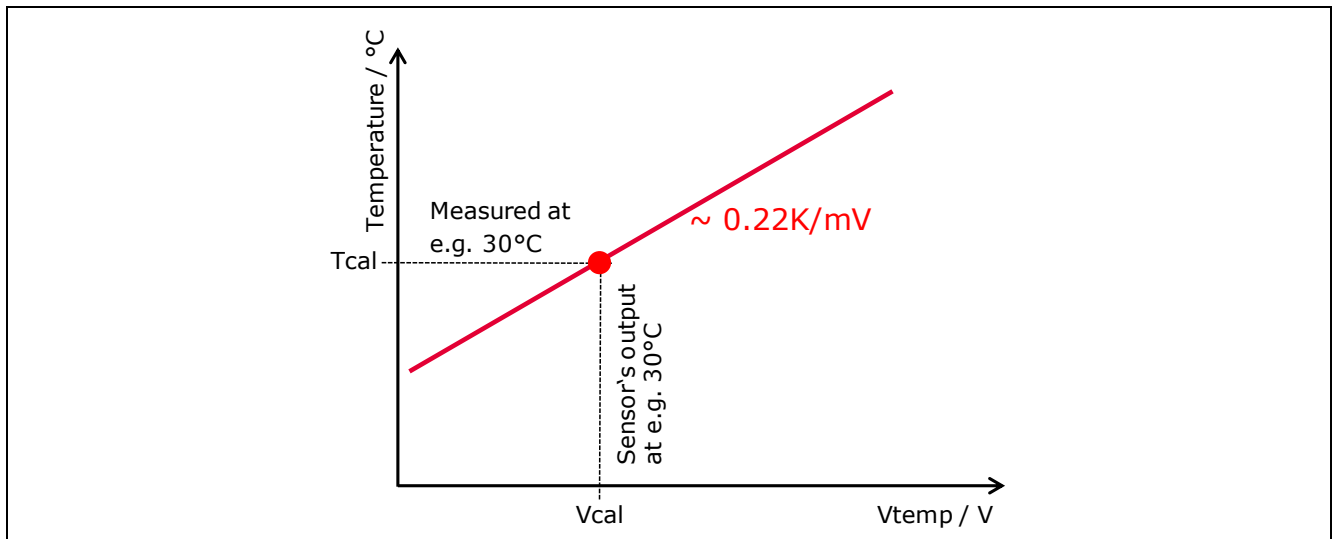

Figure 9   Calibration of temperature sensor.

Authors

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