



Tsi382 (LQFP)[™] Evaluation Board User Manual

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About this Document

This document describes how to test the key features of the Tsi382 (LQFP) using the Tsi382 (LQFP) evaluation board. It can be used in conjunction with the *Tsi382 (LQFP) Evaluation Board Schematics*.

Related Information

- *Tsi382 User Manual*
- *Tsi382 (LQFP) Evaluation Board Schematics*
- *Tsi382 Board Design Guidelines*
- *PCI Express Base Specification (Revision 1.1)*
- *PCI Express CEM Specification (Revision 1.1)*
- *PCI Express-to-PCI/PCI-X Bridge Specification (Revision 1.0)*

Terms

| Term | Definition |
|--------|----------------------|
| PCIe | PCI Express |
| SerDes | Serial/De-serializer |

Revision History

60E2020_MA001_02, Formal, September 2009

This document was rebranded as IDT. It does not include any technical changes.

60E2020_MA001_01, Formal, June 2008

This is the first version of the *Tsi382 PCIe-to-PCI Bridge User Manual*.

1. Board Design

Topics discussed include the following:

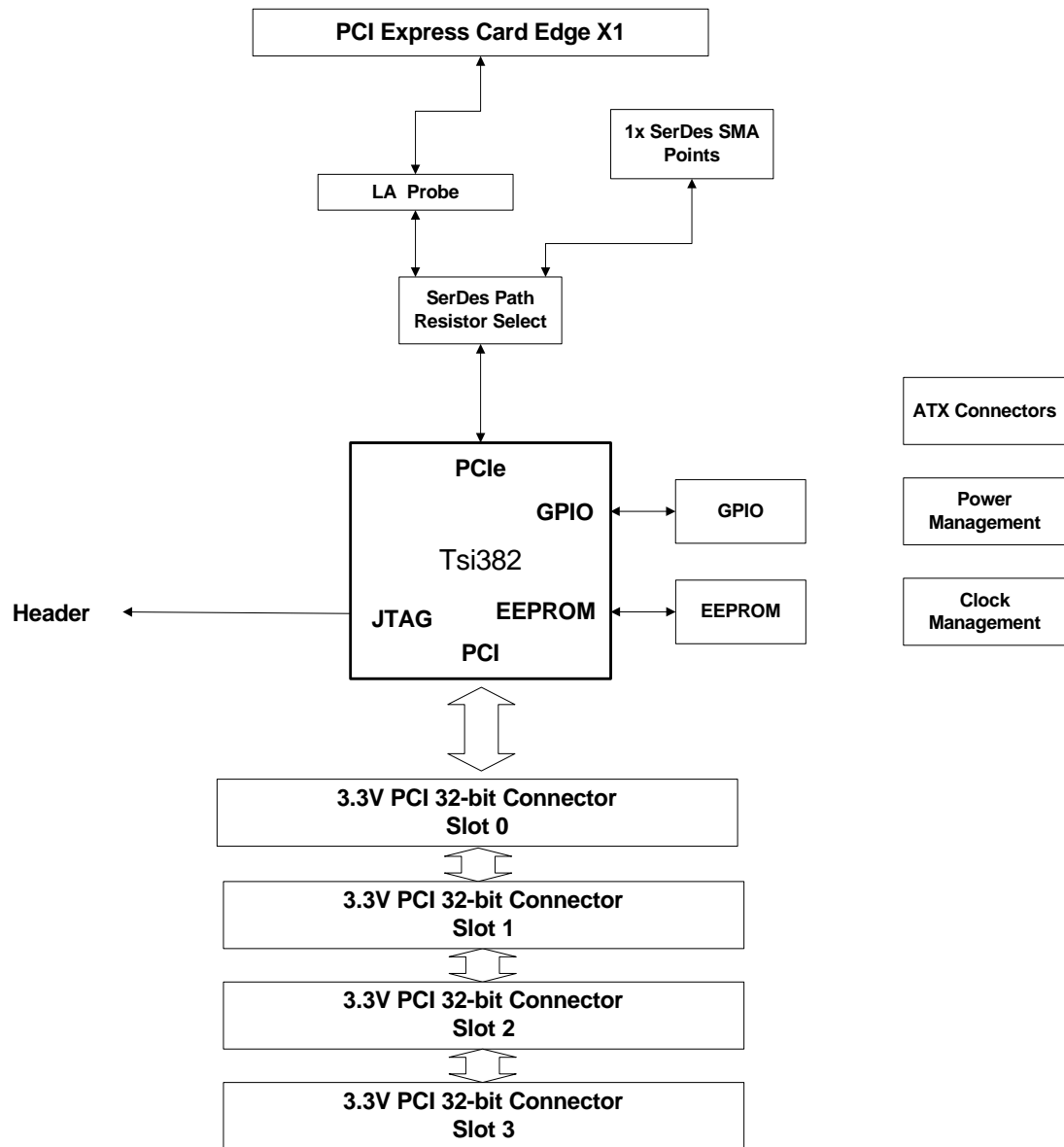
- “Overview” on page 7
- “PCI Interface” on page 9
- “PCIe Interface” on page 10
- “Power Management” on page 10
- “Clock Management” on page 14
- “Other Interfaces” on page 15
- “Hardware Reset” on page 16
- “Logic Analyzer Connectivity” on page 17

1.1 Overview

The key features of the Tsi382 evaluation board include the following (see also [Figure 1](#)):

- Single x1 lane, 2.5 Gbps PCIe 1.1 compatible riser card (extended height form factor)
- Four PCI slots
- 32-bit PCI bus, 25–66 MHz operation
- PCI power support through system or external supply
- PCIe compliance/debugging test points

Figure 1: Evaluation Board Block Diagram



1.2 PCI Interface

1.2.1 Overview

The PCI Interface is implemented on the board with four slots, in which one is an R/A mounted connector on the top of the board. All PCI connectors are compliant with the PCI 3.0 specification. Appropriate clearance is provided such that up to four PCI cards can be inserted for testing while the board is in an open-chassis standard ATX case.

The PCI Interface supports four slots operating at 25, 33, 50, or 66 MHz.

1.2.2 IDSEL Signals

IDSEL signals are connected in the following order:

- Slot 0 – R/A connector top slot: 150 ohms to AD16 (Device 0)
- Slot 1 – 150 ohms to AD17 (Device 1)
- Slot 2 – 150 ohms to AD19 (Device 3)
- Slot 3 – 150 ohms AD18 (Device 2)

1.2.3 Interrupt Signals

The PCI interrupt signals are connected to the slots as shown in the following table.

Table 1: PCI Interrupt Routing

| Tsi382 | Slot 0 | Slot 1 | Slot 3 | Slot 4 |
|--------|--------|--------|--------|--------|
| A | A | B | D | C |
| B | B | C | A | D |
| C | C | D | B | A |
| D | D | A | C | B |

1.2.4 Pull-up Signals

The following pull-ups are added to the PCI bus, in which a value of 8.2Kohm is used.

Table 2: PCI Pull-up Signals

| Signal | Description |
|----------------------|----------------|
| PCI_REQ#[0:3] | Bus request |
| PCI_GNT#[0:3] | Bus grant |
| PCI_FRAME# | Control signal |
| PCI_IRDY#, PCI_TRDY# | Control signal |

Table 2: PCI Pull-up Signals (Continued)

| Signal | Description |
|---------------|-------------------------------------|
| PCI_STOP# | Control signal |
| PCI_SERR# | System error |
| PCI_PERR# | Parity error |
| PCI_DEVSEL# | Device select line |
| PCI_INT#[A:D] | Interrupt line |
| PCI_PME# | PCI Power Management Event occurred |

1.3 PCIe Interface

The Tsi382 evaluation board implements a single lane PCIe Interface. It is designed to connect to a PCIe system with a standard x1 finger connector. The system must provide the REFCLK and PERSTN signals. The PCIe Interface has the following design elements:

- Supports hot insertion and removal
- Mid-bus logic analyzer pads for PCIe RXD/TXD signal probing
- AC coupling on the TXD lanes
- JTAG TDI - TDO loopback for chain continuity



The PCIE_REXT signal must be tied to ground through a 190-ohm resistor.

1.4 Power Management

1.4.1 Power Regulation

The evaluation board's power regulation is implemented as follows:

- Digital 3.3V power supply available from DC/DC regulator or ATX supply
- Digital 1.2V switching regulator
- PCIe supplies filtered using EMI ferrite networks

To support PCI cards, the following additional power resources are included:

- 12V to 5V DC/DC converter
- 12V to 3.3V DC/DC converter
- External power connectors – ATX 20-pin connector for supplying all power from an ATX power supply

1.4.2 Power Requirements

The power requirements and implementation for the Tsi382 is as follows.

Table 3: Tsi382 Power Requirements

| Supply Name | Symbol | Supplied Source |
|------------------|------------|---|
| Device Core | 1.2V_384 | DC/DC switching regulator w/Enable pin |
| PCIe 1.2V Core | 1.2V_A_384 | Passive Filter |
| PCI 3.3V supply | 3.3V_384 | Power switch w optional Ferrite filter to reduce EMI/noise from PCI environment |
| PCIe 3.3V supply | 3.3V_A_384 | Passive Filter |

The target power draw of the Tsi382 is a maximum of 1W, all supplies combined. The supplies to the Tsi382 are controlled during ramp up using enable pins on regulators and switches.

1.4.2.1 PCIe

The *PCIe CEM Specification 1.1* defines power limits on PCIe slots according to the number of lanes available on a card. Power rules regarding x1 PCIe slots are a maximum of 25W slot. Current limits are included in [Table 4](#).

Table 4: PCIe Connector Current Limits

| Rail | Current |
|------|---------|
| 3.3V | 3A |
| 12V | 2.1A |

The usage of the 12V supply provides access to the full 25W available from the system to the board. The PCIe pinout design includes more 12V power pins as it allows more power-per-pin capability. The evaluation board regulates all power from the 12V system rail; however, 3.3V from the system remains unused.

1.4.2.2 PCI

The PCISIG defines the power rules regarding PCI cards as a maximum of 25 Watts per card (All power rails combined power draw). The individual current limits on voltage rails are included in [Table 5](#).

Table 5: PCI Connector Current Limits

| Rail | Current |
|------|---------|
| 3.3V | 7.6a |
| 5V | 5a |
| -12V | 100ma |
| 12V | 500ma |

It is not possible to provide the full power required to the PCI bus without violating the specification while drawing power from only a x1 PCIe system. Up to 23W not including regulator efficiency losses can be made available. The evaluation board provides the power requirements in one of two ways depending on the application:

- PCIe system power
- ATX System connector

The following conditions summarize the power available for a single PCI card without external supply. An efficiency of 85% is taken into account for switching regulators. These limits can be exceeded in cases where the system can provide more than the suggested limit, which is usually only implemented in hot swap systems.

Table 6: PCI Connector Current Limit with No External Supply

| Rail | Supplying Topology | Current (Maximum) |
|------|-----------------------|-------------------|
| 3.3V | 12V to 3.3V regulator | 6A |
| 12V | 12V directly | 500mA |
| -12V | N/A | N/A |
| 5V | 12V to 5V regulator | 4A |

For additional slots, or in cases where the system cannot supply enough power, a separate ATX power connector is used to power the card. The evaluation board senses the presence of this supply, and disables the slave PCIe slot power. For the case of a separate external ATX supply, all four slots are provided with the required power.

1.4.3 Power Sequencing

On power-up, the board's power sequence is as follows:

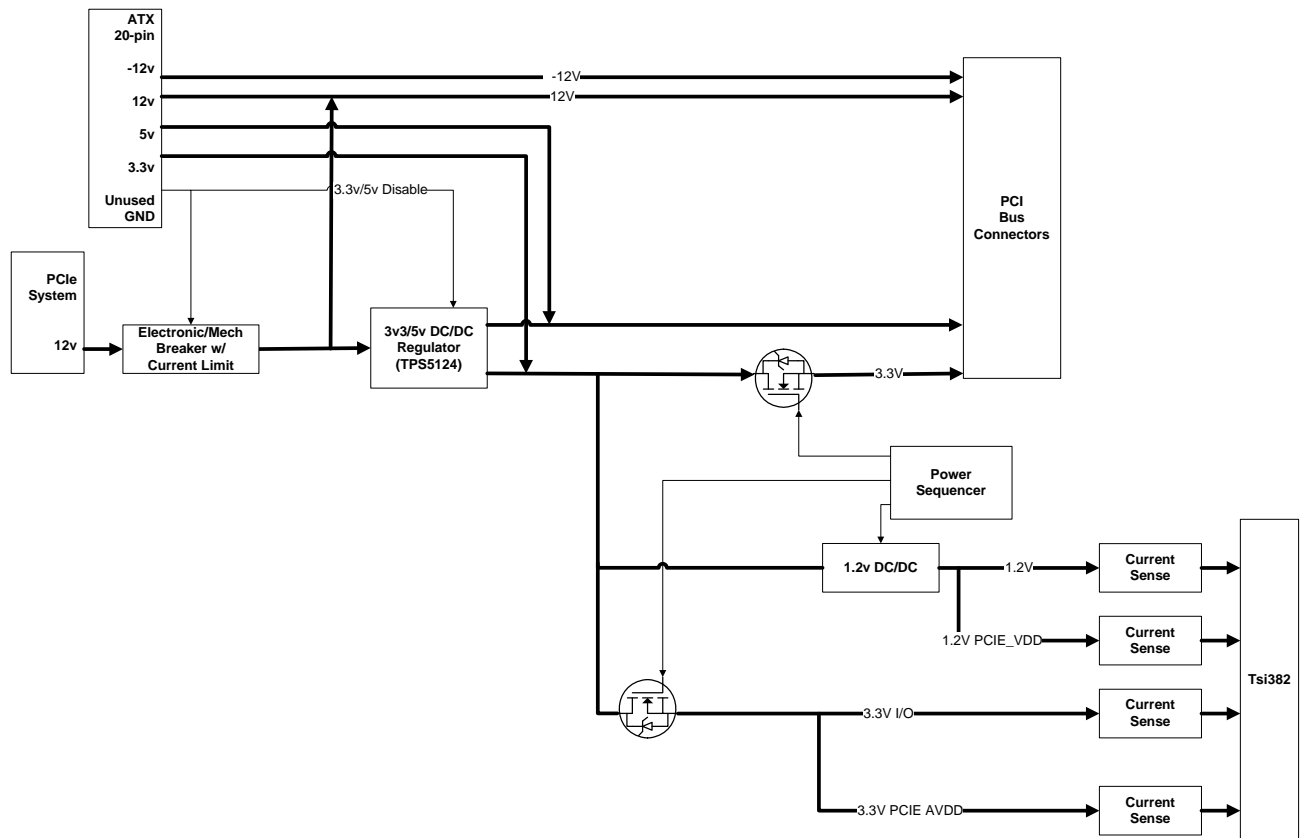
1. 1.2V powered on
 2. PCI I/O slot power and pull-ups, and Tsi382 3.3V
- 12V/-12V/5V PCI are not sequence controlled.

1.4.4 System Power Design

Figure 2 illustrates the power distribution for the riser card. The following list is a functional summary of the power design:

1. Sequencing control over the following rails:
 - 3.3V PCI
 - 3.3V Tsi382 I/O/PCIe A_{VDD}
 - 1.2V Tsi382 Core/PCIe V_{DD}
2. ATX 20-pin connector override, which disables all power draw from the PCIe system.

Figure 2: System Power Distribution



1.4.5 PCI Vaux (PCI Auxiliary) Support

PCI connectors are provided with a 3.3V supply to the vaux pins only during operation. There is no support for this power supply in standby mode. This feature is not documented in the Tsi382 evaluation board schematic.

1.5 Clock Management

The Tsi382 requires up to two input clocks to operate:

- 25–66 MHz clock for PCI
- 100-MHz reference clock for PCIe

The PCI and PCIe input clocks are briefly discussed.



The Tsi382 supports five PCI clock outputs, PCI_CLKO[0:4]. The Tsi382 evaluation board demonstrates only PCI_CLKO[0:1].

1.5.1 PCI

The evaluation board supports master and slave clocking for PCI.

- Master – When in master mode, the Tsi382 generates the required PCI clock for all slots.
- Slave – When in slave mode, an on-board selectable 25–66 MHz clock generator is used.

On-board resistor muxes are used to multiplex either Tsi382's PCI clock or the external clock generator.

1.5.1.1 PCIe

For PCIe clocking, a 100-MHz differential HCSL clock source is required. The clock source is available in two forms:

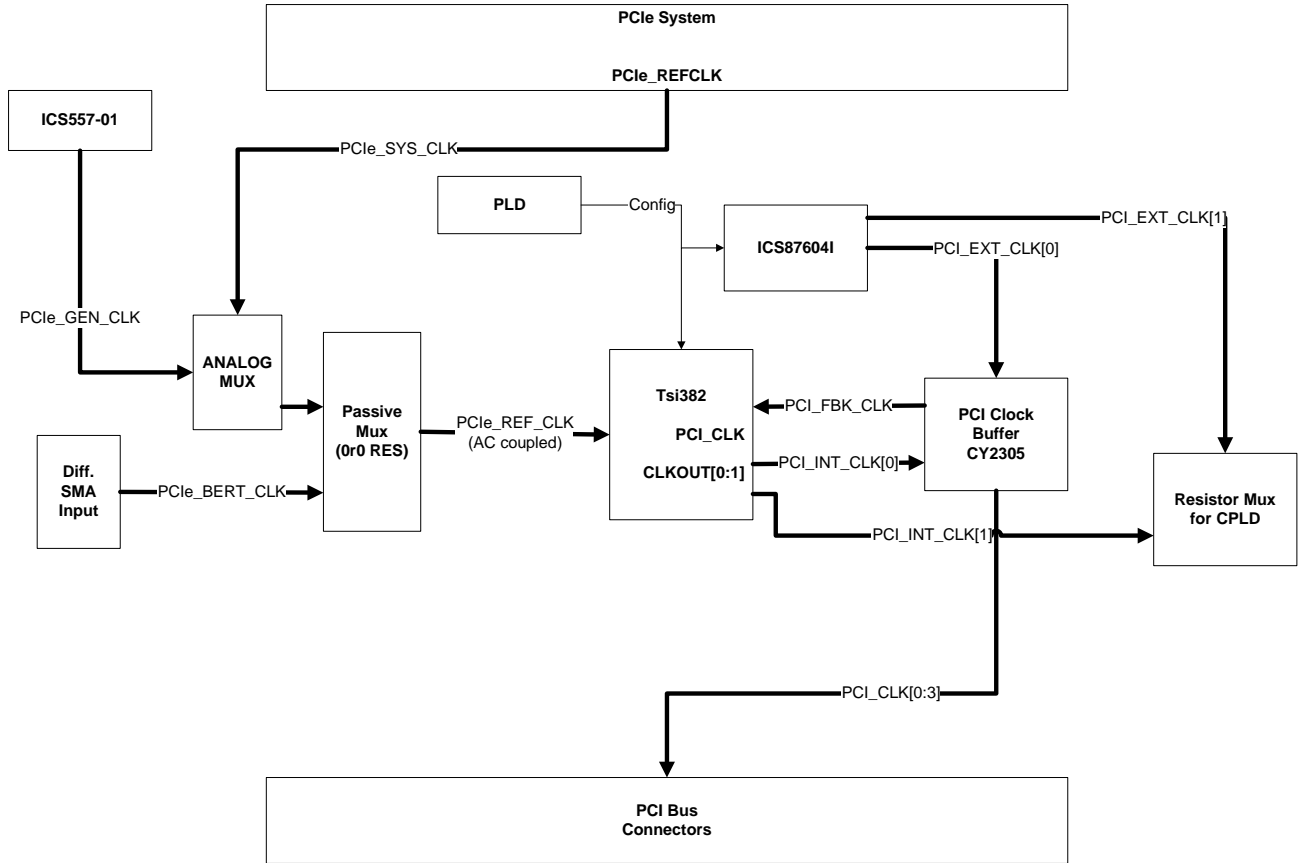
- Edge connector clock source – This clock source synchronizes the system SerDes with the Tsi382.
- On-board 100-MHz reference – This clock source can separate the clock domains between the bridge and the root complex.

The two PCIe clock sources are multiplexed with an analog multiplexer to select between the system clock or on-board clock (see [Figure 3](#)).

1.5.2 System Clock Distribution

The following figure shows the distribution of the system clock on the Tsi382 evaluation board.

Figure 3: System Clock Distribution



1.6 Other Interfaces

1.6.1 JTAG Interface

To support debug and testing of device, JTAG access to the Tsi382 is available using a standard JTAG header for Wiggler connection.



For more information about accessing the Tsi382 using JTAG, see the *JTAG Register Access Software Application Note*.

1.6.2 EEPROM Interface

A single EEPROM device socket is available for programming the Tsi382's registers during startup. The socket is in an 8-pin DIP format.

1.6.3 GPIO Interface

The GPIO Interface is comprised of the following:

- On-board LEDs on GPIO lines
- Available 100mil Header to send/receive external 3.3V level signals

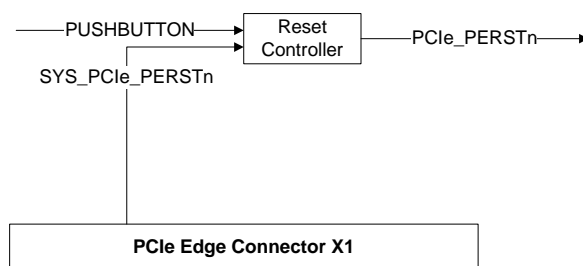
The following list outlines the connections to GPIO:

- External I/O header:
 - J7.1: NC
 - J7.2: GPIO0
 - J7.3: GPIO1
 - J7.4: GPIO2
 - J7.5: GPIO3
 - J7.6: Connected to ground
- LEDs:
 - D11: GPIO0, active led when driven low
 - D1: GPIO1, active led when driven low
 - D13: GPIO2, active led when driven low
 - D12: GPIO3, active led when driven low

1.7 Hardware Reset

The following figure shows the reset options of the Tsi382 evaluation board.

Figure 4: Board Reset



Three levels of reset are available:

- Cold reset – This reset is applied during power up. System (card edge) PCIe_PERSTn is muxed with the board's reset controller.
- Warm reset – This reset is activated by a push-button reset on the board.
- Hot reset – This reset is activated by the in-band message sent by the root complex. No supporting hardware is necessary.



For more information on cold, warm, and hot reset levels, see the “Resets, Clocking, and Initialization Options” chapter in the *Tsi382 User Manual*.

1.8 Logic Analyzer Connectivity

The serial buses have Midbus pads (TMS818 probe) for visibility of SerDes lines using a pre-processor. Each probing pad provides access to the RX and TX segments of a x1 link.

To access the PCI bus, a Nexus PCI interposer card can be used with Tektronix mictor cables. The card can be plugged into any PCI edge slot, or in-line with the device under test.

2. Configurable Options

Topics discussed include the following:

- “Switches” on page 19
- “Shunt Jumpers” on page 24
- “Debug Headers” on page 26
- “Connectors” on page 29
- “LEDs” on page 31

2.1 Switches

2.1.1 DIP Switches

Switches S1 to S6 combine four, small slide switches identified with numbers 1 to 4 (see [Table 7](#) for individual switch definition).

Figure 5: DIP Switch Package/Individual Switch Position

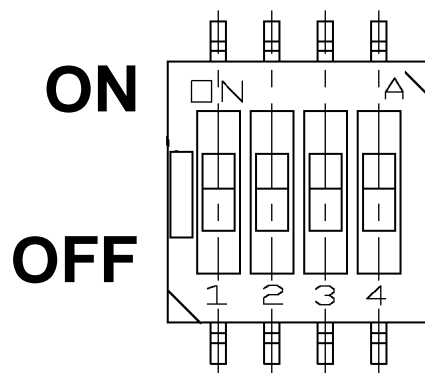
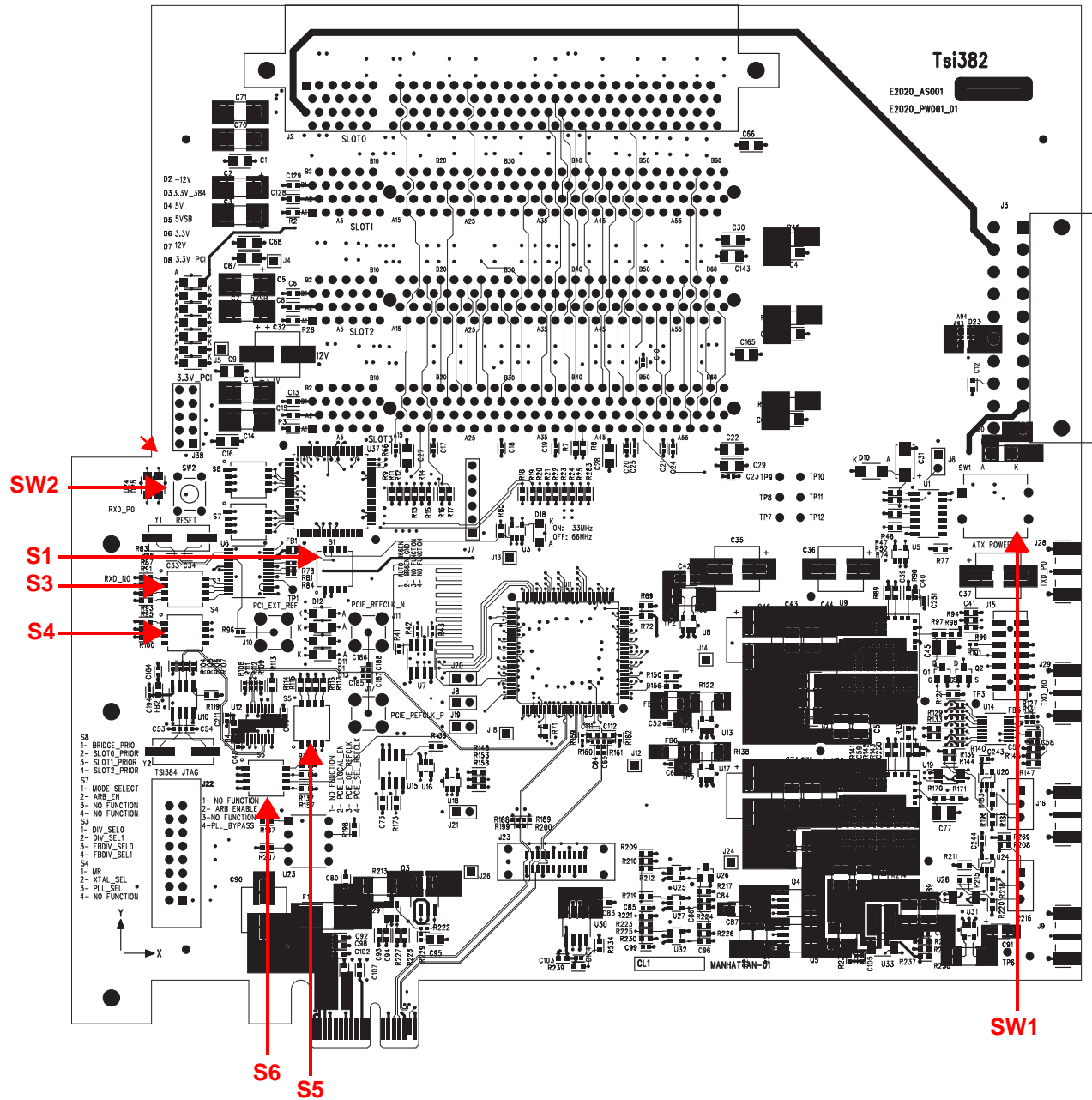


Figure 6: Switch Locations



Switch S1 is used to manually set PCI bus modes.

Table 7: S1 Settings

| Switch Number | Description | Default Setting | On/Off Setting |
|---------------|-------------|-----------------|---|
| 1 | M66EN | ON | ON = Connects M66EN to all cards OFF = Forces M66EN high if S1.2 OFF |
| 2 | M66EN | OFF | ON = Forces M66EN to GND OFF = Disables forcing M66EN to GND |

Switches S3 and S4 are used to set the PCI bus external clock frequency. By default the PCI bus clock source is the Tsi382. The external clock can only be connected to the PCI bus by replacing resistors on the board. When an external clock source is used, an on-board PLL is used to set the proper bus clock frequency. [Table 8](#) contains the clock frequency settings for S3.

Table 8: S3 Settings

| Switch Number | Description | Default Setting | On/Off Setting |
|---------------|-------------|-----------------|---|
| 1 | DIV_SEL0 | OFF | [FBDIV_SEL1, FBDIV_SEL0, DIV_SEL1, DIV_SEL0] ON = 1 OFF = 0 0,0,0,0 = x 4 0,0,0,1 = x 3 0,0,1,0 = x 2 0,0,1,1 = x 1 0,1,0,0 = x 5.33 0,1,0,1 = x 4 0,1,1,0 = x 2.667 0,1,1,1 = x 1.33 1,0,0,0 = x 6.667 1,0,0,1 = x 5 1,0,1,0 = x 3.33 1,0,1,1 = x 1.67 1,1,0,0 = x 8 1,1,0,1 = x 6 1,1,1,0 = x 4 1,1,1,1 = x 2 |
| 2 | DIV_SEL1 | OFF | |
| 3 | FBDIV_SEL0 | OFF | |
| 4 | FBDIV_SEL1 | OFF | |

Switch S4 controls the external clock PLL.

Table 9: S4 Settings

| Switch Number | Description | Default Setting | On/Off Setting |
|---------------|-------------|-----------------|---|
| 1 | PLL Reset | ON | ON = PLL in reset. PLL clock outputs are low. OFF = PLL is active and clock outputs are enabled. |
| 2 | XTAL select | OFF | ON = Clock source for PLL is reference clock from connector J10 OFF = Clock source for PLL is a 25-MHz oscillator. |
| 3 | PLL select | OFF | ON = PLL is bypassed. OFF = PLL is enabled. External clock source is multiplied as per S3 setting |
| 4 | No function | - | - |

Switch S5 controls the PCIe clock multiplexer and the on-board PCIe reference clock PLL.

Table 10: S5 Settings

| Switch Number | Description | Default Setting | On/Off Setting |
|---------------|-------------------------------|-----------------|--|
| 1 | No Function | - | - |
| 2 | PCIe on-board PLL enable | ON | ON = On-board PCIe reference clock PLL is disabled. OFF = On-board PCIe reference clock PLL is enabled. |
| 3 | PCIe clock multiplexer enable | OFF | ON = On-board PCIe clock multiplexer is disabled. OFF = On-board PCIe clock multiplexer is enabled. |
| 4 | PCIe clock source select | OFF | ON = On-board PCIe reference clock is used. OFF = System PCIe reference clock is used. |

Switch S6 configures Tsi382's power-up options.

Table 11: S6 Settings

| Switch Number | Description | Default Setting | On/Off Setting |
|---------------|-------------------------|-----------------|--|
| 1 | No function | - | - |
| 2 | Internal arbiter option | ON | ON = Internal arbiter is enabled OFF = Internal arbiter is disabled |
| 3 | No function | - | - |
| 4 | PCI PLL bypass | ON | ON = PLL is enabled OFF = PLL is bypassed |

2.1.2 Push Button

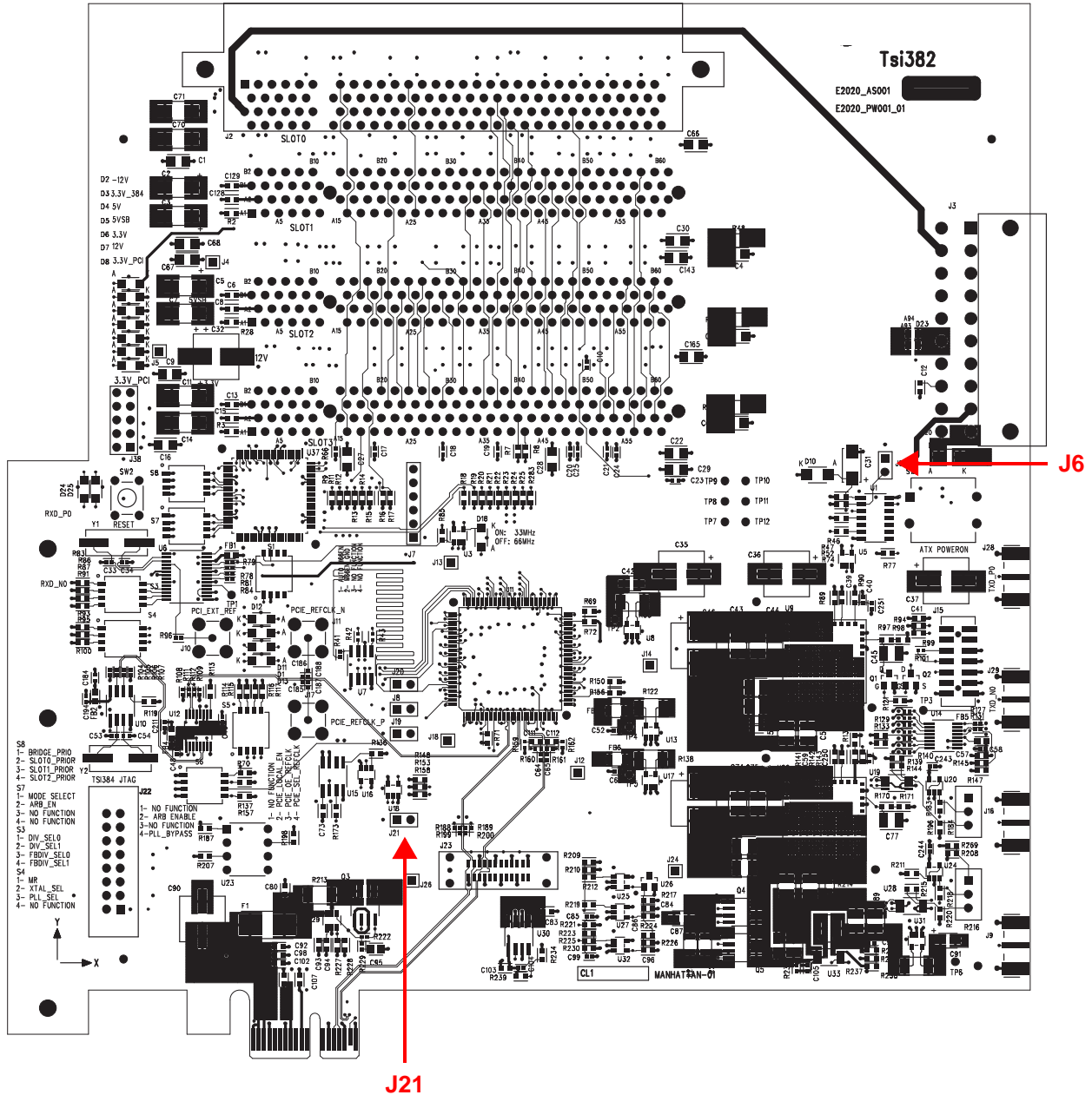
SW1 is used to turn the ATX power supply ON. This switch is used only when the Tsi382 evaluation board is powered up with a stand-alone ATX power supply.

SW2 is used to reset the evaluation board. When pushing the reset button, the board is reset the same way a PCIe system reset would reset the board.

2.2 Shunt Jumpers

Shunt jumpers control special features on the evaluation board (see Figure 7). These jumpers are explained in the following sub-sections.

Figure 7: Shunt Jumper Locations



2.2.1 J6 Shunt Jumper

J6 is used to bypass the On/Off push button to enable the ATX power supply.

Table 12: J6 Shunt Jumper Setting

| Jumper Setting | Default Setting | Function |
|----------------|-----------------|---|
| Installed | Removed | Forces ATX power supply ON. |
| Removed | | Normal operation, ATX power supply is turned On/OFF from push button. |

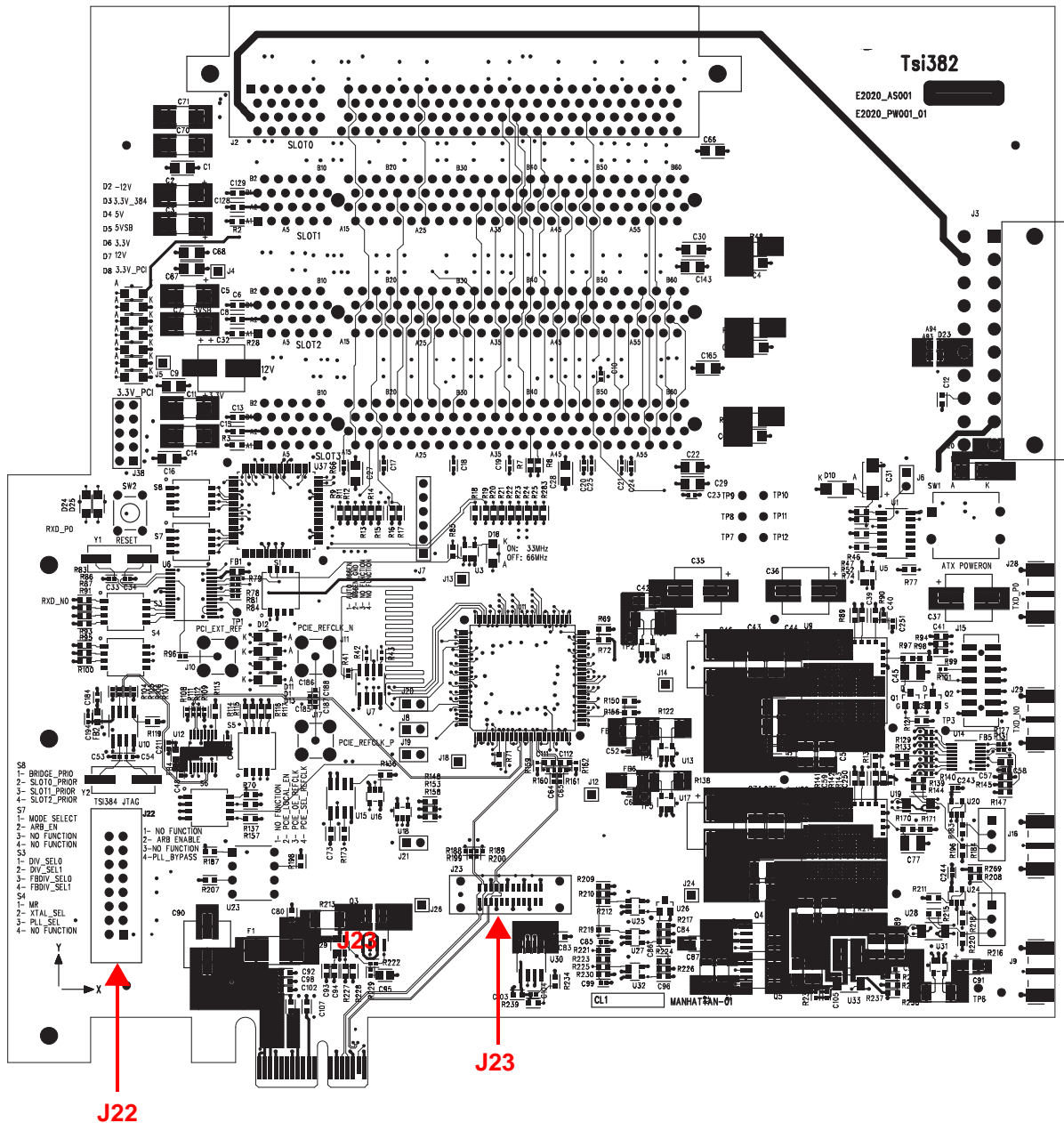
2.2.2 J21 Shunt Jumper

J21 is used to force the Tsi382 into a special debug mode. The default setting for this jumper is ON.

2.3 Debug Headers

Debug headers are used to connect to signals on the evaluation board. This section provides header pinouts.

Figure 8: Debug Header Locations



2.3.1 J22 Tsi382 JTAG

Table 13: J22 Pin Assignment

| Pin Number | Signal Assignment | Pin Location |
|------------|-------------------|--|
| 1 | TDO | <div style="display: flex; align-items: center; justify-content: center;"> <div style="margin-right: 20px;">J22</div> </div> |
| 2 | NC | |
| 3 | TDI | |
| 4 | 3.3V | |
| 5 | NC | |
| 6 | 3.3V | |
| 7 | TCK | |
| 8 | NC | |
| 9 | TMS | |
| 10 | NC | |
| 11 | NC | |
| 12 | GND | |
| 13 | NC | |
| 14 | NC | |
| 15 | NC | |
| 16 | GND | |

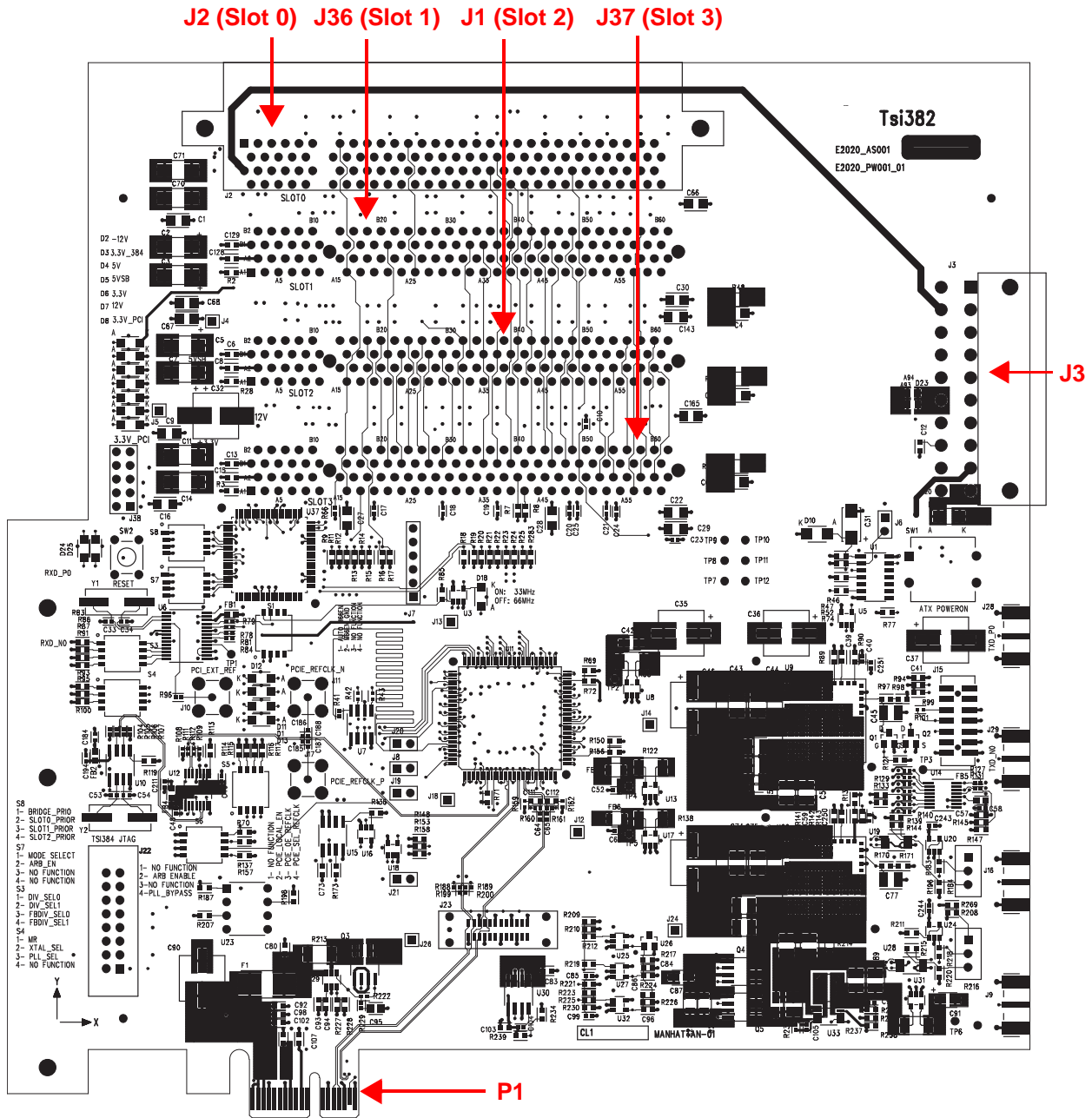
2.3.2 J23 Logic Analyzer PADS

Table 14: J23 Pin Assignment

| Pin Number | Signal Assignment | Pin Location |
|------------|-------------------|--------------|
| 1 | PCIE_RXD_EDG_P0 | |
| 2 | GND | |
| 3 | PCIE_RXD_EDG_N0 | |
| 4 | PCIE_TXD_EDG_P0 | |
| 5 | GND | |
| 6 | PCIE_TXD_EDG_N0 | |
| 7 | N/C | |
| 8 | GND | |
| 9 | N/C | |
| 10 | N/C | |
| 11 | GND | |
| 12 | N/C | |
| 13 | N/C | |
| 14 | GND | |
| 15 | N/C | |
| 16 | N/C | |
| 17 | GND | |
| 18 | N/C | |
| 19 | N/C | |
| 20 | GND | |
| 21 | N/C | |
| 22 | N/C | |
| 23 | GND | |
| 24 | N/C | |

2.4 Connectors

Figure 9: Board Connector Locations



2.4.1 J1, J2, J36, J37 Connectors

These connectors are used to connect a plug-in card to the Tsi382's PCI Interface. The connectors' pin assignments are as per the PCI standard for 32-bit connectors.

2.4.2 J3 ATX Power Connector

A standard ATX power supply can be used to power up the board when used stand alone (not plugged into a PCIe system).

Table 15: J3 Pin Assignment

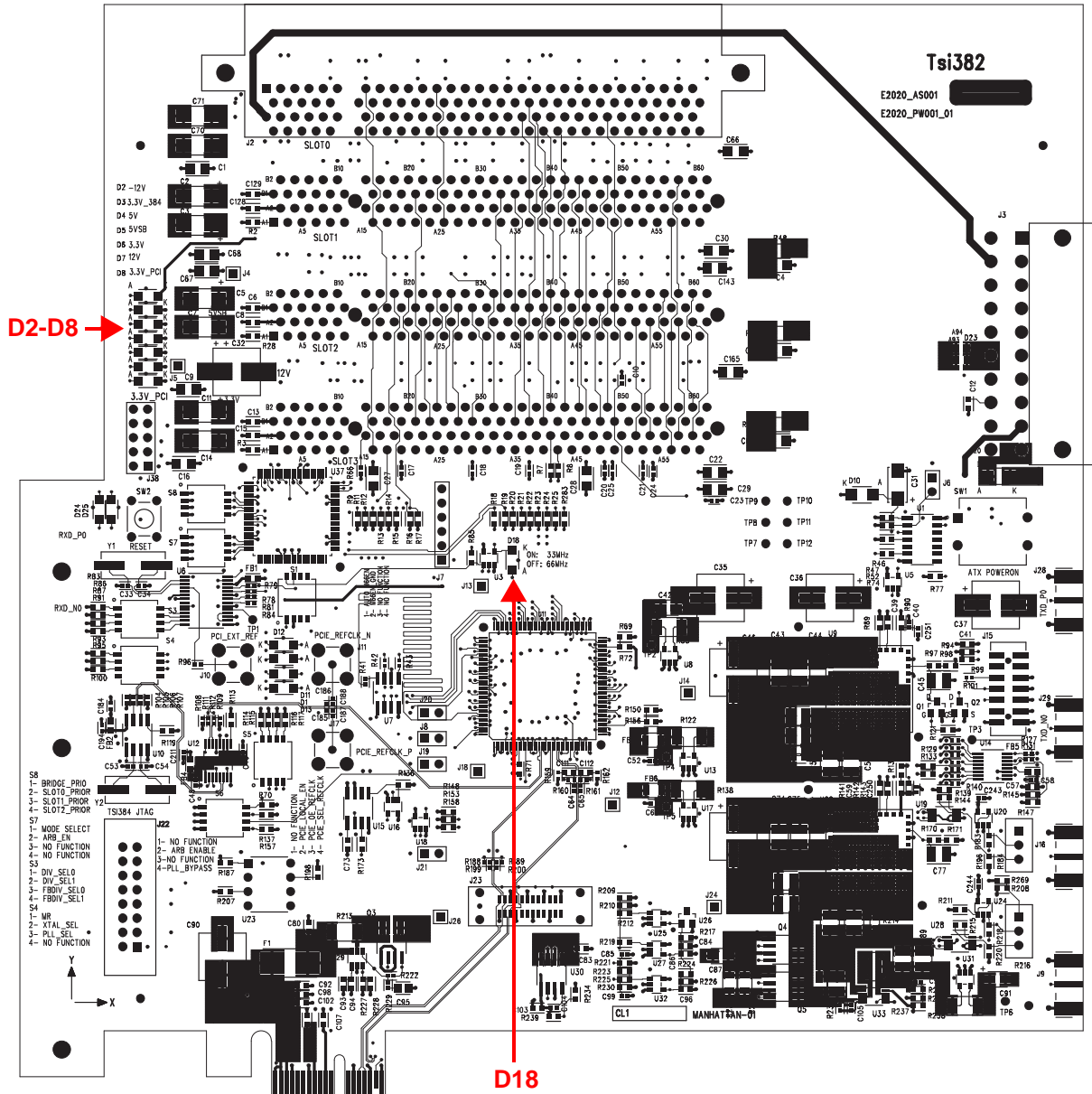
| Pin Number | Signal Assignment | J3 Pin Location |
|------------|-------------------|-----------------|
| 1 | 3.3V | |
| 2 | 3.3V | |
| 3 | GND | |
| 4 | 5V | |
| 5 | GND | |
| 6 | 5V | |
| 7 | GND | |
| 8 | N.C. | |
| 9 | 5VSB | |
| 10 | 12V | |
| 11 | 3.3V | |
| 12 | -12V | |
| 13 | GND | |
| 14 | GND | |
| 15 | GND | |
| 16 | GND | |
| 17 | GND | |
| 18 | N.C. | |
| 19 | 5V | |
| 20 | 5V | |

2.4.3 P1 x1 PCIe Finger Connector

The pin assignment for the finger connector is as per the PCIe standard. Note that the JTAG signals TDI and TDO are connected together on the board.

2.5 LEDs

Figure 10: LED Locations



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