NCV47411

LDO Regulator - Adjustable Dual, Adjustable Current Limit

3.3 V to 20 V

The NCV47411 is a dual integrated low dropout regulator with 100 mA per channel designed for use in harsh automotive environments. It includes wide operating temperature and input voltage ranges. The device is offered with adjustable voltage version available in 3% output voltage accuracy. It has a high peak input voltage tolerance and reverse input voltage protection. It also provides overcurrent protection, overtemperature protection and enable for control of the state of the output voltage of each channel. The integrated current sense feature provides diagnosis and system protection functionality. The current limit of the device is adjustable by resistor connected to CSO pin for each channel. CSO pin output current creates voltage drop across CSO resistor which is proportional to output current of each channel.

Features

- Two Adjustable Outputs: (from 3.3 V to 20 V) ±3% Output Voltage
- Enable Inputs (3.3 V Logic Compatible Thresholds)
- Adjustable Current Limit up to 150 mA
- Protection Features:
  - Current Limitation
  - Thermal Shutdown
  - Reverse Input Voltage
- This is a Pb−Free Device

Typical Applications

- Audio and Infotainment System
- Instrument Cluster
- Navigation
- Satellite Radio

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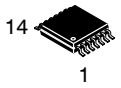
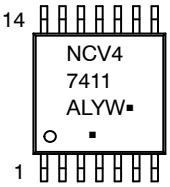
MARKING DIAGRAM



TSSOP−14 EP
CASE 948AW

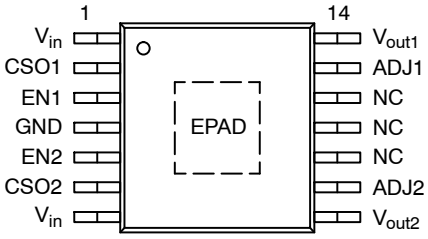


NCV47411	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

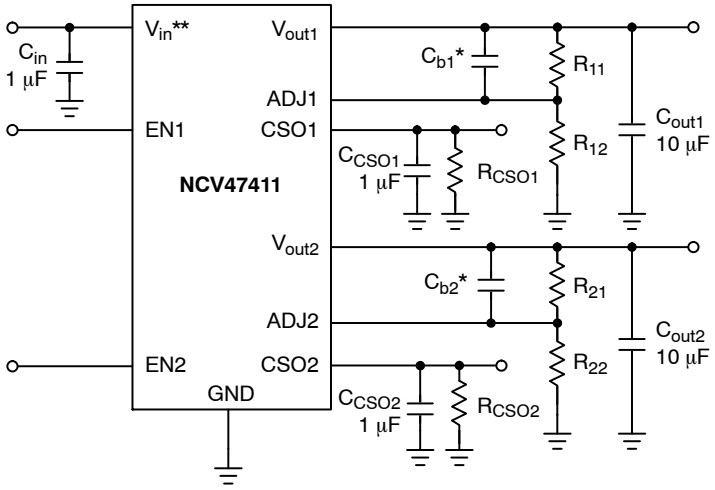
PIN CONNECTIONS

Top View



ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.



C_{b1}*, C_{b2}* – Optional, see Regulator Stability Considerations section
** – Both V_{in} pins must be connected together on PCB

Figure 1. Application Schematic
(See Application Section for More Datails)

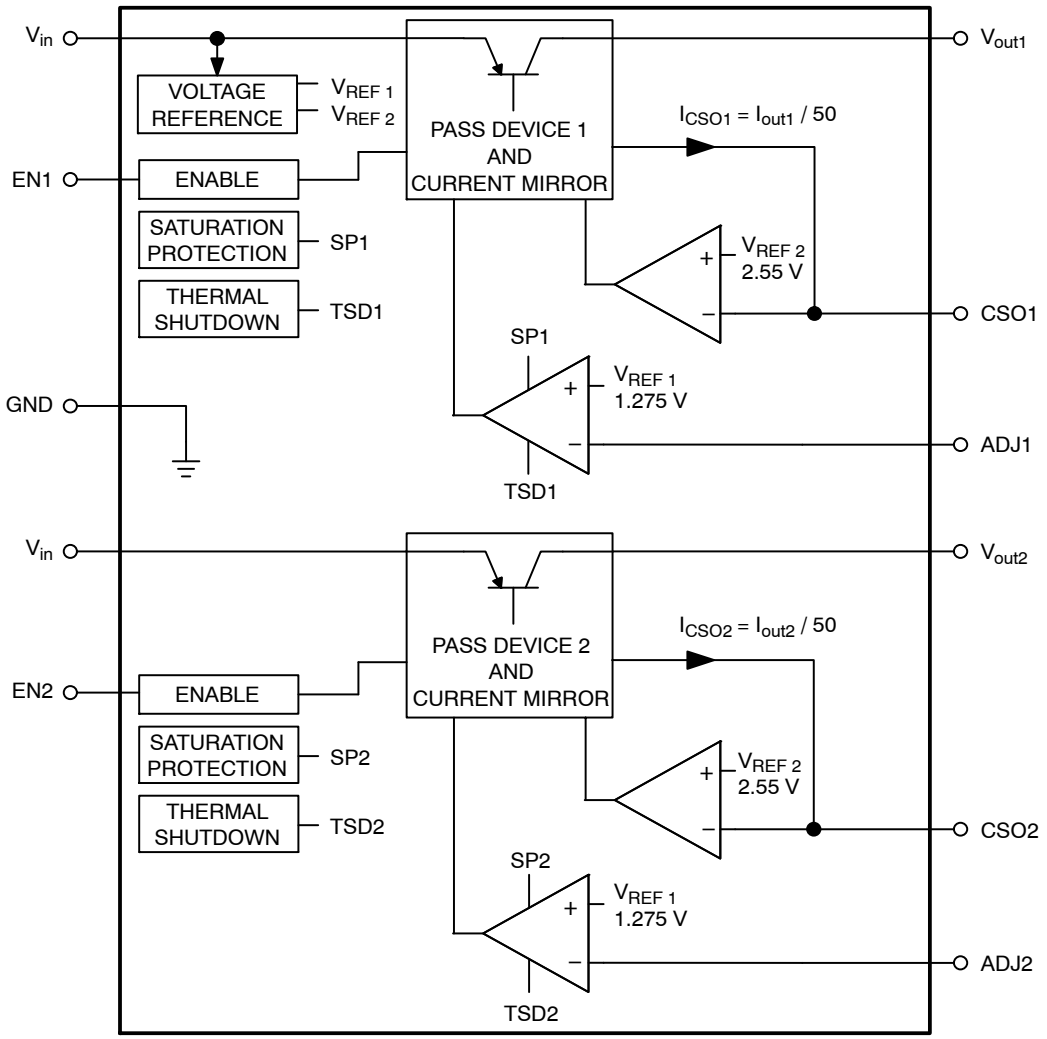


Figure 2. Simplified Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	V_{in}	Power Supply Input. (All V_{in} pins must be connected on PCB)
2	CSO1	Current Sense Output 1, Current Limit setting and Output Current value information. See Application Section for more details.
3	EN1	Enable Input 1; low level disables the Channel 1.
4	GND	Power Supply Ground.
5	EN2	Enable Input 2; low level disables the Channel 2.
6	CSO2	Current Sense Output 2, Current Limit setting and Output Current value information. See Application Section for more details.
7	V_{in}	Power Supply Input. (All V_{in} pins must be connected on PCB)
8	V_{out2}	Regulated Output Voltage 2.
9	ADJ2	Adjustable Voltage Setting Input 2. See Application Section for more details.
10	NC	Not Connected. (Not internally bonded)
11	NC	Not Connected. (Not internally bonded)
12	NC	Not Connected. (Not internally bonded)
13	ADJ1	Adjustable Voltage Setting Input 1. See Application Section for more details.
14	V_{out1}	Regulated Output Voltage 1.
EPAD	EPAD	Exposed Pad is connected to Ground. Connect to GND plane on PCB.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Input Voltage DC	V_{in}	−42	45	V
Enable Input Voltage	$V_{EN1,2}$	−42	45	V
ADJ Input Voltage	$V_{ADJ1,2}$	−0.3	10	V
CSO Voltage	$V_{CSO1,2}$	−0.3	7	V
Output Voltage	$V_{out1,2}$	−1	40	V
Junction Temperature	T_J	−40	150	°C
Storage Temperature	T_{STG}	−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. ESD CAPABILITY (Note 1)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	ESD_{HBM}	−2	2	kV
ESD Capability, Machine Model	ESD_{MM}	−200	200	V

1. This device series incorporates ESD protection and is tested by the following methods:
   a) ESD Human Body Model tested per AEC−Q100−002 (JS−001−2010)
   b) ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)

Table 4. LEAD SOLDERING TEMPERATURE AND MSL (Note 2)

Rating	Symbol	Min	Max	Unit
Moisture Sensitivity Level	MSL	1	1	−
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions	T_{SLD}	−	265 peak	°C

2. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

Table 5. THERMAL CHARACTERISTICS (Note 3)

Rating	Symbol	Value	Unit
Thermal Characteristics (single layer PCB) Thermal Resistance, Junction−to−Air (Note 4) Thermal Reference, Junction−to−Lead (Note 4)	 $R_{\theta JA}$ $R_{\psi JL}$	 52 9.5	°C/W
Thermal Characteristics (4 layers PCB) Thermal Resistance, Junction−to−Air (Note 4) Thermal Reference, Junction−to−Lead (Note 4)	 $R_{\theta JA}$ $R_{\psi JL}$	 28.5 8.4	°C/W

3. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
4. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate, assuming equal power dissipation of both channels. Single layer − according to JEDEC51.3, 4 layers − according to JEDEC51.7

Table 6. RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 5)	V_{in}	4.4	40	V
Nominal Output Voltages	$V_{out\_nom1,2}$	3.3	20	V
Output Current Limit (Note 6)	$I_{LIM1,2}$	10	150	mA
Junction Temperature	T_J	−40	150	°C
Current Sense Output (CSO) Capacitor	$C_{CSO1,2}$	1.0	4.7	μF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
5. Minimum V_{in} = 4.4 V or ($V_{out\_nom1,2}$ + 0.5 V), whichever is higher.
6. Corresponding $R_{CSO1,2}$ is in range from 12.75 kΩ down to 850 Ω.

Table 7. ELECTRICAL CHARACTERISTICS

V_{in} = 13.5 V, $V_{EN1,2}$ = 3.3 V, $R_{CSO1,2}$ = 0 Ω, $C_{CSO1,2}$ = 1 μF, C_{in} = 1 μF, $C_{out1,2}$ = 10 μF, ESR = 1.5 Ω. Min and Max values are valid for temperature range −40°C ≤ T_J ≤ +150°C unless noted otherwise and are guaranteed by test, design or statistical correlation. Typical values are referenced to T_J = 25°C (Note 7)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
REGULATOR OUTPUTS						
Output Voltage (Accuracy %) (Note 8)	V_{in} = V_{in_min} to 40 V $I_{out1,2}$ = 5 mA to 100 mA	$V_{out1,2}$	−3	–	+3	%
Line Regulation (Note 8)	V_{in} = V_{in_min} to ($V_{out\_nom1,2}$ + 20 V) $I_{out1,2}$ = 5 mA	$Reg_{line1,2}$	–	0.05	1.0	%
Load Regulation	V_{in} = ($V_{out\_nom1,2}$ + 8.5 V) $I_{out1,2}$ = 5 mA to 100 mA	$Reg_{load1,2}$	–	0.05	1.4	%
Dropout Voltage (Note 9)	$V_{out\_nom1,2}$ = 5 V, $I_{out1,2}$ = 100 mA $V_{DO1,2}$ = V_{in} − $V_{out1,2}$	$V_{DO1,2}$	–	250	550	mV
DISABLE AND QUIESCENT CURRENTS						
Disable Current	$V_{EN1,2}$ = 0 V	I_{DIS}	–	0.07	10	μA
Quiescent Current, I_q = I_{in} − (I_{out1} + I_{out2})	$I_{out1,2}$ = 500 μA, V_{in} = ($V_{out\_nom1,2}$ + 8.5 V)	I_q	–	235	370	μA
Quiescent Current, I_q = I_{in} − (I_{out1} + I_{out2})	$I_{out1,2}$ = 100 mA, V_{in} = ($V_{out\_nom1,2}$ + 8.5 V)	I_q	–	15	50	mA
CURRENT LIMIT PROTECTION						
Current Limit	$V_{out1,2}$ = 0.9 x $V_{out\_nom1,2}$ V_{in} = ($V_{out\_nom1,2}$ + 8.5 V)	$I_{LIM1,2}$	150	–	–	mA
PSRR & NOISE						
Power Supply Ripple Rejection	f = 100 Hz, 0.5 $V_{p-p1,2}$	$PSRR_{1,2}$	–	75	–	dB
Output Noise Voltage	f = 10 Hz to 100 kHz, $C_{b1,2}$ = 10 nF	$V_{n1,2}$	–	130	–	μV_{rms}
ENABLE						
Enable Input Threshold Voltage Logic Low (OFF) Logic High (ON)	 $V_{out1,2}$ ≤ 0.1 V $V_{out1,2}$ ≥ 0.9 x $V_{out\_nom1,2}$	$V_{th(EN1,2)}$	 0.99 –	 1.8 1.9	 – 2.31	V
Enable Input Current	$V_{EN1,2}$ = 3.3 V	$I_{EN1,2}$	2	9	20	μA
Turn On Time from Enable ON to 90% of V_{out}	$I_{out1,2}$ = 100 mA, $C_{b1,2}$ = 10 nF, R_{n1} = 82 kΩ, R_{n2} = 27 kΩ	t_{on}	 –	 1.6	 –	ms
OUTPUT CURRENT SENSE						
CSO Voltage Level at Current Limit	$V_{out1,2}$ = 0.9 x $V_{out\_nom1,2}$, ($V_{out\_nom1,2}$ = 5 V) $R_{CSO1,2}$ = 2.55 kΩ	$V_{CSO\_Ilim1.2}$	2.346 (−8 %)	2.55	2.754 (+8 %)	V
CSO Transient Voltage Level	$C_{CSO1,2}$ = 4.7 μF, $R_{CSO1,2}$ = 2.55 kΩ $I_{out1,2}$ pulse from 10 mA to 100 mA, tr = 1 μs	$V_{CSO1,2}$	–	–	3.3	V
Output Current to CSO Current Ratio (Note 10)	$V_{CSO1,2}$ = 2 V, $I_{out1,2}$ = 10 mA to 100 mA ($V_{out\_nom1,2}$ = 5 V)	$I_{out1,2}/I_{CSO1,2}$	– (−10 %)	50	– (+10 %)	–
CSO Current at no Load Current	$V_{CSO1,2}$ = 0 V, $I_{out1,2}$ = 0 mA, ($V_{out\_nom1,2}$ = 5 V)	$I_{CSO\_off1,2}$	–	–	10	μA
THERMAL SHUTDOWN						
Thermal Shutdown Temperature	$I_{out1,2}$ = 2.5 mA	$T_{SD1,2}$	150	–	195	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
8. Minimum input voltage V_{in_min} is 4.4 V or ($V_{out\_nom1,2}$ + 1 V) whichever is higher
9. Measured when the output voltage $V_{out1,2}$ has dropped by 2% of $V_{out1,2}$ from the nominal value obtained at V_{in} = $V_{out\_nom1,2}$ + 8.5 V.
10. Not guaranteed in dropout.

TYPICAL CHARACTERISTICS

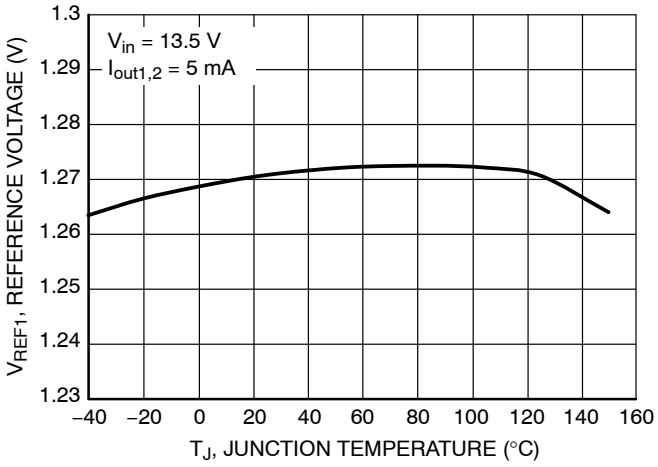


Figure 3. Reference Voltage vs. Temperature

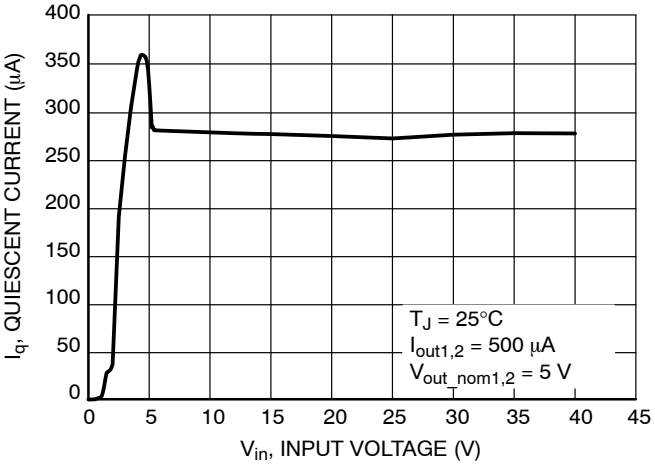


Figure 4. Quiescent Current vs. Input Voltage

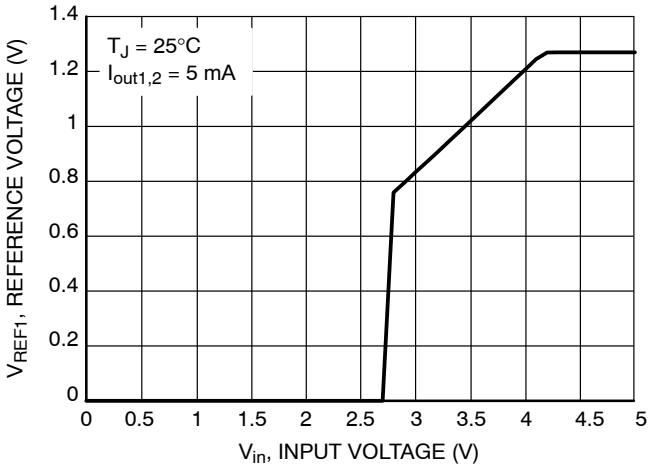


Figure 5. Reference Voltage vs. Input Voltage

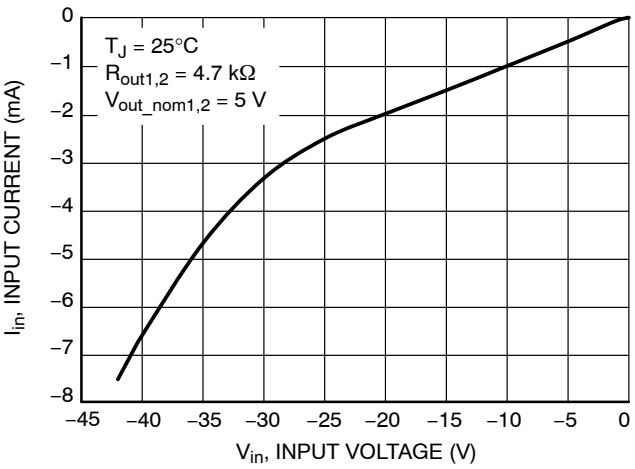


Figure 6. Input Current vs. Input Voltage (Reverse Input Voltage)

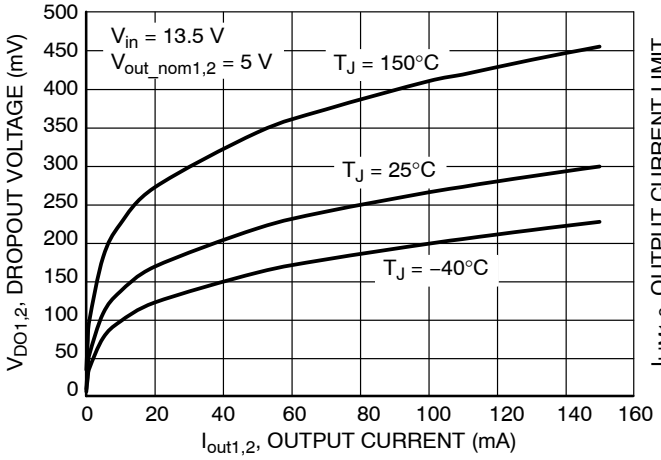


Figure 7. Dropout Voltage vs. Output Current

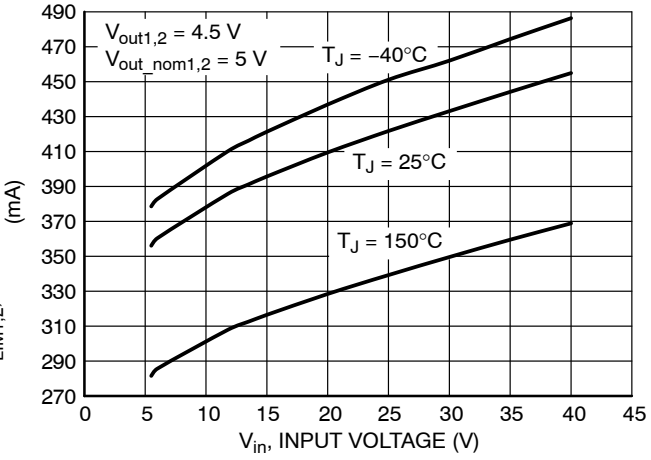


Figure 8. Output Current Limit vs. Input Voltage

TYPICAL CHARACTERISTICS

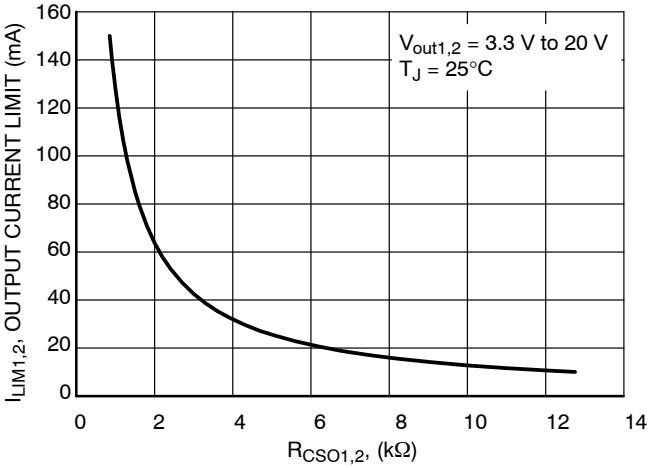


Figure 9. Output Current Limit vs. R_{CSO}

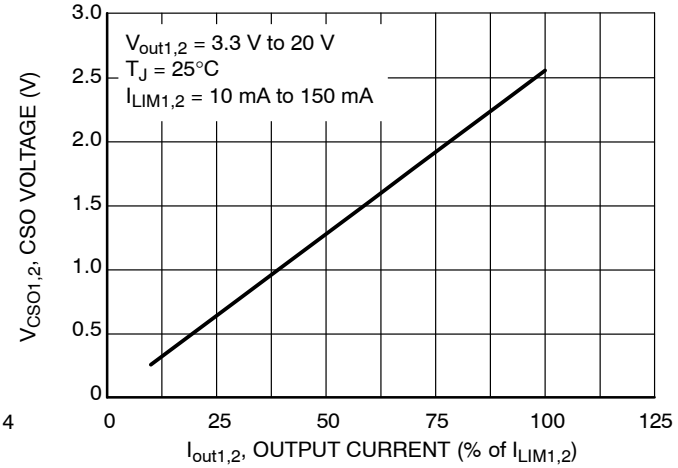


Figure 10. Output Current (% of I_{LIM}) vs. CSO Voltage

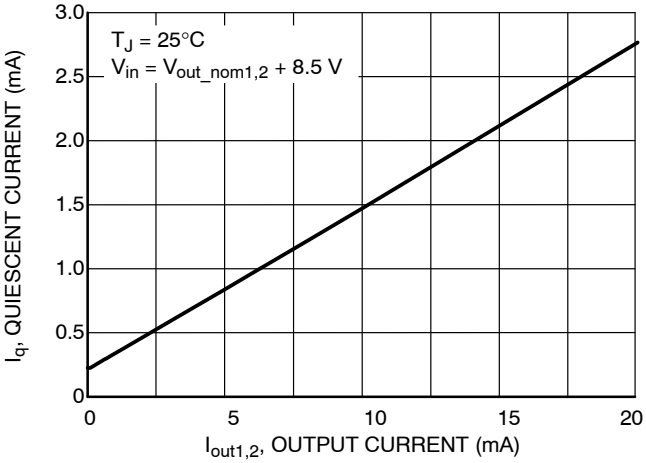


Figure 11. Quiescent Current vs. Output Current (Low Load)

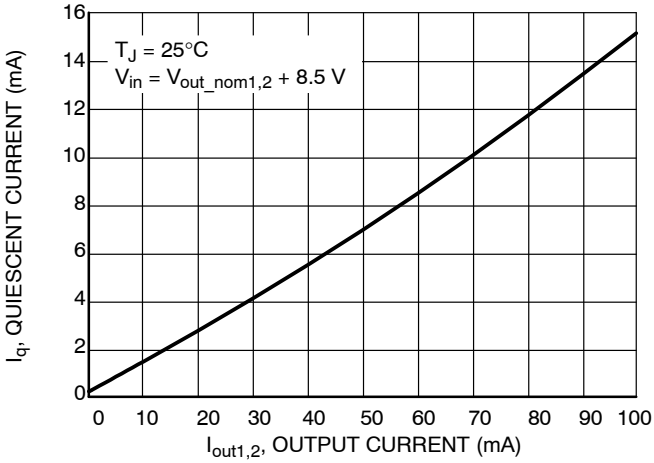


Figure 12. Quiescent Current vs. Output Current (High Load)

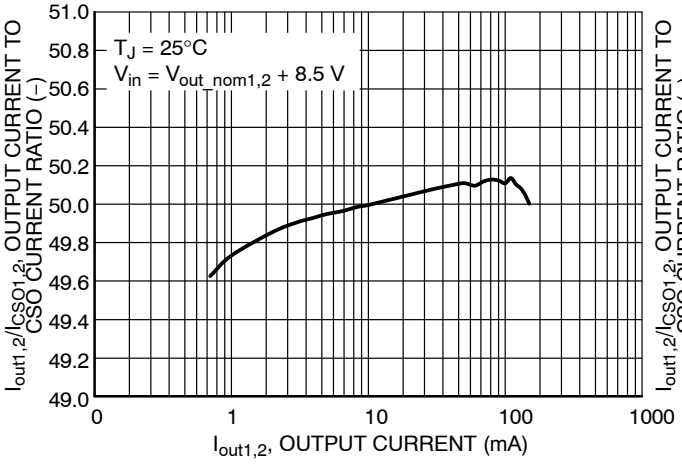


Figure 13. Output Current to CSO Current Ratio vs. Output Current

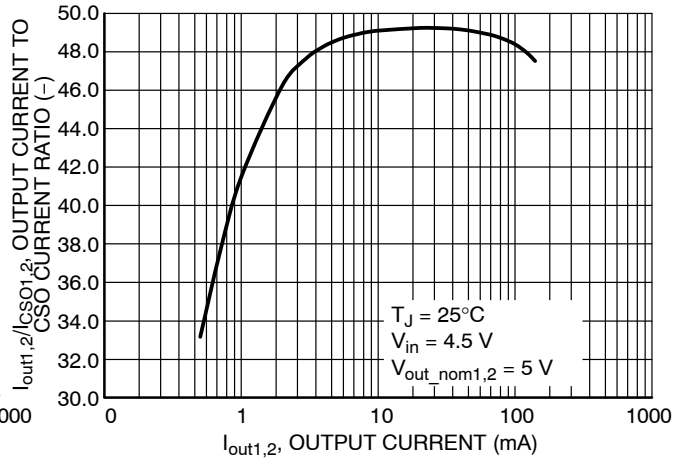


Figure 14. Output Current to CSO Current Ratio vs. Output Current (In Dropout)

TYPICAL CHARACTERISTICS

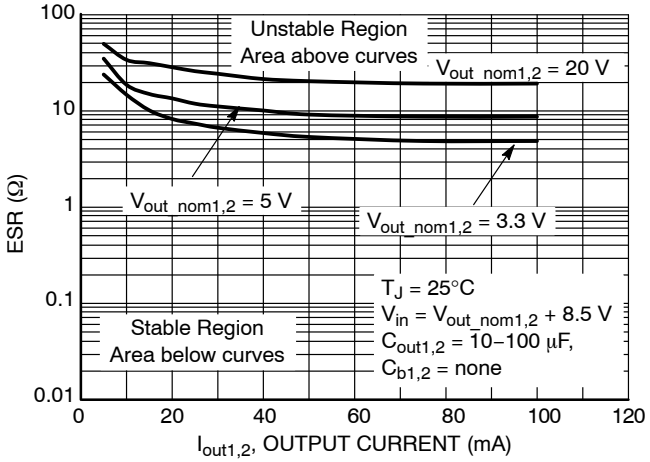


Figure 15. Output Capacitor Stability Region vs. Output Current

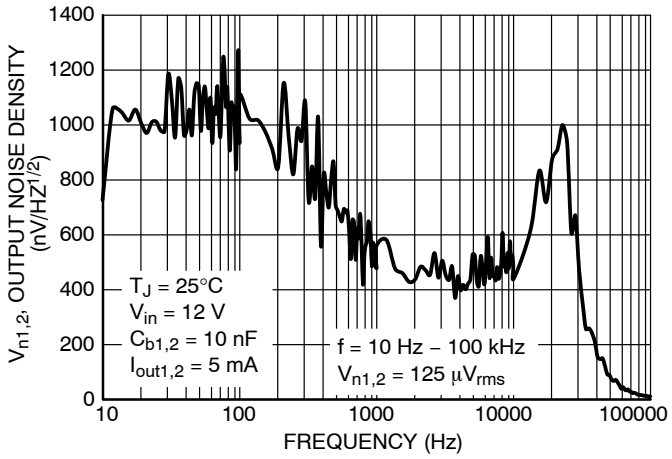


Figure 16. Noise vs. Frequency

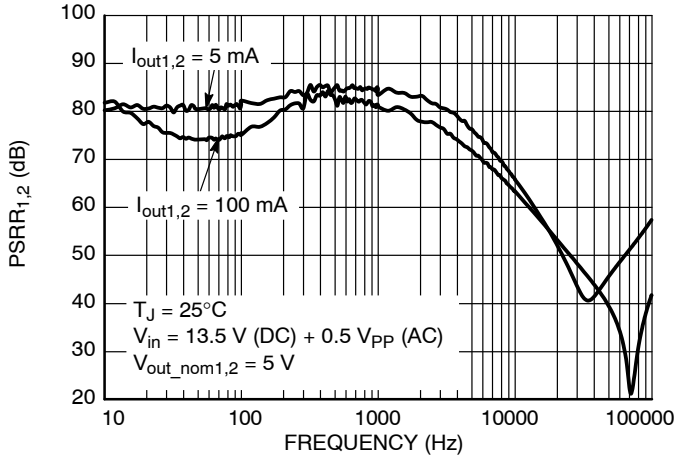


Figure 17. PSRR vs. Frequency

DEFINITIONS

General

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

Output voltage

The output voltage parameter is defined for specific temperature, input voltage and output current values or specified over Line, Load and Temperature ranges.

Line Regulation

The change in output voltage for a change in input voltage measured for specific output current over operating ambient temperature range.

Load Regulation

The change in output voltage for a change in output current measured for specific input voltage over operating ambient temperature range.

Dropout Voltage

The input to output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. It is measured when the output drops 2% of $V_{out\_nom\_n}$ below its nominal value. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Quiescent and Disable Currents

Quiescent Current (I_q) is the difference between the input current (measured through the LDO input pin) and the output load current. If Enable pin is set to LOW the regulator reduces its internal bias and shuts off the output, this term is called the disable current (I_{DIS}).

Current Limit

Current Limit is value of output current by which output voltage drops below 90% of its nominal value.

PSRR

Power Supply Rejection Ratio is defined as ratio of output voltage and input voltage ripple. It is measured in decibels (dB).

Line Transient Response

Typical output voltage overshoot and undershoot response when the input voltage is excited with a given slope.

Load Transient Response

Typical output voltage overshoot and undershoot response when the output current is excited with a given slope between low-load and high-load conditions.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

APPLICATIONS INFORMATION

Circuit Description

The NCV47411 is an integrated dual low dropout regulator that provides a regulated voltage at 100 mA to each output. It is enabled with an input to the enable pin. The regulator voltage is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference, which gives it the lowest possible dropout voltage. The output current capability is 100 mA per output, and the base drive quiescent current is controlled to prevent oversaturation when the input voltage is low or when the output is overloaded. The integrated current sense feature provides diagnosis and system protection functionality. The current limit of the device is adjustable by resistor connected to CSO1,2 pin. Voltage on CSO1,2 pin is proportional to output current. The regulator is protected by both current limit and thermal shutdown. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

Regulator

The error amplifier compares the reference voltage to a sample of the output voltage ($V_{out1,2}$) and drives the base of a PNP series pass transistor via a buffer. The reference is a bandgap design to give it a temperature stable output. Saturation control of the PNP is a function of the load current and input voltage. Oversaturation of the output power device is prevented, and quiescent current in the ground pin is minimized.

Regulator Stability Considerations

The input capacitor (C_{in}) is necessary to stabilize the input impedance to avoid voltage line influences. The output capacitor ($C_{out1,2}$) helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information. The value for the output capacitor $C_{out1,2}$, shown in Figure 1 should work for most applications; see also Figure 12 for output stability at various load and Output Capacitor ESR conditions. Stable region of ESR in Figure 12 shows ESR values at which the LDO output voltage does not have any permanent oscillations at any dynamic changes of output load current. Marginal ESR is the value at which the output voltage waving is fully damped during four periods after the load change and no oscillation is further observable.

ESR characteristics were measured with ceramic capacitors and additional series resistors to emulate ESR. Low duty cycle pulse load current technique has been used to maintain junction temperature close to ambient temperature.

Calculating Bypass Capacitor

If improved stability (reducing output voltage ringing during transients) is demanded, connect the bypass capacitor $C_{b1,2}$ between Adjustable Input pin and $V_{out1,2}$ pin according to Applications circuit at Figure 1. Parallel combination of bypass capacitor $C_{b1,2}$ with the feedback resistor R_{n1} contributes in the device transfer function as an additional zero and affects the device loop stability, therefore its value must be optimized. Attention to the Output Capacitor value and its ESR must be paid. See also Stability in High Speed Linear LDO Regulators Application Note, AND8037/D for more information. Optimal value of bypass capacitor is given by following expression

$$C_{bn} = \frac{1}{2 \times \pi \times f_z \times R_{n1}} \ (F) \qquad \text{(eq. 1)}$$

where:

R_{n1} - the upper feedback resistor

f_z - the frequency of the zero added into the device transfer function by R_{n1} and C_{b1} external components.

Set the R_{n1} resistor according to output voltage requirement. Chose the f_Z with regard on the output capacitance $C_{out1,2}$, refer to the table below.

$C_{out1,2}$ (μF)	10	22	47	100
f_Z range (kHz)	min 1.9	min 0.87	min 1.24	N/A*

*For $C_{out1,2}$ = 100 μF and higher $C_{b1,2}$ capacitors are not needed for stability improvement. $C_{b1,2}$ capacitors are useful for noise reduction. See electrical characteristic table.

Ceramic capacitors and its part numbers listed bellow have been used as low ESR output capacitors $C_{out1,2}$ from the table above to define the frequency ranges of additional zero required for stability:

GRM31CR71C106KAC7 (10 μF, 16 V, X7R, 1206)

GRM32ER71C226KE18 (22 μF, 16 V, X7R, 1210)

GRM32ER61C476ME15 (47 μF, 16 V, X5R, 1210)

GRM32ER60J107ME20 (100 μF, 6.3 V, X5R, 1210)

Enable Inputs

An enable pin is used to turn a channel on or off. By holding the pin down to a voltage less than 0.99 V, the output of the channel will be turned off. When the voltage on the enable pin is greater than 2.31 V, the output of the channel will be enabled to power its output to the regulated output voltage. The enable pins may be connected directly to the input pin to give constant enable to the output channel.

Setting the Output Voltage

The output voltage range can be set between 3.3 V and 20 V. This is accomplished with an external resistor divider feeding back the voltage to the IC back to the error amplifier by the voltage adjust pin ADJ1,2. The internal reference voltage is set to a temperature stable reference (V_{REF1}) of 1.275 V. The output voltage is calculated from the following formula. Ignoring the bias current into the ADJ1,2 pin:

$$V_{out\_nom\_n} = V_{REF1}\left(1 + \frac{R_{n1}}{R_{n2}}\right) \quad \text{(eq. 2)}$$

Use $R_{n2} < 50\ k\Omega$ to avoid significant voltage output errors due to ADJ1,2 bias current.

Designers should consider the tolerance of R_{n1} and R_{n2} during the design phase.

Setting the Output Current Limit

The output current limit can be set between 10 mA and 150 mA by external resistor $R_{CSO1,2}$ (see Figure 1). Capacitor $C_{CSO1,2}$ of 1 μF in parallel with $R_{CSO1,2}$ is required for stability of current limit control circuitry (see Figure 1).

$$V_{CSO1,2} = I_{out1,2}\left(R_{CSO1,2} \times \frac{1}{50}\right) \quad \text{(eq. 3)}$$

$$I_{LIM1,2} = \frac{50}{1} \times \frac{2.55}{R_{CSO1,2}} \quad \text{(eq. 4)}$$

$$R_{CSO1,2} = \frac{50}{1} \times \frac{2.55}{I_{LIM1,2}} \quad \text{(eq. 5)}$$

where:

$R_{CSO1,2}$ – current limit setting resistor
$V_{CSO1,2}$ – voltage at CSO pin proportional to $I_{out1,2}$
$I_{LIM1,2}$ – current limit value
$I_{out1,2}$ – output current actual value

CSO1,2 pin provides information about output current actual value. The CSO1,2 voltage is proportional to output current according to Equation 3.

Once output current reaches its limit value ($I_{LIM1,2}$) set by external resistor $R_{CSO1,2}$ than voltage at CSO1,2 pin is typically 2.55 V. Calculations of $I_{LIM1,2}$ or $R_{CSO1,2}$ values can be done using equations Equations 4 and 5, respectively.

Designers should consider the tolerance of $R_{CSO1,2}$ during the design phase.

Thermal Considerations

As power in the NCV47411 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV47411 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV47411 can handle is given by:

$$P_{D(MAX)} = \frac{[T_{J(MAX)} - T_A]}{R_{\theta JA}} \quad \text{(eq. 6)}$$

Since T_J is not recommended to exceed 150°C, then the NCV47411 soldered on 645 mm^2, 1 oz copper area, FR4 can dissipate up to 2.4 W (single layer PCB) when the ambient temperature (T_A) is 25°C. See Figure 18 for $R_{\theta JA}$ versus PCB area. The power dissipated by the NCV47411 can be calculated from the following equations:

$$P_D \approx V_{in}\left(I_q@I_{out1,2}\right) + I_{out1}\left(V_{in} - V_{out1}\right) + I_{out2}\left(V_{in} - V_{out2}\right) \quad \text{(eq. 7)}$$

or

$$V_{in(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{out1} \times I_{out1}\right) + \left(V_{out2} \times I_{out2}\right)}{I_{out1} + I_{out2} + I_q} \quad \text{(eq. 8)}$$

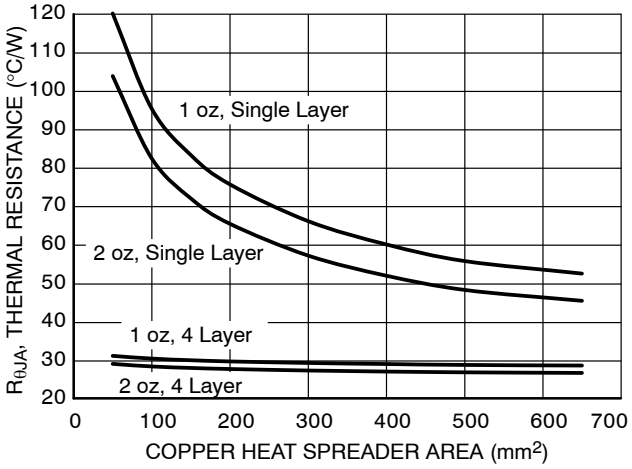


Figure 18. Thermal Resistance vs. PCB Copper Area

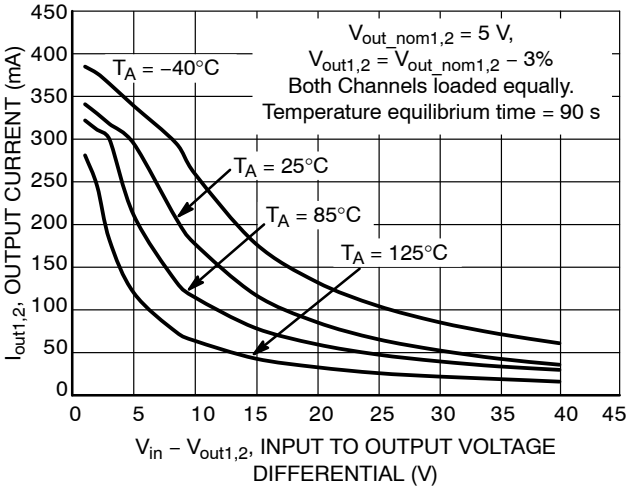


Figure 19. Maximum DC Output Current vs. Input to Output Voltage Differential

Example of safe operating area (SOA) restricted by maximum DC output current per channel (both channels loaded equally) and input to output voltage differential (both nominal output voltages are equal) in ambient temperature range from −40°C to 125°C is shown in Figure 19. The maximum DC output current per channel is the current when the output voltage of corresponding channel has dropped 3% below its nominal output voltage without activation of thermal shutdown protection. Measurement was done in temperature chamber using double−sized PCB 3 x 3 inch (75 x 75 mm), Cu layers thickness 1 oz (35 μm) with copper occupying more than 90% of both sides surface.

Hints

V_{in} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV47411 and make traces as short as possible. To achieve better GND potential distribution on PCB towards output resistor dividers connect not internally bonded pin No. 11 to GND plane and EPAD.

Table 8. ORDERING INFORMATION

Device	Output Voltage	Marking	Package	Shipping†
NCV47411PAAJR2G	Adjustable	Line1: NCV4 Line2: 7411	TSSOP−14 Exposed Pad (Pb−Free)	2500 / Tape & Reel

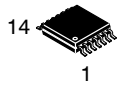
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

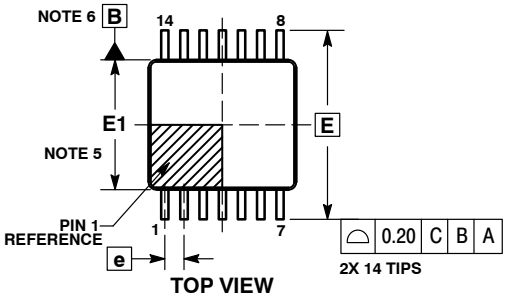
ON Semiconductor®

TSSOP−14 EP
CASE 948AW
ISSUE C

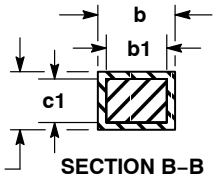
DATE 09 OCT 2012



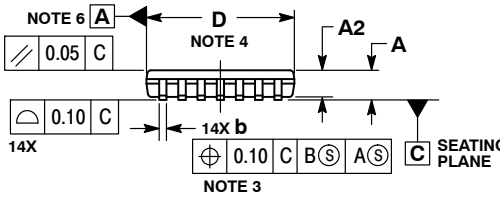
SCALE 1:1



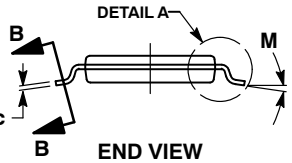
TOP VIEW



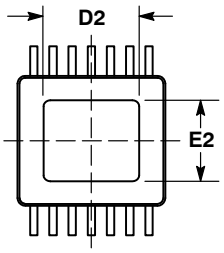
SECTION B−B
NOTE 8



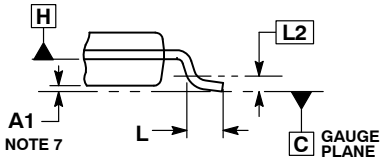
SIDE VIEW



END VIEW



BOTTOM VIEW

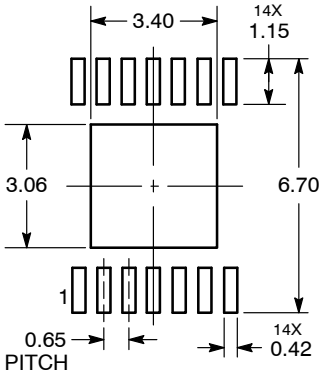


DETAIL A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.07 mm MAX. AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION D IS DETERMINED AT DATUM H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM H.
6. DATUMS A AND B ARE DETERMINED AT DATUM H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. SECTION B−B TO BE DETERMINED AT 0.10 TO 0.25 mm FROM THE LEAD TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	----	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
b1	0.19	0.25
c	0.09	0.20
c1	0.09	0.16
D	4.90	5.10
D2	3.09	3.62
E	6.40 BSC	
E1	4.30	4.50
E2	2.69	3.22
e	0.65 BSC	
L	0.45	0.75
L2	0.25 BSC	
M	0 °	8 °

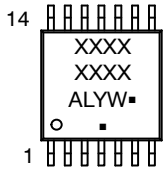
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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