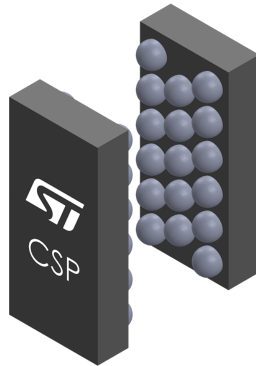
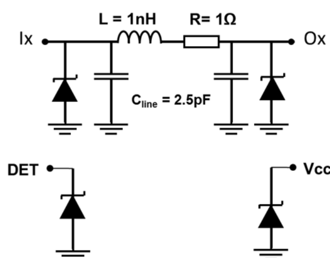
EMIF06-HSD03F3

Datasheet

6-line low capacitance EMI filter array with integrated ESD protections for microSD Card™



CSP pitch 0.4 mm
(17 bumps)



Functional diagram (top view)

Product status link
EMIF06-HSD03F3

Product summary	
Order code	EMIF06-HSD03F3
Package	CSP P 0.4 mm
Packing	Tape and reel

Features

- EMI filter with integrated ESD protection on each SD card pins in one easy routing package
- Very low line capacitance to compensate long PCB tracks
- Ultra-low leakage current at V_{RM}: 20 nA max
- Very low PCB space consumption: 1.1 mm x 2.4 mm
- ECOPACK2 RoHS compliant component
- **Benefits**
  - Very good matching between lines thanks to proprietary solid-state silicon technology
  - Very low capacitance between lines to GND for optimized data integrity and speed
  - Enhanced ESD protection with fast response time and low clamping voltage: IEC 61000-4-2 level 4 compliance guaranteed at device level, hence greater immunity at system level
  - Integrated ESD protection of VCC and DET minimizes PCB space
  - Easy PCB routing thanks to flow-through package pinout
- **Complies with following standards:**
  - UL94, V0
  - IEC 61000-4-2 exceeding level 4: ±18 kV (air discharge – Ix pins)
  - IEC 61000-4-2 exceeding level 4: ±18 kV (contact discharge – Ix pins)

Applications

- SD3.0, UHS-1 SDR104 (208 MHz)
- Secure Digital (SD) Memory Card Interfaces
  - Mobile phones
  - Digital still cameras
  - Portable electronic equipment
  - Navigation systems
  - Security cameras

Description

The EMIF06-HSD03F3 is a 6-line highly integrated low pass filter designed to suppress EMI / RFI noise for micro secure digital interface.

This filter integrates ESD protection diodes, designed to protect sensitive devices from damage when subjected to ESD surges up 18 kV contact.

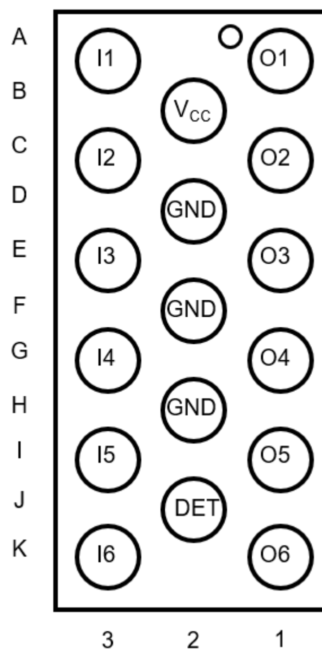
The very low line capacitance ensures a high level of signal integrity without compromising protection of sensitive ICs against transient surge events.

1 Pin configuration and functions

Table 1. Pin description

Pin #	Name	Description
A1	O1	Filtered line – IC side
A3	I1	Filtered line – SD card side
B2	VCC	Power supply input
C1	O2	Filtered line – IC side
C3	I2	Filtered line – SD card side
D2	GND	Ground
E1	O3	Filtered line – IC side
E3	I3	Filtered line – SD card side
F2	GND	Ground
G1	O4	Filtered line – IC side
G3	I4	Filtered line – SD card side
H2	GND	Ground
I1	O5	Filtered line – IC side
I3	I5	Filtered line – SD card side
J2	DET	Card detection pin
K1	O6	Filtered line – IC side
K3	I6	Filtered line – SD card side

Figure 1. Pinout (bump side)



Note: For lower ground parasitics leading to better filtering performances and ESD robustness, GND bumps must be connected together on PCB. Ground loop inductance can be reduced by using multiple vias to make the connection to the ground plane.

2 Characteristics

Table 2. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2 level 4 - C = 150 pF, R = 330 Ω for IX pins:		kV
		Air discharge	±18	
		Contact discharge	±18	
		IEC 61000-4-2 level 4 - C = 150 pF, R = 330 Ω for OX pins:		
		Air discharge	±10	
		Contact discharge	±10	
Tj	Maximum junction temperature range		125	°C
T_{op}	Maximum operating temperature range		-40 to +125	°C
T_{stg}	Storage temperature range		-55 to +150	°C

Figure 2. Electrical characteristics (definitions)

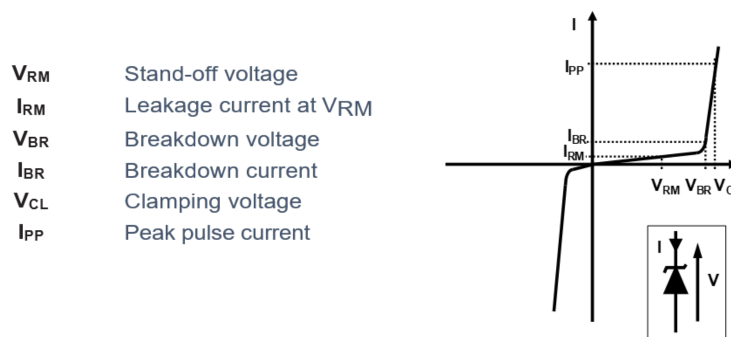


Table 3. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_{RM}	Reverse stand-off voltage					3	V
I_{RM}	Reverse leakage current at V_{RM}	V_{RM} = 3.0 V per line				20	nA
V_{BR}	Reverse breakdown voltage	I_{BR} = 1 mA		5		9	V
$R_{I/O}$	Serial resistance	Between any Ix and Ox			1.0		Ω
L(1)	Serial inductance	Between any Ix and Ox			1.0		nH
V_{CL}(1)	ESD clamping voltage	IEC 61000-4-2–C = 150 pF, R = 330 Ω, +8 kV contact discharge, measured at 30 ns			18.5		V
R_D(1)	Dynamic resistance	Tp = 100ns	IO-GND (positive polarity)		650		mΩ
			GND-IO (negative polarity)		320		mΩ
$C_{I/O-GND}$(1)	Line capacitance between Ix/Ox / GND	V_R = 0 V, 1 MHz, V_{OSC} = 30 mV			2.5	3.0	pF
$C_{VCC-GND}$(1)	Line capacitance between V_{CC} / GND	V_R = 0 V, 1 MHz, V_{OSC} = 30 mV			40		pF
$C_{DET-GND}$(1)	Line capacitance between DET / GND	V_R = 0 V, 1 MHz, V_{OSC} = 30 mV			40		pF

1. *Specified by design, not tested in production.*

2.1 Characteristics (curves)

Figure 3. Insertion Loss (S21) - I/Os

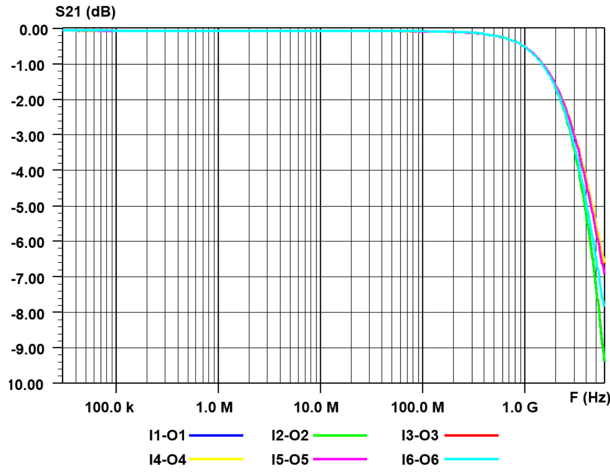


Figure 4. Insertion Loss (S21) - Vcc, DET

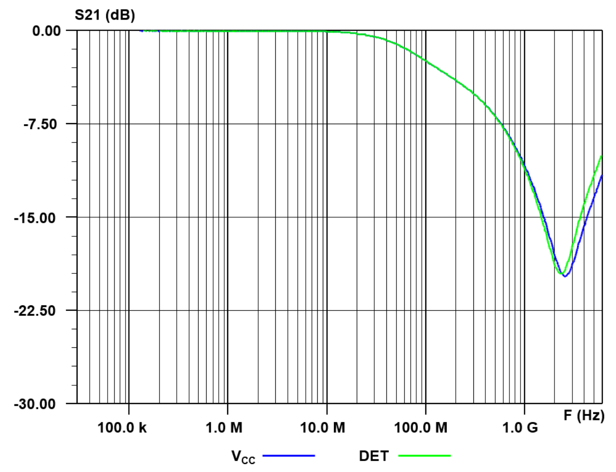


Figure 5. Digital crosstalk I6-O1

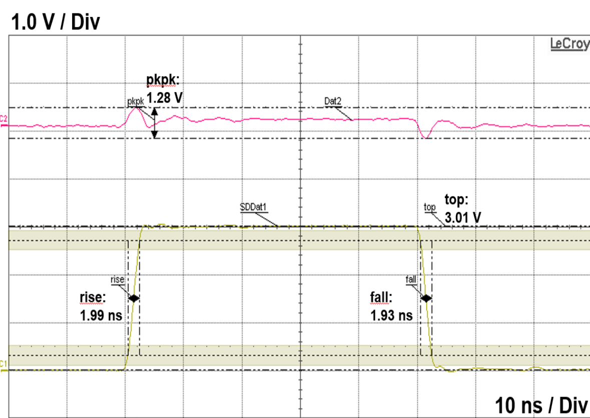


Figure 6. Analog crosstalk versus frequency

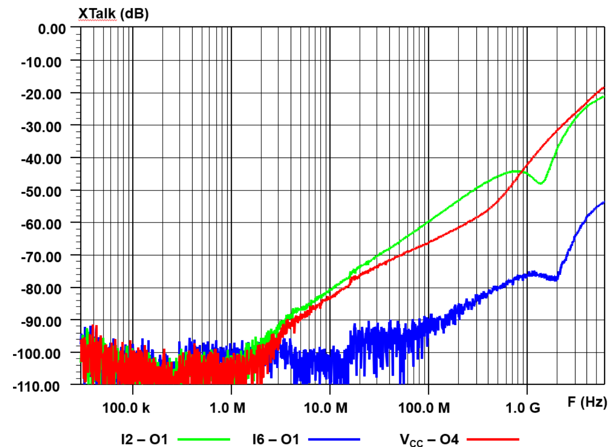
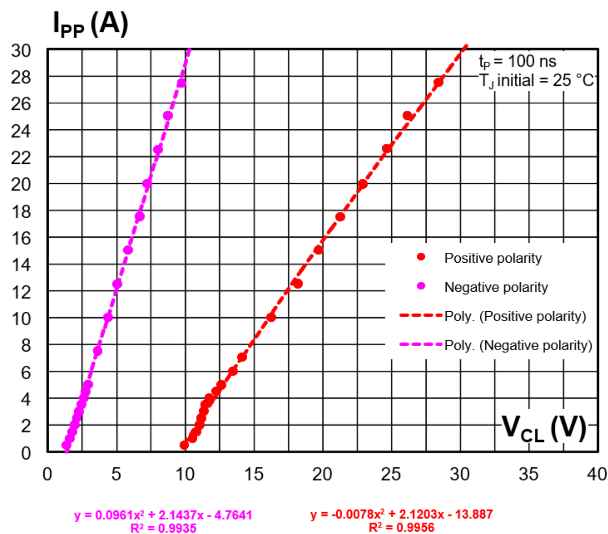


Figure 7. TLP characteristic



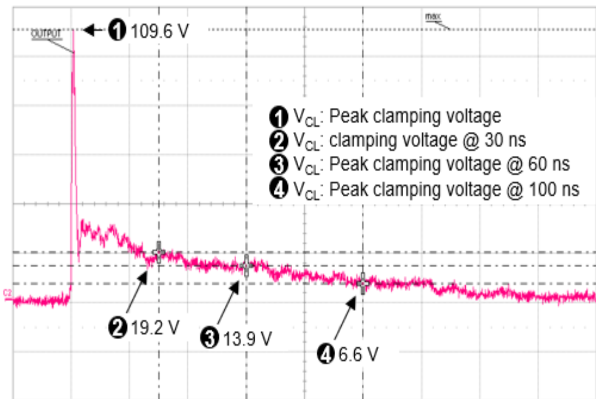


Figure 8. Response to IEC61000-4-2 – Ix pins (+8 kV contact)

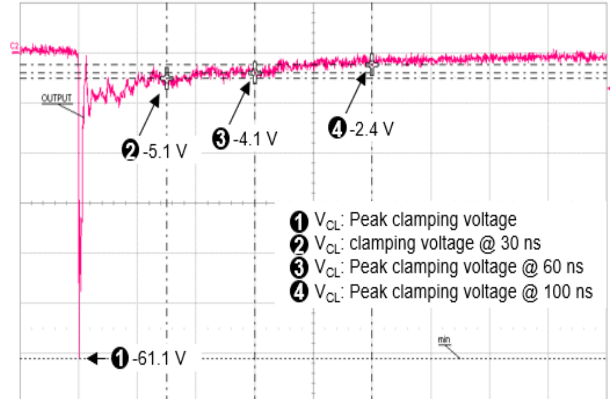


Figure 9. Response to IEC61000-4-2 – Ix pins (-8 kV contact)

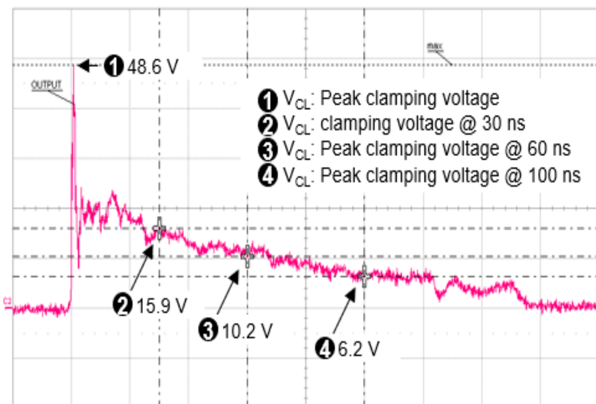


Figure 10. Response to IEC61000-4-2 – DET pin (+8 kV contact)

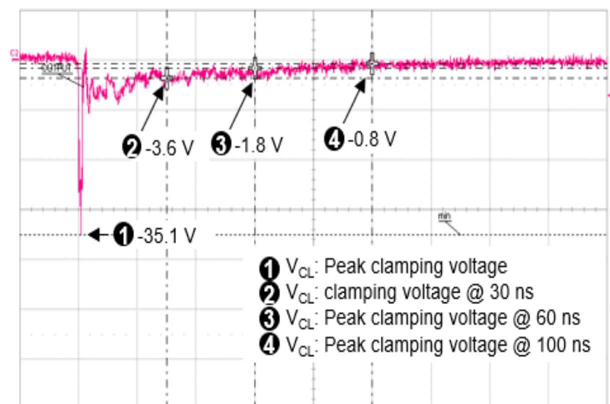
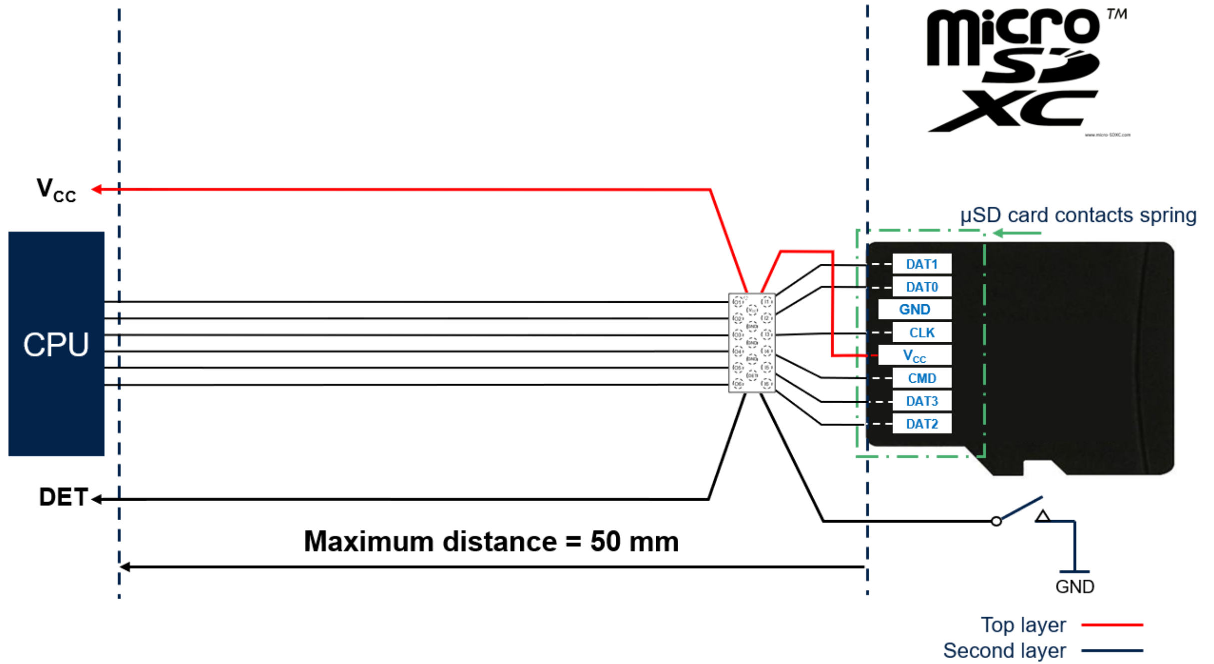


Figure 11. Response to IEC61000-4-2 – DET pin (-8 kV contact)

3 Technical information

3.1 Application diagram

Figure 12. Layout recommendation



Note: More information is available in the application notes:

- *AN1751, "EMI filters: recommendations and measurements"*
- *AN4541: "EMI Filters for SD3.0 card: High speed SD card protection and filtering devices"*

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 Chip scale package (CSP) pitch 0.4 mm package information

- Epoxy meets UL94, V0

Figure 13. Chip scale package (CSP) pitch 0.4 mm package outline

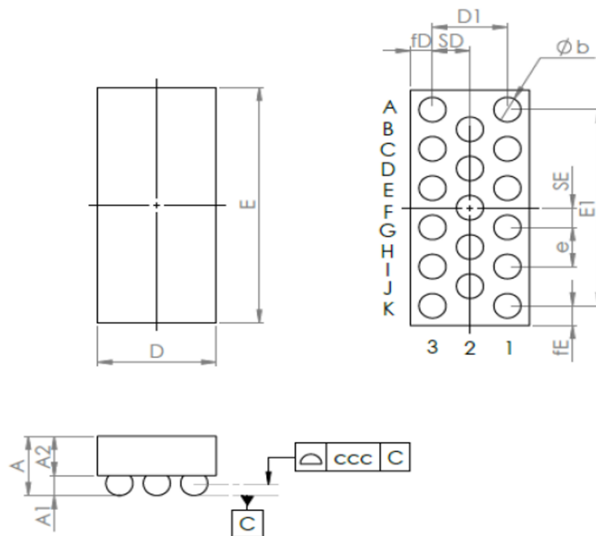


Table 4. Chip scale package (CSP) pitch 0.4 mm package mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.560	0.605	0.650
A1	0.180	0.205	0.230
A2	0.380	0.400	0.420
b	0.230	0.250	0.290
D	1.060	1.100	1.140
D1		0.692	
SD		0.346	
E	2.360	2.40	2.440
E1		2.00	
SE		0.200	
e		0.400	
fD	0.194	0.204	0.214
fE	0.190	0.200	0.210
ccc			0.075

Figure 14. **Footprint recommendations**

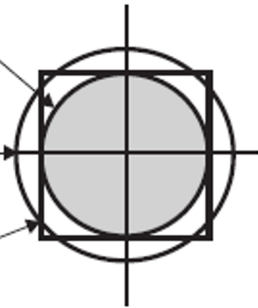
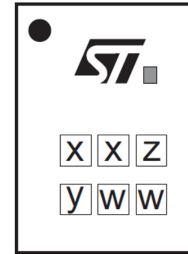
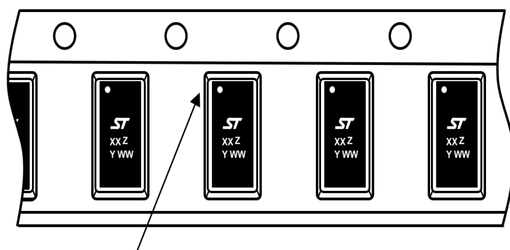


Figure 15. **Marking**



The marking can be rotated to differentiate assembly location. Refer to Ordering information table

Figure 16. **Package orientation in reel**



Note: Pocket dimensions are not to scale

Figure 17. **Tape and reel orientation**

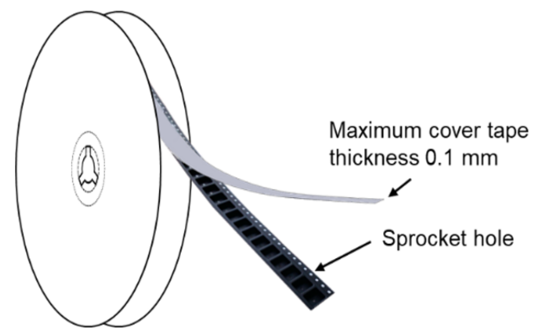


Figure 18. **7" reel dimension values**

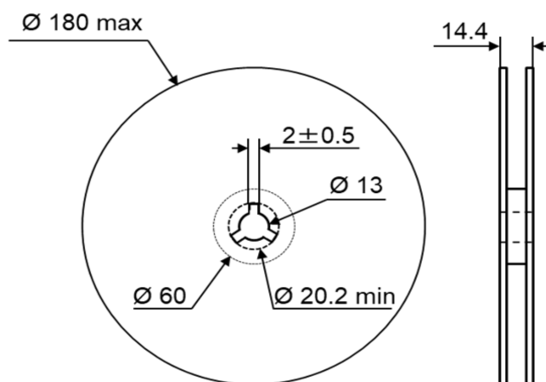
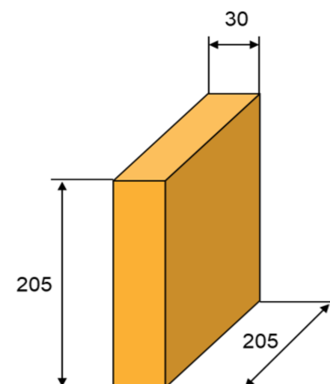


Figure 19. **Inner box dimensions (mm)**



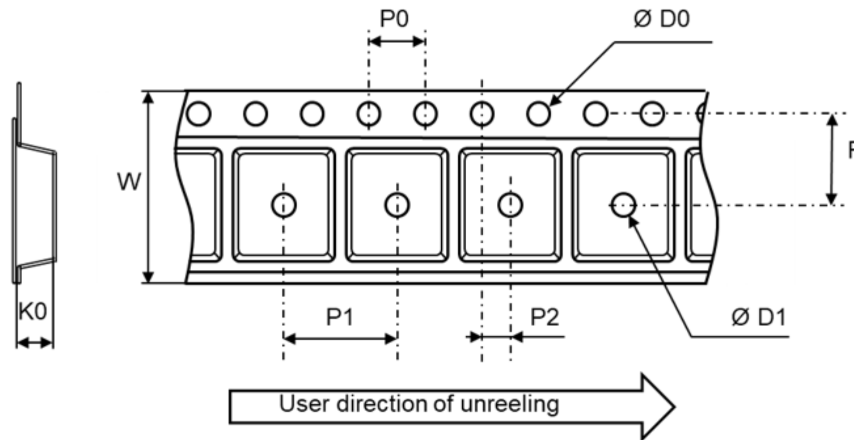
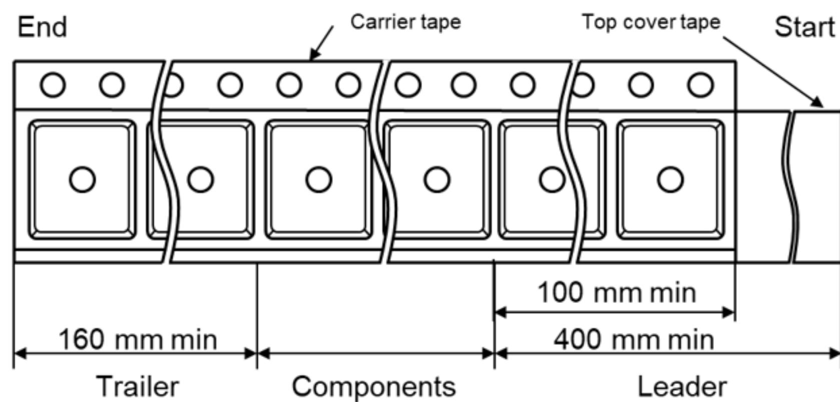


Figure 20. Tape and reel outline

Table 5. Tape dimension values

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
D0	1.45	1.50	1.60
D1	0.35	0.40	0.45
F	3.45	3.50	3.55
K0	0.64	0.69	0.74
P0	3.90	4.00	4.10
P1	3.90	4.00	4.10
P2	1.95	2.00	2.05
W	7.90	8.00	8.30

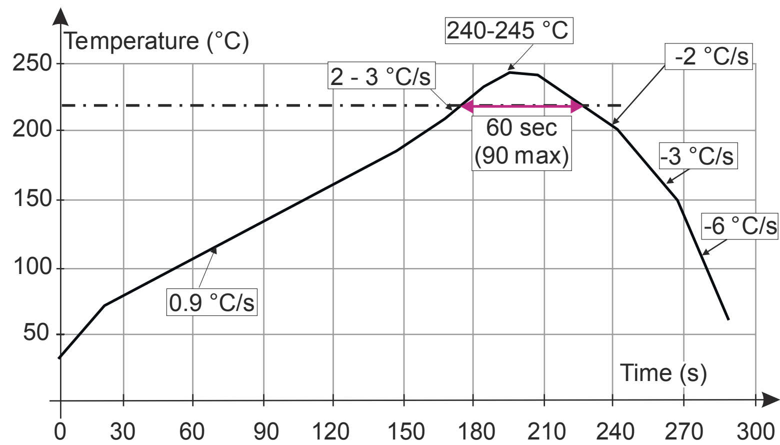
Figure 21. Tape leader and trailer dimensions



5 Recommendation on PCB assembly

5.1 Reflow profile

Figure 22. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

6 Ordering information

Figure 23. Ordering information scheme

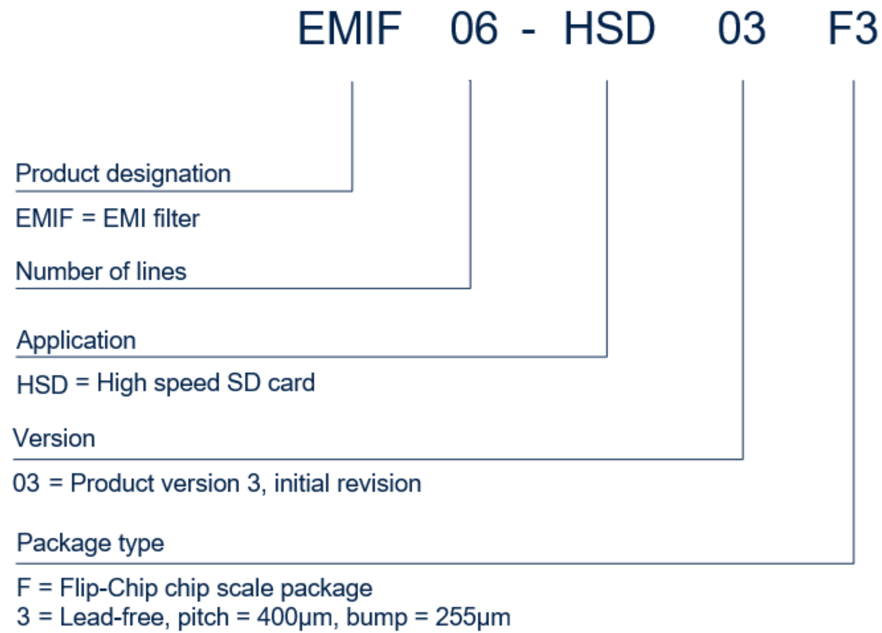


Table 6. Ordering information

Part number	Marking	Package	Weight	Base qty.	Delivery mode
EMIF06-HSD03F3	KK(1)	CSP P 0.4 mm	3.4 mg	5000	Tape and reel (7”)

1. *The marking can be rotated by multiples of 90° to differentiate assembly locations.*

Revision history

Table 7. **Document revision history**

Date	Version	Changes
19-Nov-2013	1	Initial release.
09-Jan-2014	2	Corrected typographical error.
06-Jan-2015	3	Added mention for new AN4541.
06-Oct-2016	4	Updated Figure 1. Pin configuration (bump side).
10-Jun-2022	5	Updated Section 4.1 Chip scale package (CSP) pitch 0.4 mm package information. Minor text changes.

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