UM11777

FRDMGD3160HB8EVM half-bridge evaluation board

Rev. 1 — 6 May 2022 User manual

Document information

Information	Content
Keywords	automotive, half-bridge, GD3160, gate driver
Abstract	This document describes key features and usage requirements for performing evaluation of GD3160 gate driver with FRDMGD3160HB8EVM.

Revision history

Rev	Date	Description
1	20220506	initial version

1 Important notice

IMPORTANT NOTICE

For engineering development or evaluation purposes only

NXP provides the product under the following conditions:

This evaluation kit is for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed-circuit board to make it easier to access inputs, outputs and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by connecting it to the host MCU computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application heavily depends on proper printed-circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The product provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end device incorporating the product. Due to the open construction of the product, it is the responsibility of the user to take all appropriate precautions for electric discharge. In order to minimize risks associated with the customers' applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

2 FRDMGD3160HB8EVM

Figure 1. FRDMGD3160HB8EVM

3 Getting started

NXP analog product development boards provide a platform for evaluating a broad range of NXP analog, mixed-signal, and power solution products. NXP analog product development boards incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology. NXP products offer a long battery life, a small form factor, reduced component counts, low cost, and improved performance in powering state-of-the-art systems.

The tool summary page for the FRDMGD3160HB8EVM evaluation board is at http://www.nxp.com/FRDMGD3160HB8EVM. The tool summary page provides information related to using the evaluation board. The page contains the following sections:

- Overview – A brief summary of the evaluation board and its capabilities
- Supported Devices – A list of devices that the evaluation board supports
- Specifications – An overview of the technical and functional specifications for the board
- Documents and Software/Design Resources – All of the information and resources required by users who have already purchased the FRDMGD3160HB8EVM. This section includes:
  - Design Tools & Files – Click the download button to download the board bill of materials and the Gerber files for the printed-circuit board (PCB) assemblies.
  - Printed Circuit Boards and Schematics – Click the download button to download a .pdf version of the FRDMGD3160HB8EVM board schematics.

The Get Started link in the upper left of the menu bar provides information applicable to using the FRDMGD3160HB8EVM.

3.1 Kit contents/packing list

The FRDMGD3160HB8EVM kit contents include:

- Complete assembly of FRDMGD3160HB8EVM evaluation board
- 3.3 V to 5.0 V KITGD31xTREVB translator board connected to FRDM-KL25Z
- USB cable, type A male/type mini B male, 3 ft
- 1.27 mm jumpers for configuration (included with kit boards)
- Quick start guide

3.2 Required equipment

The kit requires the following equipment:

- Compatible P6 SiC module
- DC link capacitor compatible with the SiC module
- 30 µH to 50 µH, high current air core inductor for double pulse testing
- HV power supply with protection shield and hearing protection
- 25 V, 1.0 A DC power supply
- 500 MHz 2.5 GS/s 4-channel oscilloscope
- Rogowski coil, PEM Model CWT Mini HF60R, or CTW MiniHF30 (smaller diameter)
- Isolated high-voltage probe (CAL Test Electric CT2593-1, LeCroy AP030)
- Digital voltmeter

3.3 System requirements

The kit requires the following to function properly with the software:

- Windows 7 or higher operating system

4 Getting to know the hardware

4.1 Overview

The FRDMGD3160HB8EVM is a half-bridge evaluation kit populated with two GD3160 single channel gate drive devices. The kit includes the Freedom KL25Z microcontroller hardware for interfacing a PC installed with FlexGUI software for communication to the serial peripheral interface (SPI) registers on the GD3160 gate drive devices in either daisy chain or standalone configuration.

The KITGD316xTREVB translator board is used to translate 3.3 V signals to 5.0 V signals between the MCU and the GD3160 gate drivers. The evaluation kit can be connected to a compatible insulated gate bipolar transistor (IGBT) or SiC module for half-bridge evaluations and applications development.

4.2 Board features

- Capability to connect to P6 SiC module for half-bridge evaluations
- Negative VEE gate low drive level (−3.9 V DC)
- VCCREG regulated high gate drive level (+15 V DC)
- Jumper configurable for disabling dead time fault protection when short-circuit testing
- Easy access power, ground, and signal test points
- Easy to install and use FlexGUI for interfacing via SPI through PC; software includes double pulse and short-circuit testing capability
- DC link bus voltage monitor on low-side driver via AMUXIN and AOUT
- Negative temperature coefficient (NTC) connection and configurable for monitoring module temperature

4.3 Device features

Table 1. Device features

Device	Description	Features
GD3160	The GD3160 is an advanced single channel gate driver for IGBT and SiC.	• Compatible with current sense and temp sense IGBTs • DESAT detection capability for detecting V_{CE} desaturation condition • Fast short-circuit protection for IGBTs with current sense feedback • Compliant with automotive safety integrity level (ASIL) C/D ISO 26262 functional safety requirements • SPI interface for safety monitoring, programmability, and flexibility • Integrated galvanic signal isolation • Integrated gate drive power stage capable of 10 A peak source and sink • Interrupt pin for fast response to faults • Compatible with negative gate supply • Compatible with 200 V to 1700 V IGBTs, power range > 125 kW

4.4 Board description

The FRDMGD3160HB8EVM is a half-bridge evaluation board populated with two GD3160 single channel IGBT or SiC gate drive devices. The board supports connection to an FRDM-KL25Z microcontroller for SPI communication configuration programming and monitoring. The board includes DESAT circuitry for short-circuit detection and implementation of GD3160 shutdown protection capabilities.

The evaluation board is designed to connect to a P6 SiC metal-oxide-semiconductor field-effect transistor (MOSFET) for evaluation of the GD3160 performance and capabilities.

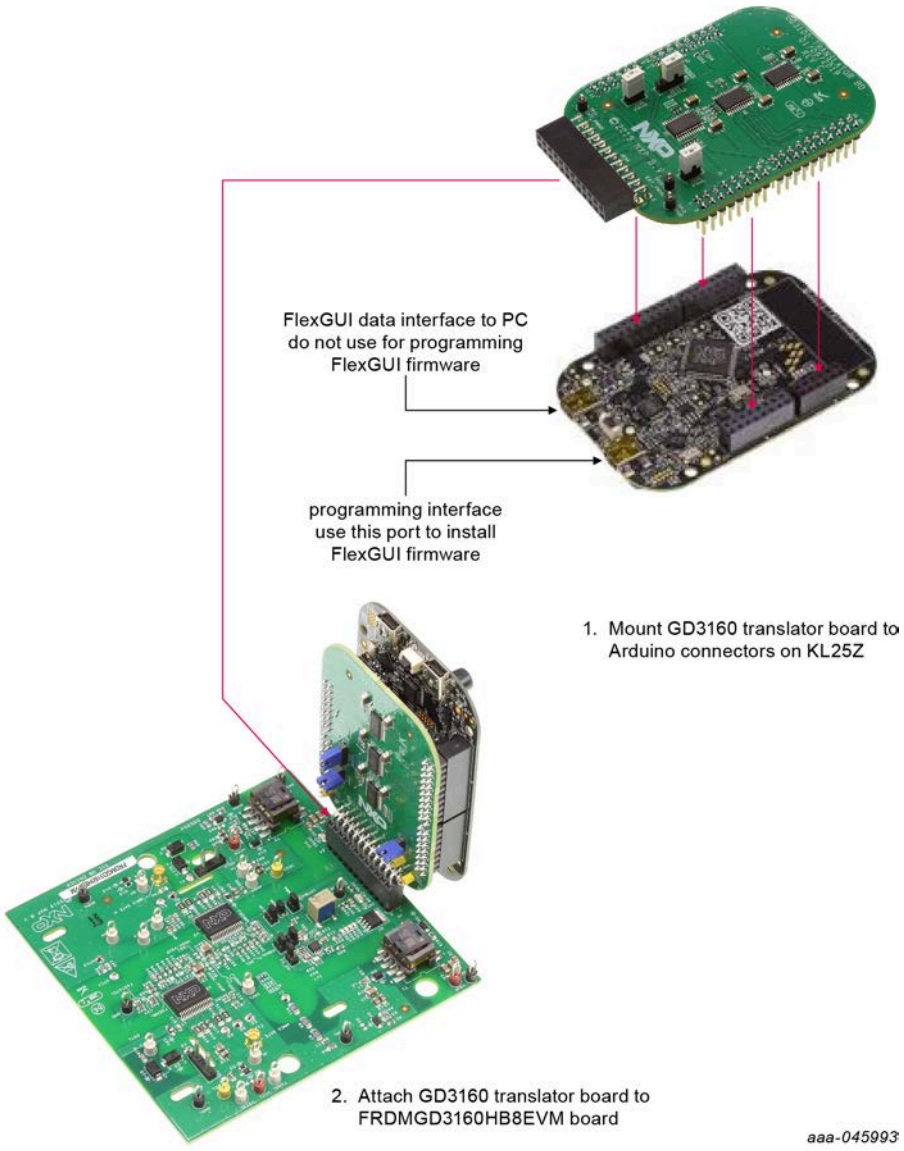

Figure 2. Connecting FRDM-KL25Z, FRDMGD3160HB8EVM and KITGD316xTREVB translator board

4.4.1 Low-voltage logic and control connector

The low-voltage domain is 12 V VSUP domain that interfaces with the MCU and GD3160 control registers through the 24-pin connector interface.

The low-side driver and high-side driver domains are driver control interfaces to SiC module single phase connections and test points.

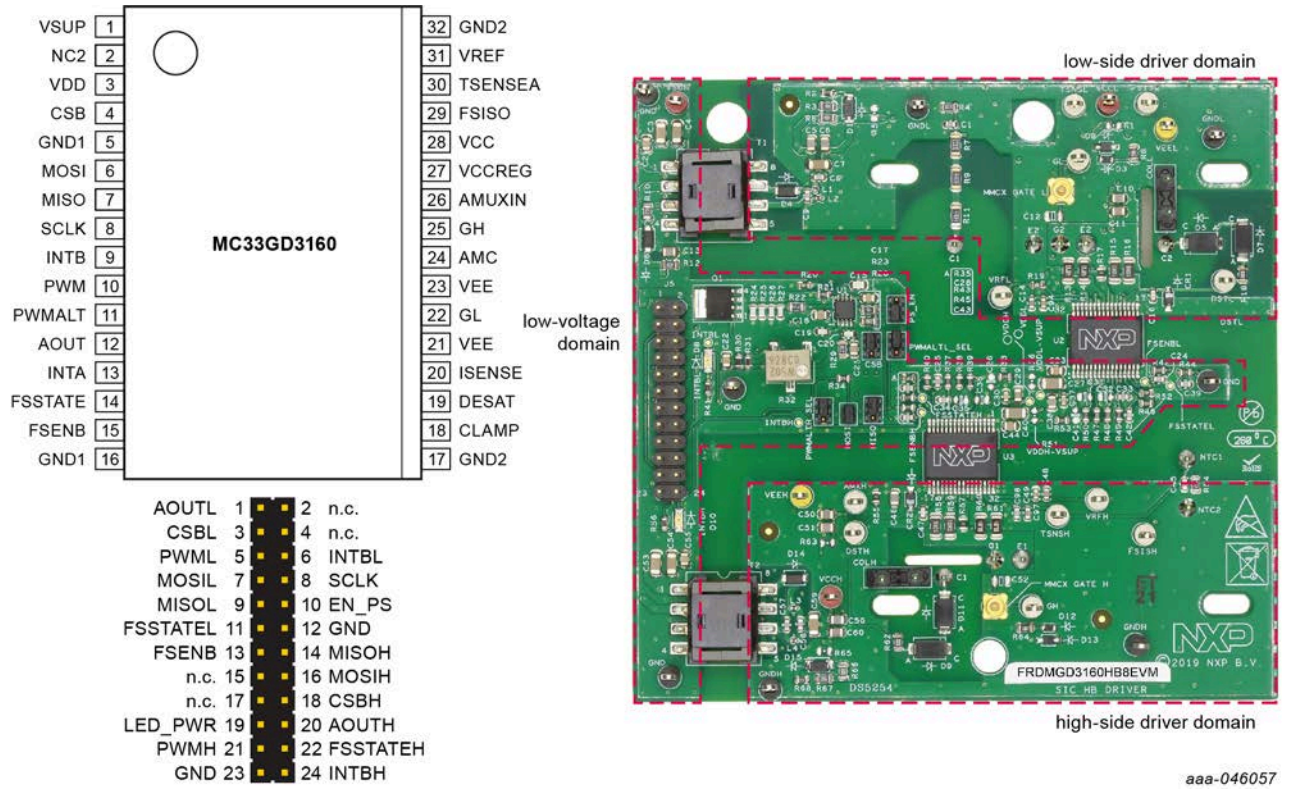

Figure 3. FRDMGD3160HB8EVM board voltage and interface domains

Table 2. Low-voltage domain 24-pin connector definitions

Pin	Name	Function
1	AOUTL	analog output duty cycle encoded signal (low side) for reading temperature via TSENSEA or voltage via AMUXIN
2	n.c.	not connected
3	CSBL	chip select bar (low side)
4	n.c.	not connected
5	PWML	pulse width modulation (PWM) input (low side)
6	INTBL	interrupt bar (low side)
7	MOSIL	master out slave in (low side)
8	SCLK	serial clock input
9	MISOL	master in slave out (low side)
10	EN_PS	MCU signal to enable flyback power supply for high-side VCC and low-side VCC
11	FSSTATEL	fail-safe state (low side)
12	GND	ground
13	FSENB	fail-safe enable (high side and low side)
14	MISOH	master in slave out (high side)
15	n.c.	not connected

Table 2. Low-voltage domain 24-pin connector definitions...*continued*

Pin	Name	Function
16	MOSIH	master out slave in (high side)
17	n.c.	not connected
18	CSBH	chip select bar (high side)
19	LED_PWR	USB 3.3 V power for INTB LEDs (high side and low side)
20	AOUTH	duty cycle encoded signal (high side)
21	PWMH	PWM input (high side)
22	FSSTATEH	fail-safe state (high side)
23	GND	ground
24	INTBH	interrupt bar (high side)

4.4.2 Test point definitions

All test points are clearly marked on the evaluation board. Figure 4 shows the location of various test points.

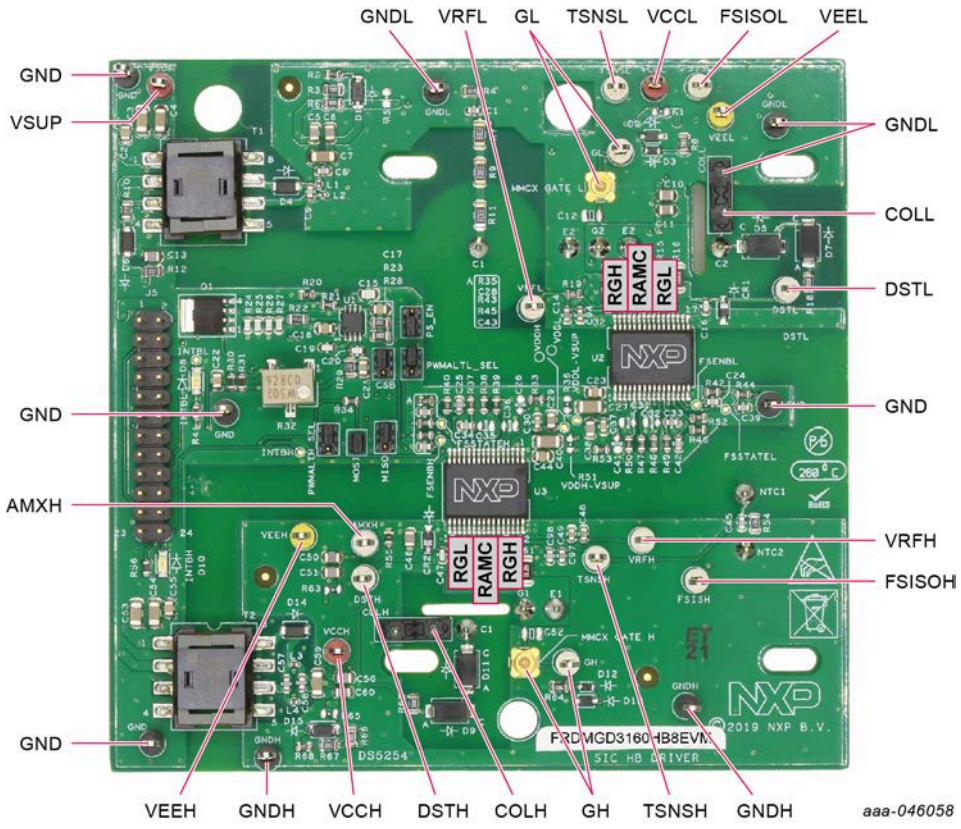

Figure 4. Key test point locations

Table 3. Test point definitions

Name	Test Point	Definition
Low-voltage domain		
GND	TP2	grounding point for low-voltage domain
VSUP	TP26	DC voltage source connection point for VSUP power input of GD3160 devices; typically supplied by vehicle battery +12 V DC
Low-side driver domain		
COLL	J90	collector test point/connection low side
DSTL	TP10	V_{CE} desaturation test point connected to high-side driver DESAT pin and circuitry
GL	TP5	module gate test point on low-side driver domain which is the charging pin of gate; including MMCX probe connection
GND	TP13, TP16, TP27	grounding point for low-side driver domain
GNDL	TP3, TP7	grounding point for isolated low-side driver grounding plane
TSNSL	TP8	test point connection to low-side gate drive TSENSE pin
VCCL	TP1	positive voltage supply test point for isolated circuitry and low-side driver domain
VEEL	TP4	negative voltage supply test point for low-side driver gate of IGBT or SiC module
VRFL	TP9	5.0 V reference test point for isolated analog circuitry on low-side driver
High-side driver domain		
AMXH	TP23	high-side driver test point for analog MUX input
COLH	J101	collector test point/connection high side
DSTH	TP25	V_{CE} desaturation test point connected to high-side driver DESAT pin and circuitry
GH	TP28	module gate test point on high-side driver domain which is the charging pin of gate; including MMCX probe connection
GNDH	TP31, TP32	grounding point for isolated high-side driver grounding plane
TSNSH	TP21	test point connection to high-side gate drive TSENSE pin
VCCH	TP29	positive voltage supply test point for isolated circuitry and high-side driver domain
VEEH	TP30	negative voltage supply test point for high-side driver gate of IGBT or SiC module
VRFH	TP22	5.0 V reference test point for isolated analog circuitry on high-side driver

4.4.3 Power supply and jumper configuration

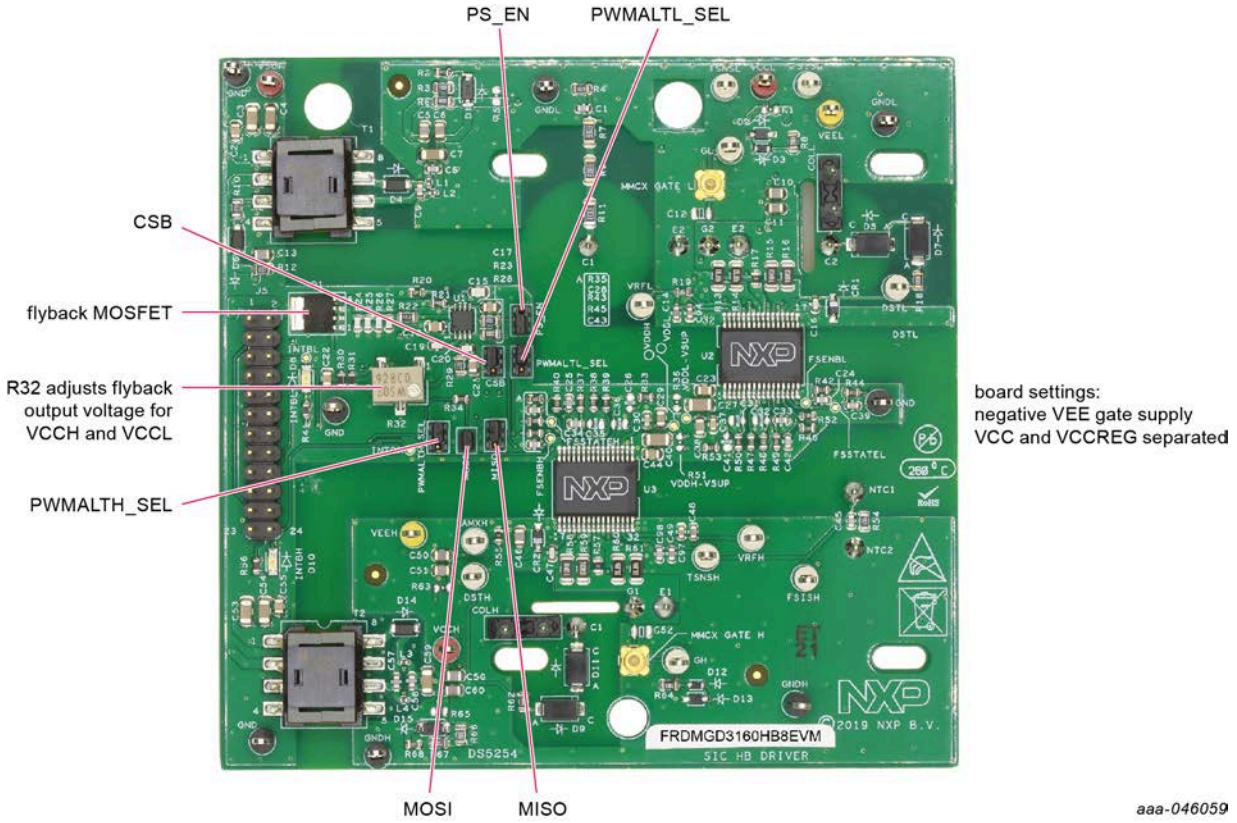

Figure 5. Power supply and jumper configuration

Table 4. Jumper definitions

Jumper	Position	Function
PWMALTL_SEL (J4)	1-2	dead time fault protection enabled (high side)
	2-3	dead time fault protection disabled (use for short-circuit testing)
PS_EN (J2)	1–2	flyback power supply enable controlled from MCU
	2–3	flyback power supply enable always on
CSB (J3)	1–2	normal operation
	2–3	daisy chain operation
PWMALTH_SEL (J7)	1-2	dead time fault protection enabled (low side)
	2-3	dead time fault protection disabled (use for short-circuit testing)
MOSI (J8)	open	daisy chain operation
	close	normal operation
MISO (J6)	1-2	normal operation
	2-3	daisy chain operation

Table 5. Power supply definition

Component	Definition
Flyback MOSFET (Q1)	AEC Q101-compliant logic level N-channel MOSFET
Potentiometer (R32)	adjusts resistor R3 for VCCH/VCCL and VEEH/VEEL tune VCC-GNDISO for +17 V

4.4.4 Bottom view

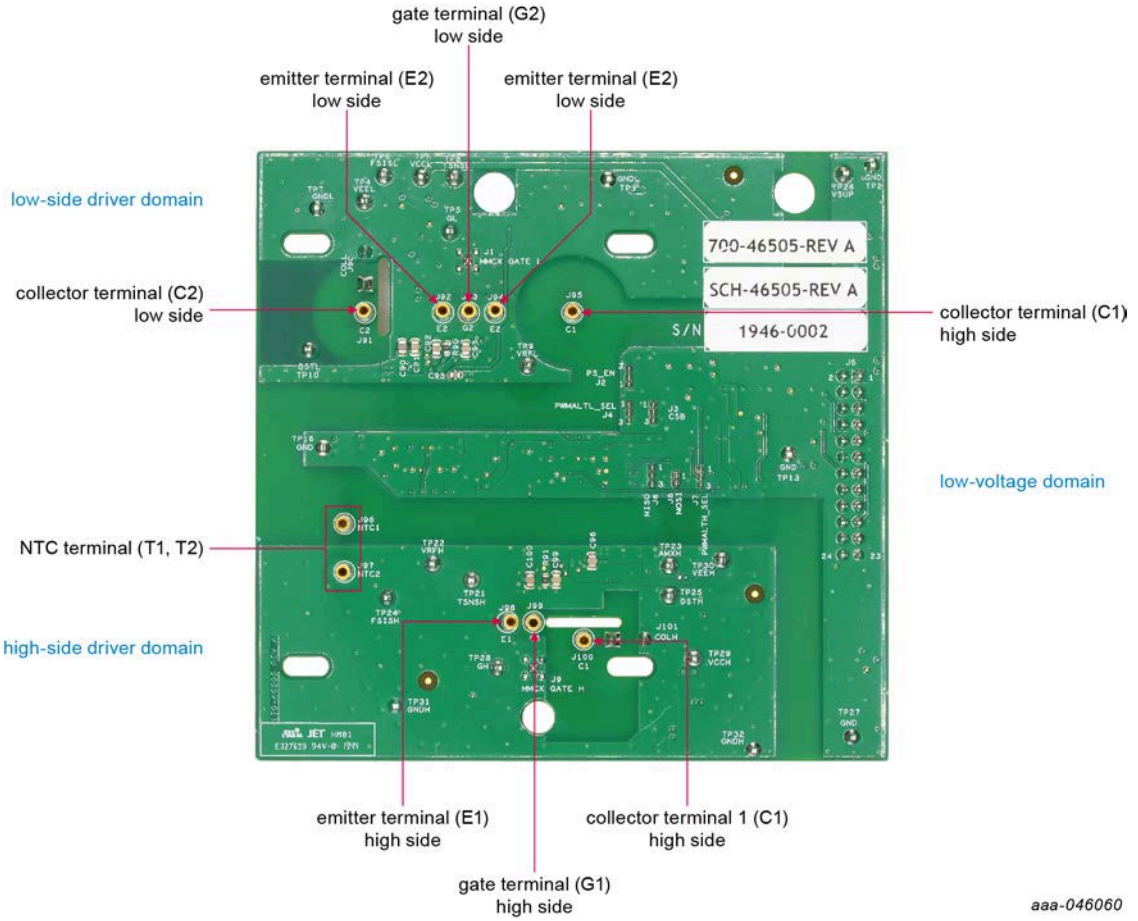

Figure 6. FRDMGD3100HB8EVM bottom view

4.4.5 Gate drive resistors

- RGH - gate high resistor in series with the GH pin at the output of the GD3160 gate high driver and P6 SiC module gate that controls the turn-on current for SiC MOSFET gate.
- RGL - gate low resistor in series with the GL pin at the output of the GD3160 gate low driver and P6 SiC module gate that controls the turn-off current for SiC MOSFET gate.
- RAMC - series resistor between P6 SiC module gate and AMC input pin of the GD3160 driver for gate sensing and active Miller clamping.

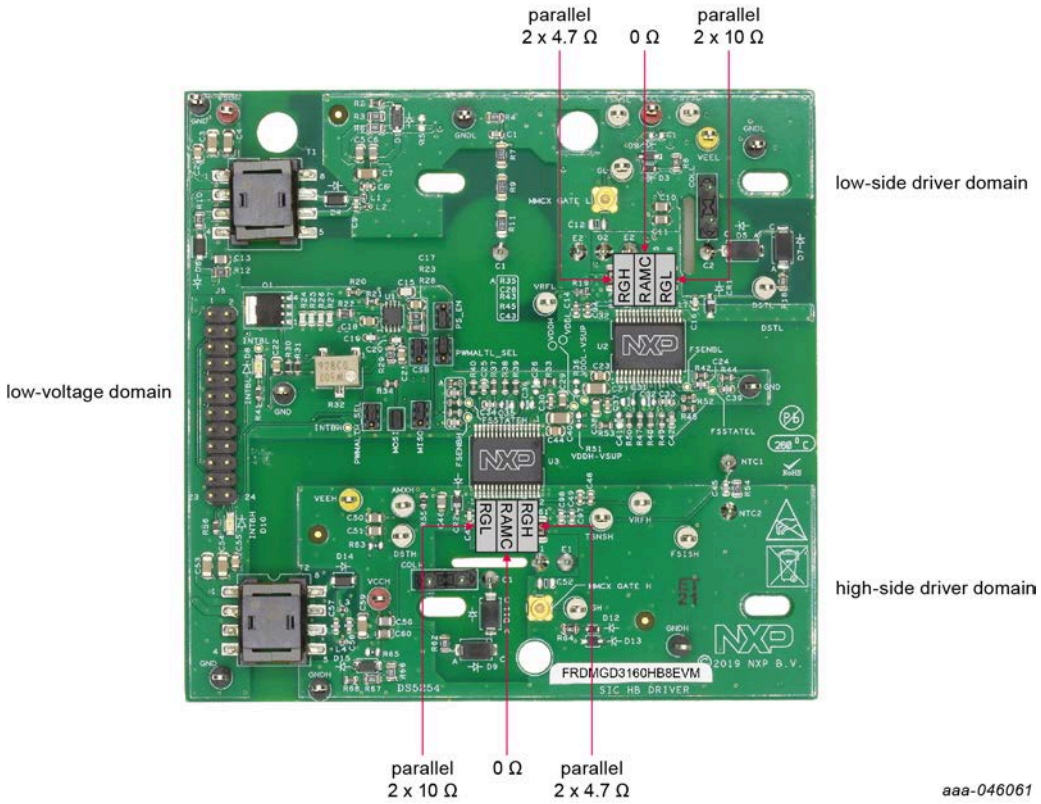

Figure 7. Gate drive resistors

4.4.6 LED interrupt indicators

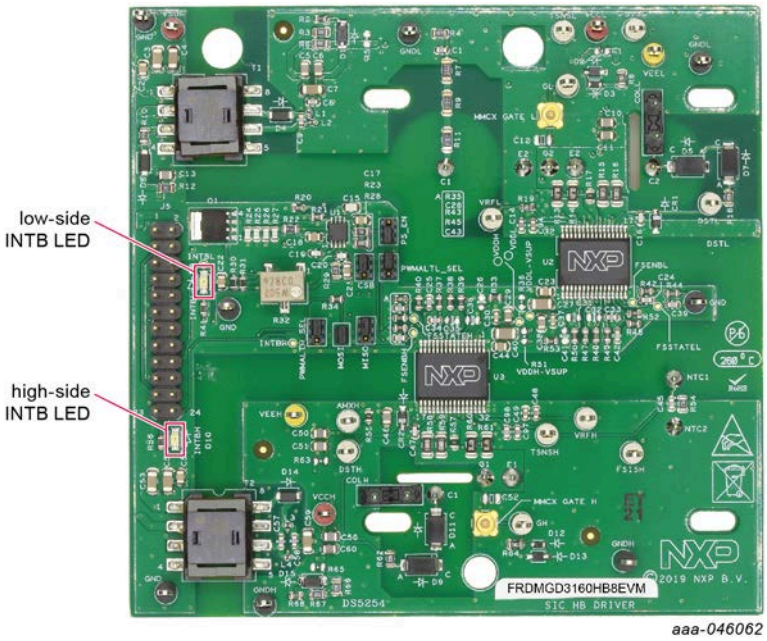

Figure 8. LED interrupt indicators

Table 6. LED interrupt indicators

LED	Description
Low-side INTB	connected to the INTB output pin of low-side driver indicating reported fault status when on (active LOW)
High-side INTB	connected to the INTB interrupt output pin of high-side driver indicating reported fault status when on (active LOW)

4.5 Kinetis KL25Z Freedom board

The Freedom KL25Z is an ultra low-cost development platform for Kinetis L series MCU built on Arm Cortex-M0+ processor.

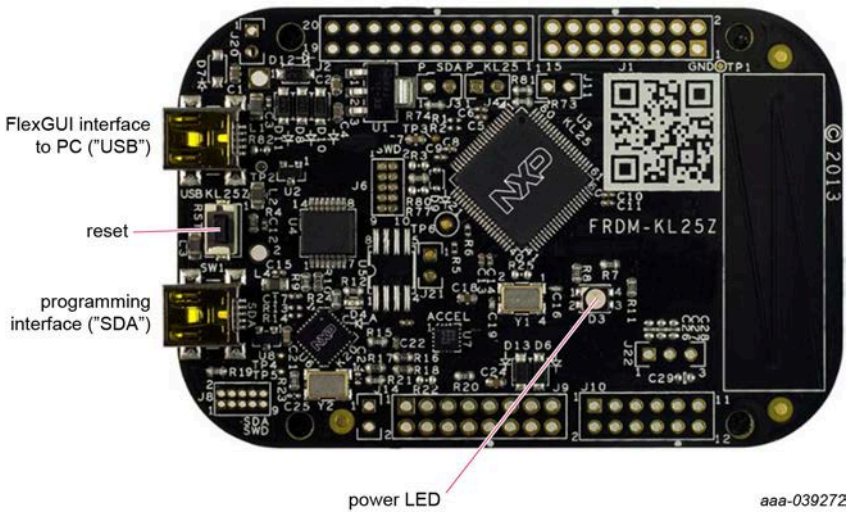

Figure 9. Freedom development platform

4.6 3.3 V to 5.0 V translator board

KITGD316xTREVB translator enables level shifting of signals from MCU 3.3 V to 5.0 V SPI communication.

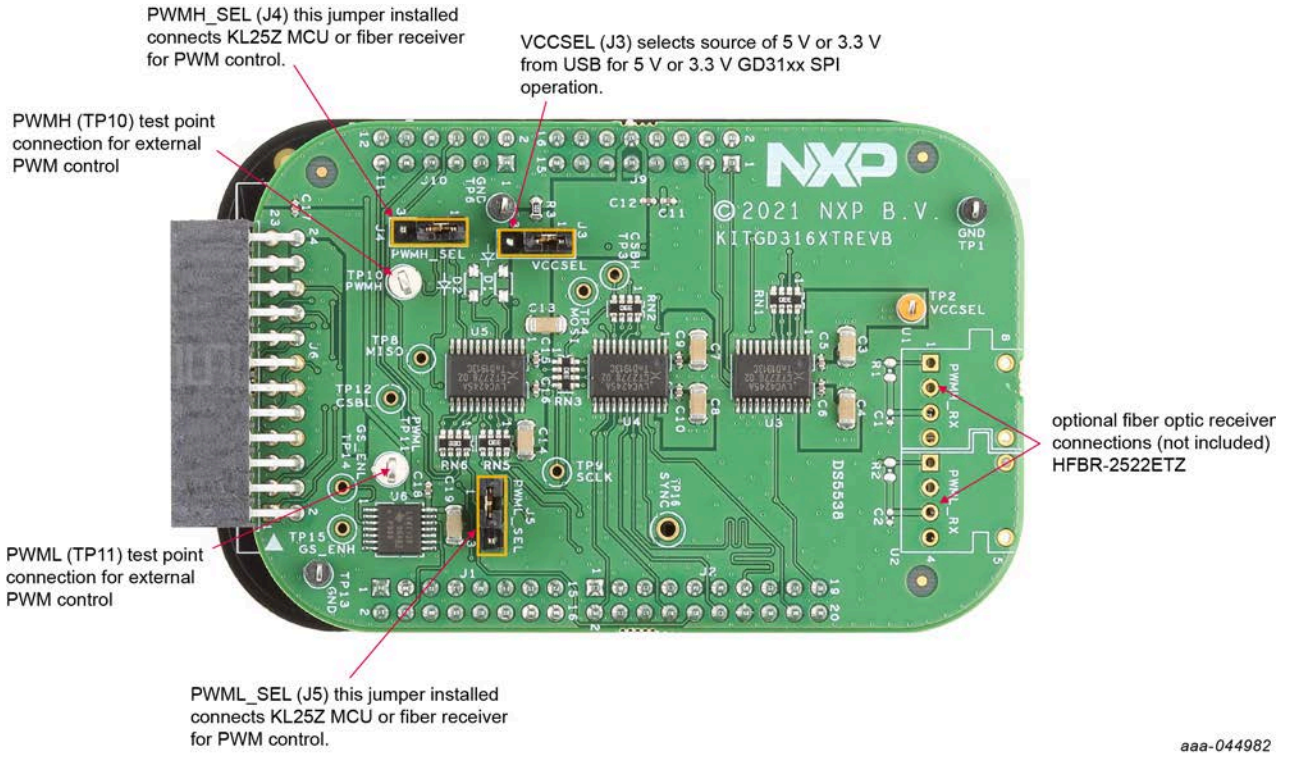

Figure 10. Translator board

Table 7. Translator board jumper definitions

Jumper	Position	Function
VCCSEL (J3)	1-2	selects 5.0 V for 5.0 V compatible gate drive
	2-3	selects 3.3 V for 3.3 V compatible gate drive
PWMH_SEL (J4)	1-2	selects PWM high-side control from KL25Z MCU
	2-3	selects PWM high-side control from fiber optic receiver inputs
PWML_SEL (J5)	1-2	selects PWM low-side control from KL25Z MCU
	2-3	selects PWM low-side control from fiber optic receiver inputs

5 Configuring the hardware

FRDMGD3160HB8EVM is connected to a GD3160 translator board and a FRDM-KL25Z board as shown in Figure 11. Double pulse and short-circuit testing can be conducted using a Windows based PC with FlexGUI software.

Suggested equipment needed for test:

- Rogowski coil high-current probe
- High-voltage differential voltage probe
- High sample rate digital oscilloscope with probes
- DC link capacitor
- SiC MOSFET P6 module
- Windows based PC
- High-voltage DC power supply for DC link voltage
- Low-voltage DC power supply for VSUP
  - +12 V DC gate drive board low-voltage domain
- Voltmeter for monitoring high-voltage DC link supply
- Load coil for double pulse and short-circuit testing

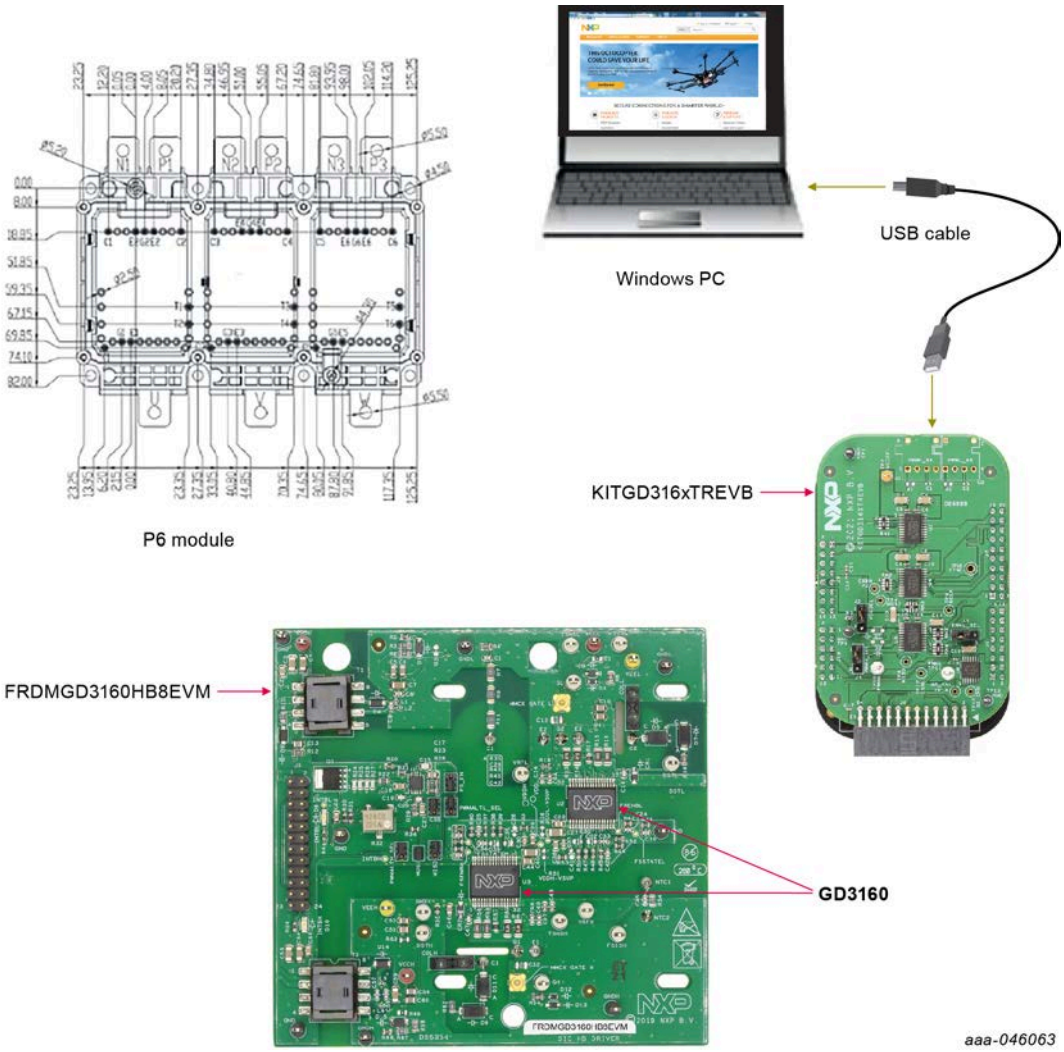

Figure 11. Evaluation board and system setup

6 Installation and use of software tools

Software for FRDMGD3160HB8EVM is distributed with the FlexGUI tool (available on NXP.com). Necessary firmware comes pre-installed on the FRDM-KL25Z with the kit.

Even if the user intends to test with other software or PWM, it is recommended to install this software as a backup or to help debugging.

6.1 Installing FlexGUI on your computer

The latest version of FlexGUI supports all versions of GD31xx gate drivers. It is designed to run on any Windows 10 or Windows 8 based operating system. To install the software, do the following:

1. Go to www.nxp.com/FlexGUI and click **Download**.
2. When the FlexGUI software page appears, click **Download** and select the version associated with your PC operating system.
3. FlexGUI wizard creates a shortcut, an NXP FlexGUI icon appears on the desktop. By default, the FlexGUI executable file is installed at **C:\NXP_GD31xx_GUI-x.x.x.msi**. Installing the device drivers overwrites any previous FlexGUI installation and replaces it with a current version containing the GD31xx drivers. However, configuration files from the previous version remain intact.

6.2 Configuring the FRDM-KL25Z microcode

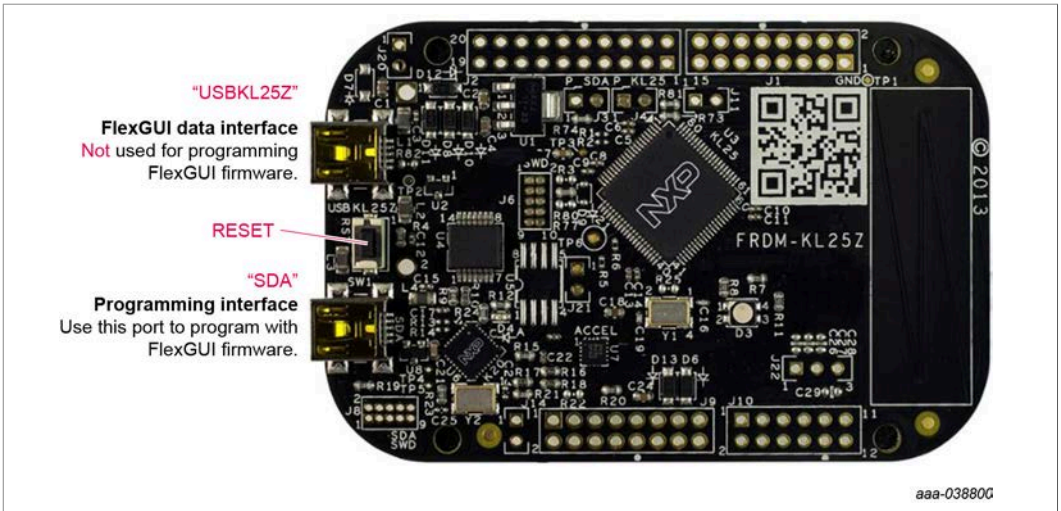

Figure 12. FRDM-KL25Z setup and interface

By default, the FRDM-KL25Z delivered with this kit is preprogrammed with the current and most up-to-date firmware available for the kit.

A way to check quickly that the microcode is programmed and the board is functioning properly, is to plug the KL25Z into the computer, open FlexGUI, and verify that the software version at the bottom is 6.4 or later (see Figure 13).

If a loss of functionality following a board reset, reprogramming, or a corrupted data issue, the microcode may be rewritten per the following steps:

1. To clear the memory and place the board in boot loader mode, hold down the reset button while plugging a USB cable into the **OpenSDA** USB port.
2. Verify that the board appears as a BOOTLOADER device and continue with step 3. If the board appears as KL25Z, you may go to step 6.
3. Download the **Firmware Apps** .zip archive from the PEmicro OpenSDA webpage (http://www.pemicro.com/opensda/). Validate your email address to access the files.
4. Find the most recent MDS-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA and copy/drag-and-drop into the **BOOTLOADER** device.
5. Reboot the board by unplugging and replugging the connection to the **OpenSDA** port. Verify now that the device appears as a KL25Z device to continue.
6. Locate the most recent KL25Z firmware; which is distributed as part of the FlexGUI package.
   a. From the FlexGUI install directory or zip file, downloaded, find the firmware bin file “flexgui-fw-KL25Z_usb_hid_gd31xx-Vx.x.x.bin”.
   b. This .bin file is a product/family-specific configuration file for FRDM-KL25Z containing the pin definitions, SPI/PWM generation code, and pin mapping assignments necessary to interface with the translator board as part of FRDMGD3160HB8EVM.
7. With the KL25Z still plugged through the **OpenSDA** port, copy/drag-and-drop the .bin file into the KL25Z device memory. Once done, disconnect the USB for OpenSDA port and plug into the other USB port, labeled **KL25Z**.
   a. The device may not appear as a distinct device to the computer while connected through the KL25Z USB port, this is normal.
8. The FRDM-KL25Z board is now fully set up to work with FRDMGD3160HB8EVM and the FlexGUI.
   a. There is no software stored or present on either the driver or translator boards, only on the FRDM-KL25Z MCU board.

All uploaded firmware is stored in non-volatile memory until the reset button is hit on the FRDM-KL25Z. There is no need to repeat this process upon every power up, and there is no loss of data associated with a single unplug event.

6.3 Using the FlexGUI

The FlexGUI is available from http://www.nxp.com/FlexGUI as an evaluation tool demonstrating GD31xx-specific functionality, configuration, and fault reporting. FlexGUI also includes basic capacity for the FRDMGD3160HB8EVM to control an IGBT or SiC module, enabling double pulse or short-circuit testing.

SPI messages can be realized graphically or in hexadecimal format. CSB is selectable to address one or both GD31xx on the board via daisy chain. See Figure 13 to Figure 32 for FlexGUI for GD31xx internal register read and write access.

Starting FlexGUI for GD31xx

- FlexGUI install program (C:\NXP_GD31xx_GUI-x.x.x.msi)
- Download FlexGUI and run the install program on your PC.
- When you start the application, Figure 13 allows you to select the target application board, feature set (standard or daisy chain), target MCU, and USB interface. Leave all settings as shown.

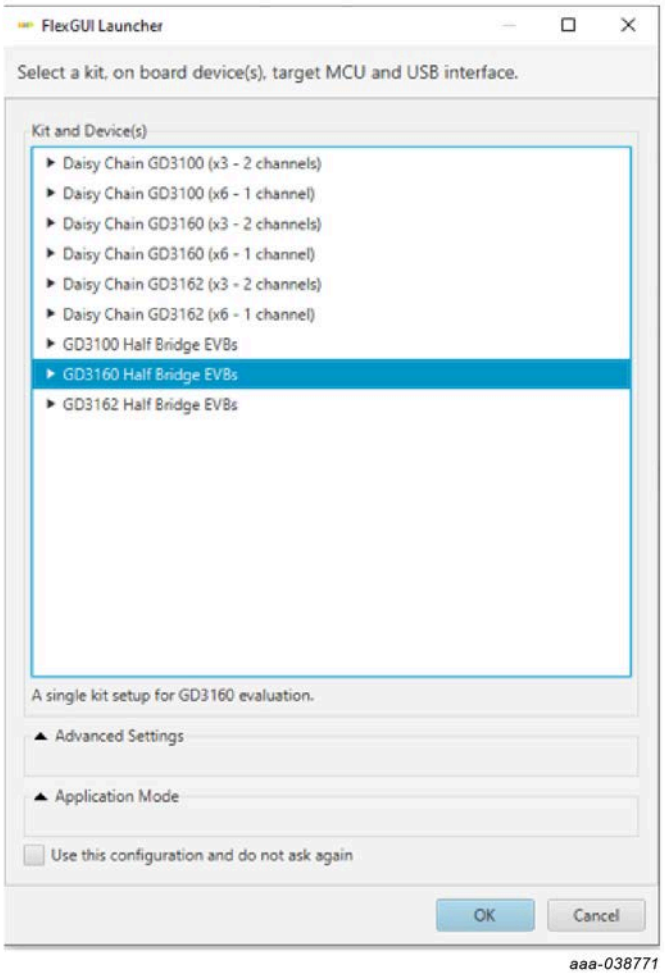

Figure 13. Kit selection

FlexGUI settings

- Access settings by selecting Settings from the File menu

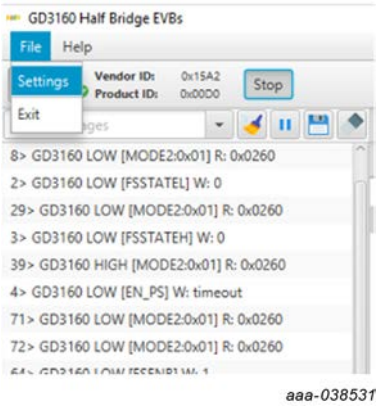

Figure 14. GUI settings menu

- The Loader and Logs settings are shown below:

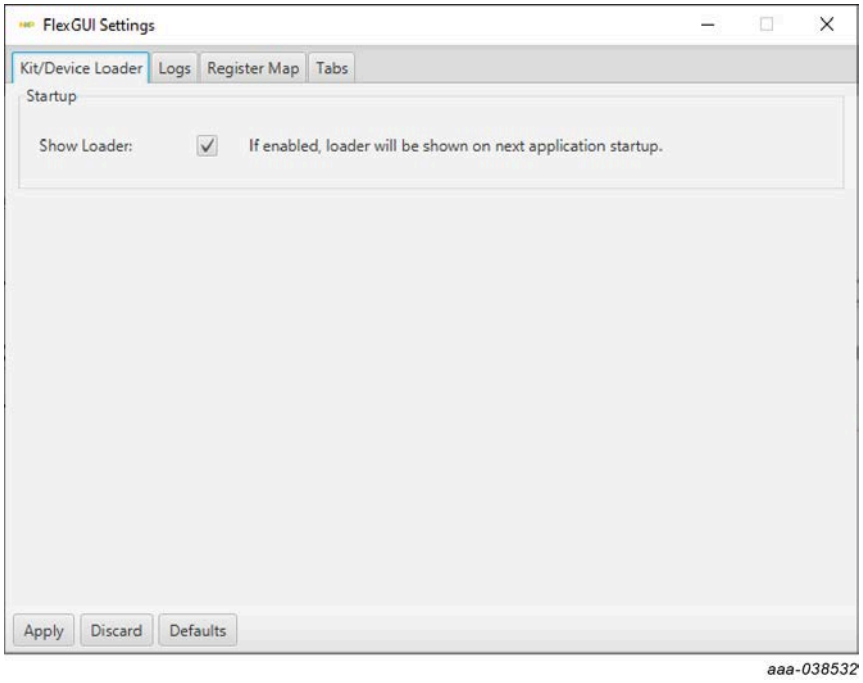

Figure 15. Loader settings

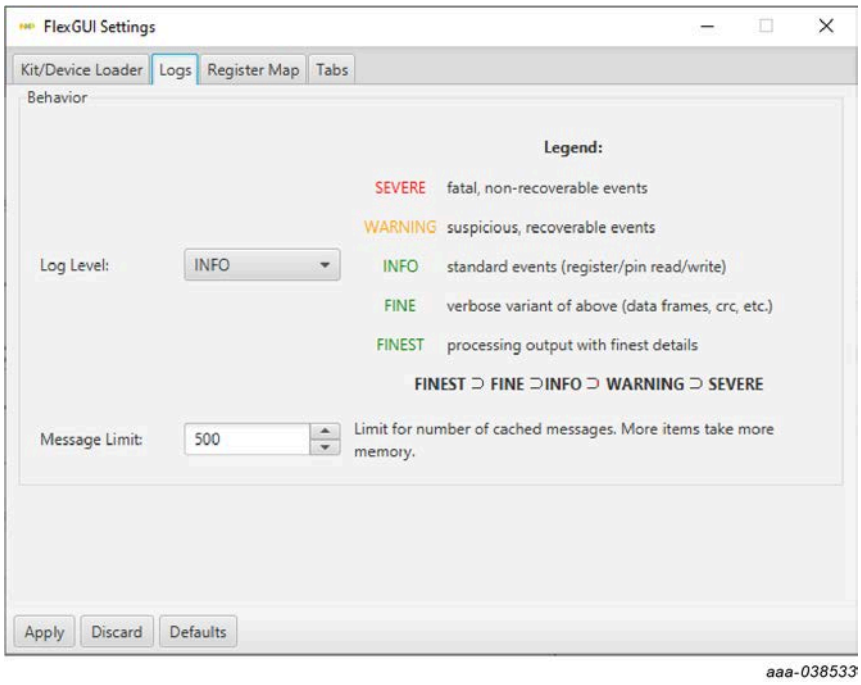

Figure 16. Logs settings

- Access settings by selecting Settings from the File menu.
- The Register Map and Tabs settings are shown below:

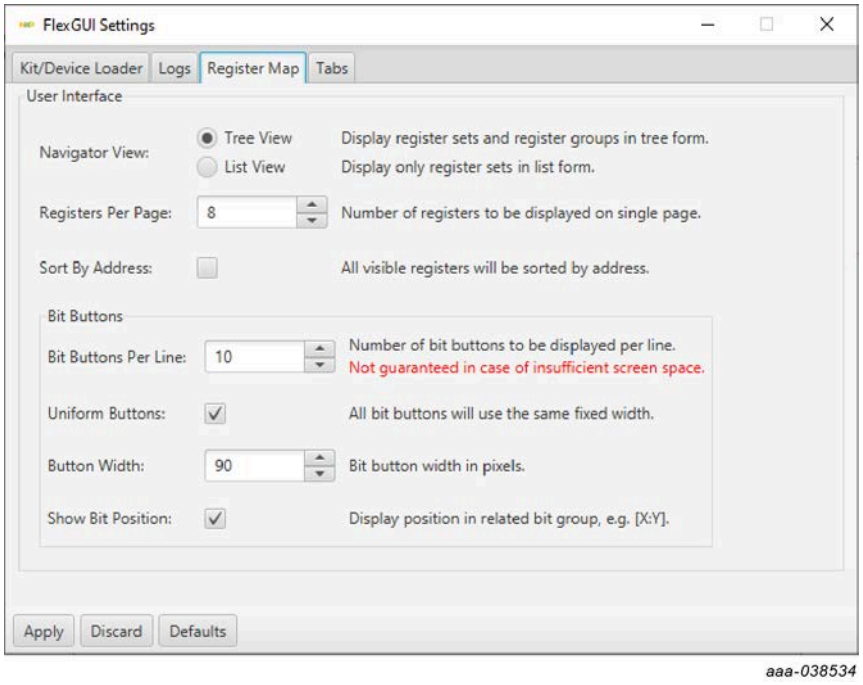

Figure 17. Register map settings

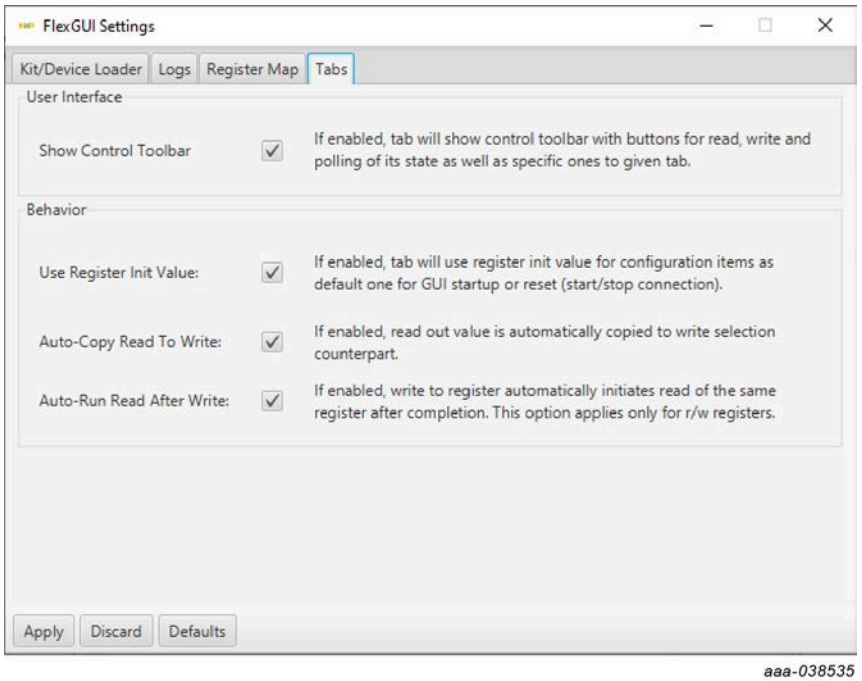

Figure 18. Tabs settings

Command Log window

- The Command Log area informs the user about application events.

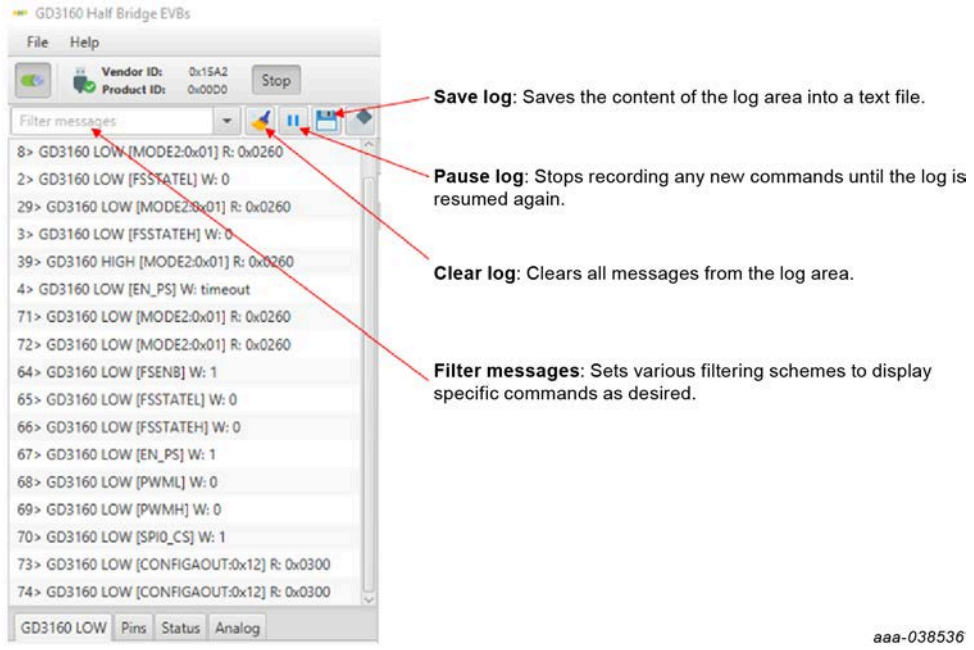

Figure 19. Command Log area

Global workspace controls

- Always visible in the lower left corner of the main application window.
  - GD3160 tab functionality
    - Switch modes between run and configuration mode
    - Set SPI frequency
    - Check pin status and clear faults if needed
    - Poll/read analog measurements

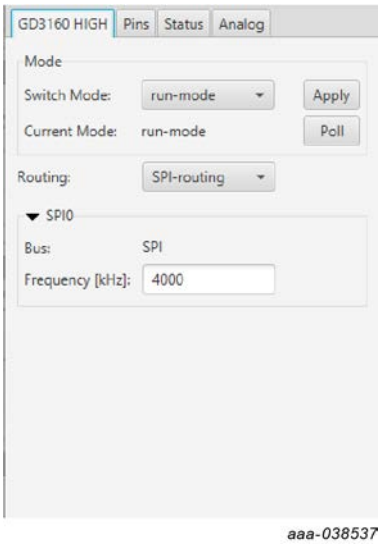

Figure 20. Device pins settings and status menus

- Pins tab functionality
  - Set control levels. Default values are shown.
  - Control pins set values to a default to a functional state.
    - FSENB - enable/disable fail-safe enable
    - EN_PS - enables flyback supply on EVB at 17 V V_{CC} on high side and low side
    - FSSTATEL and FSSTATEH set the fail-safe state when FSENB is enabled
    - PWML and PWMH set the default state PWM inputs for high side and low side

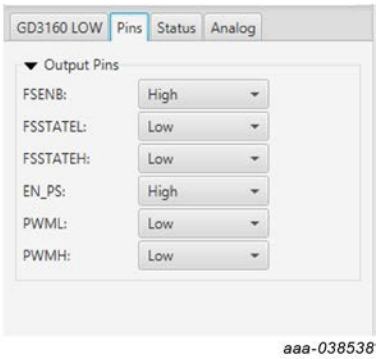

Figure 21. Pins tab functionality

- Status tab functionality
  - Monitors Status 1 and Status 2 fault bits. Bits that are set are shown in red.
  - Ability to clear all faults and automatically poll status registers.

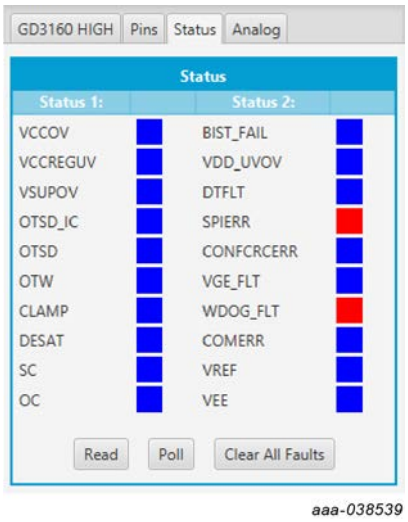

Figure 22. Status tab functionality

- Analog tab functionality
  - Read and poll ADC values from the high-voltage domain
  - Displays raw ADC and converted values

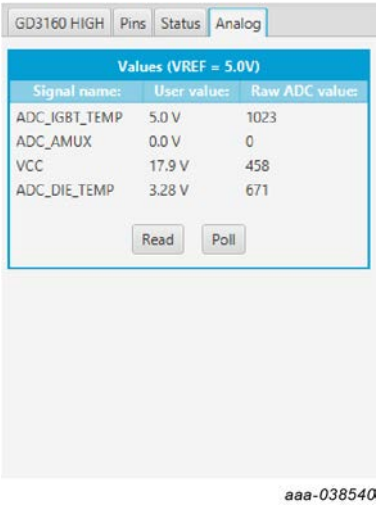

Figure 23. Analog tab functionality

Register map

- Registers are grouped according to function; independent lines to read and write the registers
- Individual registers can be read by clicking the R button and can be written by using the W button.
- Copy button to copy the read values to the write line; can be set to copy automatically
- Reset button to undo the changes on the write line and reset to the previous value
- Global register controls perform the selected command on all registers with the checkbox selected.

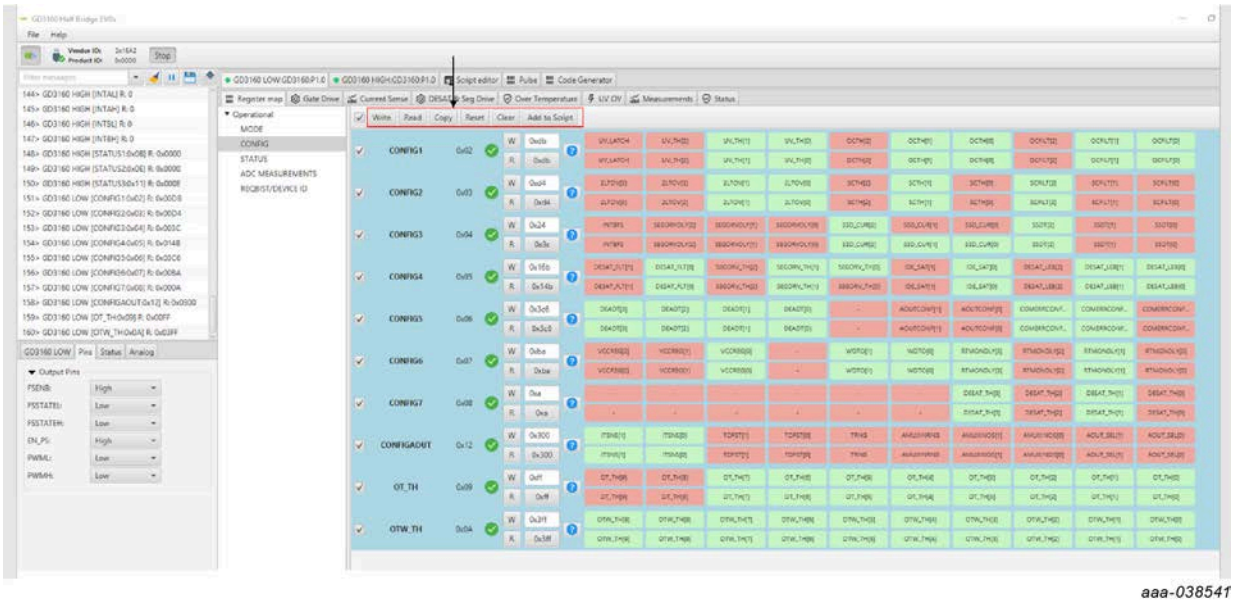

Figure 24. Register map

Gate Drive tab

- Allows setting of parameters related to the gate drive; controls are disabled when not in config mode
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

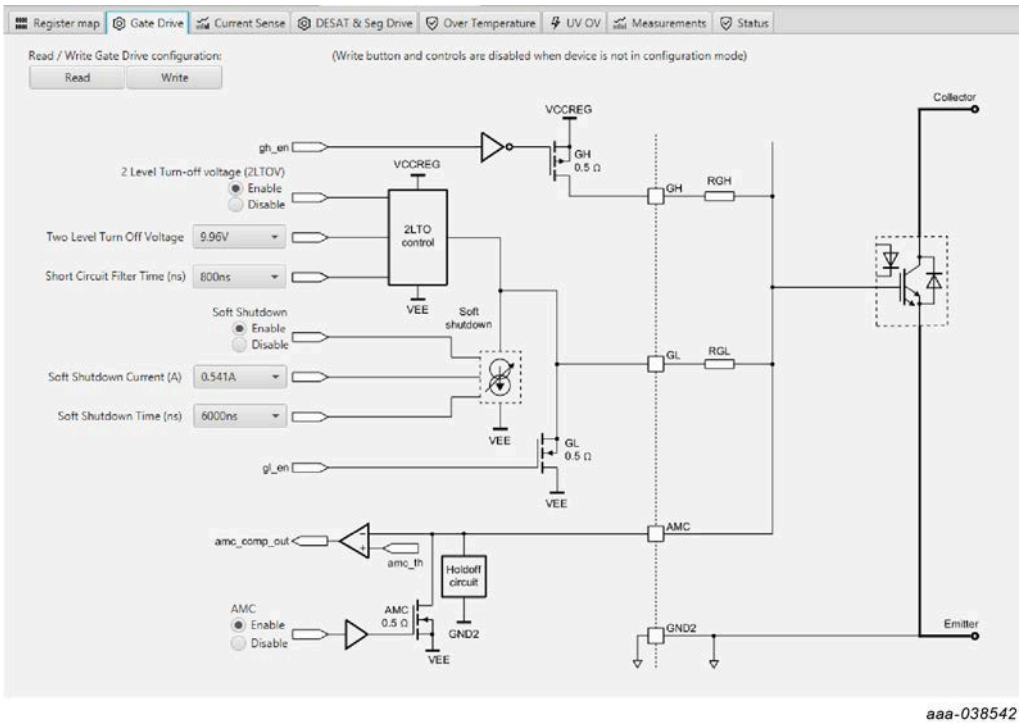

Figure 25. Gate drive tab

Current Sense tab

- Allows setting of parameters related to current sense
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

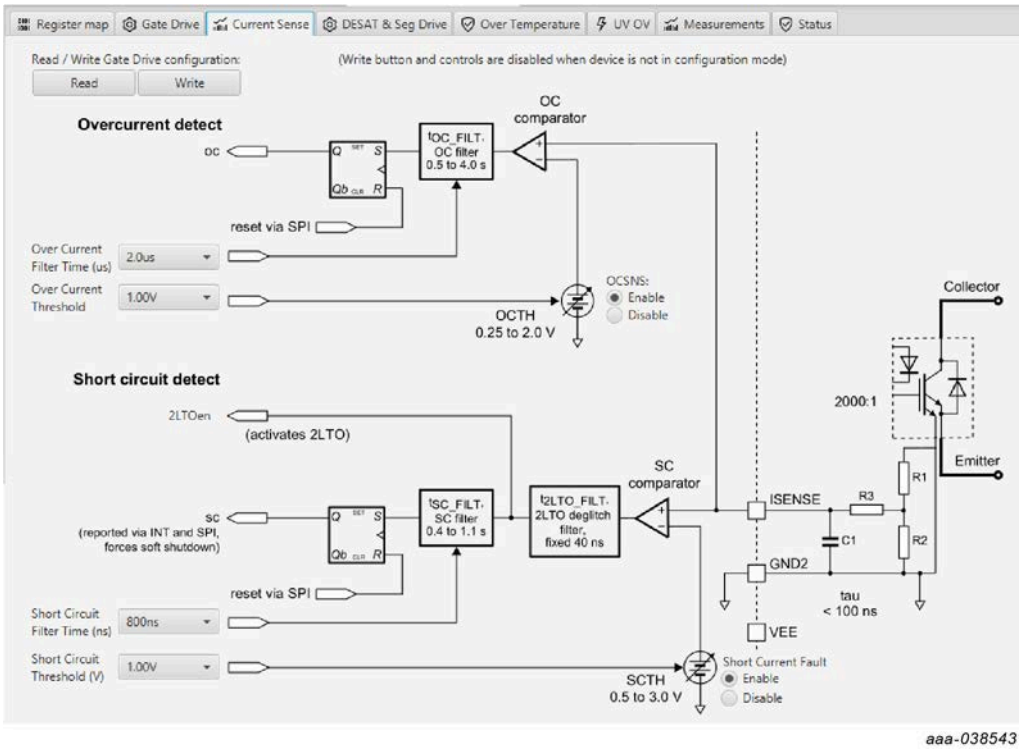

Figure 26. Current sense tab

DESAT & Seg Drive tab

- Allows setting of parameters related to desat and segmented drive
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

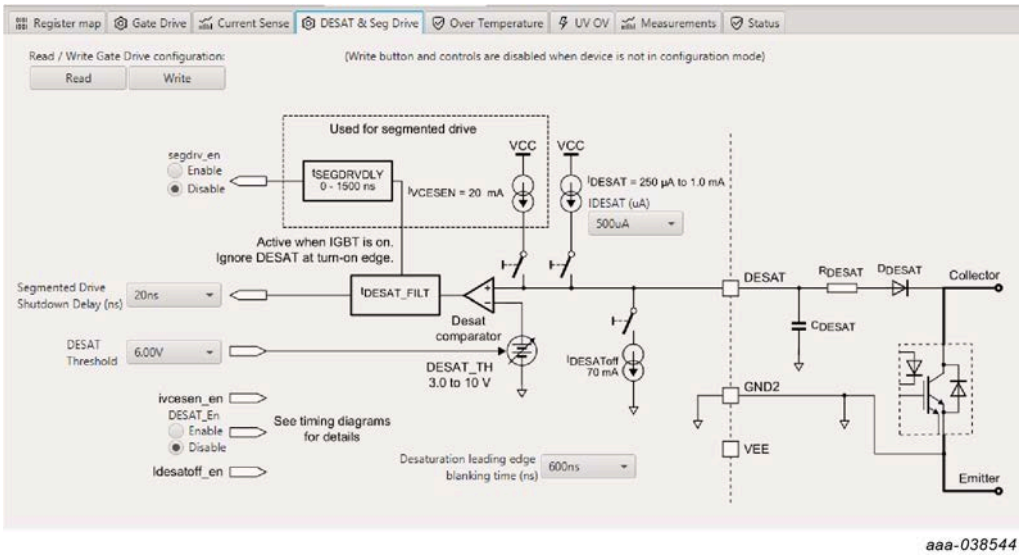

Figure 27. Desat and segmented drive tab

Overtemperature tab

- Allows setting of parameters related to overtemperature and overtemperature warning thresholds
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

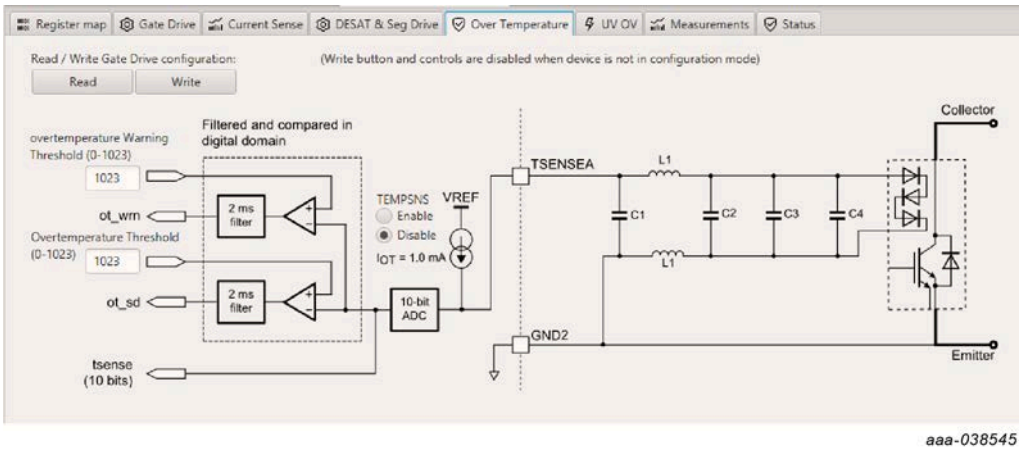

Figure 28. Overtemperature tab

Undervoltage and overvoltage threshold tab

- Allows setting of parameters related to undervoltage and overvoltage threshold
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

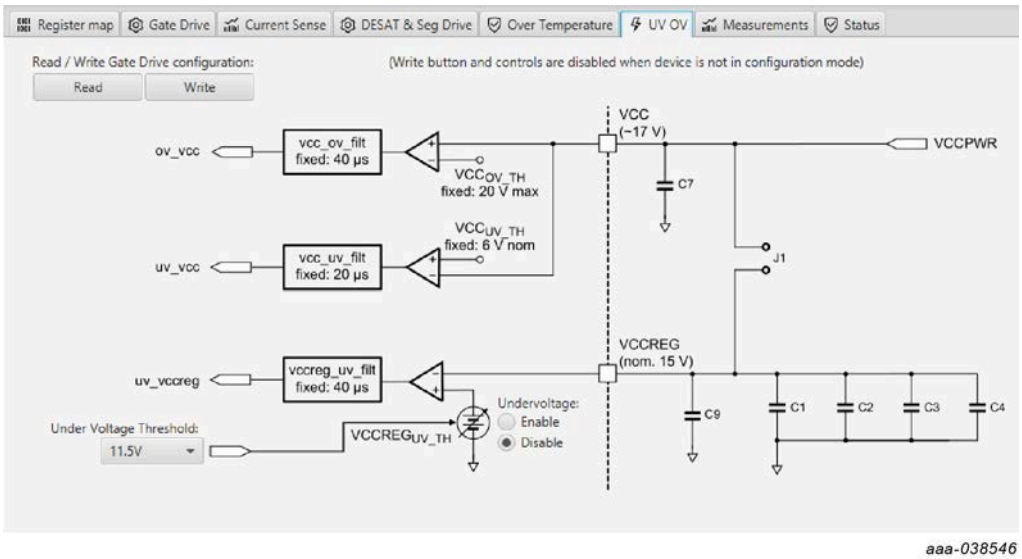

Figure 29. Undervoltage and overvoltage threshold tab

Measurements tab

- Allows monitoring and graphing of ADC and temperature values

Figure 30. Measurements tab

Status tab

- Allows monitoring of Status 1, Status 2, and Status 3 register values
- Status 1 and Status 2 faults can be cleared
- Status mask registers can be modified when in configuration mode
- Red indicates, that a fault has been latched

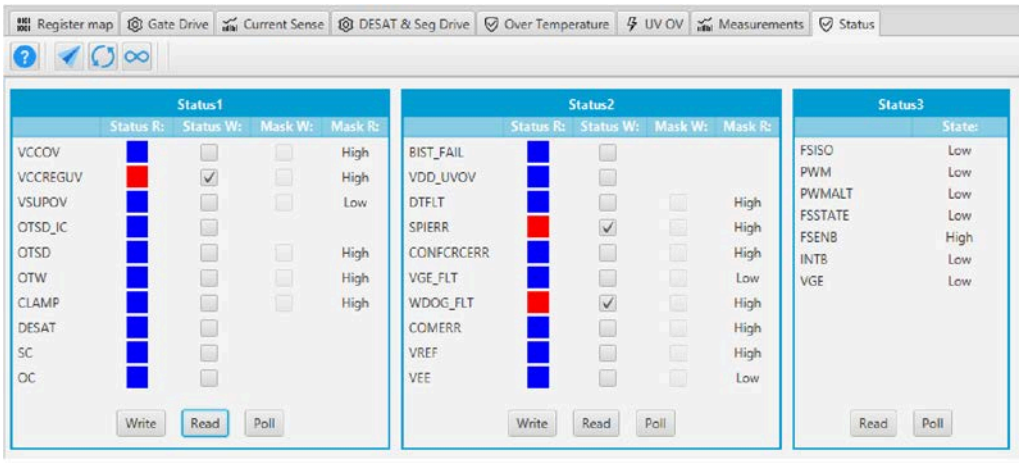

Figure 31. Status tab

Pulse tab

- Used for double pulse, short circuit, and PWM testing
- Select desired T1, T2, and T3 timings for each test type; select enable then generate pulses

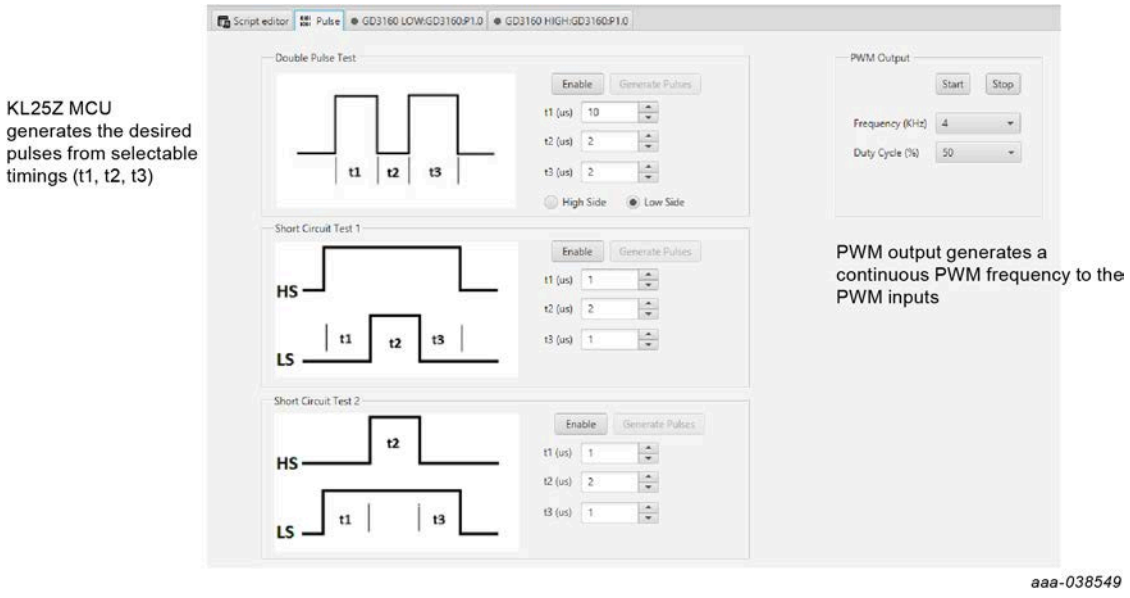

Figure 32. Pulse tab

6.4 Troubleshooting

Some common issues and troubleshooting procedures are detailed below. This is not an exhaustive list by any means, and additional debug may be needed:

Problem	Evaluation	Explanation	Corrective action(s)
No PWM output (no fault reported)	Check PWM jumper position on translator board	Incorrect PWM jumpers obstruct signal path but not report fault	Set PWMH_SEL (J4) and PWML_SEL (J5) jumpers properly, for desired control method: • 3.3 V to 5.0 V translator board reviewed in Section 4.6
	Check PWM control signal	Ensure that proper PWM signal is reaching GD3160 PWM input	Monitor EXT_PWML (TP14) and EXT_PWMH (TP15) for commanded PWM state
	Check FSENB status (see GD3160 pin 15, STATUS3)	PWM is disabled when FSENB = LOW	Set pin FSENB = HIGH (pin 15) to continue
	Check CONFIG_EN bit (MODE2)	PWM is disabled when CONFIG_EN is logic 1	Write CONFIG_EN = logic 0 to continue
No PWM output (fault reported)	Check VGE fault (VGE_FLT)	A short on IGBT or SiC module gate, or too low of VGEMON delay setting causes VGE fault, locking out PWM control of the gate.	Clear VGE_FLT bit (STATUS2) to continue. Increase VGEMON delay setting (CONFIG6). If safe operating condition can be guaranteed, set VGE_FLTM (MSK2) bit to logic 0, to mask fault.
	Check for short-circuit fault (SC) in STATUS1 register	SC is a severe fault that disables PWM. SC fault cannot be masked	Clear SC fault to continue. Consider adjusting SC fault settings on GD3160: • Adjust short-circuit threshold setting (CONFIG2) • Adjust short-circuit filter setting (CONFIG2)
PWM output is good, but with persistent fault reported	Check for dead time fault (DTFLT) in STATUS2 register	Dead time is enforced, but fault indicates that PWM controls signals are in violation	Clear DTFLT fault bit (STATUS2). Check PWMHSEL (J10) and PWMLSEL (J9) are configured to bypass dead time faults. Consider adjusting dead time settings on GD3160: • Change mandatory PWM dead time setting (CONFIG5) • Mask dead time fault (MSK2)
	Check for overcurrent (OC) fault in STATUS1 register	OC fault latches, but does not disable PWM. OC fault cannot be masked.	Clear OC fault bit (STATUS1). Adjust OC fault detection settings on GD3160: • Adjust overcurrent threshold setting (CONFIG1) • Adjust overcurrent filter setting (CONFIG1)
PWM or FSSTATE rising edge has longer delay than falling edge	Check translator output voltage versus GD3160 VDD voltage	Low translator output voltage (compared with correct VDD at GD3160) causes the high threshold at the GD3160 pin to be crossed later than commanded	Check translator output voltage selection (J233) is configured to the same level as the GD3160 VDD Check VCCSEL supply or translator outputs on the translator board for excessive loading or supply droop/pulldown
WDOG_FLT reported on startup	Check VSUP and VCC are powered	On initialization, watchdog fault is reported when one die is powered up before the other	Check VSUP and VCC both have power applied. Clear WDOG_FLT bit (STATUS2) to continue.
SPIERR reported on startup	Check KL25Z/translator connection	On initialization, SPIERR can occur when the SPI bus is open, or when GD3160 IC is powered up before the translator (which provides CSB).	Clear SPIERR fault to continue. Reinitialize power to GD3160 after translator is powered (over USB).

Problem	Evaluation	Explanation	Corrective action(s)
SPIERR reported after SPI message	Check bit length of message sent	There is SPIERR if SCLK does not see a n*24 multiple of cycles	Use 24-bit message length for SPI messages
	Check CRC	SPIERR faults if CRC provided in sent message is not good	Use FlexGUI to generate commands with valid CRC. The command can be copied in binary or hexadecimal and sent from another program.
	Check for sufficient dead time between SPI messages	SPIERR fault bit is set when the time between SPI messages (txfer_delay) received is too short. Minimum required delay time is 19 µs.	Check time between CSB rising edge (old message end) and CSB falling edge (new message start) during normal SPI read, and ensure transfer delay dead time check. SPIERR can also be cleared in BIST.
VCCREGUV reported on startup	Check VCCREG potential	Caused by low VCC	Clear VCCREGUV fault bit (STATUS1). Tune VCC-GNDISO potential with power supply set resistor (R22).
VREFUV reported on startup	Check HV domain is powered correctly	Related to slow rise time of VCC supply on HV domain, or failed VREF regulator	Clear VREFUV bit (STATUS2). Reset HV domain supply if fault bit does not clear.
	Check VCC for undervoltage condition	Low VCC is visible indirectly through other HV domain faults	Tune VCC-GNDISO using R22 feedback
VCCOV fault reported on startup	Check VEE level on suspect domain.	If VEE level is not at desired negative voltage it could cause excessive VCC level.	Check Zener diode in power supply circuit for proper value in setting VEE level. Clear VCCOV bit (STATUS1) to continue.
	Check VCC-GNDISO potential	PWM is disabled during a VCC overvoltage (20 V nom.)	Tune VCC-GNDISO potential to suitable level with power supply set resistor (R22). Clear VCCOV bit (STATUS1) to continue.
No PWM during short circuit test	Check PWMxSEL jumpers	Incorrect configuration of PWMALT pins prevent short-circuit test by enforcing dead time	For short-circuit test, set PWMLSEL (J9) and PWMHSEL (J10) to bypass dead time. See Section 4.4.3 for details.
Bad SPI data, appears to repeat previous response	Check VSUP/VDD for undervoltage condition	VDD_UV latches SPI buffer contents, preventing updated fault reporting.	Check voltage provided at VDD pin (pin 3). On each read, compare the address from the sent command and response (a difference indicates that the SPI response is latched due to inactive). Read multiple addresses to ensure a good comparison.
	Check PS_EN is set to HIGH in FlexGUI; see Figure 21	VCC/VEE can be enabled/disabled in software.	Enable VCC/VEE from FlexGUI
	Check VCC for undervoltage	Unpowered VCC prevents HV domain from updating data	Tune VCC-GNDISO using R22 feedback

7 Schematics, board layout, and bill of materials

The board schematics, board layout, and bill of materials are available at http://www.nxp.com/FRDMGD3160HB8EVM.

8 References

[1] Tool summary page for FRDMGD3160HB8EVM http://www.nxp.com/FRDMGD3160HB8EVM

[2] Product summary page for GD3160 device http://www.nxp.com/GD3160

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