MC33368

High Voltage GreenLine™ Power Factor Controller

The MC33368 is an active power factor controller that functions as a boost preconverter in off−line power supply applications. MC33368 is optimized for low power, high density power supplies requiring a minimum board area, reduced component count and low power dissipation. The narrow body SOIC package provides a small footprint. Integration of the high voltage startup saves approximately 0.7 W of power compared to resistor bootstrapped circuits.

The MC33368 features a watchdog timer to initiate output switching, a one quadrant multiplier to force the line current to follow the instantaneous line voltage a zero current detector to ensure critical conduction operation, a transconductance error amplifier, a current sensing comparator, a 5.0 V reference, an undervoltage lockout (UVLO) circuit which monitors the V_{CC} supply voltage and a CMOS driver for driving MOSFETs. The MC33368 also includes a programmable output switching frequency clamp. Protection features include an output overvoltage comparator to minimize overshoot, a restart delay timer and cycle−by−cycle current limiting.

Features

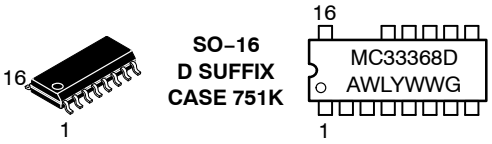
- Lossless Off−Line Startup
- Output Overvoltage Comparator
- Leading Edge Blanking (LEB) for Noise Immunity
- Watchdog Timer to Initiate Switching
- Restart Delay Timer
- This is a Pb−Free Device*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

http://onsemi.com

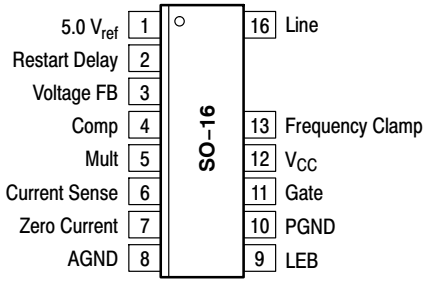
MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
YY, Y	= Year
WW	= Work Week
G	= Pb−Free Package

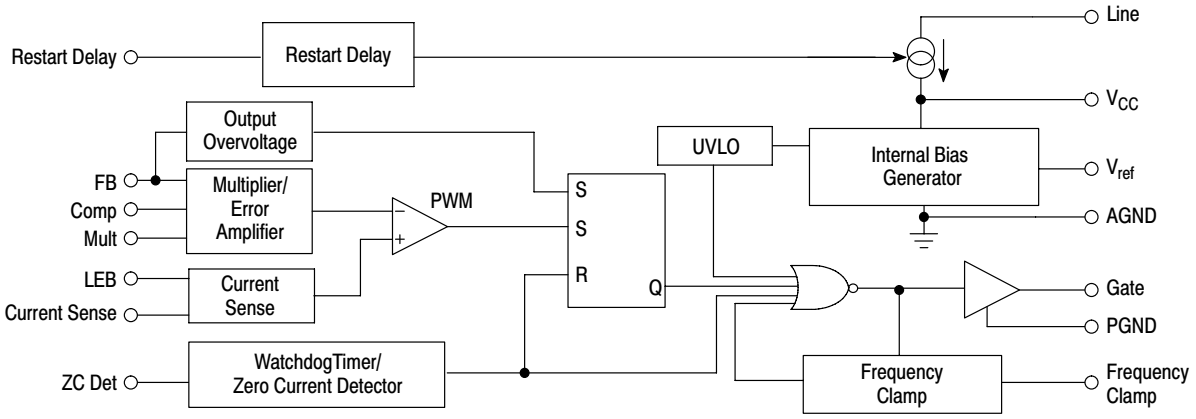
PIN CONNECTIONS

(TOP VIEW)



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.



This device contains 240 active transistors.

Figure 1. Representative Block Diagram

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage (Transient)	V_{CC}	20	V
Power Supply Voltage (Operating)	V_{CC}	16	V
Line Voltage	V_{Line}	500	V
Current Sense, Multiplier, Compensation, Voltage Feedback, Restart Delay and Zero Current Input Voltage	V_{in1}	−1.0 to +10	V
LEB Input, Frequency Clamp Input	V_{in2}	−1.0 to +20	V
Zero Current Detect Input	I_{in}	±5.0	mA
Restart Diode Current	I_{in}	5.0	mA
Power Dissipation and Thermal Characteristics D Suffix, Plastic Package Case 751K Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction−to−Air	 P_D $R_{\theta JA}$	 450 178	 mW °C/W
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature	T_A	−25 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 14.5 V, for typical values T_A = 25°C, for min/max values T_J = −25 to +125°C)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER					
Input Bias Current (V_{FB} = 5.0 V)	I_{IB}	–	0	1.0	μA
Input Offset Voltage (V_{Comp} = 3.0 V)	V_{IO}	–	2.0	50	mV
Transconductance (V_{Comp} = 3.0 V)	g_m	30	51	80	μmho
Output Source (V_{FB} = 4.6 V, V_{Comp} = 3.0 V) Output Sink (V_{FB} = 5.4 V, V_{Comp} = 3.0 V)	I_O I_O	9.0 9.0	17.5 17.5	30 30	μA
OVERVOLTAGE COMPARATOR					
Voltage Feedback Input Threshold	$V_{FB(OV)}$	1.07 V_{FB}	1.084 V_{FB}	1.1 V_{FB}	V
Propagation Time to Output	T_P	–	705	–	ns
MULTIPLIER					
Input Bias Current, V_{Mult} (V_{FB} = 0 V)	I_{IB}	–	−0.2	−1.0	μA
Input Threshold, V_{Comp}	$V_{th(M)}$	1.8	2.1	2.4	V
Dynamic Input Voltage Range Multiplier Input Compensation	 V_{Mult} V_{Comp}	 0 to 2.5 $V_{th(M)}$ to ($V_{th(M)}$ + 1.0)	 0 to 3.5 $V_{th(M)}$ to ($V_{th(M)}$ + 2.0)	 – –	V
Multiplier Gain (V_{Mult} = 0.5 V, V_{Comp} = $V_{th(M)}$ + 1.0 V) $\left(K = \frac{V_{CS}\ \text{Threshold}}{V_{Mult}\left(V_{Comp} - V_{th(M)}\right)}\right)$	K	0.25	0.51	0.75	1/V
VOLTAGE REFERENCE					
Voltage Reference (I_O = 0 mA, T_J = 25°C)	V_{ref}	4.95	5.0	5.05	V
Line Regulation (V_{CC} = 10 V to 16 V)	Reg_{line}	–	5.0	100	mV
Load Regulation (I_O = 0 – 5.0 mA)	Reg_{load}	–	5.0	100	mV
Total Output Variation Over Line, Load and Temperature	V_{ref}	4.8	–	5.2	V
Maximum Output Current	I_O	5.0	10	–	mA
Reference Undervoltage Lockout Threshold	V_{th}	–	4.5	–	V
ZERO CURRENT DETECTOR					
Input Threshold Voltage (V_{in} Increasing)	V_{th}	1.0	1.2	1.4	V
Hysteresis (V_{in} Decreasing)	V_H	100	200	300	mV
Delay to Output	T_{pd}	–	127	–	ns
CURRENT SENSE COMPARATOR					
Input Bias Current (V_{CS} = 0 to 2.0 V)	I_{IB}	–	0.2	1.0	μA
Input Offset Voltage (V_{Mult} = −0.2 V)	V_{IO}	–	4.0	50	mV
Maximum Current Sense Input Threshold (V_{Comp} = 5.0 V, V_{Mult} = 5.0 V)	$V_{th(max)}$	1.3	1.5	1.8	V
Delay to Output (V_{LEB} = 12 V, V_{Comp} = 5.0 V, V_{Mult} = 5.0 V) (V_{CS} = 0 to 5.0 V Step, C_L = 1.0 nF)	$t_{PHL(in/out)}$	50	270	425	ns
FREQUENCY CLAMP					
Frequency Clamp Input Threshold	$V_{th(FC)}$	1.9	2.0	2.1	V
Frequency Clamp Capacitor Reset Current (V_{FC} = 0.5 V)	I_{reset}	0.5	1.7	4.0	mA
Frequency Clamp Disable Voltage	V_{DFC}	–	7.3	8.0	V

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 14.5 V, for typical values T_A = 25°C, for min/max values T_J = −25 to +125°C)

Characteristic	Symbol	Min	Typ	Max	Unit
DRIVE OUTPUT					
Source Resistance (Current Sense = 0 V, V_{Gate} = V_{CC} − 1.0 V) Sink Resistance (Current Sense = 3.0 V, V_{Gate} = 1.0 V)	R_{OH} R_{OL}	4.0 4.0	8.6 7.2	20 20	Ω
Output Voltage Rise Time (25% − 75%) (C_L = 1.0 nF)	t_r	−	55	200	ns
Output Voltage Fall Time (75% − 25%) (C_L = 1.0 nF)	t_f	−	70	200	ns
Output Voltage in Undervoltage (V_{CC} = 7.0 V, I_{Sink} = 1.0 mA)	$V_{O(UV)}$	−	0.01	0.25	V
LEADING EDGE BLANKING					
Input Bias Current	I_{bias}	−	0.1	0.5	μA
Threshold (as Offset from V_{CC}) (V_{LEB} Increasing)	V_{LEB}	1.0	2.25	2.75	V
Hysteresis (V_{LEB} Decreasing)	V_H	100	270	500	mV
UNDERVOLTAGE LOCKOUT					
Startup Threshold (V_{CC} Increasing)	$V_{th(on)}$	11.5	13	14.5	V
Minimum Operating Voltage After Turn−On (V_{CC} Decreasing)	$V_{Shutdown}$	7.0	8.5	10	V
Hysteresis	V_H	−	4.5	−	V
TIMER					
Watchdog Timer	t_{DLY}	180	385	800	μs
Restart Timer Threshold	$V_{th(restart)}$	1.5	2.3	3.0	V
Restart Pin Output Current ($V_{restart}$ = 0 V, V_{ref} = 5.0 V)	$I_{restart}$	3.1	5.2	7.1	mA
TOTAL DEVICE					
Line Startup Current (V_{CC} = 0 V, V_{Line} = 50 V)	I_{SU}	5.0	16	25	mA
Line Operating Current (V_{CC} = $V_{th(on)}$, V_{Line} = 50 V)	I_{OP}	3.0	12.9	20	mA
V_{CC} Dynamic Operating Current (50 kHz, C_L = 1.0 nF) V_{CC} Static Operating Current (I_O = 0)	I_{CC}	− −	5.3 3.0	8.5 −	mA
Line Pin Leakage (V_{Line} = 500 V)	I_{Line}	−	30	80	μA

ORDERING INFORMATION

Device	Package	Shipping†
MC33368DG	SOIC−16 (Pb−Free)	48 Units / Rail
MC33368DR2G	SOIC−16 (Pb−Free)	2500 Units / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

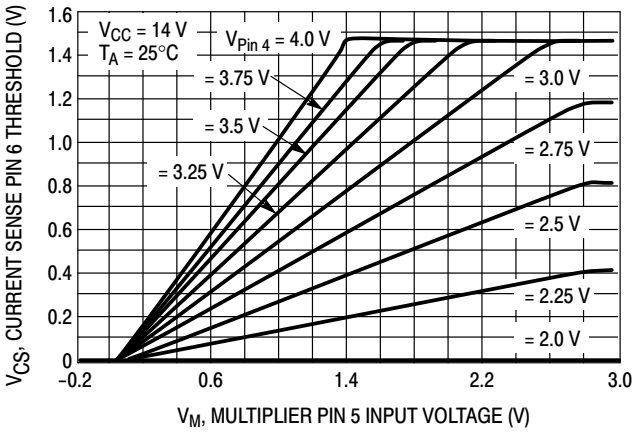


Figure 2. Current Sense Input Threshold versus Multiplier Input

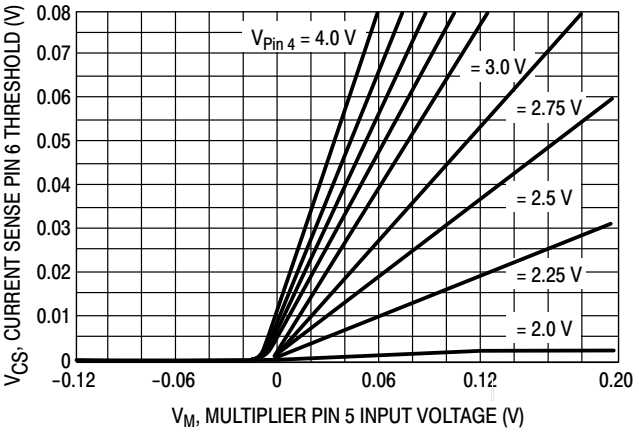


Figure 3. Current Sense Input Threshold versus Multiplier Input, Expanded View

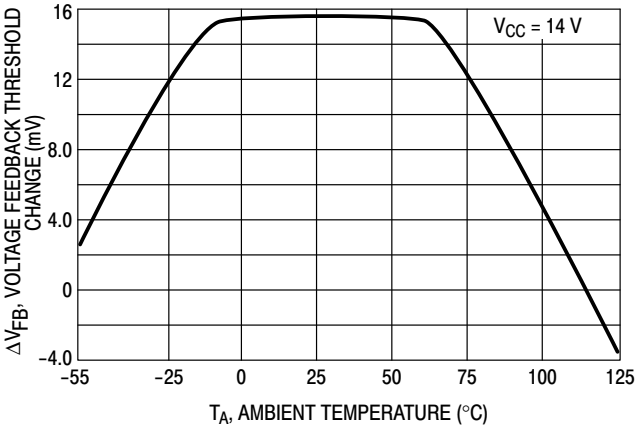


Figure 4. Reference Voltage versus Temperature

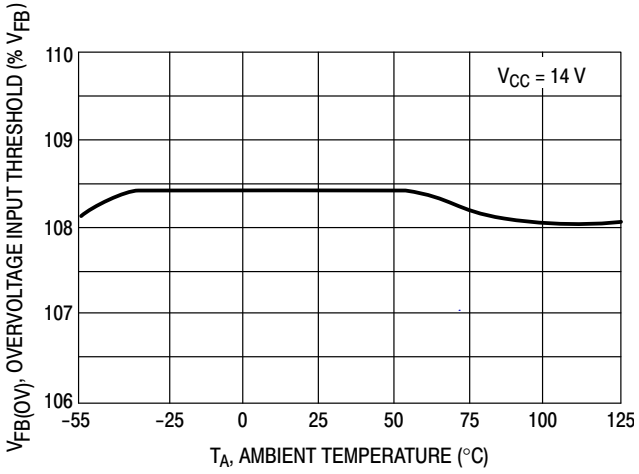


Figure 5. Overvoltage Comparator Input Threshold versus Temperature

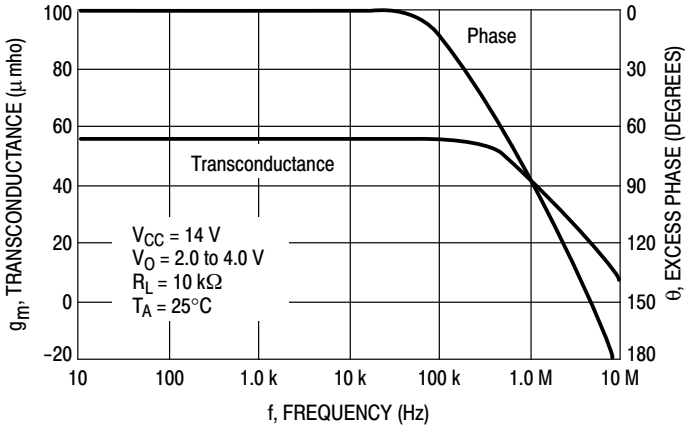


Figure 6. Error Amplifier Transconductance and Phase versus Frequency

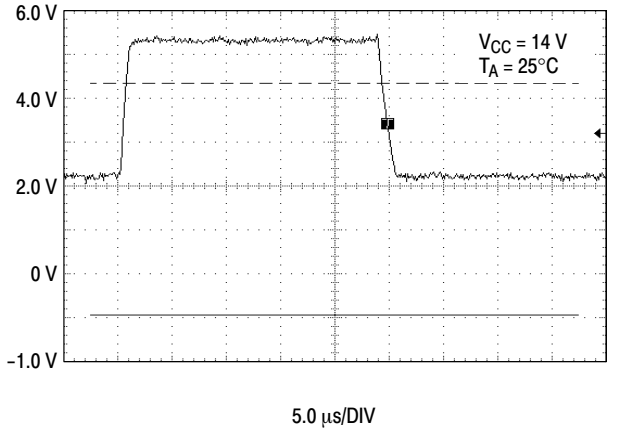


Figure 7. Error Amplifier Transient Response

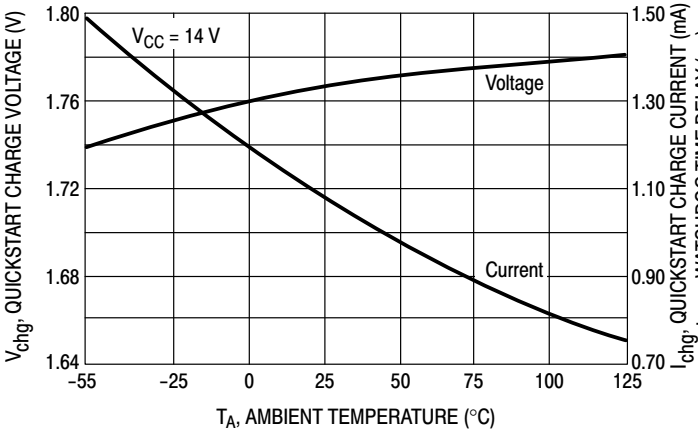


Figure 8. Quickstart Charge Current versus Temperature

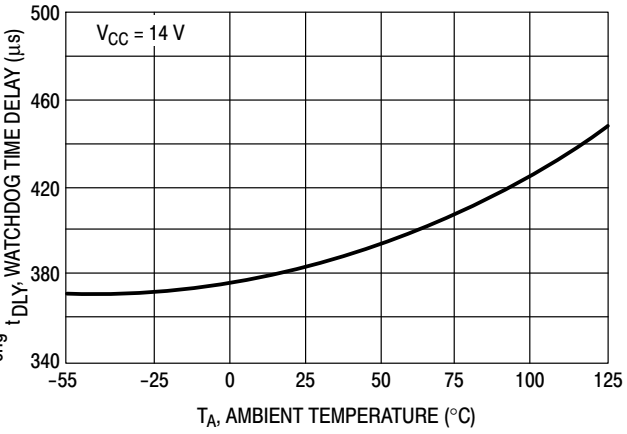


Figure 9. Watchdog Timer Delay versus Temperature

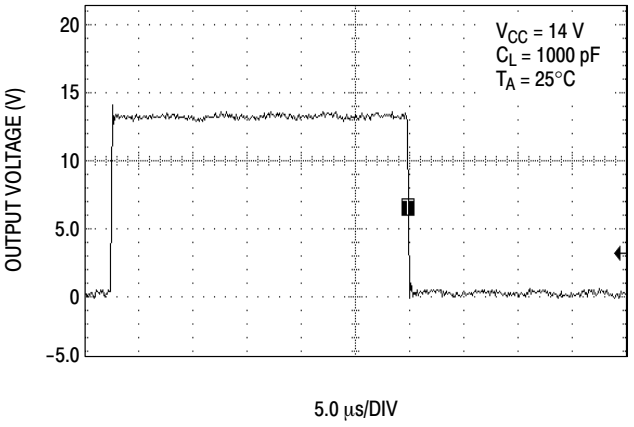


Figure 10. Drive Output Waveform

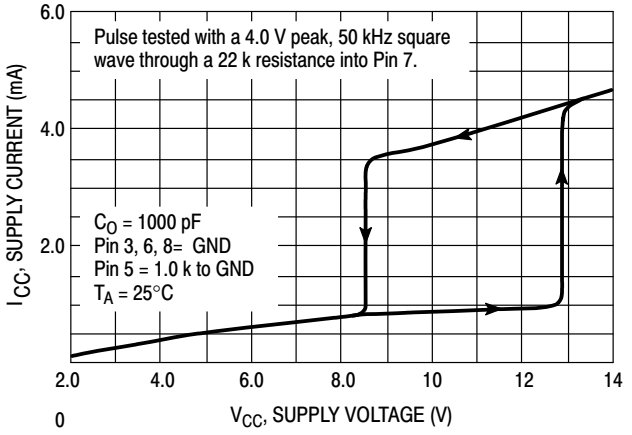


Figure 11. Supply Current versus Supply Voltage

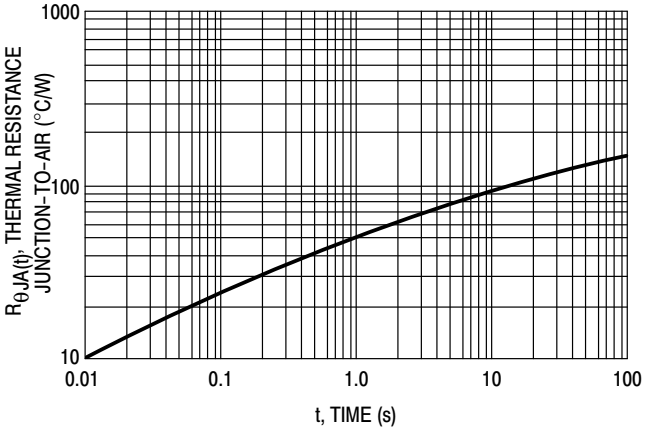


Figure 12. Transient Thermal Resistance

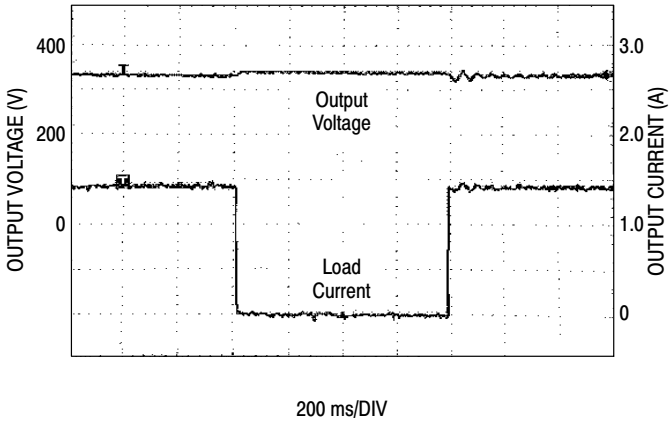


Figure 13. Low Load Detection Response Waveform

FUNCTIONAL DESCRIPTION

INTRODUCTION

With the goal of exceeding the requirements of legislation on line current harmonic content, there is an ever increasing demand for an economical method of obtaining a unity power factor. This data sheet describes a monolithic control IC that was specifically designed for power factor control with minimal external components. It offers the designer a simple cost effective solution to obtain the benefits of active power factor correction.

Most electronic ballasts and switching power supplies use a bridge rectifier and a bulk storage capacitor to derive raw dc voltage from the utility ac line, Figure 14.

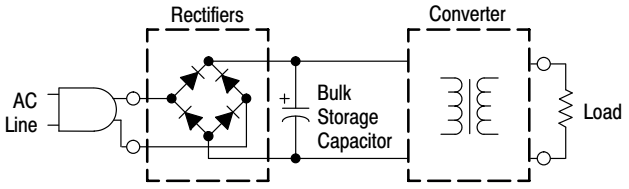


Figure 14. Uncorrected Power Factor Circuit

This simple rectifying circuit draws power from the line when the instantaneous ac voltage exceeds the capacitor voltage. This occurs near the line voltage peak and results in a high charge current spike, Figure 15. Since power is only taken near the line voltage peaks, the resulting spikes of current are extremely nonsinusoidal with a high content of harmonics. This results in a poor power factor condition where the apparent input power is much higher than the real power. Power factor ratios of 0.5 to 0.7 are common.

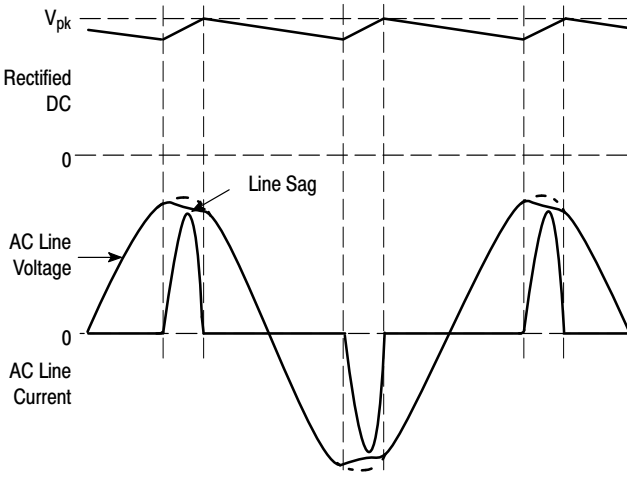


Figure 15. Uncorrected Power Factor Input Waveforms

Power factor correction can be achieved with the use of either a passive or active input circuit. Passive circuits usually contain a combination of large capacitors, inductors, and rectifiers that operate at the ac line frequency. Active circuits incorporate some form of a high frequency switching converter for the power processing with the boost converter being the most popular topology. Since active input circuits operate at a frequency much higher than that of the ac line, they are smaller, lighter in weight, and more efficient than a passive circuit that yields similar results. With proper control of the preconverter, almost any complex load can be made to appear resistive to the ac line, thus significantly reducing the harmonic current content.

Operating Description

The MC33368 contains many of the building blocks and protection features that are employed in modern high performance current mode power supply controllers. Referring to the block diagram in Figure 16, note that a multiplier has been added to the current sense loop and that this device does not contain an oscillator. A description of each of the functional blocks is given below.

Error Amplifier

An Error Amplifier with access to the inverting input and output is provided. The amplifier is a transconductance type, meaning that it has high output impedance with controlled voltage−to−current gain ($g_m \approx 50$ μmhos). The noninverting input is internally biased at 5.0 V ±2.0%. The output voltage of the power factor converter is typically divided down and monitored by the inverting input. The maximum input bias current is −1.0 μA which can cause an output voltage error that is equal to the product of the input bias current and the value of the upper divider resistor R2. The Error Amplifier output is internally connected to the Multiplier and is pinned out (Pin 4) for external loop compensation. Typically, the bandwidth is set below 20 Hz so that the amplifier's output voltage is relatively constant over a given ac line cycle. In effect, the error amplifier monitors the average output voltage of the converter over several line cycles resulting in a fixed Drive Output on−time. The amplifier output stage can sink and source 11.5 μA of current and is capable of swinging from 1.7 to 5.0 V, assuring that the Multiplier can be driven over its entire dynamic range.

Note that by using a transconductance type amplifier, the input is allowed to move independently with respect to the output, since the compensation capacitor is connected to ground. This allows dual usage of the Voltage Feedback pin by the Error Amplifier and Overvoltage Comparator.

Overvoltage Comparator

An Overvoltage Comparator is incorporated to eliminate the possibility of runaway output voltage. This condition can occur during initial startup, sudden load removal, or during output arcing and is the result of the low bandwidth that must be used in the Error Amplifier control loop. The Overvoltage Comparator monitors the peak output voltage of the converter, and when exceeded, immediately terminates MOSFET switching. The comparator threshold is internally set to 1.08 V_{ref}. In order to prevent false tripping during normal operation, the value of the output filter capacitor C3 must be large enough to keep the peak−to−peak ripple less than 16% of the average dc output.

Multiplier

A single quadrant, two input multiplier is the critical element that enables this device to control power factor. The ac haversines are monitored at Pin 5 with respect to ground while the Error Amplifier output at Pin 4 is monitored with respect to the Voltage Feedback Input threshold. A graph of the Multiplier transfer curve is shown in Figure 2. Note that both inputs are extremely linear over a wide dynamic range, 0 to 3.2 V for Pin 5 and 2.5 to 4.0 V for Pin 4. The Multiplier output controls the Current Sense Comparator threshold as the ac voltage traverses sinusoidally from zero to peak line. This has the effect of forcing the MOSFET on−time to track the input line voltage, thus making the preconverter load appear to be resistive.

$$\text{Pin 6 Threshold} \approx 0.55 \left(V_{\text{Pin 4}} - V_{\text{Pin 3}}\right) V_{\text{Pin 5}}$$

Zero Current Detector

The MC33368 operates as a critical conduction current mode controller, whereby output switch conduction is initiated by the Zero Current Detector and terminated when the peak inductor current reaches the threshold level established by the Multiplier output. The Zero Current Detector initiates the next on−time by setting the R_S Latch at the instant the inductor current reaches zero. This critical conduction mode of operation has two significant benefits. First, since the MOSFET cannot turn−on until the inductor current reaches zero, the output rectifier's reverse recovery time becomes less critical allowing the use of an inexpensive rectifier. Second, since there are no deadtime gaps between cycles, the ac line current is continuous thus limiting the peak switch to twice the average input current

The Zero Current Detector indirectly senses the inductor current by monitoring when the auxiliary winding voltage falls below 1.2 V. To prevent false tripping, 200 mV of hysteresis is provided. The Zero Current Detector input is internally protected by two clamps. The upper 10 V clamp prevents input overvoltage breakdown while the lower −0.7 V clamp prevents substrate injection. An external resistor must be used in series with the auxiliary winding to limit the current through the clamps to 5.0 mA or less.

Current Sense Comparator and RS Latch

The Current Sense Comparator R_S Latch configuration used ensures that only a single pulse appears at the Drive Output during a given cycle. The inductor current is converted to a voltage by inserting a ground−referenced sense resistor R7 in series with the source of output switch. This voltage is monitored by the Current Sense Input and compared to a level derived from the Multiplier output. The peak inductor current under normal operating conditions is controlled by the threshold voltage of Pin 6 where:

$$I_{pk} = \frac{\text{Pin 6 Threshold}}{R7}$$

Abnormal operating conditions occur when the preconverter is running at extremely low line or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.5 V. Therefore, the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.5\ V}{R7}$$

With the component values shown in Figure 16, the Current Sense Comparator threshold, at the peak of the haversine, varies from 110 mV at 90 Vac to 100 mV at 268 Vac. The Current Sense Input to Drive Output propagation delay is typically 200 ns.

Timer

A watchdog timer function was added to the IC to eliminate the need for an external oscillator when used in stand alone applications. The Timer provides a means to automatically start or restart the preconverter if the Drive Output has been off for more than 385 μs after the inductor current reaches zero.

Undervoltage Lockout and Quickstart

The MC33368 has a 5.0 V internal reference brought out to Pin 1 and capable of sourcing 10 mA typically. It also contains an Undervoltage Lockout (UVLO) circuit which suppresses the Gate output at Pin 11 if the V_{CC} supply voltage drops below 8.5 V typical.

A Quickstart circuit has been incorporated to optimize converter startup. During initial startup, compensation capacitor C1 will be discharged, holding the Error Amplifier output below the Multiplier's threshold. This will prevent Drive Output switching and delay bootstraping of capacitor C4 by diode D6. If Pin 4 does not reach the multiplier threshold before C4 discharges below the lower SMPS UVLO threshold, the converter will hiccup and experience a significant startup delay. The Quickstart circuit is designed to precharge C1 to 1.7 V. This level is slightly below the Pin 4 Multiplier threshold, allowing immediate Drive Output switching.

Restart Delay

A restart delay pin is provided to allow hiccup mode fault protection in case of a short circuit condition and to prevent the SMPS from repeatedly trying to restart after the input line voltage has been removed. When power is first applied, there is no startup delay, but subsequent cycling of the V_{CC} voltage will result in delay times that are programmed by an external resistor and capacitor. The Restart Delay, Pin 2, is a high impedance, so that an external capacitor can provide delay times as long as several seconds.

If the SMPS output is short circuited, the transformer winding, which provides the V_{CC} voltage to the control IC and the MC33368, will be unable to sustain V_{CC} to the control circuits. The restart delay capacitor at Pin 2 of the MC33368 prevents the high voltage startup transistor within the IC from maintaining the voltage on C4. After V_{CC} drops below the UVLO threshold in the SMPS, the SMPS switching transistors are held off for the time programmed by the values of the restart capacitor (C9) and resistor (R8).

In this manner, the SMPS switching transistors are operated at very low duty cycles, preventing their destruction. If the short circuit fault is removed, the power supply system will turn on by itself in a normal startup mode after the restart delay has timed out.

Output Switching Frequency Clamp

In normal operation, the MC33368 operates the boost inductor in the critical mode. That is, the inductor current ramps to a peak value, ramps down to zero, then immediately begins ramping positive again. The peak current is programmed by the multiplier output within the IC. As the input voltage haversine declines to near zero, the output switch on−time becomes constant, rather than going to zero because of the small integrated dc voltage at Pin 5 caused by C2, R3 and R5. Because of this, the average line current does not exactly follow the line voltage near the zero crossings. The Output Switching Frequency Clamp remedies this situation to improve power factor and minimize EMI generated in this operating region. The values of R10 and C7, as shown in Figure 16, program a minimum off−time in the frequency clamp which overrides the zero current detect signal, forcing a minimum off−time. This allows discontinuous conduction operation of the boost inductor in the zero crossing region, and the average line current more nearly follows the voltage. The Output Switching Frequency Clamp function can be disabled by connecting the FC input, Pin 13, to the V_{CC} supply Pin 12.

For best results, the minimum off−time, determined by the values of R10 and C7, should be chosen so that $t_{s(min)} = t_{(on)} + t_{(off)fc}$. Output drive is inhibited when the voltage at the frequency clamp input is less than 2.0 V. When the output drive is high, C7 is discharged through an internal 100 μA current source. When the output drive switches low, C7 is charged through R10. The drive output is inhibited until the voltage across C7 reaches 2.0 V, establishing a minimum off−time where:

$$t_{(off)fc} = - R10\ C7\ \log_e \left[1 - \left(\frac{2}{V_{CC}} \right) \right]$$

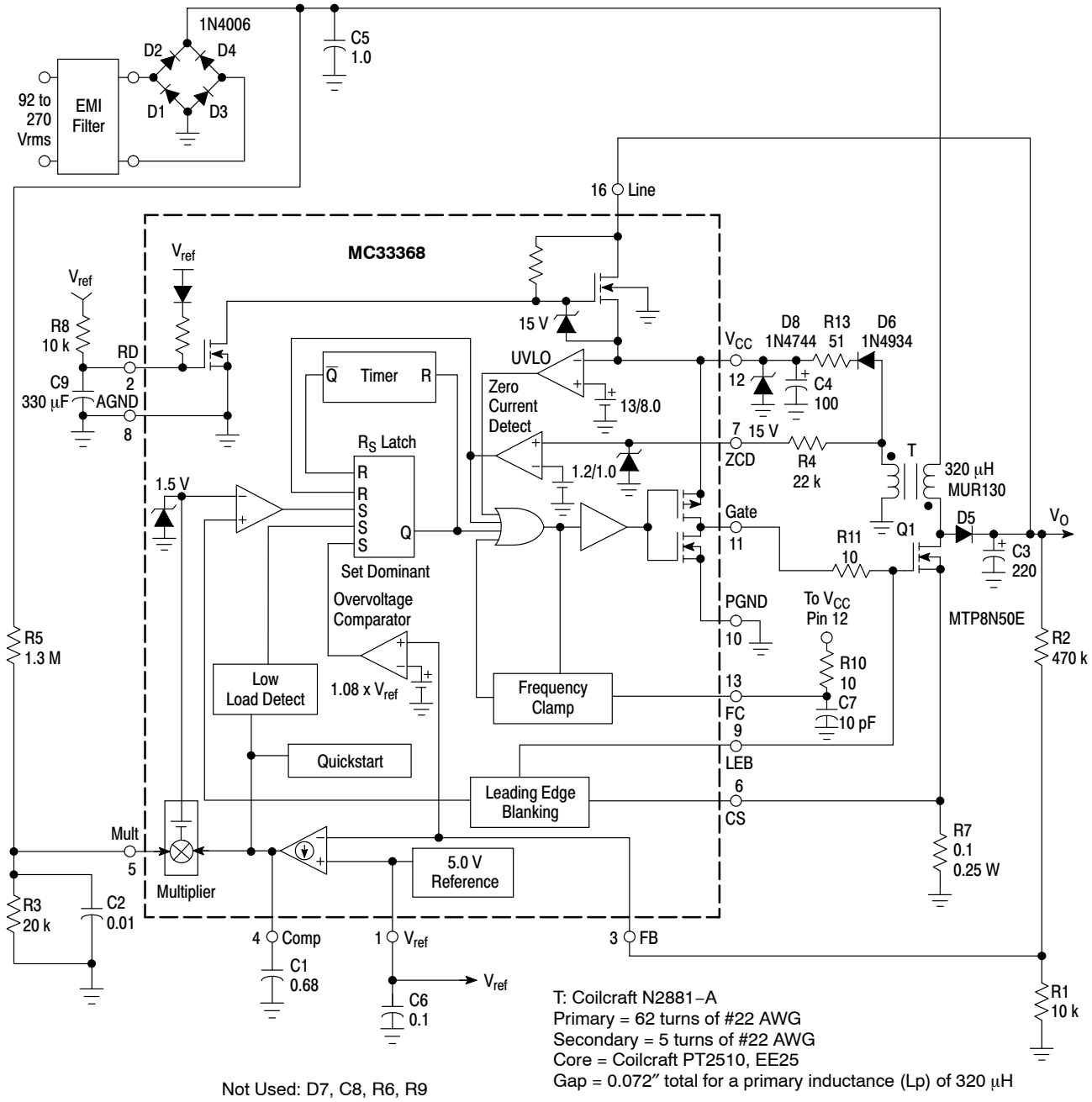
Output

The IC contains a CMOS output driver that was specifically designed for direct drive of power MOSFETs. The Gate Output is capable of up to ±1500 mA peak current with a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Gate Output in a sinking mode whenever the Undervoltage Lockout is active. This characteristic eliminates the need for an external gate pull−down resistor. The totem−pole output has been optimized to minimize cross−conduction current during high speed operation.

Table 1. Design Equations

Calculation	Formula	Notes
Converter Output Power	$P_O = V_O I_O$	Calculate the maximum required output power.
Peak Indicator Current	$I_{L(pk)} = \frac{2\sqrt{2}\,P_O}{\eta\,Vac_{(LL)}}$	Calculated at the minimum required ac line voltage for output regulation. Let the efficiency η = 0.92 for low line operation.
Inductance	$L_P = \frac{t\left(\frac{V_O}{\sqrt{2}} - Vac_{(LL)}\right)\eta\,Vac_{(LL)}^2}{\sqrt{2}\,V_O\,P_O}$	Let the switching cycle t = 40 μs for universal input (85 to 265 Vac) operation and 20 μs for fixed input (92 to 138 Vac, or 184 to 276 Vac) operation.
Switch On−Time	$t_{(on)} = \frac{2\,P_O\,L_P}{\eta\,Vac^2}$	In theory, the on−time $t_{(on)}$ is constant. In practice, $t_{(on)}$ tends to increase at the ac line zero crossings due to the charge on capacitor C5. Let Vac = $Vac_{(LL)}$ for initial $t_{(on)}$ and $t_{(off)}$ calculations.
Switch Off−Time	$t_{(off)} = \frac{t_{(on)}}{\frac{V_O}{\sqrt{2}\ Vac\ \lvert Sin\ \theta\rvert} - 1}$	The off−time $t_{(off)}$ is greatest at the peak of the ac line voltage and approaches zero at the ac line zero crossings. Theta (θ) represents the angle of the ac line voltage.
Minimum Switch Off−Time	$t_{(off)_{min}} = \frac{L_P\,I_{L(pk)}}{V_O}$	The off−time is at a minimum at ac line crossings. This equation is used to calculate $t_{(off)}$ as Theta approaches zero.
Delay Time	$t_d = -R10\,C7\,\ln\left(\frac{V_{CC} - 2}{V_{CC}}\right)$	The delay time is used to override the minimum off−time at the ac line zero crossings by programming the Frequency Clamp with C7 and R10.
Switching Frequency	$f = \frac{1}{t_{(on)} + t_{(off)}}$	The minimum switching frequency occurs at the peak of the ac line voltage. As the ac line voltage traverses from peak to zero, $t_{(off)}$ approaches zero producing an increase in switching frequency.
Peak Switch Current	$R7 = \frac{V_{CS}}{I_{L(pk)}}$	Set the current sense threshold V_{CS} to 1.0 V for universal input (85 to 265 Vac) operation and to 0.5 V for fixed input (92 to 138 Vac, or 184 to 276 Vac) operation. Note that V_{CS} must be less than 1.4 V.
Multiplier Input Voltage	$V_M = \frac{Vac\ \sqrt{2}}{\left(\frac{R5}{R3} + 1\right)}$	Set the multiplier input voltage V_M to 3.0 V at high line. Empirically adjust V_M for the lowest distortion over the ac line voltage range while guaranteeing startup at minimum line.
Converter Output Voltage	$V_O = V_{ref}\left(\frac{R2}{R1} + 1\right) - I_{IB}\,R1$	The I_{IB} R1 error term can be minimized with a divider current in excess of 100 μA.
Converter Output Peak−to−Peak Ripple Voltage	$\Delta V_{O(pp)} = I_{L(pk)}\sqrt{\left(\frac{1}{2\,\pi\,f_{ac}\,C3}\right)^2 + ESR^2}$	The calculated peak−to−peak ripple must be less than 16% of the average dc output voltage to prevent false tripping of the Overvoltage Comparator. Refer to the Overvoltage Comparator Text. ESR is the equivalent series resistance of C3.
Error Amplifier Bandwidth	$BW = \frac{g_m}{2\,\pi\,C1}$	The bandwidth is typically set to 20 Hz. When operating at high ac line, the value of C1 may need to be increased.

NOTE: The following converter characteristics must be chosen:
V_O = Desired output voltage. $Vac_{(LL)}$ = AC RMS minimum required operating line voltage for output regulation.
I_O = Desired output current. ΔV_O = Converter output peak−to−peak ripple voltage.
Vac = AC RMS operating line voltage.



T: Coilcraft N2881−A
Primary = 62 turns of #22 AWG
Secondary = 5 turns of #22 AWG
Core = Coilcraft PT2510, EE25
Gap = 0.072″ total for a primary inductance (Lp) of 320 μH

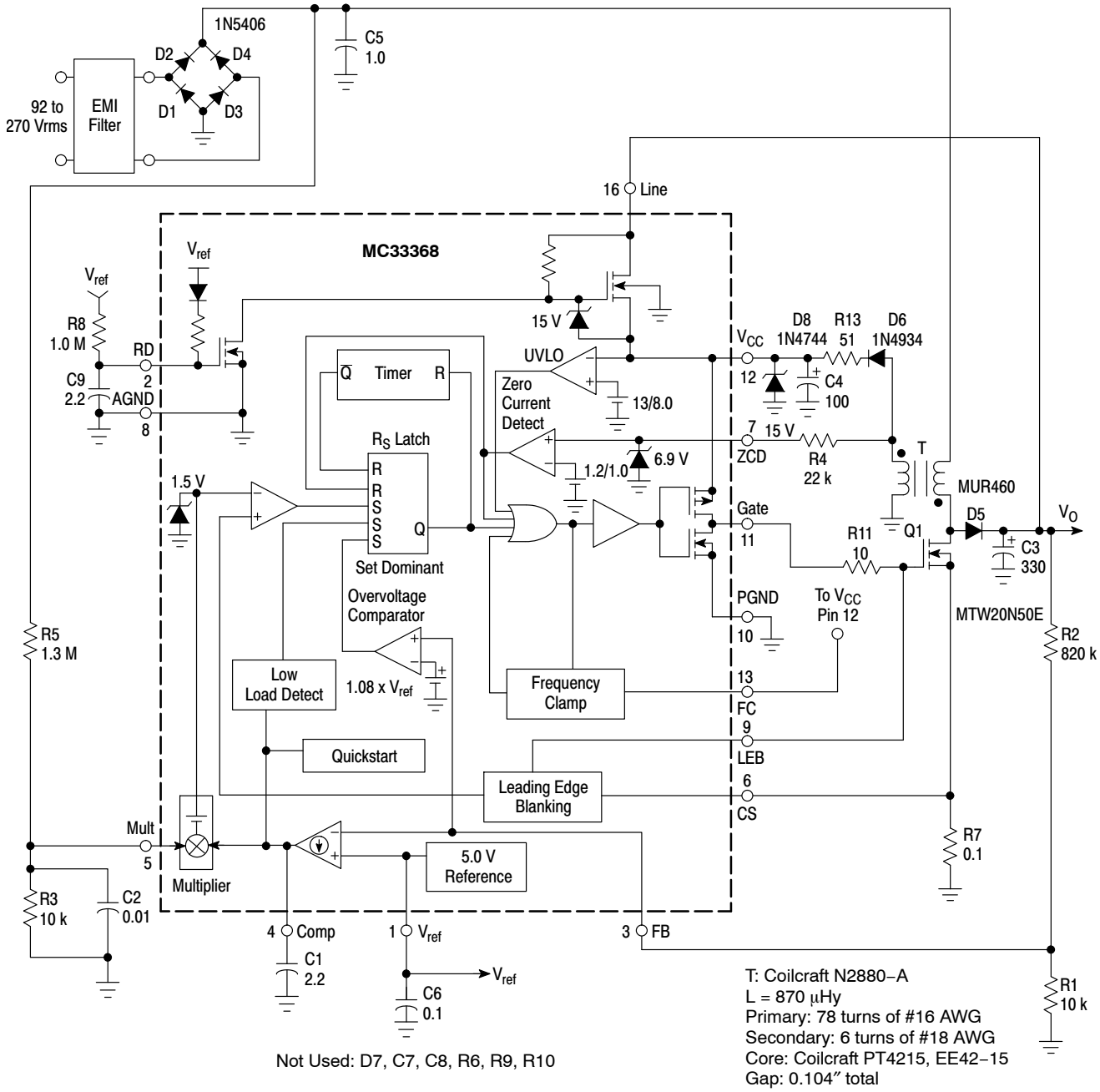
Not Used: D7, C8, R6, R9

Power Factor Controller Test Data

AC Line Input									DC Output				
				Current Harmonic Distortion (% I_{fund})									
V_{rms}	Pin	PF	I_{fund}	THD	2	3	5	7	$V_{O(pp)}$	V_O	I_O	P_O	n(%)
90	79.7	0.999	0.89	0.5	0.15	0.09	0.06	0.09	3.0	244.4	0.31	76.01	95.4
100	79.3	0.998	0.79	0.5	0.14	0.09	0.08	0.10	3.0	242.9	0.31	75.54	95.3
110	78.9	0.997	0.72	0.5	0.16	0.13	0.08	0.10	3.0	242.9	0.31	75.30	95.4
120	78.5	0.996	0.66	0.5	0.15	0.12	0.08	0.13	3.0	243.0	0.31	75.57	96.3
130	78.1	0.994	0.60	0.5	0.14	0.12	0.07	0.14	3.0	243.0	0.31	75.57	96.7
138	77.8	0.991	0.57	0.5	0.15	0.14	0.08	0.14	3.0	243.0	0.31	75.57	97.1

Heatsink = AAVID Engineering Inc., 590302B03600, or 593002B03400

Figure 16. 80 W Power Factor Controller



Not Used: D7, C7, C8, R6, R9, R10

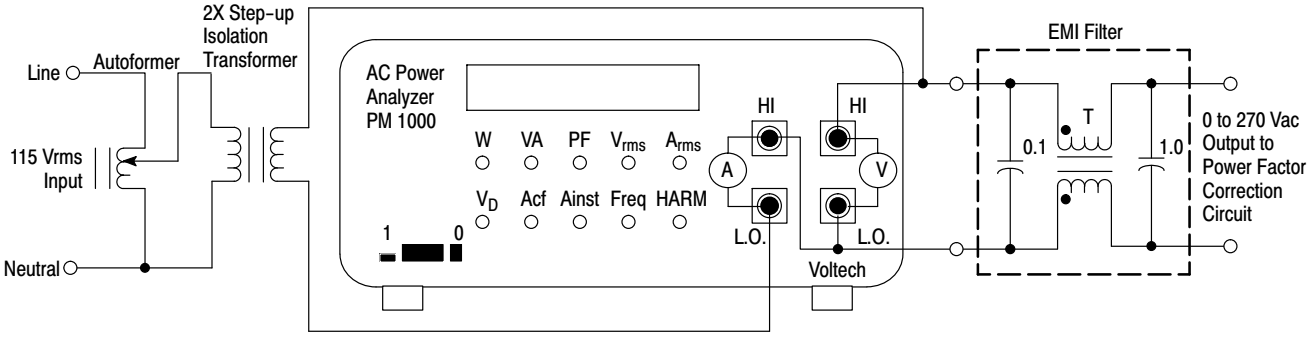
T: Coilcraft N2880−A
L = 870 μHy
Primary: 78 turns of #16 AWG
Secondary: 6 turns of #18 AWG
Core: Coilcraft PT4215, EE42−15
Gap: 0.104″ total

Power Factor Controller Test Data

AC Line Input									DC Output				
				Current Harmonic Distortion (% I_{fund})									
V_{rms}	Pin	PF	I_{fund}	THD	2	3	5	7	$V_{O(pp)}$	V_O	I_O	P_O	n(%)
90	190.4	0.995	2.11	5.8	0.16	0.32	0.24	0.80	3.6	398.0	0.44	175.9	92.4
120	192.1	0.997	1.60	3.2	0.08	0.17	0.07	0.30	3.6	398.9	0.44	177.1	92.2
138	192.7	0.997	1.40	0.9	0.08	0.24	0.03	0.15	3.6	402.3	0.45	179.0	92.9
180	194.3	0.995	1.08	0.9	0.04	0.18	0.04	0.08	3.6	409.1	0.45	182.9	94.1
240	189.3	0.983	0.80	0.7	0.08	0.21	0.08	0.06	3.6	407.0	0.45	181.1	95.7
268	186.3	0.972	0.71	0.6	0.11	0.32	0.10	0.10	3.6	406.2	0.44	180.4	96.8

Heatsink = AAVID Engineering Inc., 590302B03600

Figure 17. 175 W Universal Input Power Factor Controller



An RFI filter is required for best performance when connecting the preconverter directly to the ac line. The filter attenuates the level of high frequency switching that appears on the ac line current waveform. Figures 16 and 17 work well with commercially available two stage filters such as the Delta Electronics 03DPCG6. Shown above is a single stage test filter that can easily be constructed with four ac line rated capacitors and a common−mode transformer. Coilcraft CMT3−28−2 was used to test Figures 16 and 17. It has a minimum inductance of 28 mH and a maximum current rating of 2.0 A. Coilcraft CMT4−17−9 was used to test Figure 20. It has a minimum inductance of 17 mH and a maximum current rating of 9.0 A. Circuit conversion efficiency η (%) was calculated without the power loss of the RFI filter.

Figure 18. Power Factor Test Setup

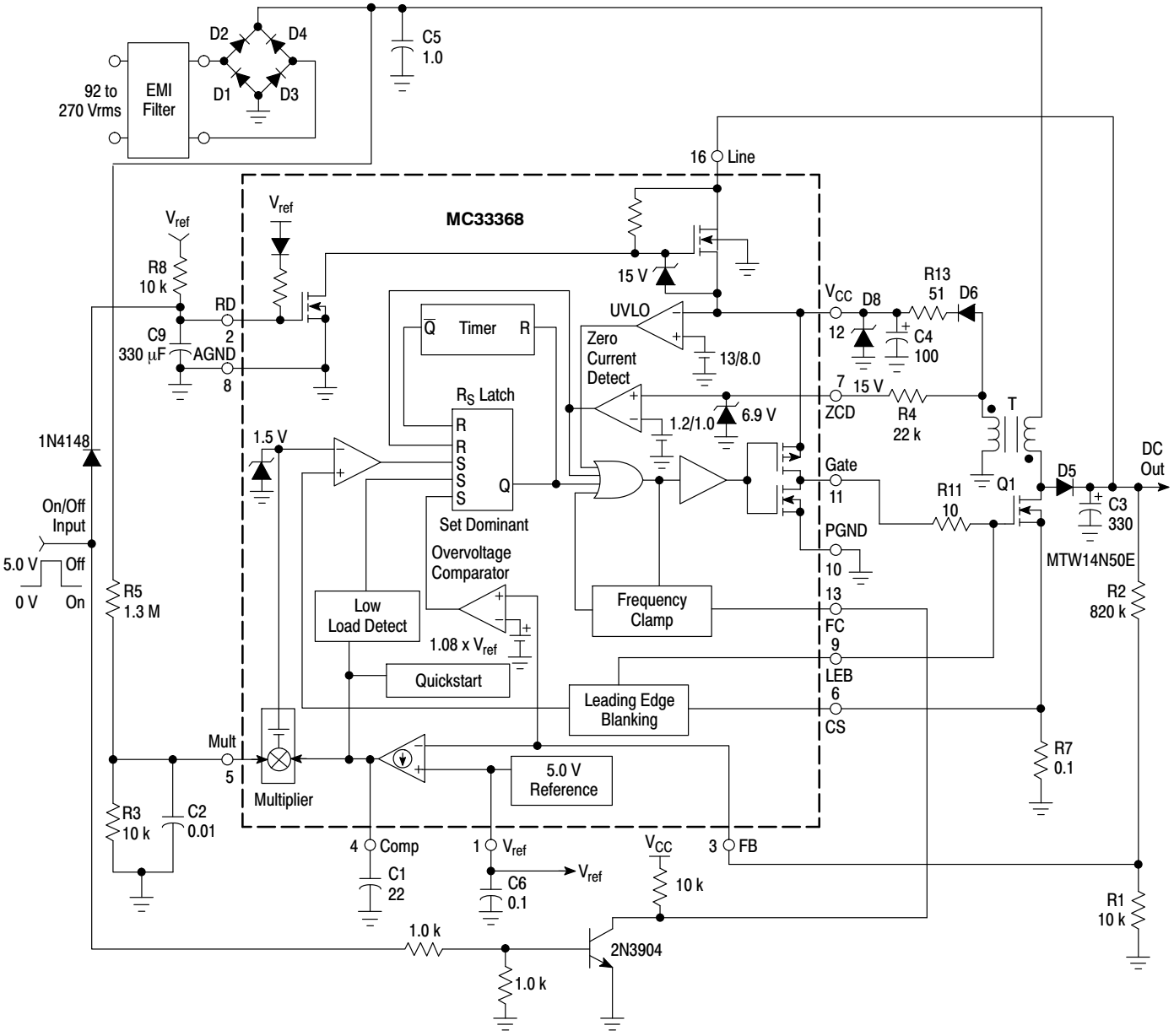


Figure 19. On/Off Control

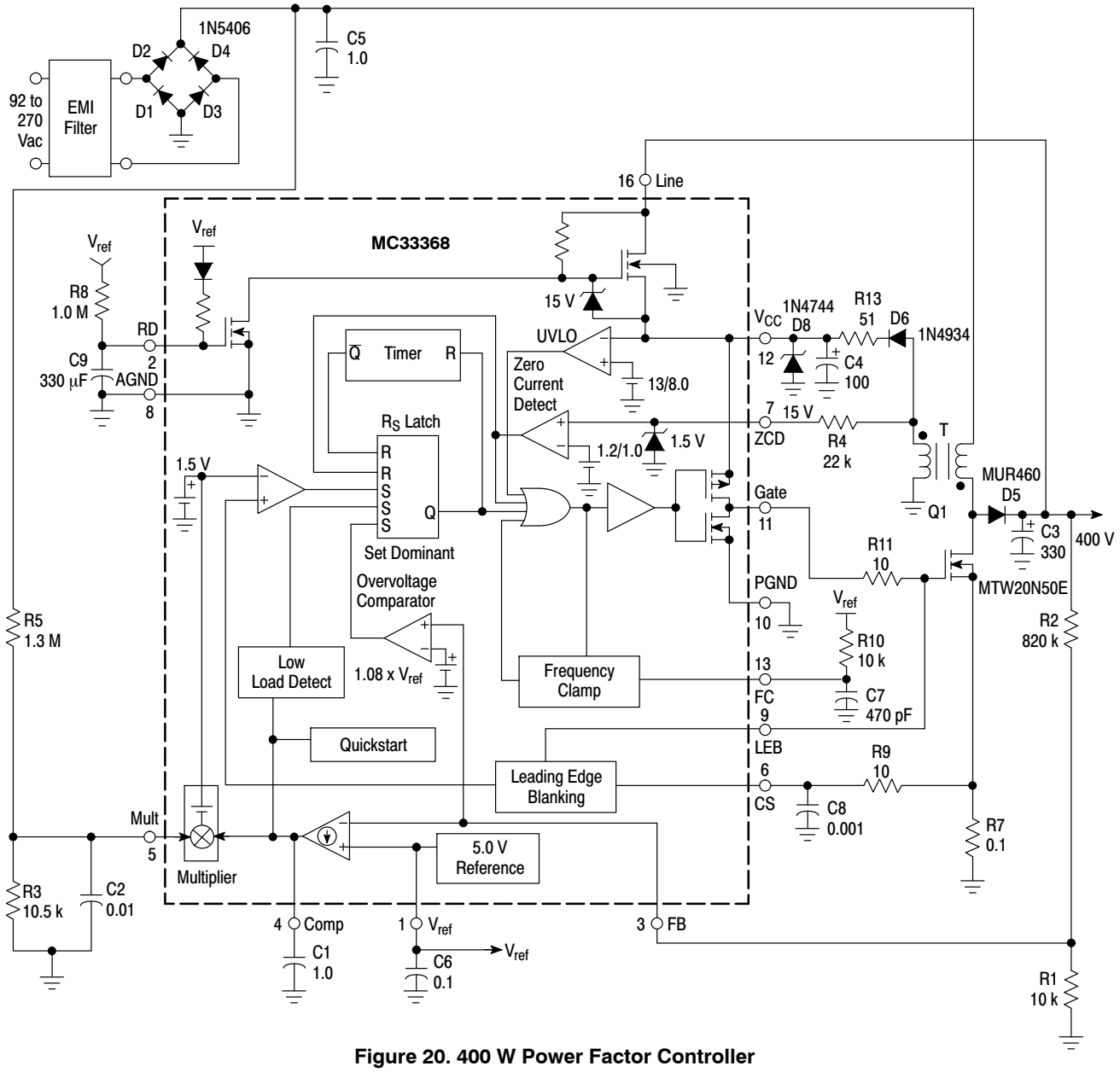
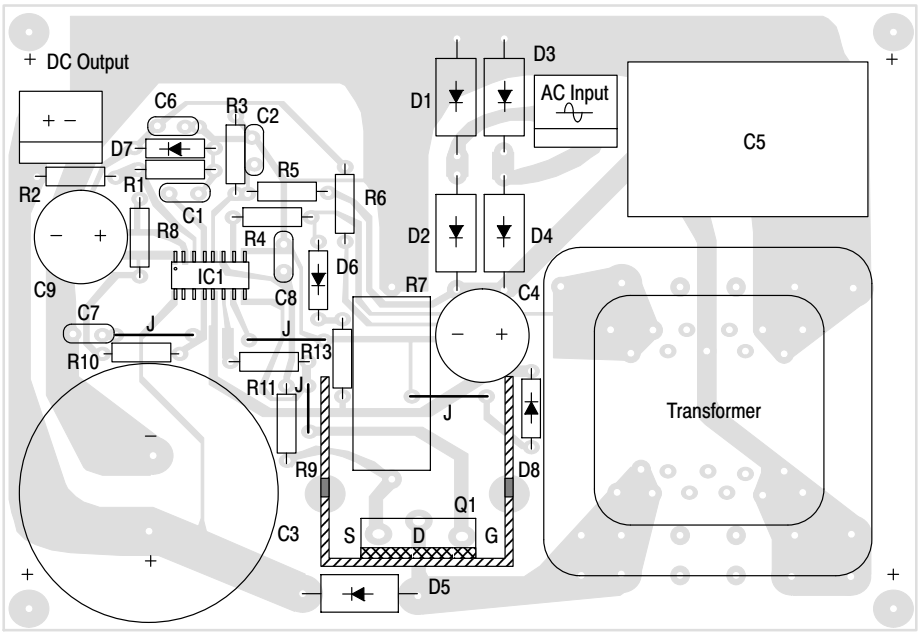
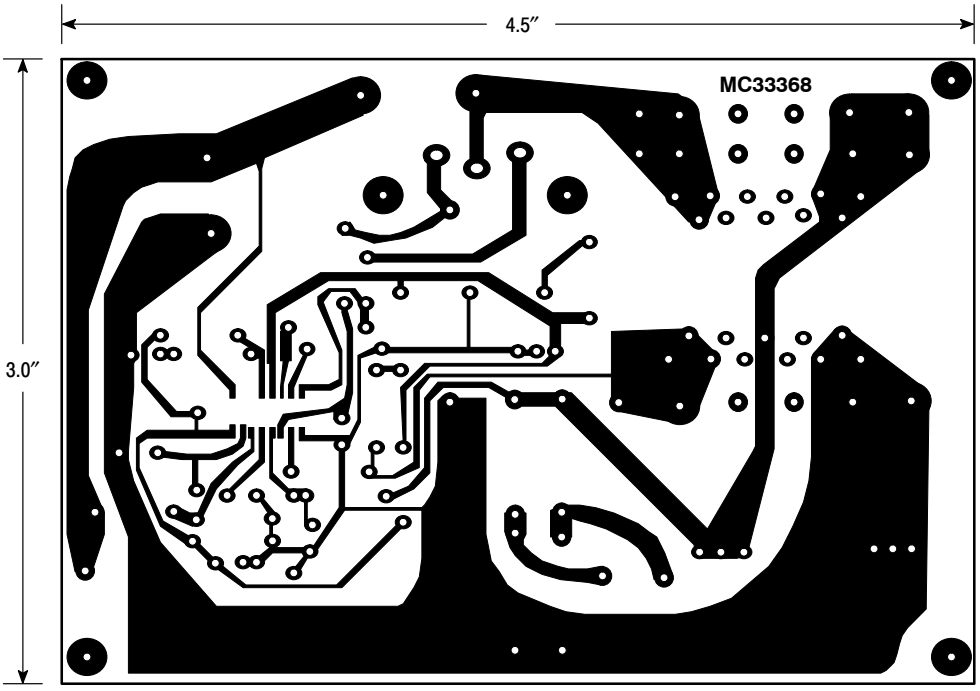


Figure 20. 400 W Power Factor Controller



J = Jumper

(Top View)



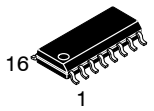
(Bottom View)

Figure 21. Printed Circuit Board and Component Layout (Circuits of Figures 16 and 17)

GreenLine is a trademark of Motorola, Inc.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

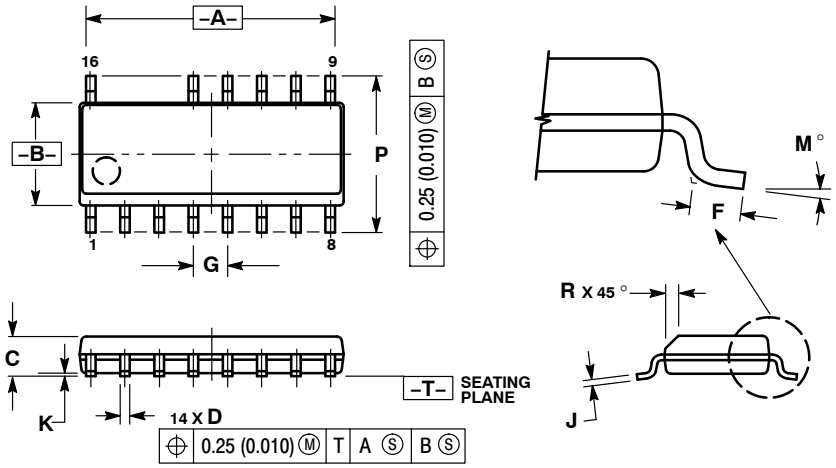
ON Semiconductor®



SCALE 1:1

SOIC−16 MINUS PINS 14, 15
CASE 751K−01
ISSUE O

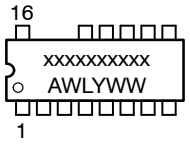
DATE 12/22/1993



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.368	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

MARKING DIAGRAM



xx = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

DOCUMENT NUMBER:	**98ASH70103A**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−16 MINUS PINS 14,15**		**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊