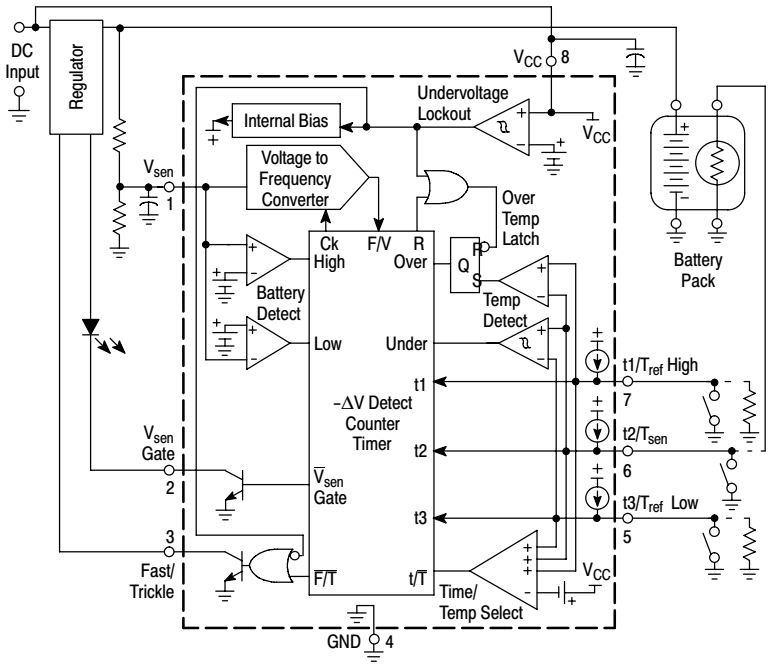
MC33340, MC33342

Battery Fast Charge Controllers

The MC33340 and MC33342 are monolithic control IC's that are specifically designed as fast charge controllers for Nickel Cadmium (NiCd) and Nickel Metal Hydride (NiMH) batteries. These devices feature negative slope voltage detection as the primary means for fast charge termination. Accurate detection is ensured by an output that momentarily interrupts the charge current for precise voltage sampling. An additional secondary backup termination method can be selected that consists of either a programmable time or temperature limit. Protective features include battery over and undervoltage detection, latched over temperature detection, and power supply input undervoltage lockout with hysteresis. Fast charge holdoff time is the only difference between the MC33340 and the MC33342. The MC33340 has a typical holdoff time of 177 seconds and the MC33342 has a typical holdoff time of 708 seconds.

- Negative Slope Voltage Detection with 4.0 mV Sensitivity
- Accurate Zero Current Battery Voltage Sensing
- High Noise Immunity with Synchronous VFC/Logic
- Programmable 1 to 4 Hour Fast Charge Time Limit
- Programmable Over/Undertemperature Detection
- Battery Over and Undervoltage Fast Charge Protection
- Power Supply Input Undervoltage Lockout with Hysteresis
- Operating Voltage Range of 3.25 V to 18 V
- 177 seconds Fast Change Holdoff Time (MC33340)
- 708 seconds Fast Change Holdoff Time (MC33342)
- Pb−Free Packages are Available



This device contains 2,512 active transistors.

Figure 1. Simplified Block Diagram

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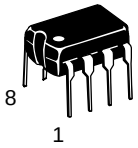
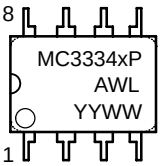
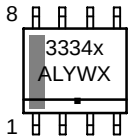
MARKING DIAGRAMS



PDIP−8
P SUFFIX
CASE 626

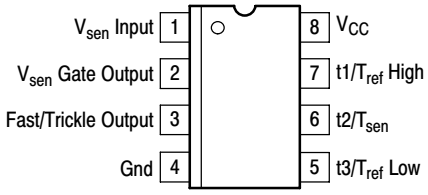


SOIC−8
NB SUFFIX
CASE 751



x	= 0 or 2
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 8)	V_{CC}	18	V
Input Voltage Range			V
Time/Temperature Select (Pins 5, 6, 7)	$V_{IR(t/T)}$	−1.0 to V_{CC}	
Battery Sense, (Note 2) (Pin 1)	$V_{IR(sen)}$	−1.0 to V_{CC} + 0.6 or −1.0 to 10	
V_{sen} Gate Output (Pin 2)			
Voltage	$V_{O(gate)}$	20	V
Current	$I_{O(gate)}$	50	mA
Fast/Trickle Output (Pin 3)			
Voltage	$V_{O(F/T)}$	20	V
Current	$I_{O(F/T)}$	50	mA
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$		°C/W
P Suffix, DIP Plastic Package, Case 626		100	
D Suffix, SO−8 Plastic Package, Case 751		178	
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3)	T_A	−25 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per MIL−STD−883, Method 3015 Machine Model Method 400 V

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 V, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
BATTERY SENSE INPUT (Pin 1)					
Input Sensitivity for −ΔV Detection	$-\Delta V_{th}$	−	−4.0	−	mV
Overvoltage Threshold	$V_{th(OV)}$	1.9	2.0	2.1	V
Undervoltage Threshold	$V_{th(UV)}$	0.95	1.0	1.05	mV
Input Bias Current	I_{IB}	−	10	−	nA
Input Resistance	R_{in}	−	6.0	−	MΩ
TIME/TEMPERATURE INPUTS (Pins 5, 6, 7)					
Programing Inputs (V_{in} = 1.5 V) Input Current Input Current Matching	 I_{in} ΔI_{in}	 −24 −	 −30 1.0	 −36 2.0	 μA %
Input Offset Voltage, Over and Under Temperature Comparators	V_{IO}	−	5.0	−	mV
Under Temperature Comparator Hysteresis (Pin 5)	$V_{H(T)}$	−	44	−	mV
Temperature Select Threshold	$V_{th(t/T)}$	−	V_{CC} −0.7	−	V
INTERNAL TIMING					
Internal Clock Oscillator Frequency	f_{OSC}	−	760	−	kHz
V_{sen} Gate Output (Pin 2) Gate Time Gate Repetition Rate	t_{gate}	 − −	 33 1.38	 − −	 ms s
Fast Charge Holdoff from −ΔV Detection MC33340 MC33342	t_{hold}	 − −	 177 708	 − −	s
V_{sen} GATE OUTPUT (Pin 2)					
Off−State Leakage Current (V_O = 20 V)	I_{off}	−	10	−	nA
Low State Saturation Voltage (I_{sink} = 10 mA)	V_{OL}	−	1.2	−	V
FAST/TRICKLE OUTPUT (Pin 3)					
Off−State Leakage Current (V_O = 20 V)	I_{off}	−	10	−	nA
Low State Saturation Voltage (I_{sink} = 10 mA)	V_{OL}	−	1.0	−	V
UNDERVOLTAGE LOCKOUT (Pin 8)					
Startup Threshold (V_{CC} Increasing, T_A = 25°C)	$V_{th(on)}$	−	3.0	3.25	V
Turn−Off Threshold (V_{CC} Decreasing, T_A = 25°C)	$V_{th(off)}$	2.75	2.85	−	V
TOTAL DEVICE (Pin 8)					
Power Supply Current (Pins 5, 6, 7 Open) Startup (V_{CC} = 2.9 V) Operating (V_{CC} = 6.0 V)	I_{CC}	 − −	 0.65 0.61	 2.0 2.0	mA

2. Whichever voltage is lower.
3. Tested junction temperature range for the MC33340/342: T_{low} = −25°C T_{high} = +85°C

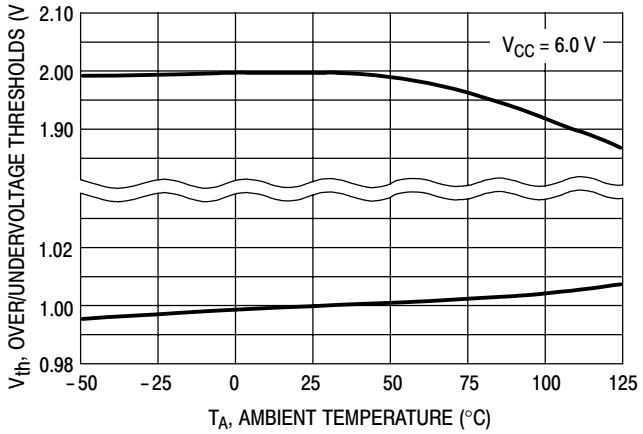


Figure 2. Battery Sense Input Thresholds versus Temperature

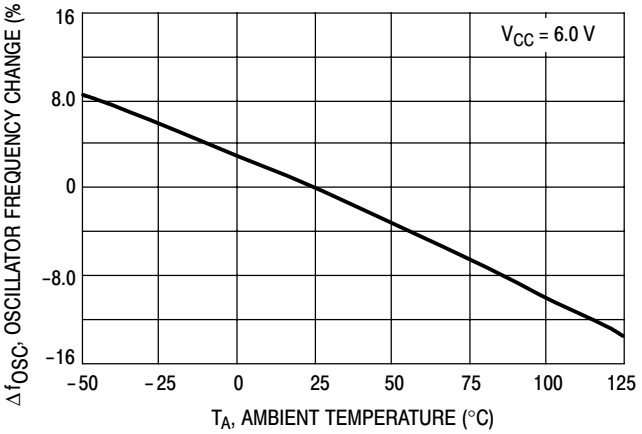


Figure 3. Oscillator Frequency versus Temperature

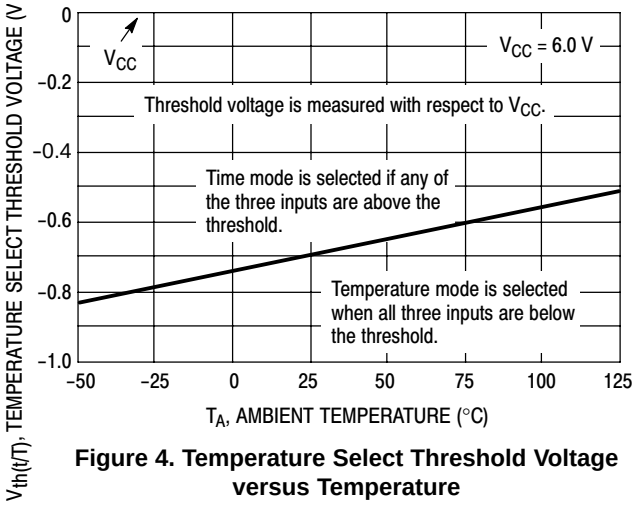


Figure 4. Temperature Select Threshold Voltage versus Temperature

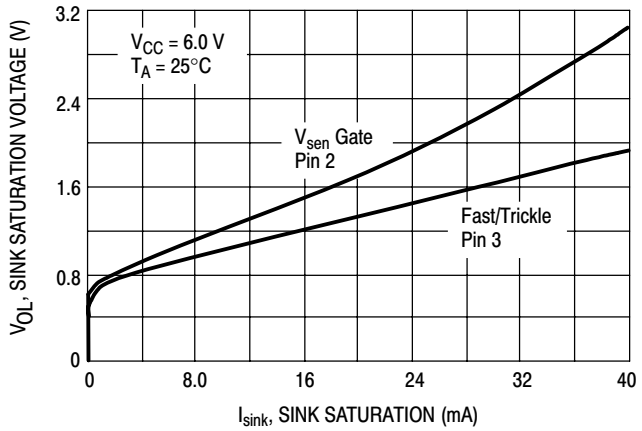


Figure 5. Saturation Voltage versus Sink Current V_{sen} Gate and Fast/Trickle Outputs

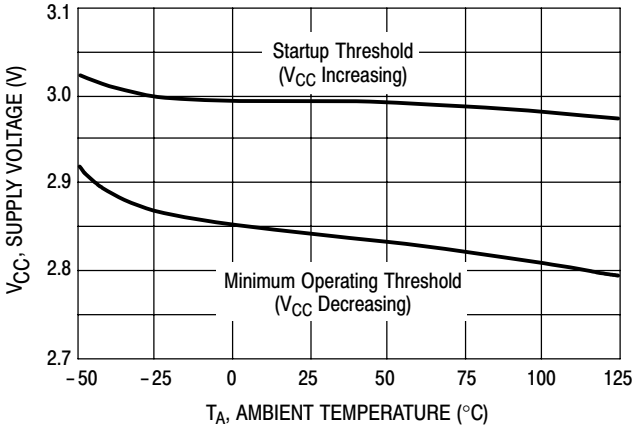


Figure 6. Undervoltage Lockout Thresholds versus Temperature

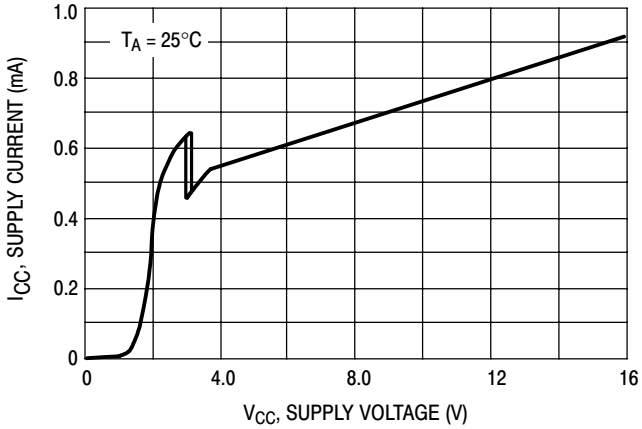


Figure 7. Supply Current versus Supply Voltage

INTRODUCTION

Nickel Cadmium and Nickel Metal Hydride batteries require precise charge termination control to maximize cell capacity and operating time while preventing overcharging. Overcharging can result in a reduction of battery life as well as physical harm to the end user. Since most portable applications require the batteries to be charged rapidly, a primary and usually a secondary or redundant charge sensing technique is employed into the charging system. It is also desirable to disable rapid charging if the battery voltage or temperature is either too high or too low. In order to address these issues, an economical and flexible fast charge controller was developed.

The MC33340/342 contains many of the building blocks and protection features that are employed in modern high performance battery charger controllers that are specifically designed for Nickel Cadmium and Nickel Metal Hydride batteries. The device is designed to interface with either primary or secondary side regulators for easy implementation of a complete charging system. A representative block diagram in a typical charging application is shown in Figure 8.

The battery voltage is monitored by the V_{sen} input that internally connects to a voltage to frequency converter and counter for detection of a negative slope in battery voltage. A timer with three programming inputs is available to provide backup charge termination. Alternatively, these inputs can be used to monitor the battery pack temperature and to set the over and undertemperature limits also for backup charge termination.

Two active low open collector outputs are provided to interface this controller with the external charging circuit. The first output furnishes a gating pulse that momentarily interrupts the charge current. This allows an accurate method of sampling the battery voltage by eliminating voltage drops that are associated with high charge currents and wiring resistances. Also, any noise voltages generated by the charging circuitry are eliminated. The second output is designed to switch the charging source between fast and trickle modes based upon the results of voltage, time, or temperature. These outputs normally connect directly to a linear or switching regulator control circuit in non−isolated primary or secondary side applications. Both outputs can be used to drive optoisolators in primary side applications that require galvanic isolation. Figure 9 shows the typical charge characteristics for NiCd and NiMh batteries.

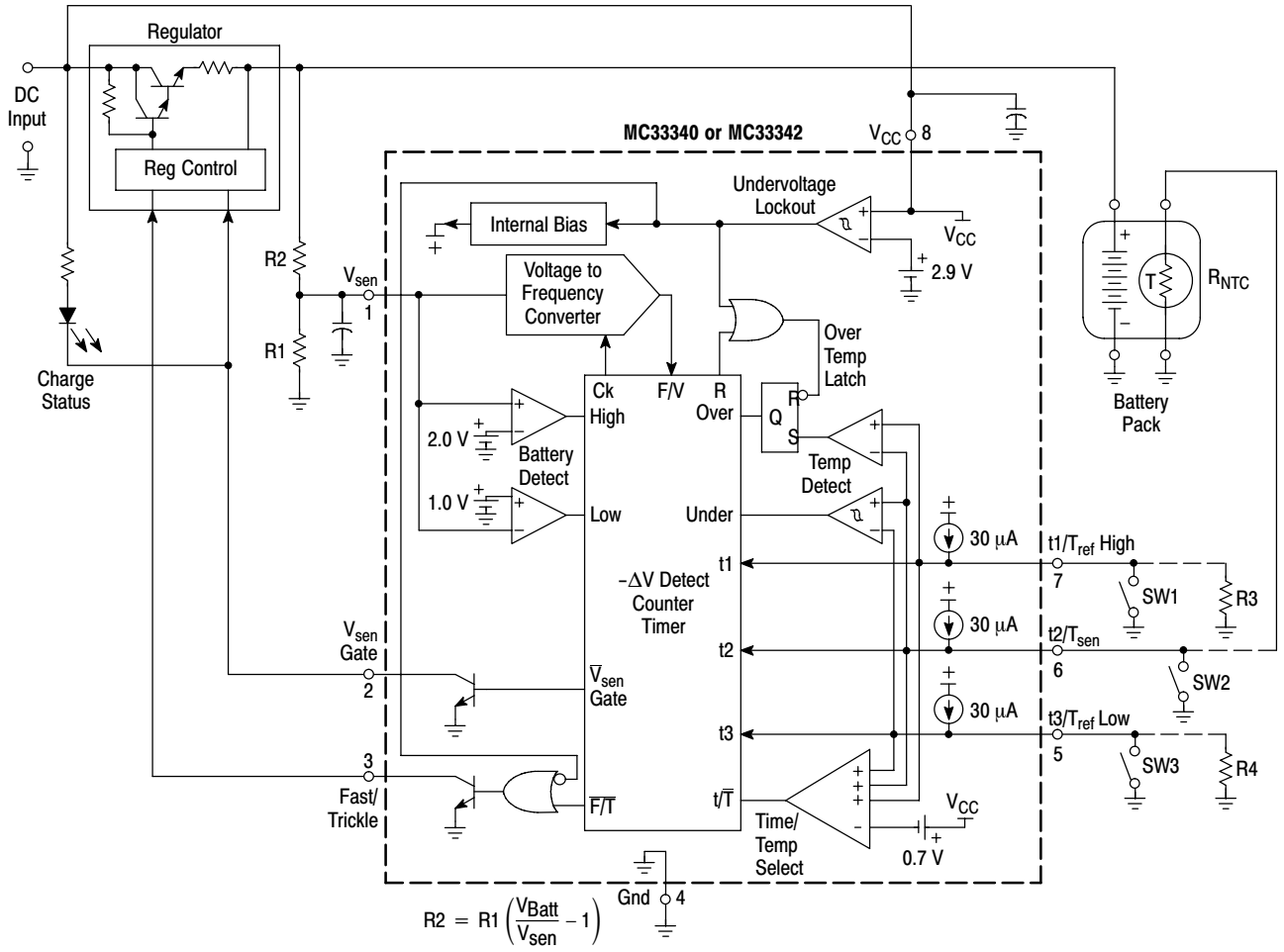


Figure 8. Typical Battery Charging Application

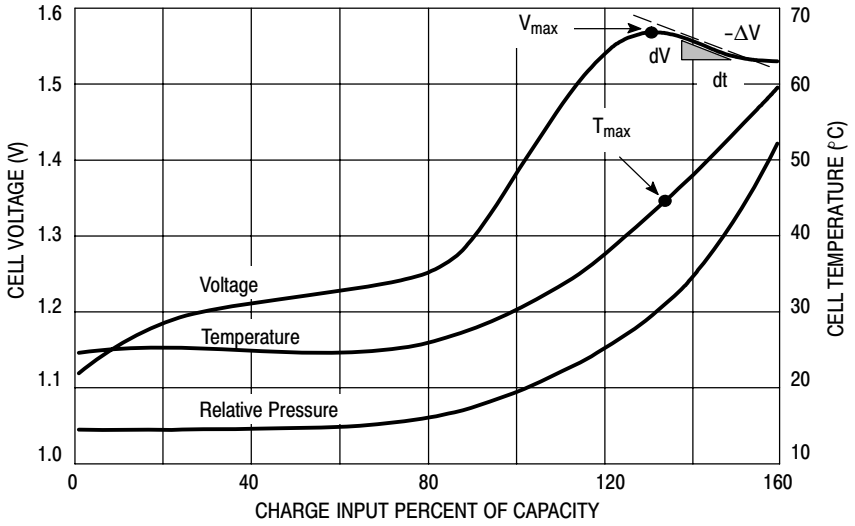


Figure 9. Typical Charge Characteristics for NiCd and NiMh Batteries

OPERATING DESCRIPTION

The MC33340/342 starts up in the fast charge mode when power is applied to V_{CC}. A change to the trickle mode can occur as a result of three possible conditions. The first is if the V_{sen} input voltage is above 2.0 V or below 1.0 V. Above 2.0 V indicates that the battery pack is open or disconnected, while below 1.0 V indicates the possibility of a shorted or defective cell. The second condition is when the MC33340/342 detects a fully charged battery by measuring a negative slope in battery voltage. The MC33340/342 recognize a negative voltage slope after the preset holdoff time (t_{hold}) has elapsed during a fast charge cycle. This indicates that the battery pack is fully charged. The third condition is either due to the battery pack being out of a programmed temperature range, or that the preset timer period has been exceeded.

There are three conditions that will cause the controller to return from trickle to fast charge mode. The first is if the V_{sen} input voltage moved to within the 1.0 to 2.0 V range from initially being either too high or too low. The second is if the battery pack temperature moved to within the programmed temperature range, but only from initially being too cold. Third is by cycling V_{CC} off and then back on causing the internal logic to reset. A concise description of the major circuit blocks is given below.

Negative Slope Voltage Detection

A representative block diagram of the negative slope voltage detector is shown in Figure 10. It includes a Synchronous Voltage to Frequency Converter, a Sample Timer, and a Ratchet Counter. The V_{sen} pin is the input for the Voltage to Frequency Converter (VFC), and it connects to the rechargeable battery pack terminals through a resistive voltage divider. The input has an impedance of approximately 6.0 MΩ and a maximum voltage range of −1.0 V to V_{CC} + 0.6 V or 0 V to 10 V, whichever is lower. The 10 V upper limit is set by an internal zener clamp that provides protection in the event of an electrostatic discharge. The VFC is a charge−balanced synchronous type which generates output pulses at a rate of $F_V = V_{sen}$ (24 kHz).

The Sample Timer circuit provides a 95 kHz system clock signal (SCK) to the VFC. This signal synchronizes the F_V output to the other Sample Timer outputs used within the detector. At 1.38 second intervals the V_{sen} Gate output goes low for a 33 ms period. This output is used to momentarily interrupt the external charging power source so that a precise voltage measurement can be taken. As the V_{sen} Gate goes low, the internal Preset control line is driven high for 11 ms. During this time, the battery voltage at the V_{sen} input is allowed to stabilize and the previous F_V count is preloaded. At the Preset high−to−low transition, the Convert line goes high for 22 ms. This gates the F_V pulses into the ratchet counter for a comparison to the preloaded count. Since the Convert time is derived from the same clock that controls the VFC, the number of F_V pulses is independent of the clock frequency. If the new sample has more counts than were preloaded, it becomes the new peak count and the cycle is repeated 1.38 seconds later. If the new sample has two fewer counts, a less than peak voltage event has occurred, and a register is initialized. If two successive less than peak voltage events occur, the −ΔV 'AND' gate output goes high and the Fast/Trickle output is latched in a low state, signifying that the battery pack has reached full charge status.

Negative slope voltage detection starts after 60 ms have elapsed in the fast charge mode. This does not affect the Fast/Trickle output until the holdoff time (t_{hold}) has elapsed during the fast charge mode. Two scenarios then exist. Trickle mode holdoff is implemented to ignore any initial drop in voltage that may occur when charging batteries that have been stored for an extended time period. If the negative slope voltage detector senses that initial drop during the holdoff time, and the input voltage rises as the battery charges, the Fast/Trickle output will remain open. However, if the negative slope voltage detector senses a negative drop in voltage during the holdoff time and the input voltage never rises above that last detected level, the Fast/Trickle output will latch into a low state. The negative slope voltage detector has a maximum resolution of 2.0 V divided by 1023 mV, or 1.955 mV per count with an uncertainty of ±1.0 count. This yields a detection range of 1.955 mV to 5.865 mV. In order to obtain maximum sensing accuracy, the R2/R1 voltage divider must be adjusted so that the V_{sen} input voltage is slightly less than 2.0 V when the battery pack is fully charged. Voltage variations due to temperature and cell manufacturing must be considered.

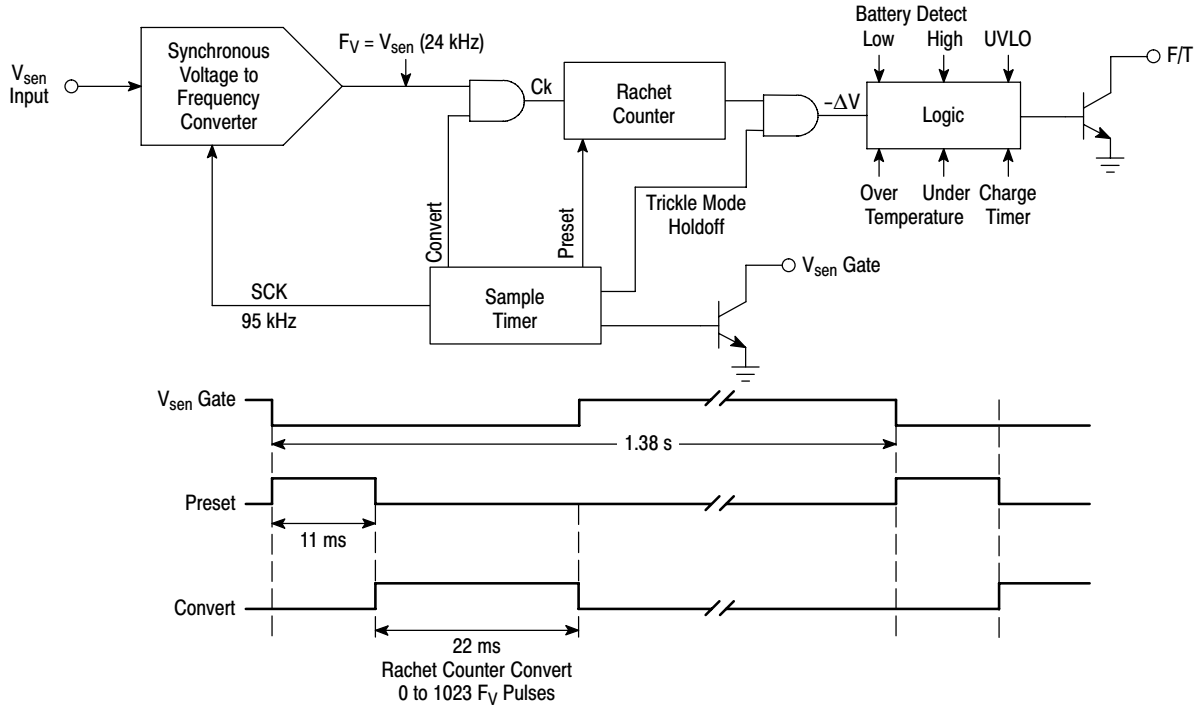


Figure 10. Negative Slope Voltage Detector

Fast Charge Timer

A programmable backup charge timer is available for fast charge termination. The timer is activated by the Time/Temp Select comparator, and is programmed from the $t1/T_{ref}$ High, $t2/T_{sen}$, and $t3/T_{ref}$ Low inputs. If one or more of these inputs is allowed to go above V_{CC} − 0.7 V or is left open, the comparator output will switch high, indicating that the timer feature is desired. The three inputs allow one of seven possible fast charge time limits to be selected. The programmable time limits, rounded to the nearest whole minute, are shown in Table 1.

Over/Under Temperature Detection

A backup over/under temperature detector is available and can be used in place of the timer for fast charge termination. The timer is disabled by the Time/Temp Select comparator when each of the three programming inputs are held below V_{CC} − 0.7 V.

Temperature sensing is accomplished by placing a negative temperature coefficient (NTC) thermistor in thermal contact with the battery pack. The thermistor connects to the $t2/T_{sen}$ input which has a 30 μA current source pull−up for developing a temperature dependent voltage. The temperature limits are set by a resistor that connects from the $t1/T_{ref}$ High and the $t3/T_{ref}$ Low inputs to ground. Since all three inputs contain matched 30 μA current source pull−ups, the required programming resistor values are identical to that of the thermistor at the desired over and under trip temperature. The temperature window detector is composed of two comparators with a common input that connects to the $t2/T_{sen}$ input.

The lower comparator senses the presence of an under temperature condition. When the lower temperature limit is exceeded, the charger is switched to the trickle mode. The comparator has 44 mV of hysteresis to prevent erratic

switching between the fast and trickle modes as the lower temperature limit is crossed. The amount of temperature rise to overcome the hysteresis is determined by the thermistor's rate of resistance change or sensitivity at the under temperature trip point. The required resistance change is:

$$\Delta R(T_{Low} \rightarrow T_{High}) = \frac{V_{H(T)}}{I_{in}} = \frac{44\ mV}{30\ \mu A} = 1.46\ k$$

The resistance change approximates a thermal hysteresis of 2°C with a 10 kΩ thermistor operating at 0°C. The under temperature fast charge inhibit feature can be disabled by biasing the $t3/T_{ref}$ Low input to a voltage that is greater than that present at $t2/T_{sen}$, and less than V_{CC} − 0.7 V. Under extremely cold conditions, it is possible that the thermistor resistance can become too high, allowing the $t2/T_{sen}$ input to go above V_{CC} − 0.7 V, and activate the timer. This condition can be prevented by placing a resistor in parallel with the thermistor. Note that the time/temperature threshold of V_{CC} − 0.7 V is a typical value at room temperature. Refer to the Electrical Characteristics table and to Figure 4 for additional information.

The upper comparator senses the presence of an over temperature condition. When the upper temperature limit is exceeded, the comparator output sets the Overtemperature Latch and the charger is switched to trickle mode. Once the latch is set, the charger cannot be returned to fast charge, even after the temperature falls below the limit. This feature prevents the battery pack from being continuously temperature cycled and overcharged. The latch can be reset by removing and reconnecting the battery pack or by cycling the power supply voltage.

If the charger does not require either the time or temperature backup features, they can both be easily disabled. This is accomplished by biasing the $t3/T_{ref}$ Low input to a voltage greater than $t2/T_{sen}$, and by grounding the $t1/T_{ref}$ High input. Under these conditions, the Time/Temp Select comparator output is low, indicating that the temperature mode is selected, and that the $t2/T_{sen}$ input is biased within the limits of an artificial temperature window.

Charging of battery packs that are used in portable power tool applications typically use temperature as the only means for fast charge termination. The MC33340/342 can be configured in this manner by constantly resetting the −ΔV detection logic. This is accomplished by biasing the V_{sen} input to ≈1.5 V from a two resistor divider that is connected between the positive battery pack terminal and ground. The V_{sen} Gate output is also connected to the V_{sen} input. Now, each time that the Sample Timer causes the V_{sen} output to go low, the V_{sen} input will be pulled below the undervoltage threshold of 1.0 V. This causes a reset of the −ΔV logic every 1.38 seconds, thus disabling detection.

Operating Logic

The order of events in the charging process is controlled by the logic circuitry. Each event is dependent upon the input conditions and the chosen method of charge termination. A table summary containing all of the possible operating modes is shown in Table 2.

Table 1. FAST CHARGE BACKUP TERMINATION TIME/TEMPERATURE LIMIT

Backup Termination Mode	Programming Inputs			Time Limit Fast Charge (Minutes)
	$t3/T_{ref}$ Low (Pin 5)	$t2/T_{sen}$ (Pin 6)	$t1/T_{ref}$ High (Pin 7)	
Time	Open	Open	Open	283
Time	Open	Open	GND	247
Time	Open	GND	Open	212
Time	Open	GND	GND	177
Time	GND	Open	Open	141
Time	GND	Open	GND	106
Time	GND	GND	Open	71
Temperature	0 V to V_{CC} − 0.7 V	0 V to V_{CC} − 0.7 V	0 V to V_{CC} − 0.7 V	Timer Disabled

Table 2. CONTROLLER OPERATING MODE TABLE

Input Condition	Controller Operation
V_{sen} Input Voltage: >1.0 V and <2.0 V	The divided down battery pack voltage is within the fast charge voltage range. The charger switches from trickle to fast charge mode as V_{sen} enters this voltage range, and a reset pulse is then applied to the timer and the overtemperature latch.
>1.0 V and <2.0 V with two consecutive −ΔV events detected after the initial holdoff period (t_{hold})	The battery pack has reached full charge and the charger switches from fast to a latched trickle mode. A reset pulse must be applied for the charger to switch back to the fast mode. The reset pulse occurs when entering the 1.0 V to 2.0 V window for V_{sen} or when V_{CC} rises above 3.0 V.
<1.0 V or >2.0 V	The divided down battery pack voltage is outside of the fast charge voltage range. The charger switches from fast to trickle mode.
Timer Backup: Within time limit	The timer has not exceeded the programmed limit. The charger will be in fast charge mode if V_{sen} and V_{CC} are within their respective operating limits.
Beyond time limit	The timer has exceeded the programmed limit. The charger switches from fast to a latched trickle mode.
Temperature Backup: Within limits	The battery pack temperature is within the programmed limits. The charger will be in fast charge mode if V_{sen} and V_{CC} are within their respective operating limits.
Below lower limit	The battery pack temperature is below the programmed lower limit. The charger will stay in trickle mode until the lower temperature limit is exceeded. When exceeded, the charger will switch from trickle to fast charge mode.
Above upper limit	The battery pack temperature has exceeded the programmed upper limit. The charger switches from fast to a latched trickle mode. A reset signal must be applied and then released for the charger to switch back to the fast charge mode. The reset pulse occurs when entering the 1.0 V to 2.0 V window for V_{sen} or when V_{CC} rises above 3.0 V.
Power Supply Voltage: V_{CC} >3.0 V and <18 V	This is the nominal power supply operating voltage range. The charger will be in fast charge mode if V_{sen}, and temperature backup or timer backup are within their respective operating limits.
V_{CC} >0.6 V and <2.8 V	The undervoltage lockout comparator will be activated and the charger will be in trickle mode. A reset signal is applied to the timer and over temperature latch.

Testing

Under normal operating conditions, it would take 283 minutes to verify the operation of the 34 stage ripple counter used in the timer. In order to significantly reduce the test time, three digital switches were added to the circuitry and are used to bypass selected divider stages. Entering each of the test modes without requiring additional package pins or affecting normal device operation proved to be challenging. Refer to the timer functional block diagram in Figure 11.

Switch 1 bypasses 19 divider stages to provide a 524,288 times speedup of the clock. This switch is enabled when the V_{sen} input falls below 1.0 V. Verification of the programmed fast charge time limit is accomplished by measuring the propagation delay from when the V_{sen} input falls below 1.0 V, to when the F/T output changes from a high−to−low state. The 71, 106, 141, 177, 212, 247 and 283 will now correspond to 8.1, 12.1, 16.2, 20.2, 24.3, 28.3 and 32.3 ms delays. It is possible to enter this test mode during operation if the equivalent battery pack voltage was to fall below 1.0 V. This will not present a problem since the device would normally switch from fast to trickle mode under these conditions, and the relatively short variable time delay would be transparent to the user.

Switch 2 bypasses 11 divider stages to provide a 2048 times speedup of the clock. This switch is necessary for testing the 19 stages that were bypassed when switch 1 was enabled. Switch 2 is enabled when the V_{sen} input falls below 1.0 V and the $t1/T_{ref}$ High input is biased at −100 mV. Verification of the 19 stages is accomplished by measuring a nominal propagation delay of 338.8 ms from when the V_{sen} input falls below 1.0 V, to when the F/T output changes from a high−to−low state.

Switch 3 is a dual switch consisting of sections “A” and “B”. Section “A” bypasses 5 divider stages to provide a 32 times speedup of the V_{sen} gate signal that is used in sampling the battery voltage. This speedup allows faster test verification of two successive −ΔV events. Section “B” bypasses 11 divider stages to provide a 2048 speedup of the trickle mode holdoff timer. Switches 3A and 3B are both activated when the $t1/T_{ref}$ High input is biased at −100 mV with respect to Pin 4.

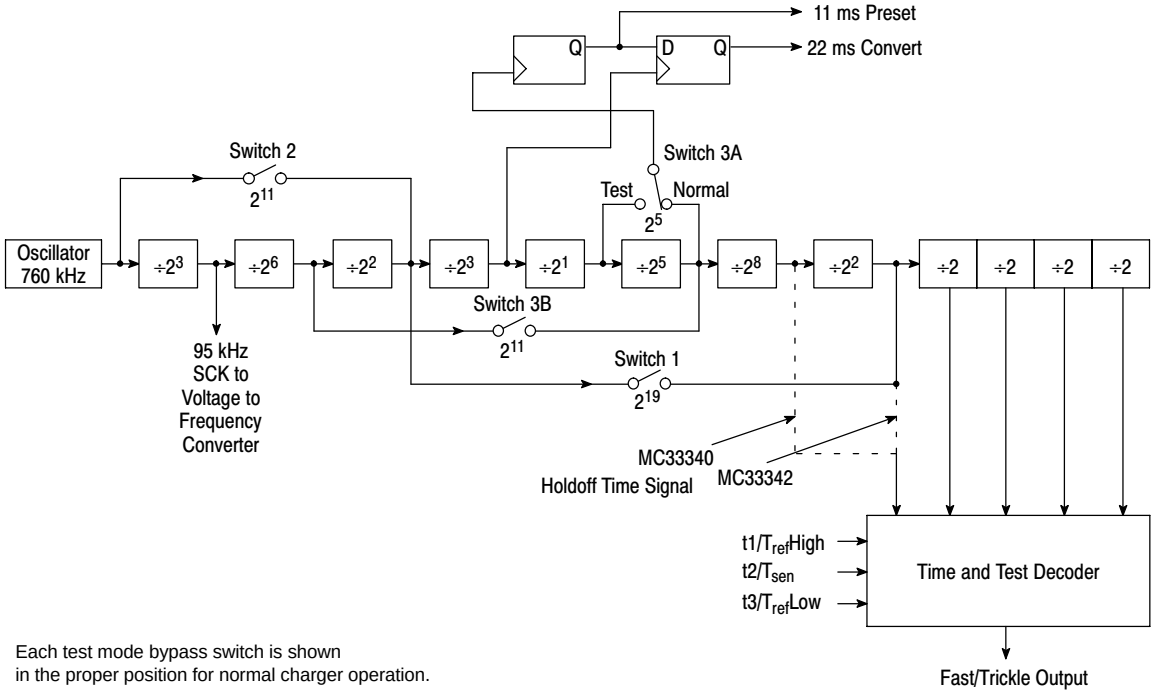
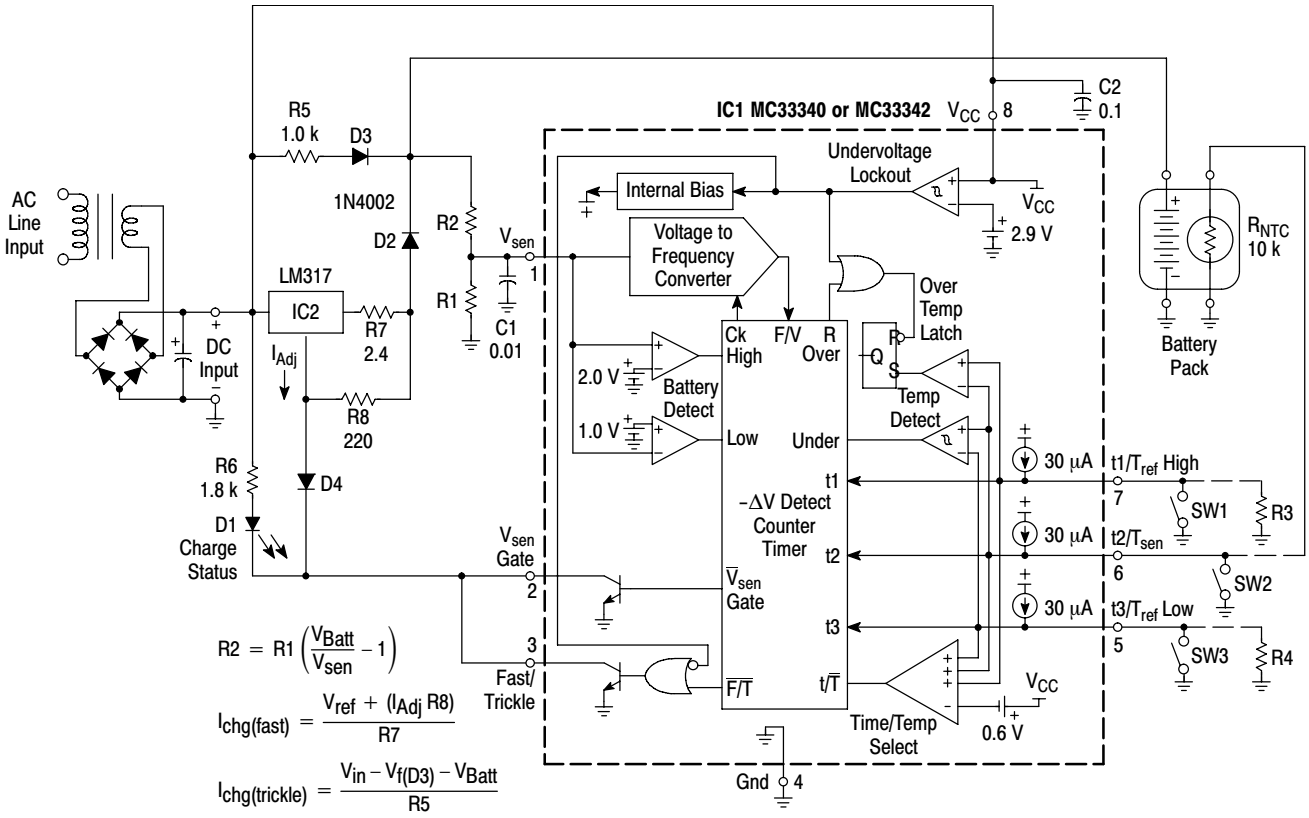


Figure 11. Timer Functional Block Diagram



This application combines the MC33340/342 with an adjustable three terminal regulator to form an isolated secondary side battery charger. Regulator IC2 operates as a constant current source with R7 setting the fast charge level. The trickle charge level is set by R5. The R2/R1 divider should be adjusted so that the V_{sen} input is less than 2.0 V when the batteries are fully charged. The printed circuit board shown below will accept the several TO−220 style heat-sinks for IC2 and are all manufactured by AAVID Engineering Inc.

Figure 12. Line Isolated Linear Regulator Charger

AAVID #	θ_{SA} °C/W
592502B03400	24.0
593002B03400	14.0
590302B03600	9.2

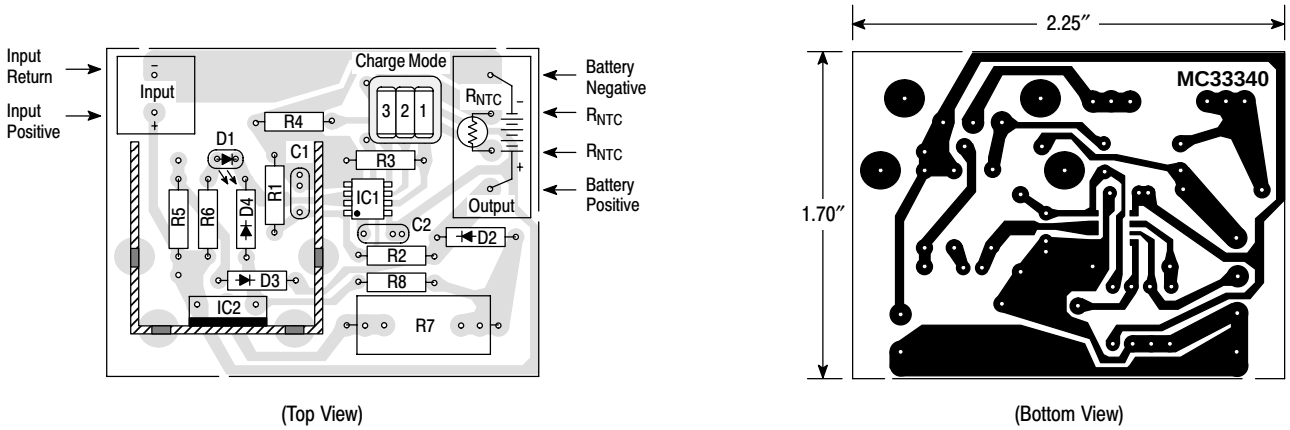
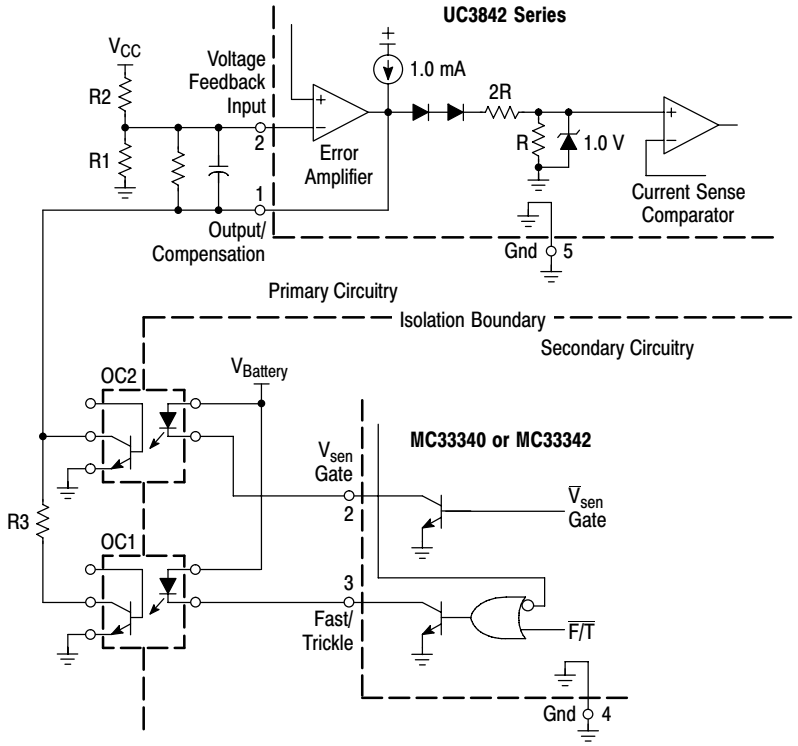
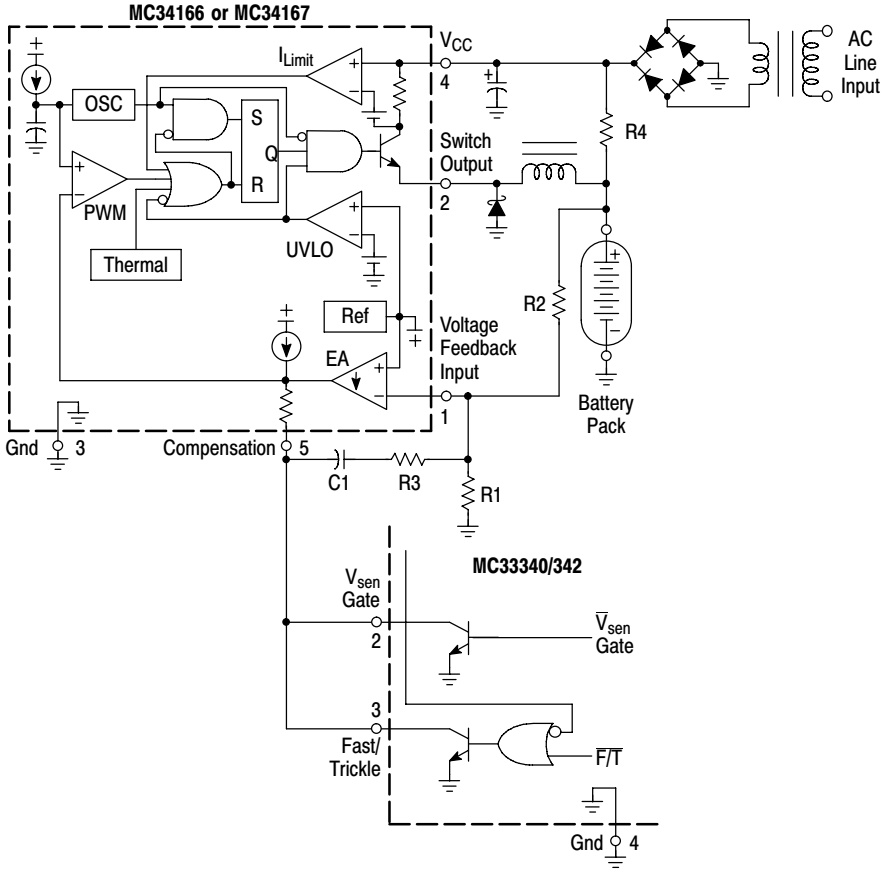


Figure 13. Printed Circuit Board and Component Layout (Circuit of Figure 12)



The MC33340/342 can be combined with any of the devices in the UC3842 family of current mode controllers to form a switch mode battery charger. In this example, optocouplers OC1 and OC2 are used to provide isolated control signals to the UC3842. During battery voltage sensing, OC2 momentarily grounds the Output/Compensation pin, effectively turning off the charger. When fast charge termination is reached, OC1 turns on, and grounds the lower side of R3. This reduces the peak switch current threshold of the Current Sense Comparator to a programmed trickle current level. For additional converter design information, refer to the UC3842 and UC3844 device family data sheets.

Figure 14. Line Isolated Switch Mode Charger



The MC33340/342 can be used to control the MC34166 or MC34167 power switching regulators to produce an economical and efficient fast charger. These devices are capable of operating continuously in current limit with an input voltage range of 7.5 to 40 V. The typical charging current for the MC34166 and MC34167 is 4.3 A and 6.5 A respectively. Resistors R2 and R1 are used to set the battery pack fast charge float voltage. If precise float voltage control is not required, components R1, R2, R3 and C1 can be deleted, and Pin 1 must be grounded. The trickle current level is set by resistor R4. It is recommended that a redundant charge termination method be employed for end user protection. This is especially true for fast charger systems. For additional converter design information, refer to the MC34166 and MC34167 data sheets.

Figure 15. Switch Mode Fast Charger

ORDERING INFORMATION

Device	Package	Shipping†
MC33340D	SO−8	98 Units / Rail
MC33340DG	SO−8 (Pb−Free)	
MC33340DR2	SO−8	2500 / Tape & Reel
MC33340DR2G	SO−8 (Pb−Free)	
MC33340P	PDIP−8	1000 Units / Rail
MC33340PG	PDIP−8 (Pb−Free)	
MC33342D	SO−8	98 Units / Rail
MC33342DG	SO−8 (Pb−Free)	
MC33342DR2	SO−8	2500 / Tape & Reel
MC33342DR2G	SO−8 (Pb−Free)	
MC33342P	PDIP−8	1000 Units / Rail
MC33342PG	PDIP−8 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

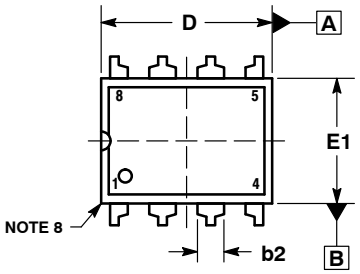
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

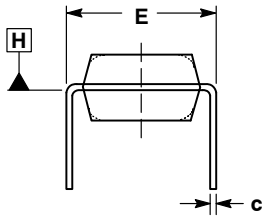
SCALE 1:1

PDIP–8
CASE 626–05
ISSUE P

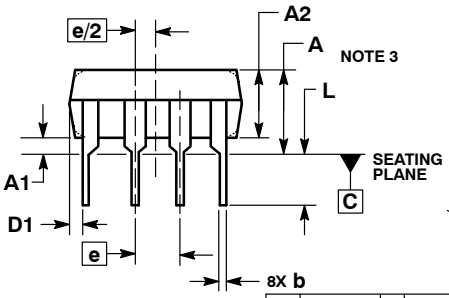
DATE 22 APR 2015



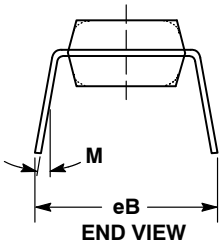
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



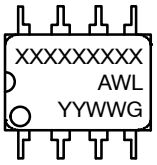
END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

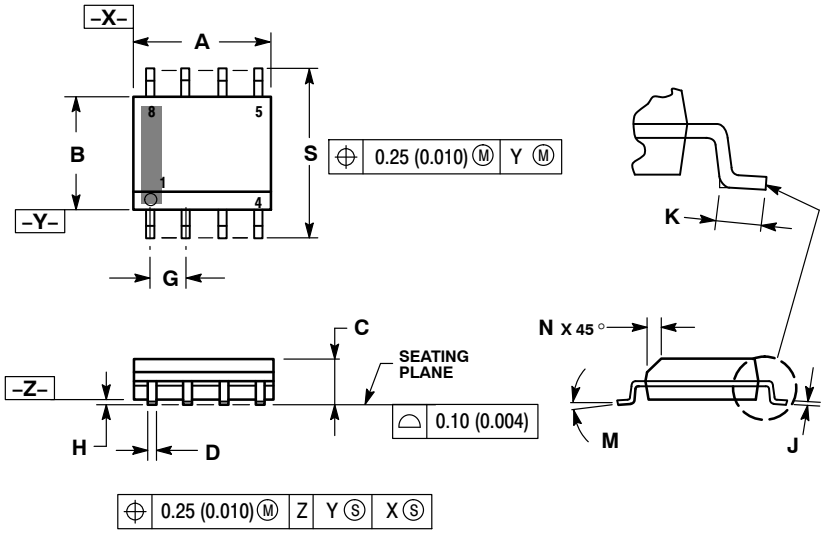
DOCUMENT NUMBER:	98ASB42420B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	PDIP–8	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

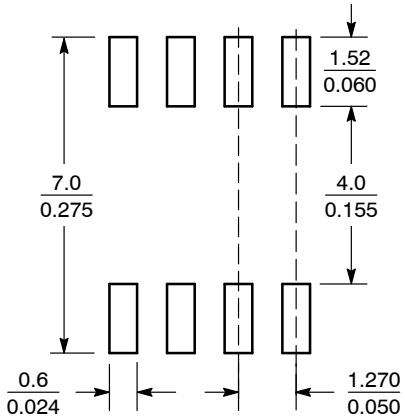
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

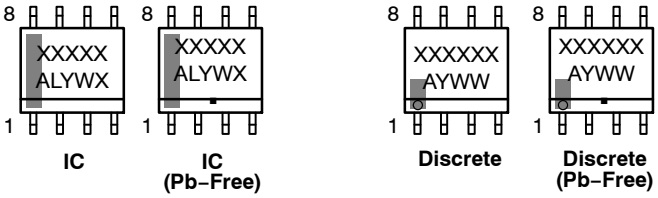
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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