PCIe-6361, PXIe-6361, and USB-6361

2022-10-07

Contents

PCIe-6361, PXIe-6361, and USB-6361 Specifications

PCIe-6361, PXIe-6361, and USB-6361 Specifications

The following specifications are typical at 25 °C, unless otherwise noted. For more information about the PCIe-6361, PXIe-6361, and USB-6361, refer to the **X Series User Manual** available from ni.com/manuals.

Analog Input

Number of channels	8 differential or 16 single ended
ADC resolution	16 bits
DNL	No missing codes guaranteed
INL	Refer to the **AI Absolute Accuracy** section.
Sample rate	
Single channel maximum	2.00 MS/s
Multichannel maximum (aggregate)	1.00 MS/s
Minimum	No minimum
Timing resolution	10 ns
Timing accuracy	50 ppm of sample rate

Input coupling	DC
Input range	±0.1 V, ±0.2 V, ±0.5 V, ±1 V, ±2 V, ±5 V, ±10 V
Maximum working voltage for analog inputs (signal + common mode)	±11 V of AI GND
CMRR (DC to 60 Hz)	100 dB

Input impedance

Device on

AI+ to AI GND	>10 GΩ in parallel with 100 pF
AI- to AI GND	>10 GΩ in parallel with 100 pF

Device off

AI+ to AI GND	820 Ω
AI- to AI GND	820 Ω

Input bias current	±100 pA

Crosstalk (at 100 kHz)

Adjacent channels	-75 dB
Non-adjacent channels	-95 dB

Small signal bandwidth (-3 dB)	1.7 MHz

Input FIFO size	2,047 samples
Scan list memory	4,095 entries
Data transfers	
PCIe/PXIe	DMA (scatter-gather), programmed I/O
USB	USB Signal Stream, programmed I/O
Overvoltage protection for all analog input and sense channels	
Device on	±25 V for up to two AI pins
Device off	±15 V for up to two AI pins
Input current during overvoltage condition	±20 mA max/AI pin

Settling Time for Multichannel Measurements

Range	±60 ppm of Step (±4 LSB for Full-Scale Step)	±15 ppm of Step (±1 LSB for Full-Scale Step)
± 10 V, ±5 V, ±2 V, ±1 V	1 µs	1.5 µs
±0.5 V	1.5 µs	2 µs
±0.2 V, ±0.1 V	2 µs	8 µs

Typical Performance Graphs

Figure 1. Settling Error versus Time for Different Source Impedances

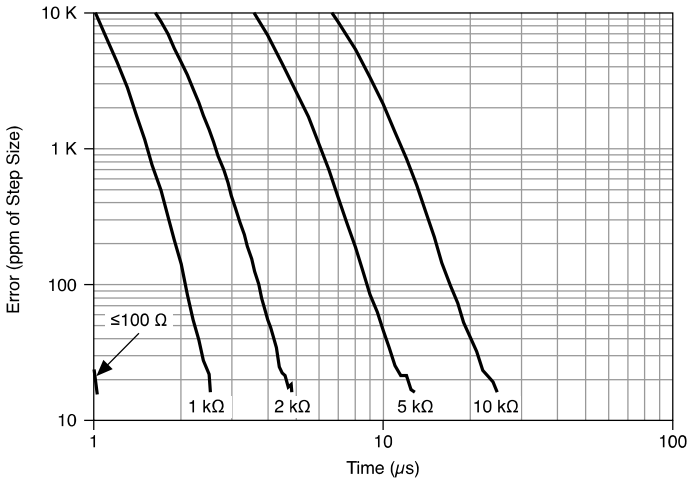


Figure 2. AI <0..15> Small Signal Bandwidth

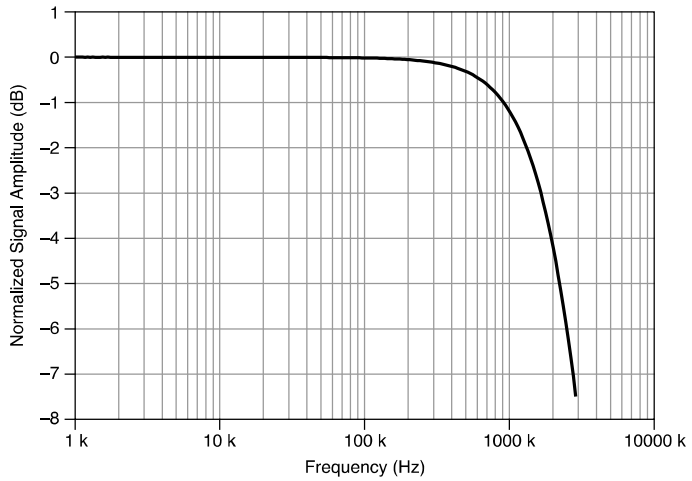
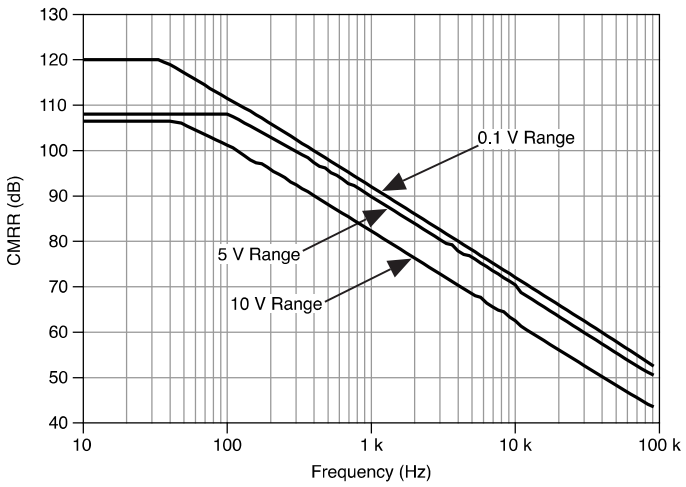


Figure 3. AI <0..15> CMRR



AI Absolute Accuracy

Nominal Range Positive Full Scale	Nominal Range Negative Full Scale	Residual Gain Error (ppm of Reading)	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	Random Noise, σ (µVrms)	Absolute Accuracy at Full Scale (µV)
10	-10	48	13	21	315	1,660
5	-5	55	13	21	157	870
2	-2	55	13	24	64	350
1	-1	65	17	27	38	190
0.5	-0.5	68	17	34	27	100
0.2	-0.2	95	27	55	21	53
0.1	-0.1	108	45	90	17	33

Table 1. AI Absolute Accuracy

For more information about absolute accuracy at full scale, refer to the AI Absolute Accuracy Example section.

Gain tempco	13 ppm/°C
Reference tempco	1 ppm/°C

INL error	60 ppm of range

> **Note** Accuracies listed are valid for up to two years from the device external calibration.

AI Absolute Accuracy Equation

AbsoluteAccuracy = Reading · (GainError) + Range · (OffsetError) + NoiseUncertainty

- GainError = ResidualGainError + GainTempco · (TempChangeFromLastInternalCal) + ReferenceTempco · (TempChangeFromLastExternalCal)
- OffsetError = ResidualOffsetError + OffsetTempco · (TempChangeFromLastInternalCal) + INLError
- NoiseUncertainty = $\frac{\text{Random Noise} \quad 3}{\sqrt{10,000}}$ for a coverage factor of 3 σ and averaging 10,000 points.

AI Absolute Accuracy Example

For example, on the 10 V range, the absolute accuracy at full scale is as follows:

- GainError: 48 ppm + 13 ppm · 1 + 1 ppm · 10 = 71 ppm
- OffsetError: 13 ppm + 21 ppm · 1 + 60 ppm = 94 ppm
- NoiseUncertainty: $\frac{315\,\mu\text{V} \quad 3}{\sqrt{10,000}}$ = 9.4 µV
- AbsoluteAccuracy: 10 V · (GainError) + 10 V · (OffsetError) + NoiseUncertainty = 1,660 µV

Analog Triggers

Number of triggers	1
Source	AI <0..15>, APFI 0
Functions	Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Convert Clock, Sample Clock Timebase

Source level

AI <0..15>	±Full scale
APFI 0	±10 V

Resolution	16 bits
Modes	Analog edge triggering, analog edge triggering with hysteresis, and analog window triggering

Bandwidth (-3 dB)

AI <0..15>	3.4 MHz
APFI 0	3.9 MHz

Accuracy	±1% of range

APFI 0 characteristics

Input impedance	10 kΩ
Coupling	DC

Protection, power on	±30 V
Protection, power off	±15 V

Analog Output

Number of channels	2
DAC resolution	16 bits
DNL	±1 LSB
Monotonicty	16 bit guaranteed
Maximum update rate (simultaneous)	
1 channel	2.86 MS/s
2 channels	2.00 MS/s
Timing accuracy	50 ppm of sample rate
Timing resolution	10 ns
Output range	±10 V, ±5 V, ±external reference on APFI 0
Output coupling	DC
Output impedance	0.2 Ω
Output current drive	±5 mA

Overdrive protection	±25 V
Overdrive current	26 mA
Power-on state	±5 mV

Power-on/off glitch

PCIe/PXIe	1.5 V peak for 200 ms
USB	1.5 V for 1.2 s, typical behavior[1]

Output FIFO size	8,191 samples shared among channels used

Data transfers

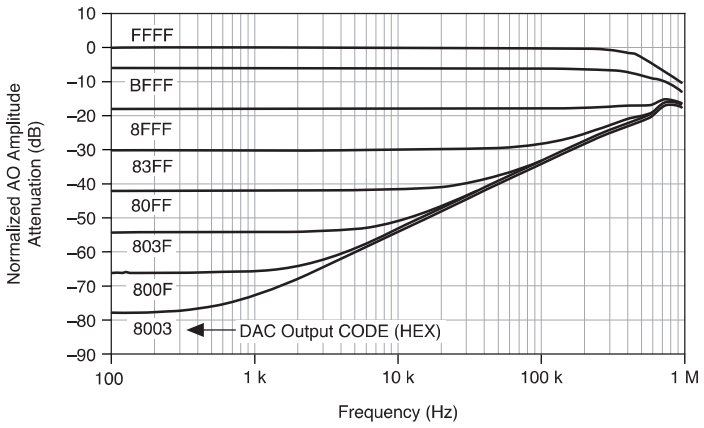
PCIe/PXIe	DMA (scatter-gather), programmed I/O
USB	USB Signal Stream, programmed I/O

AO waveform modes	Non-periodic waveform, periodic waveform regeneration mode from onboard FIFO, periodic waveform regeneration from host buffer including dynamic update
Settling time, full-scale step 15 ppm (1 LSB)	2 µs
Slew rate	20 V/µs
Glitch energy at midscale transition, ±10 V range	10 nV · s

External Reference

APFI 0 characteristics	
Input impedance	10 kΩ
Coupling	DC
Protection, device on	±30 V
Protection, device off	±15 V
Range	±11 V
Slew rate	20 V/µs

Figure 4. AO External Reference Bandwidth



AO Absolute Accuracy (Warranted)

Nominal Range Positive Full Scale (V)	Nominal Range Negative Full Scale (V)	Residual Gain Error (ppm of Reading)	Gain Tempco (ppm/°C)	Reference Tempco (ppm/°C)	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	INL Error (ppm of Range)	Absolute Accuracy at Full Scale (µV)
10	-10	63	17	1	33	2	64	1,890

Nominal Range Positive Full Scale (V)	Nominal Range Negative Full Scale (V)	Residual Gain Error (ppm of Reading)	Gain Tempco (ppm/°C)	Reference Tempco (ppm/°C)	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	INL Error (ppm of Range)	Absolute Accuracy at Full Scale (µV)
5	-5	70	8	1	33	2	64	935

Table 2. AO Absolute Accuracy

> **Note** **Absolute Accuracy at Full Scale** numbers are valid immediately following self calibration and assumes the device is operating within 10 °C of the last external calibration.

> **Note** Accuracies listed are valid for up to two years from the device external calibration.

AO Absolute Accuracy Equation

AbsoluteAccuracy = OutputValue · (GainError) + Range · (OffsetError)

- GainError = ResidualGainError + GainTempco · (TempChangeFromLastInternalCal) + ReferenceTempco · (TempChangeFromLastExternalCal)
- OffsetError = ResidualOffsetError + OffsetTempco · (TempChangeFromLastInternalCal) + INLError

Digital I/O/PFI

Static Characteristics

Number of channels	24 total, 8 (P0.<0..7>), 16 (PFI <0..7>/P1, PFI <8..15>/P2)
Ground reference	D GND
Direction control	Each terminal individually programmable as input or output

Pull-down resistor	50 kΩ typical, 20 kΩ minimum
Input voltage protection	±20 V on up to two pins

> **Caution** Stresses beyond those listed under the **Input voltage protection** specification may cause permanent damage to the device.

Waveform Characteristics (Port 0 Only)

Terminals used	Port 0 (P0.<0..7>)
Port/sample size	Up to 8 bits
Waveform generation (DO) FIFO	2,047 samples
Waveform acquisition (DI) FIFO	255 samples

DI Sample Clock frequency

PCIe/PXIe	0 to 10 MHz, system and bus activity dependent
USB	0 to 1 MHz, system and bus activity dependent

DO Sample Clock frequency

PCIe/PXIe

Regenerate from FIFO	0 to 10 MHz
Streaming from Memory	0 to 10 MHz, system and bus activity dependent

USB

Regenerate from FIFO	0 to 10 MHz

Streaming from memory	0 to 1 MHz, system and bus activity dependent

Data transfers	
PCIe/PXIe	DMA (scatter-gather), programmed I/O
USB	USB Signal Stream, programmed I/O

Digital line filter settings	160 ns, 10.24 µs, 5.12 ms, disable

PFI/Port 1/Port 2 Functionality

Functionality	Static digital input, static digital output, timing input, timing output
Timing output sources	Many AI, AO, counter, DI, DO timing signals
Debounce filter settings	90 ns, 5.12 µs, 2.56 ms, custom interval, disable; programmable high and low transitions; selectable per input

Recommended Operating Conditions

Input high voltage (V_{IH})	
Minimum	2.2 V
Maximum	5.25 V

Input low voltage (V_{IL})	
Minimum	0 V
Maximum	0.8 V

Output high current (I_{OH})	
P0.<0..7>	-24 mA maximum
PFI <0..15>/P1/P2	-16 mA maximum
Output low current (I_{OL})	
P0.<0..7>	24 mA maximum
PFI <0..15>/P1/P2	16 mA maximum

Digital I/O Characteristics

Positive-going threshold (VT+)	2.2 V maximum
Negative-going threshold (VT-)	0.8 V minimum
Delta VT hysteresis (VT+ - VT-)	0.2 V minimum
I_{IL} input low current (V_{IN} = 0 V)	-10 µA maximum
I_{IH} input high current (V_{IN} = 5 V)	250 µA maximum

Figure 5. P0.<0..7>: I_{OH} versus V_{OH}

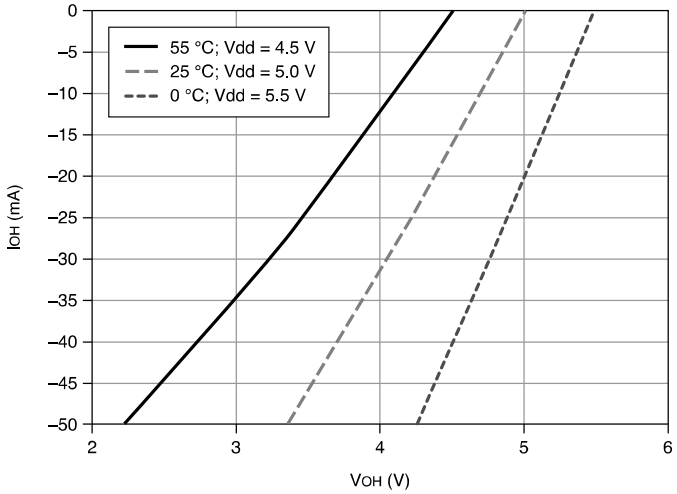


Figure 6. P0.<0..7>: I_{OL} versus V_{OL}

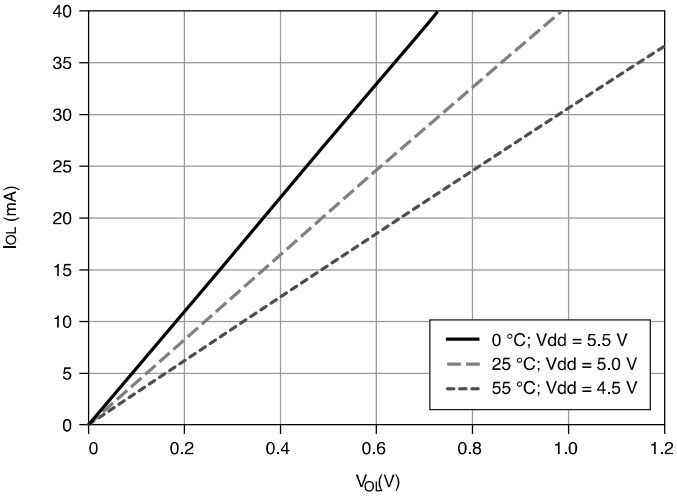


Figure 7. PFI <0..15>/P1/P2: I_{OH} versus V_{OH}

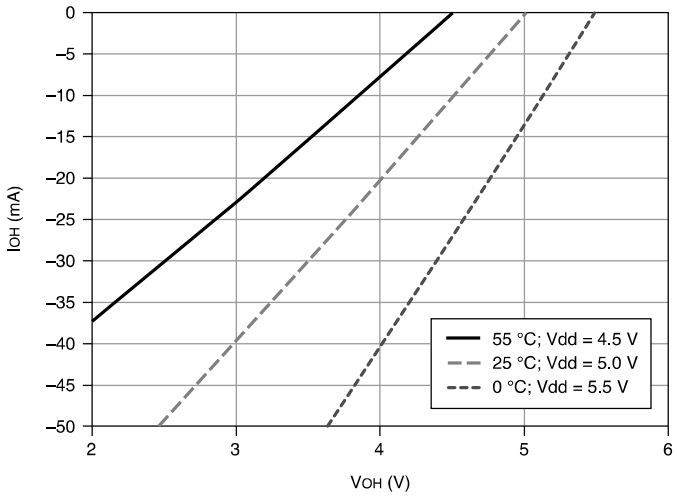
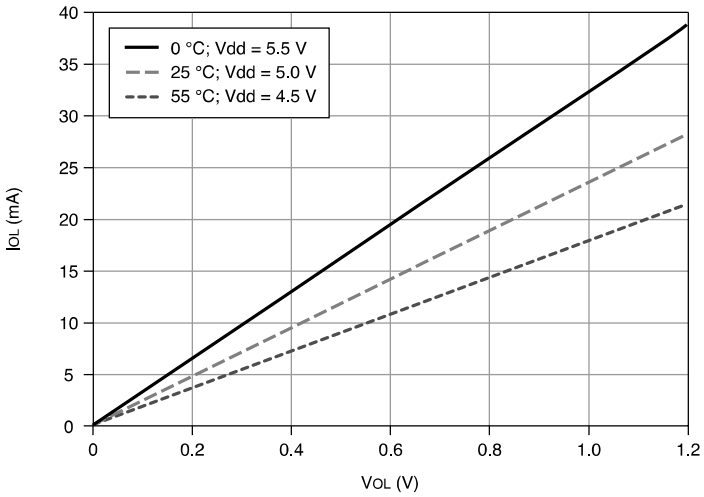


Figure 8. PFI <0..15>/P1/P2: I_{OL} versus V_{OL}



General-Purpose Counters

Number of counter/timers	4
Resolution	32 bits
Counter measurements	Edge counting, pulse, pulse width, semi-period, period, two-edge separation

Position measurements	X1, X2, X4 quadrature encoding with Channel Z reloading; two-pulse encoding
Output applications	Pulse, pulse train with dynamic updates, frequency division, equivalent time sampling
Internal base clocks	100 MHz, 20 MHz, 100 kHz

External base clock frequency

PCIe/USB	0 MHz to 25 MHz
PXIe	0 MHz to 25 MHz; 0 MHz to 100 MHz on PXIe_DSTAR <A,B>

Base clock accuracy	50 ppm
Inputs	Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down, Sample Clock

Routing options for inputs

PCIe	Any PFI, RTSI, analog trigger, many internal signals
PXIe	Any PFI, PXIe_DSTAR<A,B>, PXI_TRIG, PXI_STAR, analog trigger, many internal signals
USB	Any PFI, analog trigger, many internal signals

FIFO	127 samples per counter

Data transfers

PCIe/PXIe	Dedicated scatter-gather DMA controller for each counter/timer, programmed I/O
USB	USB Signal Stream, programmed I/O

Frequency Generator

Number of channels	1
Base clocks	20 MHz, 10 MHz, 100 kHz
Divisors	1 to 16
Base clock accuracy	50 ppm

Phase-Locked Loop (PLL)

Number of PLLs	1

Reference Signal	PCIe Locking Input Frequency (MHz)	PXIe Locking Input Frequency (MHz)	USB Locking Input Frequency (MHz)
PXIe_DSTAR<A,B>	—	10, 20, 100	—
PXI_STAR	—	10, 20	—
PXIe_CLK100	—	100	—
PXI_TRIG <0..7>	—	10, 20	—
RTSI <0..7>	10, 20	—	—
PFI <0..15>	10, 20	10, 20	10

Table 3. Reference Clock Locking Frequencies

Output of PLL	100 MHz Timebase; other signals derived from 100 MHz Timebase including 20 MHz and 100 kHz Timebases

External Digital Triggers

Source

PCIe	Any PFI, RTSI
PXIe	Any PFI, PXIe_DSTAR<A,B>, PXI_TRIG, PXI_STAR
USB	Any PFI

Polarity	Software-selectable for most signals
Analog input function	Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Convert Clock, Sample Clock Timebase
Analog output function	Start Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase
Counter/timer functions	Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down, Sample Clock
Digital waveform generation (DO) function	Start Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase
Digital waveform acquisition (DI) function	Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase

Device-to-Device Trigger Bus

Input Source	
PCIe	RTSI <0..7>[2]
PXIe	PXI_TRIG <0..7>, PXI_STAR, PXIe_DSTAR<A,B>
USB	None

Output destination

PCIe	RTSI <0..7>[2]
PXIe	PXI_TRIG <0..7>, PXIe_DSTARC
USB	None

Output selections	10 MHz Clock; frequency generator output; many internal signals
Debounce filter settings	90 ns, 5.12 µs, 2.56 ms, custom interval, disable; programmable high and low transitions; selectable per input

Bus Interface

PCIe

Form factor	x1 PCI Express, specification v1.1 compliant
Slot compatibility	x1, x4, x8, and x16 PCI Express slots [3]
DMA channels	8, can be used for analog input, analog output, digital input, digital output, counter/timer 0, counter/timer 1, counter/timer 2, counter/timer 3

PXIe

Form factor	x1 PXI Express peripheral module, specification rev 1.0 compliant
Slot compatibility	x1 and x4 PXI Express or PXI Express hybrid slots
DMA channels	8, can be used for analog input, analog output, digital input, digital output, counter/timer 0, counter/timer 1, counter/timer 2, counter/timer 3

All PXIe devices may be installed in PXI Express slots or PXI Express hybrid slots.

USB

USB compatibility	USB 2.0 Hi-Speed or full-speed[4]
USB Signal Stream	8, can be used for analog input, analog output, digital input, digital output, counter/timer 0, counter/timer 1, counter/timer 2, counter/timer 3

Power Requirements

> **Caution** The protection provided by the device can be impaired if the device is used in a manner not described in the **X Series User Manual**.

PCIe

Without disk drive power connector installed

+3.3 V	4.6 W
+12 V	5.4 W

With disk drive power connector installed

+3.3 V	1.6 W
+12 V	5.4 W
+5 V	15 W

PXIe

+3.3 V	1.6 W
+12 V	19.8 W

> **Caution** The USB device must be powered with an NI offered AC adapter or a National Electric Code (NEC) Class 2 DC source that meets the power requirements for the device and has appropriate safety certification marks for country of use.

USB

Power supply requirements	11 to 30 VDC, 30 W, 2 positions 3.5 mm pitch pluggable screw terminal with screw locks similar to Phoenix Contact MC 1,5/2-STF-3,5 BK
Power input mating connector	Phoenix Contact MC 1,5/2-GF-3,5 BK or equivalent

Current Limits

> **Caution** Exceeding the current limits may cause unpredictable device behavior.

PCIe

Without disk drive power connector installed

P0/PFI/P1/P2 and +5 V terminals combined	0.59 A max

With disk drive power connector installed

+5 V terminal (connector 0)	1 A max[5]
+5 V terminal (connector 1)	1 A max[5]
P0/PFI/P1/P2 combined	1 A max

PXIe	
+5 V terminal (connector 0)	1 A max[5]
+5 Vterminal (connector 1)	1 A max[5]
P0/PFI/P1/P2 and +5 V terminals combined	2 A max
USB	
+5 V terminal	1 A max[5]
P0/PFI/P1/P2 and +5 V terminals combined	2 A max

Physical Characteristics

Printed circuit board dimensions	
PCIe	9.9 × 16.8 cm (3.9 × 6.6 in.) (half-length)
PXIe	Standard 3U PXI

Enclosure dimensions (includes connectors)	
USB	
Mass termination	18.5 × 17.3 × 3.6 cm (7.3 × 6.8 × 1.4 in.)
Screw terminal	26.4 × 17.3 × 3.6 cm (10.4 × 6.8 × 1.4 in.)
BNC	20.3 × 18.5 × 6.8 cm (8.0 × 7.3 × 2.7 in.)

Weight

PCIe	161 g (5.6 oz)
PXIe	205 g (7.2 oz)
USB Mass Termination	965 g (2 lb2.1 oz)
USB Screw Terminal	1.413 kg (3 lb1.8 oz)
USB BNC	1.52 kg (3 lb5 oz)

I/O connector

PCIe/PXIe	1 68-pin VHDCI
USB Mass Termination	1 68-pin VHDCI
USB Screw Terminal	64 screw terminals
USB BNC	20 BNCs and 30 screw terminals

Manufacturer, Part Number	Description
MOLEX 71430-0011	68-Pos Right Angle Single Stack PCB-Mount VHDCI (Receptacle)
MOLEX 74337-0016	68-Pos Right Angle Dual Stack PCB-Mount VHDCI (Receptacle)
MOLEX 71425-3001	68-Pos Offset IDC Cable Connector (Plug) (SHC68-*)

Table 4. PCIe/PXIe Mating Connectors

PCIe disk drive power connector	Standard ATX peripheral connector (not serial ATA)
USB screw terminal wiring/BNC screw terminal wiring	16-24 AWG

Calibration

Recommended warm-up time	15 minutes
Calibration interval	2 years

Maximum Working Voltage

Maximum working voltage refers to the signal voltage plus the common-mode voltage.

Channel to earth	11 V, Measurement Category I

> **Caution** Do not use for measurements within Categories II, III, or IV.

Shock and Vibration

Operational shock	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)

Random vibration

Operating	5 to 500 Hz, 0.3 g_{rms}
Nonoperating	5 to 500 Hz, 2.4 g_{rms}
	(Tested in accordance with IEC 60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Environmental

Operating temperature	
PCIe	0 to 50 °C
PXIe	0 to 55 °C
USB	0 to 45 °C
Storage temperature	-40 to 70 °C
Operating humidity	10 to 90% RH, noncondensing
Storage humidity	5 to 95% RH, noncondensing
Pollution Degree	2
Maximum altitude	2,000 m

Indoor use only.

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

> **Note** For safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility

CE Compliance CE

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)
- 2011/65/EU; Restriction of Hazardous Substances (RoHS)
- 2014/53/EU; Radio Equipment Directive (RED)
- 2014/34/EU; Potentially Explosive Atmospheres (ATEX)

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the **Engineering a Healthy Planet** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

- **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国 RoHS）

- **中国 RoHS**— NI 符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于 NI 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

Device Pinouts

Figure 9. NI PCIe/PXIe-6361 Pinout

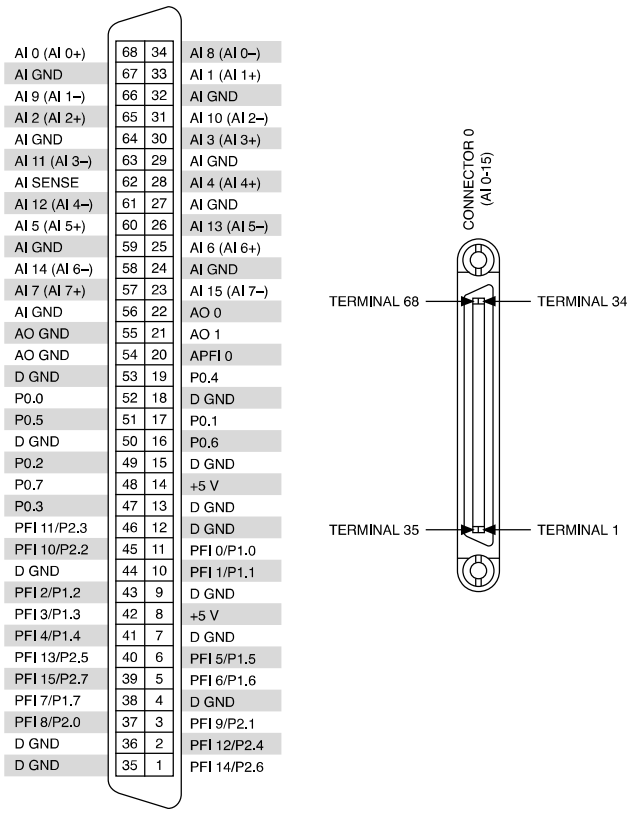


Figure 10. NI USB-6361 Mass Termination Pinout

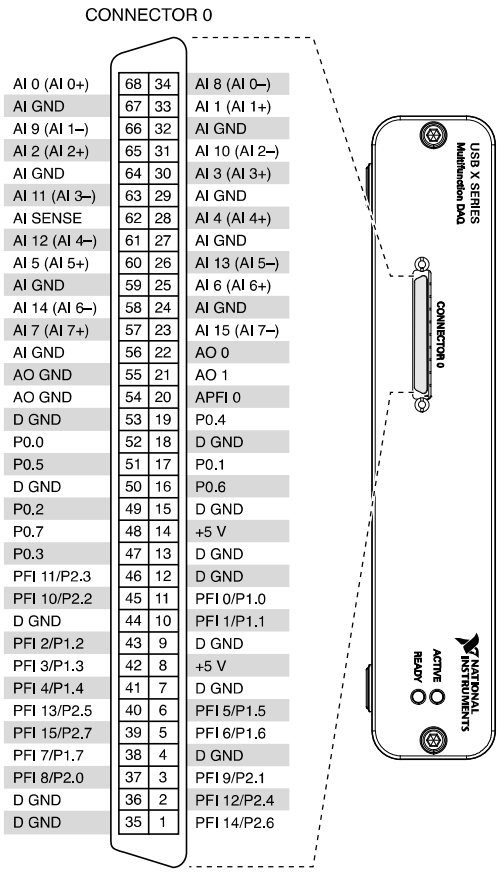


Figure 11. NI USB-6361 Screw Terminal Pinout

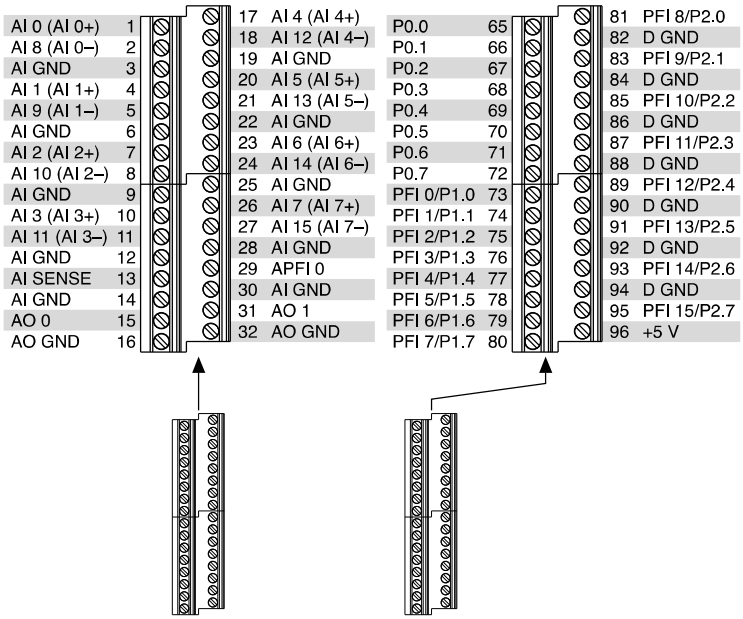
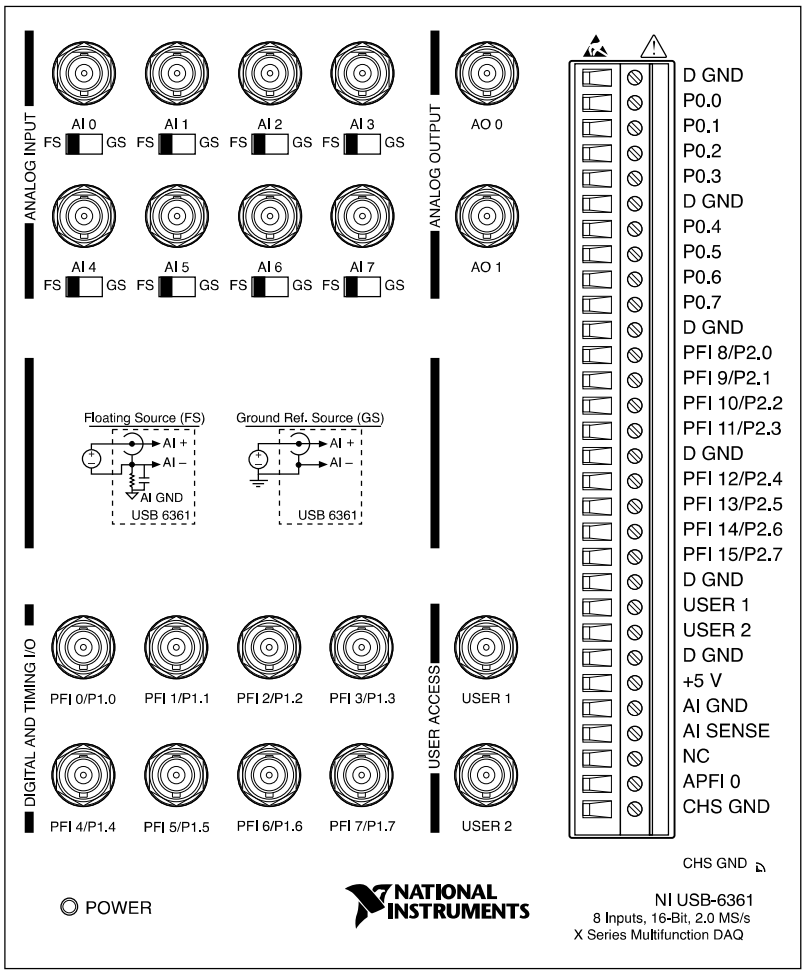


Figure 12. NI USB-6361 BNC Front Panel and Pinout



[1] Time period may be longer due to host system USB performance. Time period is longer during firmware updates.

[2] In other sections of this document, RTSI refers to RTSI <0..7> for NI PCIe-6361 or PXI_TRIG <0..7> for NI PXIe-6361.

[3] Some motherboards reserve the x16 slot for graphics use. For PCI Express guidelines, refer to ni.com/pciexpress.

[4] Operating on a full-speed bus results in lower performance, and you might not be able to achieve maximum sampling/update rates.

[5] Has self-resetting fuse that opens when current exceeds this specification.

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