

SLG59M1446V

Ultra-small Dual 40 mΩ, 1.0 A Load Switch with Discharge

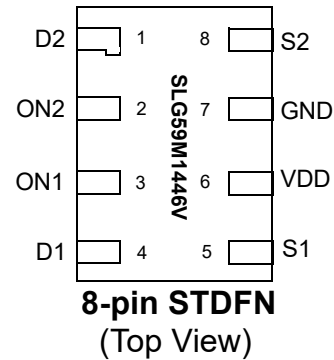
General Description

The SLG59M1446V is designed for load switching applications. The part comes with two 40 mΩ 1.0 A rated MOSFETs, each controlled by an ON control pin. Each MOSFET's ramp rate is adjustable depending on the input current level of the ON pin. The product is packaged in an ultra-small 1.6 x 1.0 mm package.

Features

- Two 40 mΩ 1.0 A MOSFETs
- Two integrated VGS Charge Pumps
- User selectable ramp rate with external resistor
- Protected by thermal shutdown
- Integrated Discharge Resistor
- Pb-Free / Halogen-Free / RoHS compliant
- STDFN 8L, 1.0 x 1.6 mm

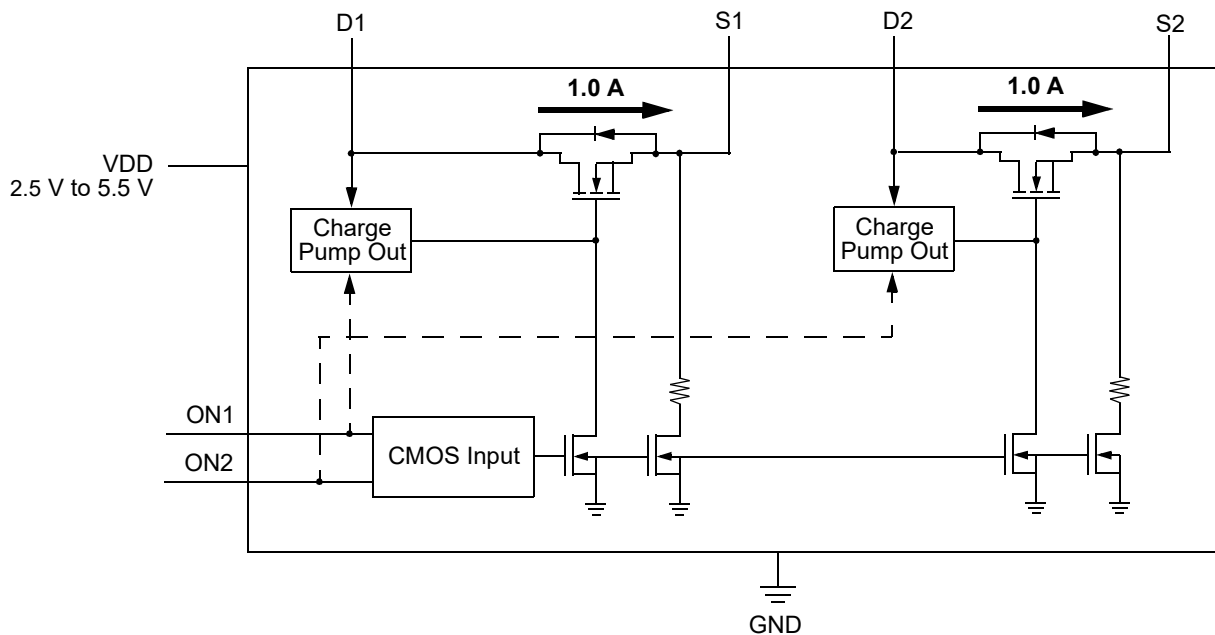
Pin Configuration



Applications

- Power-Rail Switching:
 - Notebook/Laptop/Tablet PCs
 - Smartphones/Wireless Handsets
 - High-definition Digital Cameras
 - Set-top Boxes
- Point of Sales Pins
- GPS Navigation Devices

Block Diagram



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Pin Description

| Pin # | Pin Name | Type | Pin Description |
|-------|----------|--------|--|
| 1 | D2 | MOSFET | Drain/Input terminal of Power MOSFET Channel 2. Connect a 10 μF (or larger) low ESR capacitor from this pin to GND. Capacitors used at D2 should be rated at 10 V or higher. |
| 2 | ON2 | Input | A low-to-high transition on this pin closes the Channel 2 of load switch. ON is an asserted-HIGH, level-sensitive CMOS input with $ON_V_{IL} < 0.3\text{ V}$ and $ON_V_{IH_INI} > 1.2\text{ V}$. Connect this pin to the output of a general-purpose output (GPO) from a microcontroller or other application processor. A resistor connected in series to ON2 signal sets the V_{S2} Slew Rate. Please read more information on Adjustable Slew Rate description. |
| 3 | ON1 | Input | A low-to-high transition on this pin closes the Channel 1 of load switch. ON is an asserted-HIGH, level-sensitive CMOS input with $ON_V_{IL} < 0.3\text{ V}$ and $ON_V_{IH_INI} > 1.2\text{ V}$. Connect this pin to the output of a general-purpose output (GPO) from a microcontroller or other application processor. A resistor connected in series to ON1 signal sets the V_{S1} Slew Rate. Please read more information on Adjustable Slew Rate description. |
| 4 | D1 | MOSFET | Drain/Input terminal of Power MOSFET Channel 1. Connect a 10 μF (or larger) low ESR capacitor from this pin to GND. Capacitors used at D1 should be rated at 10 V or higher. |
| 5 | S1 | MOSFET | Source/Output terminal of Power MOSFET Channel1. Connect a 10 μF (or larger) low ESR capacitor from this pin to GND. Capacitors used at S1 should be rated at 10 V or higher. |
| 6 | VDD | PWR | VDD supplies the power for the operation of the load switch and internal control circuitry where its range is $2.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$. Bypass the VDD pin to GND with a 0.1 μF (or larger) capacitor. |
| 7 | GND | GND | Ground connection. Connect this pin to system analog or power ground plane. |
| 8 | S2 | MOSFET | Source/Output terminal of Power MOSFET Channel2. Connect a 10 μF (or larger) low ESR capacitor from this pin to GND. Capacitors used at S2 should be rated at 10 V or higher. |

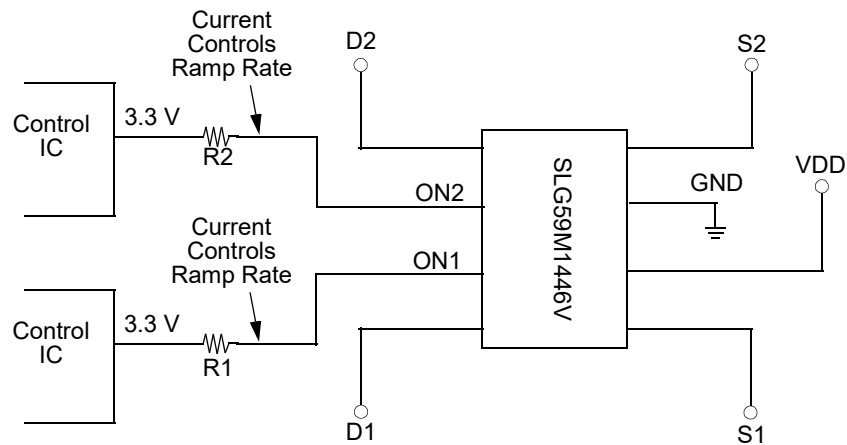
Ordering Information

| Part Number | Type | Production Flow |
|---------------|--------------------------|-----------------------------|
| SLG59M1446V | STDFN 8L | Industrial, -40 °C to 85 °C |
| SLG59M1446VTR | STDFN 8L (Tape and Reel) | Industrial, -40 °C to 85 °C |

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Application Diagram



Adjustable Ramp Rate vs. ON Pin Current (5.5 V, 25 °C)

| ON Pin Current | $V_{S(SR)}$ (typ) |
|----------------|-------------------|
| 20 μ A | 0.56 V/ms |
| 50 μ A | 1.34 V/ms |
| 100 μ A | 2.53 V/ms |
| 150 μ A | 3.71 V/ms |
| 200 μ A | 4.68 V/ms |
| 250 μ A | 5.63 V/ms |
| 400 μ A | 8.4 V/ms |

Adjustable Slew Rate (ON2 Pin 2 and ON1 Pin3)

SLG59M1446V has a built in configurable slew control feature. The configurable slew control uses current detection method on ON1/ON2. When ON voltage rises above $ON_V_{IH_INI}$ (1.2 V typical), the slew control circuit will measure the current flowing into ON1/ON2. Based on the current flowing into ON1/ON2, different slew rates will be selected by the internal control circuit. See ON Pin Current vs. $V_{S(SR)}$ table. The slew rate is configurable by selecting a different R1/R2 resistor value as shown on application diagram. Calculating the R1/R2 value depends on both the desired slew rate, and the V_{OH} level of the device driving the ON1/ON2 pin.

$$ON \text{ Pin Current} = (GPIO_V_{OH} - ON_V_{REF} (1.05 \text{ V typical})) / R$$

By driving the ON pin without any series resistor, the Slew Rate will be around 8.4 V/ms and max ON pin Current will be approximately 400 μ A.

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Absolute Maximum Ratings

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|--------------------------------------|-----------------------------------|--|------|------|------|------|
| V _{DD} | Power Supply Voltage | | -- | -- | 6 | V |
| T _S | Storage Temperature | | -65 | -- | 150 | °C |
| ESD _{HBM} | ESD Protection | Human Body Model | 2000 | -- | -- | V |
| ESD _{CDM} | ESD Protection | Charged Device Model | 1000 | -- | -- | V |
| MSL | Moisture Sensitivity Level | | 1 | | | |
| θ _{JA} | Thermal Resistance, | 1 x 1.6mm STDFN; Determined using 1 in ² , 1 oz. copper pads under each Dx and Sx terminal and FR4 pcb material | -- | 72 | -- | °C/W |
| W _{DIS} | Package Power Dissipation | | -- | -- | 0.4 | W |
| MOSFET I _{DS} _{PK} | Peak Current from Drain to Source | For no more than 1 ms with 1% duty cycle | -- | -- | 1.5 | A |

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -40 °C to 85 °C (unless otherwise stated)

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|-------------------------|--|--|---------------------------|------|-----------------|------|
| V _{DD} | Power Supply Voltage | Pin 6 | 2.5 | -- | 5.5 | V |
| V _{D1} | Load Switch Input Voltage of Channel 1 | Pin 4 | 0.85 | -- | V _{DD} | V |
| V _{D2} | Load Switch Input Voltage of Channel 2 | Pin 1 | 0.85 | -- | V _{DD} | V |
| I _{DD} | Power Supply Current (PIN 6) | when OFF | -- | 0.1 | 1 | μA |
| | | when ON, No load | -- | 35 | 50 | μA |
| RDS _{ON} [1,2] | ON Resistance | T _A = 25 °C, I _{DS} = 100 mA | -- | 40 | 50 | mΩ |
| | | T _A = 70 °C, I _{DS} = 100 mA | -- | 50 | 55 | mΩ |
| | | T _A = 85 °C, I _{DS} = 100 mA | -- | 55 | 65 | mΩ |
| MOSFET I _{DS} | Current from D[1,2] to S[1,2] | Continuous | -- | -- | 1.0 | A |
| T _{ON_Delay} | ON Delay Time | 50% ON to V _S [1,2] Ramp Start; ON Pin Current (PIN2, PIN3) = 20 μA; V _{DD} = V _D [1,2] = 5 V; C _{LOAD} = 10 μF; R _{LOAD} = 20 Ω | -- | 2.4 | 4.0 | ms |
| T _{Total_ON} | Total Turn On Time | 50% ON to 90% V _S [1,2] | Configurable ¹ | | | ms |
| | | Example: ON Pin Current (PIN2, PIN3) = 20 μA; V _{DD} = V _D [1,2] = 5 V; C _{LOAD} = 10 μF; R _{LOAD} = 20 Ω | -- | 11.7 | -- | ms |
| V _{S(SR)} | V _S [1,2] Slew Rate | 10% V _S [1,2] to 90% V _S [1,2] | Configurable ¹ | | | V/ms |
| | | Example: ON Pin Current (PIN2, PIN3) = 20 μA; V _{DD} = V _D [1,2] = 5 V; C _{LOAD} = 10 μF; R _{LOAD} = 20 Ω | -- | 0.56 | -- | V/ms |
| R _{DISCHRG} | Discharge Resistance | V _{DD} = 2.5 V to 5.5 V; V _S [1,2] = 0.4 V Input bias | 100 | 150 | 300 | Ω |

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Electrical Characteristics (continued)

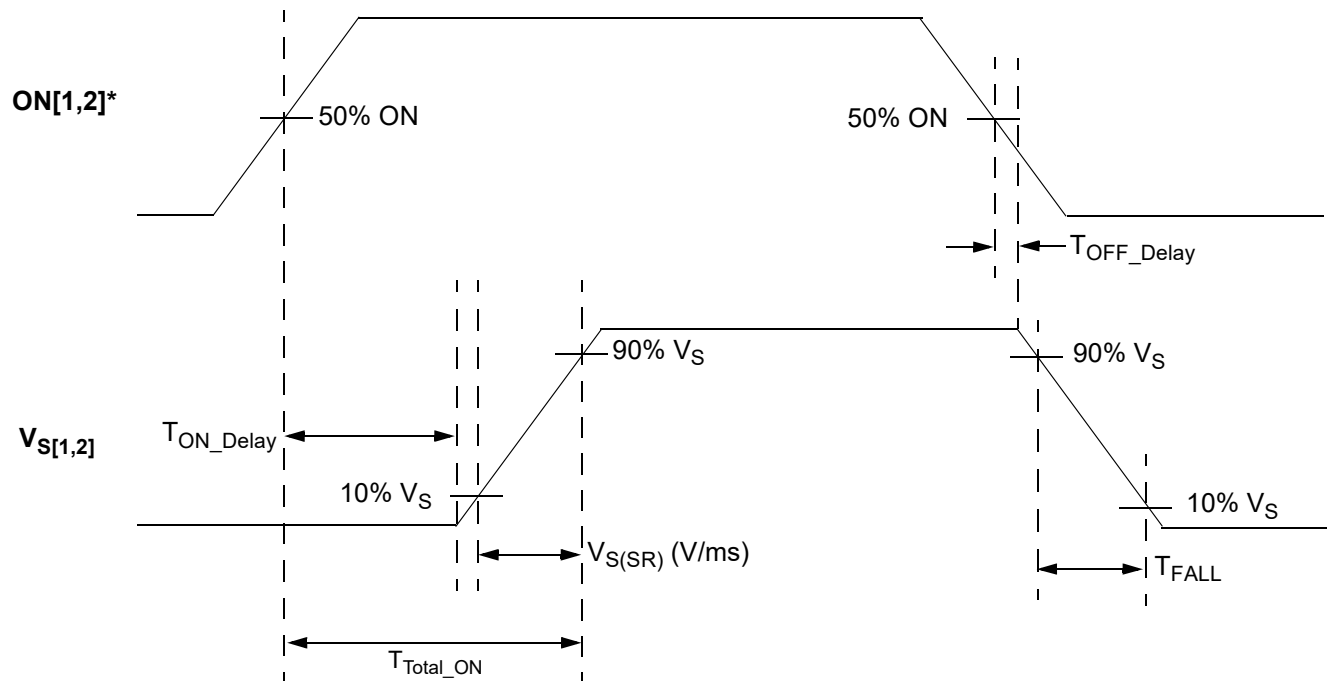
T_A = -40 °C to 85 °C (unless otherwise stated)

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|------------------------|---------------------------------------|---|------|------|-----------------|------|
| C _{LOAD} | Output Load Capacitance | C _{LOAD} connected from S[1,2] to GND | -- | -- | 100 | μF |
| ON_V _{REF} | ON Pin Reference Voltage ² | | 0.99 | 1.05 | 1.10 | V |
| ON_V _{IH_INI} | Initial Turn On Voltage | Internal Charge Pump ON | 1.2 | -- | V _{DD} | V |
| ON_V _{IL} | Low Input Voltage on ON pin | Internal Charge Pump OFF | -0.3 | 0 | 0.3 | V |
| ON_R | Input Impedance on ON pin | | 100 | -- | -- | MΩ |
| THERM _{ON} | Thermal shutoff turn-on temperature | | -- | 125 | -- | °C |
| THERM _{OFF} | Thermal shutoff turn-off temperature | | -- | 100 | -- | °C |
| THERM _{TIME} | Thermal shutoff time | | -- | -- | 1 | ms |
| T _{OFF_Delay} | OFF Delay Time | 50% ON to V _{S[1,2]} Fall Start; V _{D[1,2]} = 5 V; R _{LOAD} = 20 Ω; no C _{LOAD} | -- | 55 | 70 | μs |
| T _{FALL} | V _{S[1,2]} Fall Time | 90% V _{S[1,2]} to 10% V _{S[1,2]} ; V _{D[1,2]} = 5 V; R _{LOAD} = 20 Ω; no C _{LOAD} | -- | 32 | -- | μs |

Notes:

1. Refer to table for configuration details.
2. Voltage before ON pin resistor needs to be higher than 1.2 V to generate required I_{ON}

T_{ON_Delay}, V_{S(SR)}, and T_{Total_ON} Timing Details



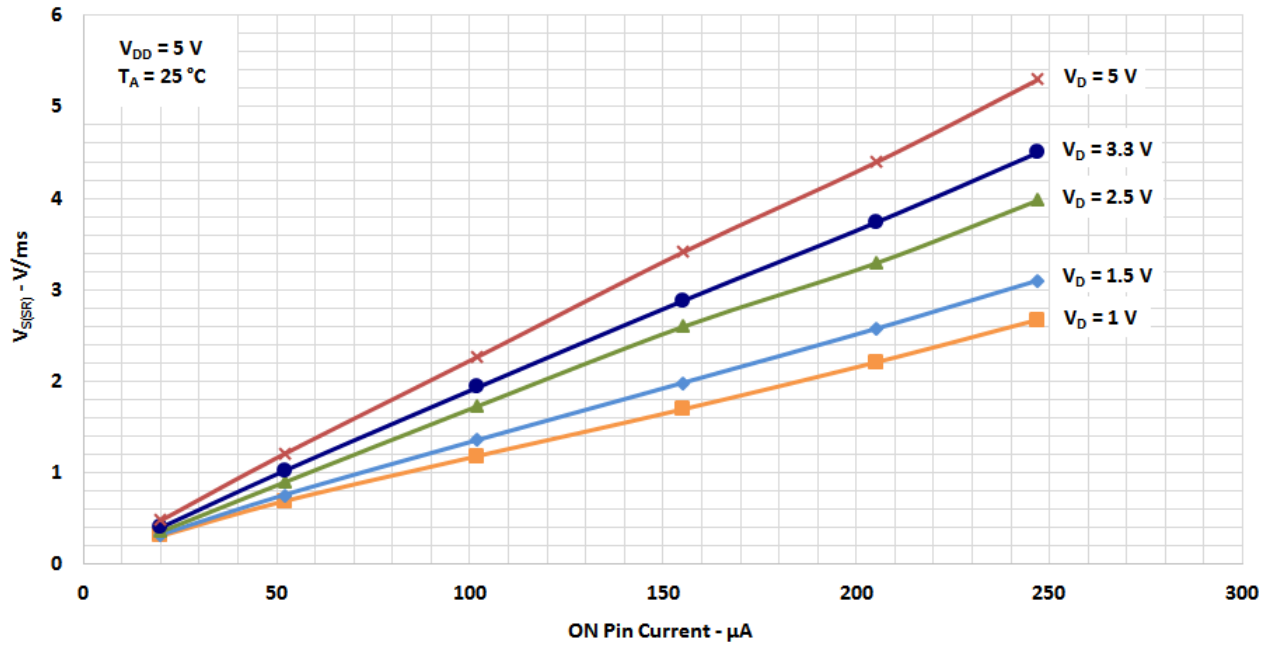
*Rise and Fall Times of the ON Signal are 100 ns

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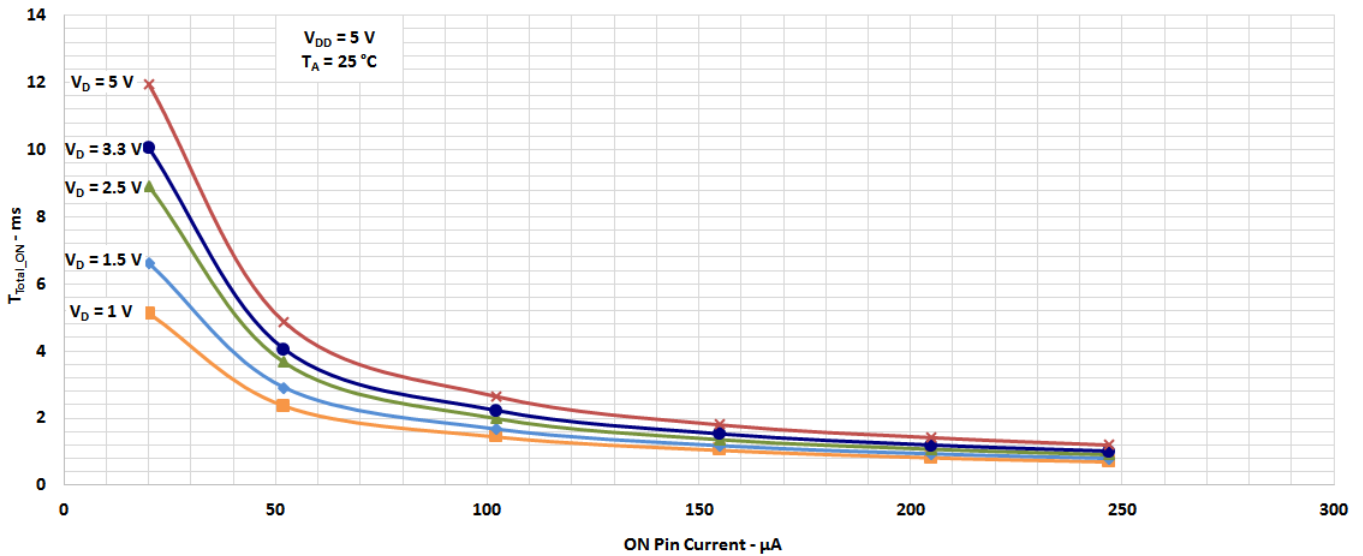
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Typical Performance Characteristics

Slew Rate vs. ON Current



T_{Total_ON} vs. ON Current



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Power Dissipation

The junction temperature of the SLG59M1446V depends on factors such as board layout, ambient temperature, external air flow over the package, load current, and the $R_{DS\text{ON}}$ -generated voltage drop across each power MOSFET. While the primary contributor to the increase in the junction temperature of the SLG59M1446V is the power dissipation of its power MOSFETs, its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD_{\text{TOTAL}} = (R_{DS\text{ON}1} \times I_{\text{DS}1}^2) + (R_{DS\text{ON}2} \times I_{\text{DS}2}^2)$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

$R_{DS\text{ON}[1,2]}$ = Channel 1 and Channel 2 Power MOSFET ON resistance, in Ohms (Ω), respectively

$I_{\text{DS}[1,2]}$ = Channel 1 and Channel 2 Output current, in Amps (A), respectively

and

$$T_J = PD_{\text{TOTAL}} \times \theta_{\text{JA}} + T_A$$

where:

T_J = Die junction temperature, in Celsius degrees ($^{\circ}\text{C}$)

θ_{JA} = Package thermal resistance, in Celsius degrees per Watt ($^{\circ}\text{C}/\text{W}$) – highly dependent on pcb layout

T_A = Ambient temperature, in Celsius degrees ($^{\circ}\text{C}$)

In nominal operating mode, the SLG59M1446V's power dissipation can also be calculated by taking into account the voltage drop across each switch ($V_{\text{D}x} - V_{\text{S}x}$) and the magnitude of that channel's output current ($I_{\text{D}Sx}$):

$$PD_{\text{TOTAL}} = [(V_{\text{D}1} - V_{\text{S}1}) \times I_{\text{D}S1}] + [(V_{\text{D}2} - V_{\text{S}2}) \times I_{\text{D}S2}] \text{ or}$$

$$PD_{\text{TOTAL}} = [(V_{\text{D}1} - (R_{\text{LOAD}1} \times I_{\text{D}S1})) \times I_{\text{D}S1}] + [(V_{\text{D}2} - (R_{\text{LOAD}2} \times I_{\text{D}S2})) \times I_{\text{D}S2}]$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

$V_{\text{D}[1,2]}$ = Channel 1 and Channel 2 Input Voltage, in Volts (V), respectively

$R_{\text{LOAD}[1,2]}$ = Channel 1 and Channel 2 Output Load Resistance, in Ohms (Ω), respectively

$I_{\text{D}S[1,2]}$ = Channel 1 and Channel 2 output current, in Amps (A), respectively

$V_{\text{S}[1,2]}$ = Channel 1 and Channel 2 output voltage, or $R_{\text{LOAD}[1,2]} \times I_{\text{D}S[1,2]}$, respectively

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Layout Guidelines:

1. The VDD pin needs a 0.1 μF external capacitor to smooth pulses from the power supply. Locate this capacitor as close as possible to the SLG59M1446V's PIN6.
2. Since the D1, D2, S1 and S2 pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in [Figure 1](#), illustrates proper techniques for heat to transfer as efficiently as possible out of the device;
3. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C_{IN} and output C_{LOAD} low-ESR capacitors as close as possible to the SLG59M1446V's D1, D2, S1 and S2 pins;
4. The GND pin should be connected to system analog or power ground plane.
5. 2 oz. copper is recommended for high current operation.

SLG59M1446V Evaluation Board:

A GreenFET Evaluation Board for SLG59M1446V is designed according to the statements above and is illustrated on [Figure 1](#). Please note that evaluation board has D_Sense and S_Sense pads. They cannot carry high currents and dedicated only for RDS_{ON} evaluation.

Please solder your SLG59M1446V here

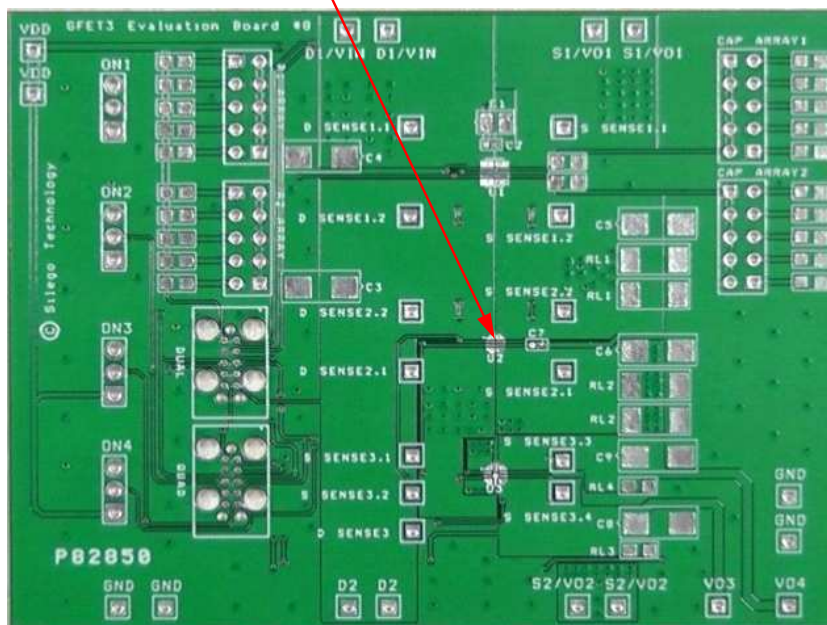


Figure 1. SLG59M1446V Evaluation Board.

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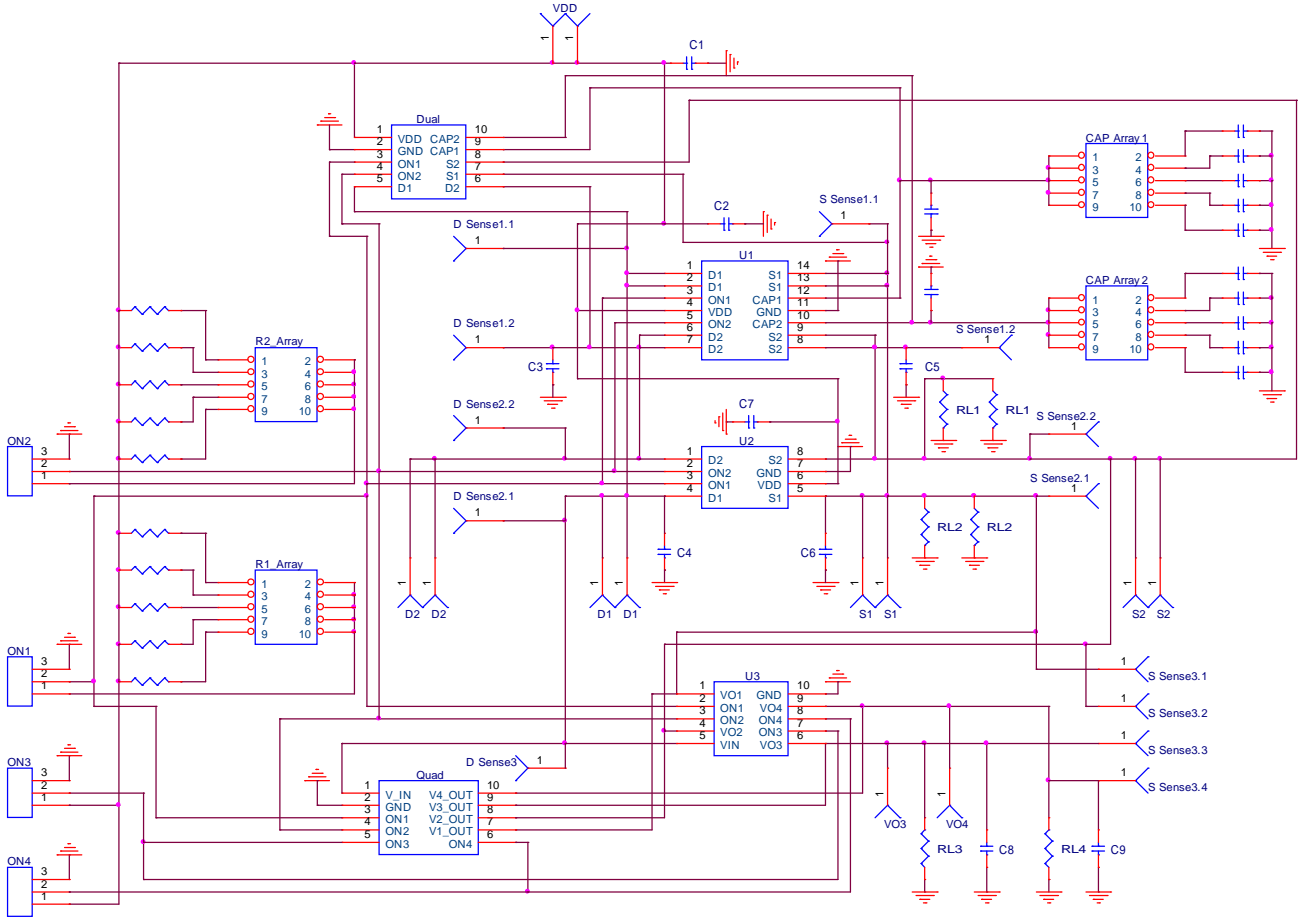


Figure 2. SLG59M1446V Evaluation Board Connection Circuit.

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Basic Test Setup and Connections

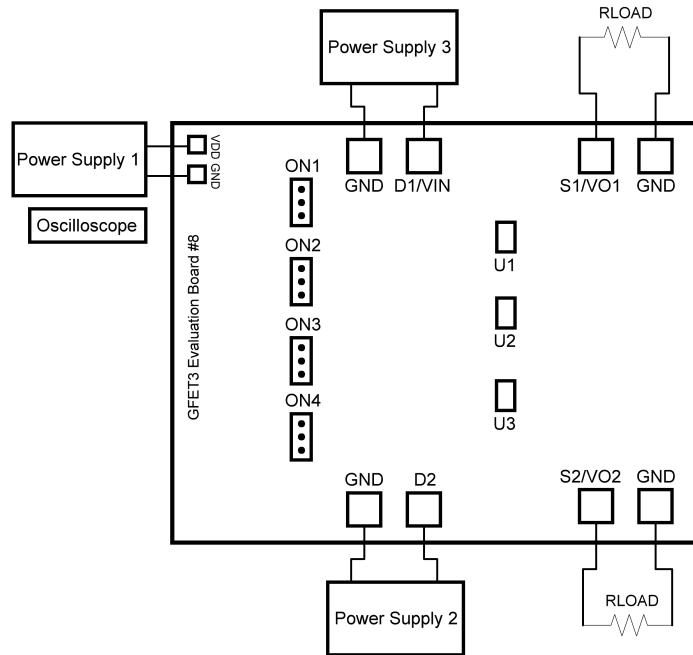


Figure 3. Typical connections for GreenFET Evaluation.

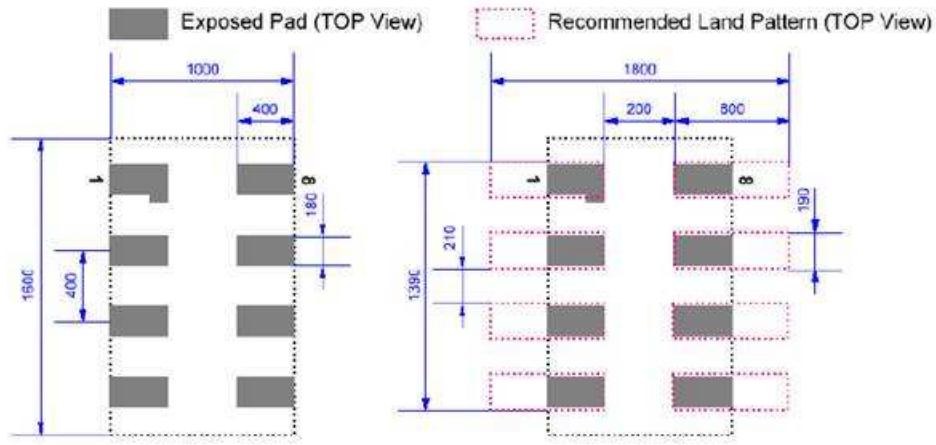
EVB Configuration

1. Connect oscilloscope probes to D1/VIN, D2, S1/VO1, S2/VO2, ON1, ON2 etc.;
2. Turn on Power Supply 1 and set desired V_{DD} from 2.5 V...5.5 V range;
3. Turn on Power Supply 2, 3 and set desired $V_{D[1,2]}$ from 0.85 V... V_{DD} range;
4. Toggle the ON[1,2] signal High or Low to observe SLG59M1446V operation.

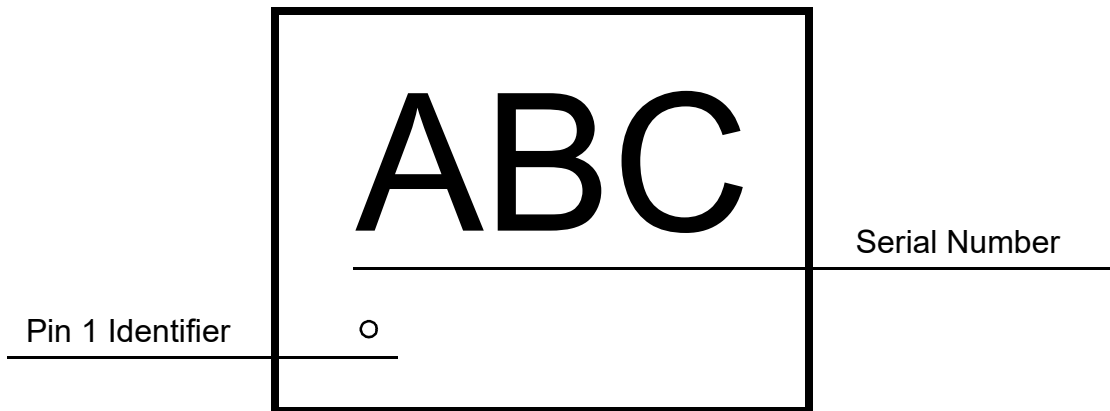
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SLG59M1446V Layout Suggestion



Package Top Marking System Definition



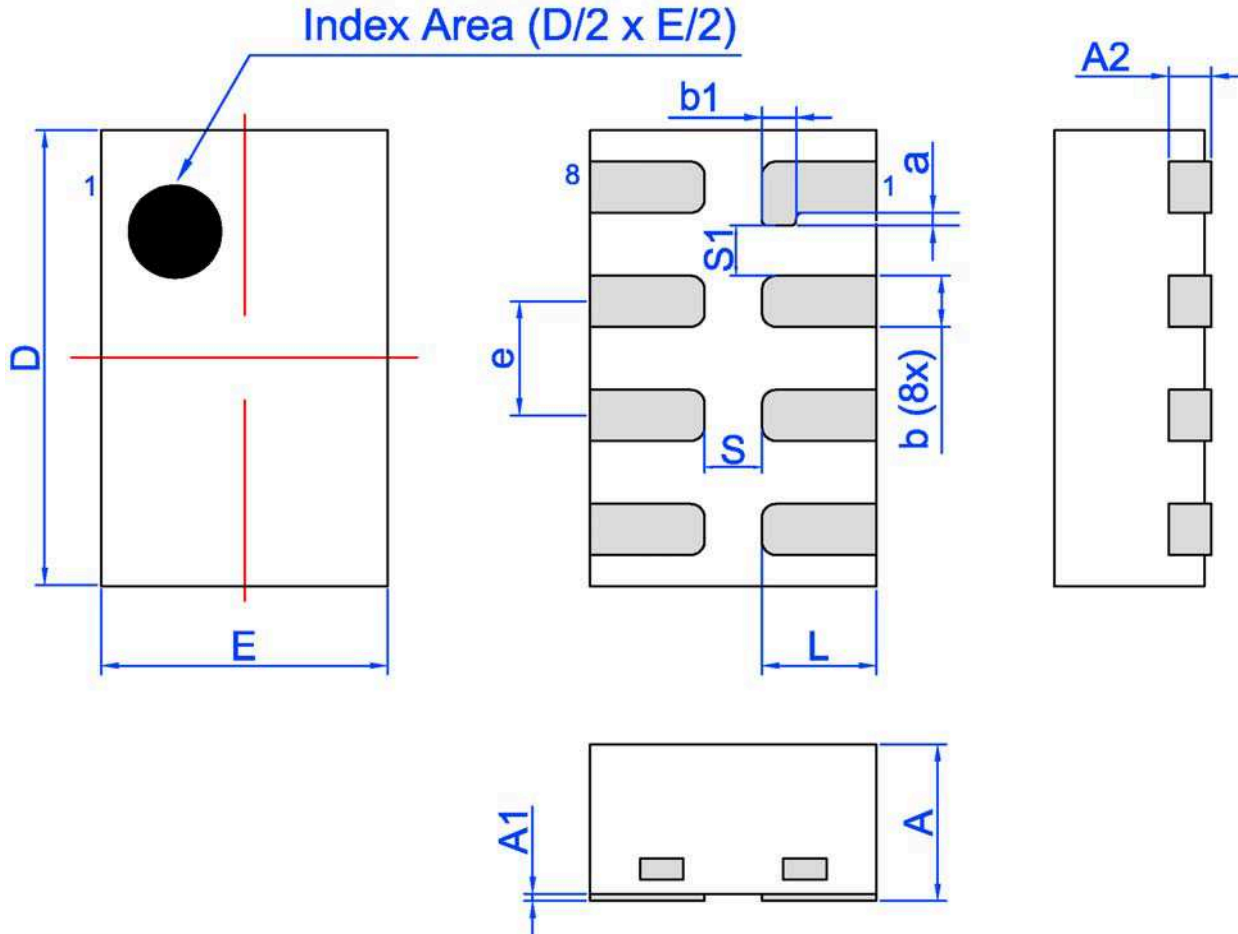
ABC - 3 alphanumeric Part Serial Number
where A, B, or C can be A-Z and 0-9

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Package Drawing and Dimensions

8 Lead STDFN Package 1.0 x 1.6 mm



Unit: mm

| Symbol | Min | Nom. | Max | Symbol | Min | Nom. | Max |
|--------|----------|------|-------|--------|-----------|------|------|
| A | 0.50 | 0.55 | 0.60 | D | 1.55 | 1.60 | 1.65 |
| A1 | 0.005 | - | 0.060 | E | 0.95 | 1.00 | 1.05 |
| A2 | 0.10 | 0.15 | 0.20 | L | 0.35 | 0.40 | 0.45 |
| b | 0.13 | 0.18 | 0.23 | S | 0.2 REF | | |
| b1 | 0.17 | 0.19 | 0.20 | a | 0.04 | 0.05 | 0.06 |
| e | 0.40 BSC | | | S1 | 0.175 REF | | |

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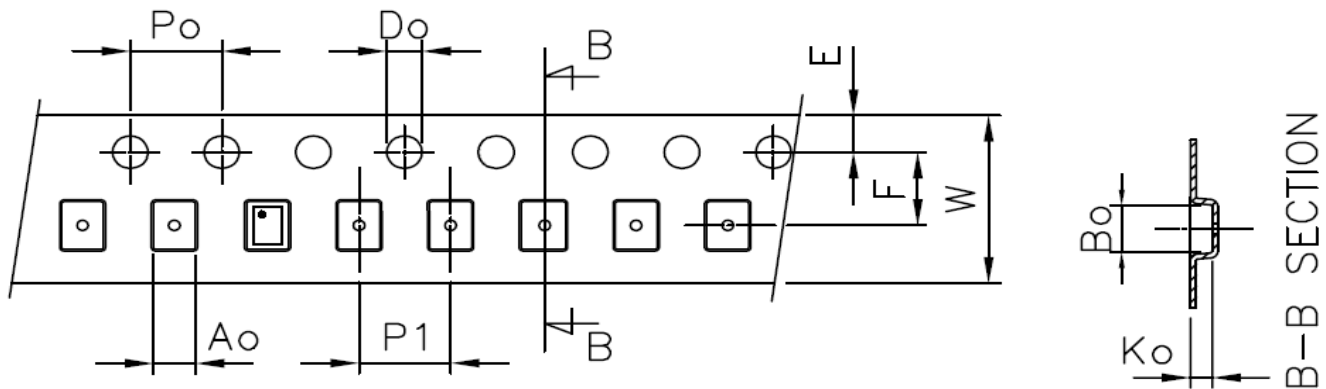
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Tape and Reel Specifications

| Package Type | # of Pins | Nominal Package Size [mm] | Max Units | | Reel & Hub Size [mm] | Leader (min) | | Trailer (min) | | Tape Width [mm] | Part Pitch [mm] |
|--------------------------------------|-----------|---------------------------|-----------|---------|----------------------|--------------|-------------|---------------|-------------|-----------------|-----------------|
| | | | per Reel | per Box | | Pockets | Length [mm] | Pockets | Length [mm] | | |
| STDFN 8L 1x1.6mm 0.4P Green | 8 | 1.0 x 1.6 x 0.55 | 3,000 | 3,000 | 178 / 60 | 100 | 400 | 100 | 400 | 8 | 4 |

Carrier Tape Drawing and Dimensions

| Package Type | Pocket BTM Length | Pocket BTM Width | Pocket Depth | Index Hole Pitch | Pocket Pitch | Index Hole Diameter | Index Hole to Tape Edge | Index Hole to Pocket Center | Tape Width |
|-----------------------------------|-------------------|------------------|--------------|------------------|--------------|---------------------|-------------------------|-----------------------------|------------|
| | A0 | B0 | K0 | P0 | P1 | D0 | E | F | W |
| STDFN 8L 1x1.6mm 0.4P Green | 1.12 | 1.72 | 0.7 | 4 | 4 | 1.55 | 1.75 | 3.5 | 8 |



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.88 mm³ (nominal). More information can be found at www.jedec.org.

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Revision History

| Date | Version | Change |
|------------|---------|---|
| 2/2/2022 | 1.07 | Updated Company name and logo Fixed typos |
| 3/10/2021 | 1.06 | Updated Slew Rate vs. ON Pin Current table |
| 9/13/2019 | 1.05 | Updated Pin Descriptions Updated style and formatting Updated Charts Added Power Dissipation Updated POD Fixed typos |
| 12/4/2015 | 1.04 | Updated Block Diagram |
| 11/20/2015 | 1.03 | Added ESD _{CDM} , MSL, and θ_{JA} specs |

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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