User's Manual

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RZ/T2M Group

Renesas Starter Kit+ for RZ/T2M

User's Manual

RZ/T Series for Real-Time Control
RZ Family
64-Bit & 32-Bit Arm®-Based High-End MPUs

Renesas Electronics
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Disclaimer

By using this Renesas Starter Kit (RSK+), the user accepts the following terms:

The RSK+ is not guaranteed to be error free, and the entire risk as to the results and performance of the RSK+ is assumed by the User. The RSK+ is provided by Renesas on an “as is” basis without warranty of any kind whether express or implied, including but not limited to the implied warranties of satisfactory quality, fitness for a particular purpose, title and non-infringement of intellectual property rights with regard to the RSK+. Renesas expressly disclaims all such warranties. Renesas or its affiliates shall in no event be liable for any loss of profit, loss of data, loss of contract, loss of business, damage to reputation or goodwill, any economic loss, any reprogramming or recall costs (whether the foregoing losses are direct or indirect) nor shall Renesas or its affiliates be liable for any other direct or indirect special, incidental or consequential damages arising out of or in relation to the use of this RSK+, even if Renesas or its affiliates have been advised of the possibility of such damages.

Precautions

The following precautions should be observed when operating any RSK+ product:

This Renesas Starter Kit is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures;

- ensure attached cables do not lie across the equipment
- reorient the receiving antenna
- increase the distance between the equipment and the receiver
- connect the equipment into an outlet on a circuit different from that which the receiver is connected
- power down the equipment when not in use
- consult the dealer or an experienced radio/TV technician for help NOTE: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken;

- The user is advised that mobile phones should not be used within 10m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Renesas Starter Kit does not represent an ideal reference design for an end product and does not fulfil the regulatory standards for an end product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the CPU Board hardware functionality, and electrical characteristics. It is intended for users designing sample code on the CPU Board platform, using the many different incorporated peripheral devices.

The manual comprises of an overview of the capabilities of the RSK+ product but does not intend to be a guide to embedded programming or hardware design.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RSK+RZT2M. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's Manual	Describes the technical details of the RSK+ hardware.	Renesas Starter Kit + for RZ/T2M User's Manual	R20UT4939EG
Quick Start Guide	Provides simple instructions to setup the RSK+ and run the first sample.	Renesas Starter Kit + for RZ/T2M Quick Start Guide	R20UT4941EG
Schematics	Full detail circuit schematics of the CPU Board.	Renesas Starter Kit + for RZ/T2M Schematics	R20UT4938EG
Hardware Manual	Provides technical details of the RZ/T2M microprocessor.	RZ/T2M Group Hardware Manual	R01UH0916EJ

2. List of Abbreviations and Acronyms

Abbreviation	Full Form
ADC	Analog-to-Digital Converter
bps	bits per second
CAN	Controller Area Network
CPU	Central Processing Unit
DIP	Dual In-line Package
DNF	Do Not Fit
EEPROM	Electronically Erasable Programmable Read Only Memory
ESC	EtherCAT Slave Controller
ESD	Electrostatic Discharge
EtherCAT	Ethernet for Control Automation Technology
GPT	General PWM Timer
I^2C (IIC)	Philips™ Inter-Integrated Circuit Connection Bus
J-Link®	SEGGER debug probe (Emulator)
J-Link® OB	SEGGER On-board debug probe (Emulator)
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MAC	Media Access Control
MCU	Micro controller Unit
MPU	Micro Processor Unit
MTU	Multi-Function Timer Pulse Unit
n/a (NA)	Not Applicable
n/c (NC)	Not Connected
NMI	Non-maskable Interrupt
PC	Personal Computer
PCB	Printed Circuit Board
POE	Port Output Enable
POEG	Port Output Enable for GPT
PWM	Pulse Width Modulation
RAM	Random Access Memory
RGMII	Reduced Gigabit Media-Independent Interface
ROM	Read Only Memory
RSK+	Renesas Starter Kit+
SCI	Serial Communications Interface
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

Table of Contents

1. Overview

1.1 Purpose

This RSK+ is an evaluation tool for Renesas microprocessors. This manual describes the technical details of the RSK+ hardware.

1.2 Features

This RSK+ provides an evaluation of the following features:

- Renesas microprocessor programming
- User code debugging
- User circuitry such as switches, LEDs and a potentiometer
- Sample applications

The RSK+ contains all the circuitry required for microprocessor operation.

1.3 Board specification

Board specification is shown in **Table 1-1** below.

Table 1-1: Board Specification

Item	Specification
Microprocessor	Part No: R9A07G075M24GBG
	Package: 320-pin FBGA
	On-Chip Memory: RAM 2MB
On-Board Memory	SDRAM: 256Mbit (Data width 16bit)*1
	NOR Flash: 256Mbit (Data width 16bit)
	Octa Flash: 512Mbit
	HyperRAM: 64Mbit
	QSPI Serial Flash: 512Mbit
	I²C EEPROM: 32Kbit
Input Clock	RZ/T2M Main: 25MHz
	RL78/G1C Main: 12MHz
	Ethernet PHY (for RGMII): 25MHz
Power Supply	DC Power Jack: 5 V Input
	USB Type-C Connector: 5V Input
	Power Supply IC: 5V Input, 3.3V Output
	Power Supply IC: 5V Input, 1.8V Output
	Power Supply IC: 5V Input, 1.1V Output
	Power Supply IC: 5V Input, 1.0V Output (For Ethernet PHY)
	Power Supply IC: 5V Input, 2.5V Output (For Ethernet PHY)
Debug Interface	MIPI-10: 1.27mm pitch 10-pin header
	MIPI-20: 1.27mm pitch 20-pin header
	Mictor-38: 0.64mm pitch 38-pin header
	J-Link® OB: USB-MicroB
DIP Switch	Mode Configuration: 10-pole x 1
	Signal Select: 10-pole x 2
	User: 8-pole x 1
Push Switch	Reset Switch x 1
	User Switch x 3
Potentiometer (for ADC)	Single-turn, 10kΩ
LED	3.3V Power Indicator: green x 1
	User: green x 1, yellow x 1, red x 2
	Ethernet Status: green x 3, yellow x 3
	Ether-CAT Status: green x 4, yellow green x 1, red x 3
	J-Link® OB Status: yellow x 1
Ethernet	Connector: RJ45 x 3
	PHY: Single Port PHY x 3
CAN*2	Connector *3: 2.54mm pitch, 3-pin x 1
	CAN Driver x 1
USB	USB-Function: Mini-USB
	USB-Host: USB-Type A
RS485	Connector *3: 10-pin Connector
	RS485 Transceiver x 1
USB to Serial Converter Interface	Connector: Mini-USB
	Driver: RL78/G1C Microcontroller (Part No R5F10JBCAFP)
Pmod™	PMOD-2A, 6A: 12-pin Connector
	PMOD-3A: 12-pin Connector
mikroBUS™	2.54 mm pitch, 8-pin x 2 (J21, J22)
Grove®	2.00 mm pitch, 4-pin x 2 (J27, J28)
QWIIC®	1.00 mm pitch, 4-pin x 1 (J30)
Pin Header *3	2.54 mm pitch, 20-pin x 2 (CN1, CN3), 2.54mm pitch, 8-pin x 1 (CN2)
Application Board Interface *3	2.54 mm pitch, 26-pin x 2 (JA1, JA2), 50-pin x 1 (JA3), 24-pin x 2 (JA5, JA6)

*1: Access frequency of SRAM is up to 50MHz on this board.
*2: The CAN on this board can transfer at up to 5Mbps.
*3: This part is not mounted.

2. Power Supply

2.1 Requirements

This board has a USB Type-C connector (CN5) and an optional centre positive supply connector using a 2.0mm barrel power jack (CN6). Supply power to the CPU board from either CN5 or CN6.
The main power supply connected to CN6 should supply a minimum of 15W to ensure full functionality.

This CPU board supports two external voltage input. Details of the external power supply connection are shown in **Table 2-1** below.

Table 2-1: Main Power Supply Requirements

Connector	Supply voltage
CN5	Type-C VBUS (5VDC)
CN6	Input 5VDC*

*: There are RSK+ products which require a 12V voltage input. Since this board requires a 5V voltage input, be careful not to connect the power supply of a high-voltage output accidentally. Moreover, the main power supply connected to CN6 should supply a minimum of 15W to ensure full functionality.

3. Board Layout

3.1 Component Layout

Figure 3-1, Figure 3-3 below shows the top component layout of the board.

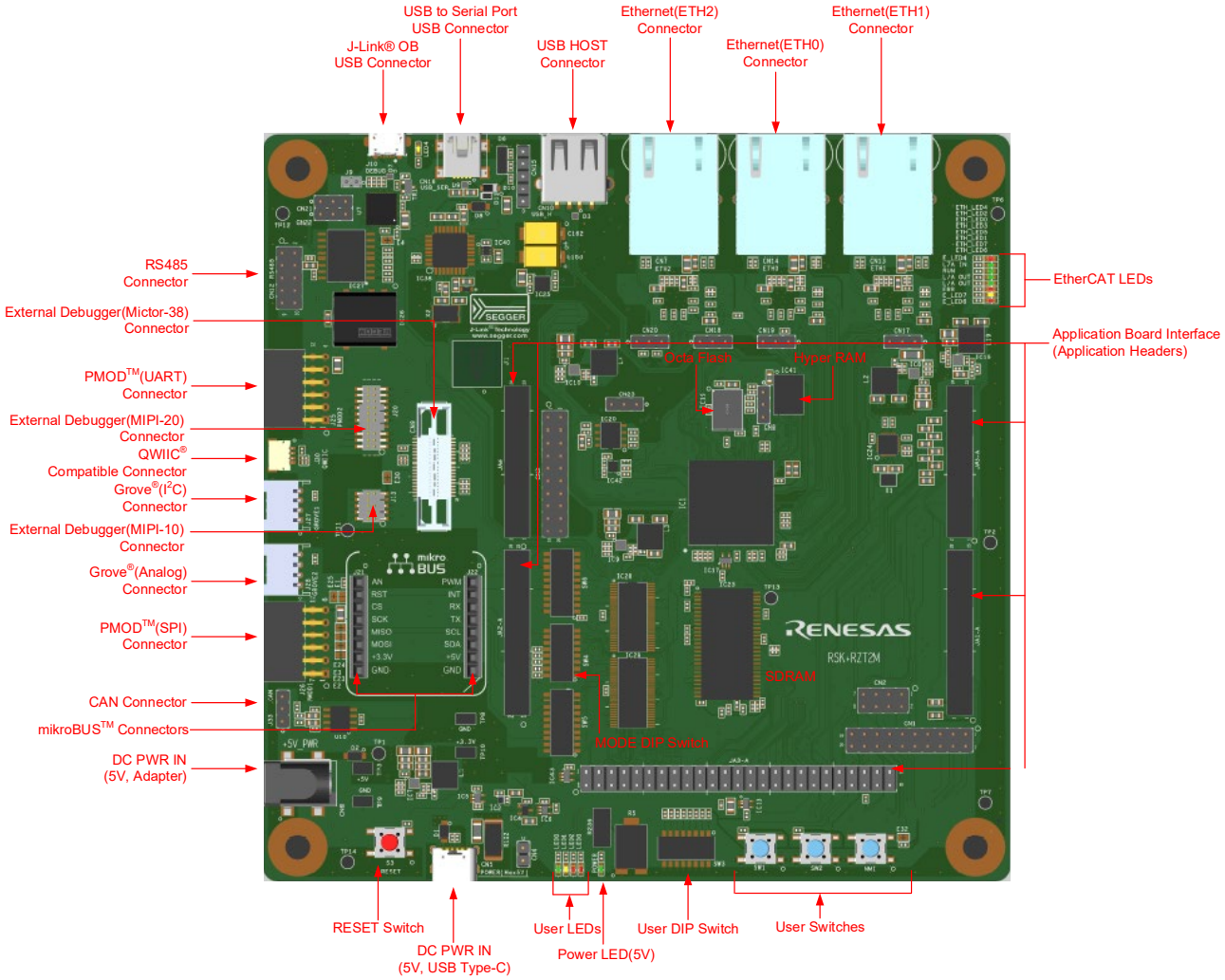

Figure 3-1: Board Layout (Top side)

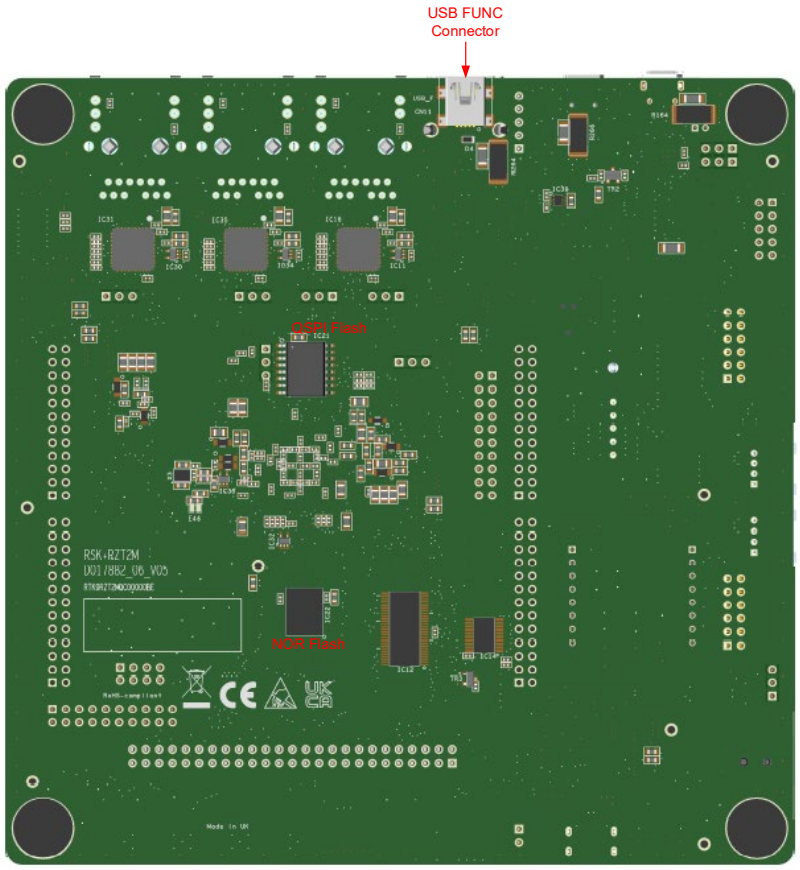

Figure 3-2: Board Layout (Bottom side)

3.2 Board Dimensions

Figure 3-3 below gives the board dimensions and connector positions. All the through-hole connectors are on a common 2.54mm pitch grid for easy interfacing.

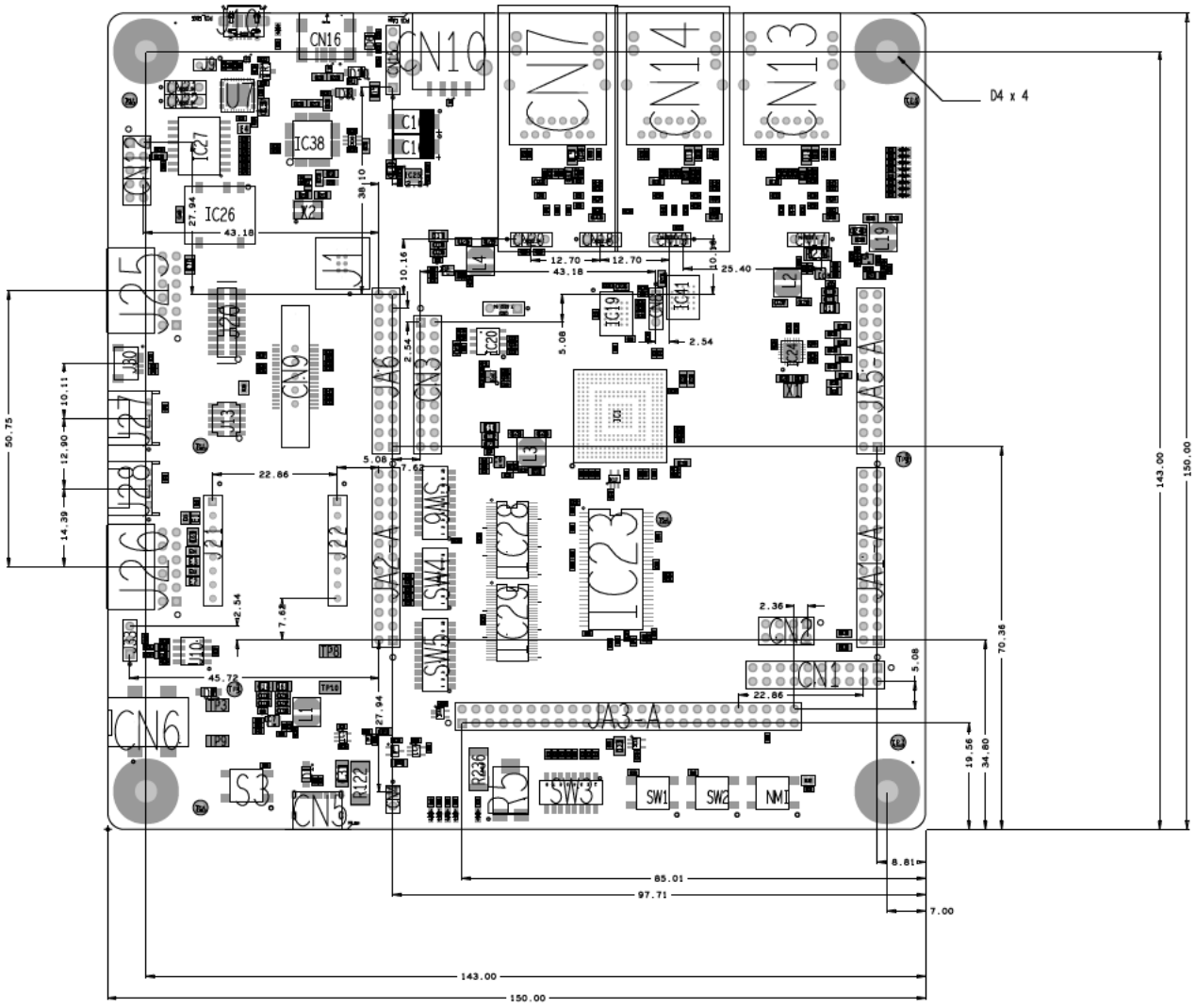

Figure 3-3: Board Dimensions (Unit: mm)

3.3 Component Placement

For placement details of individual components on the board, refer to section [10. Appendix].

4. Connectivity

4.1 Internal Board Connections

The diagram below shows the CPU board components and their connectivity to the MPU.

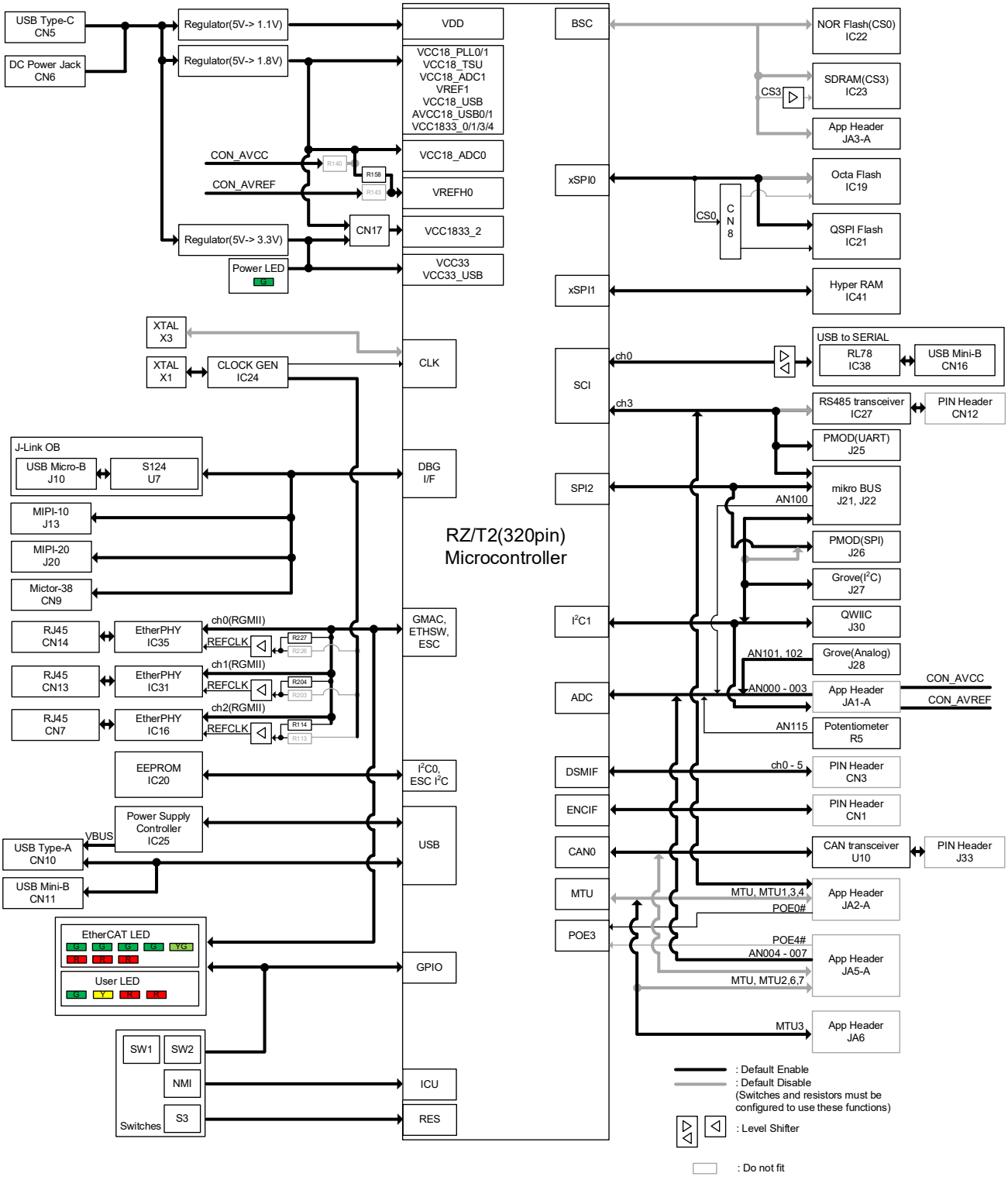

Figure 4-1: Internal Board Block Diagram

4.2 Emulator Connections

Figure 4-2 below shows the connection between the CPU board, emulator and the host PC, **Figure 4-3** below shows the connection between the CPU board, J-Link® OB and the host PC.

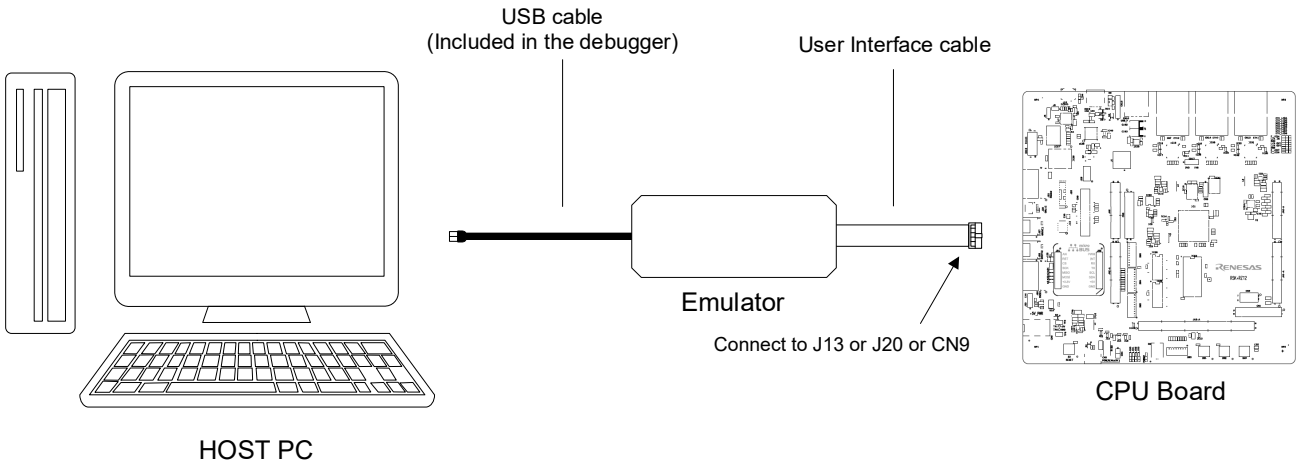

Figure 4-2: Emulator Connection Diagram (External Emulator)

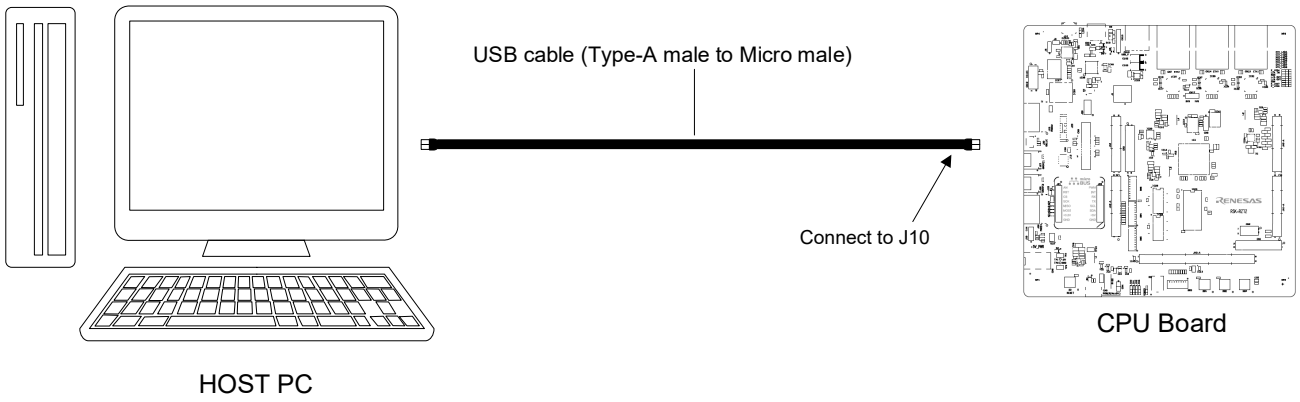

Figure 4-3: Emulator Connection Diagram (J-Link® OB)

5. User Circuitry

5.1 Reset Circuit

A reset control circuit is fitted to the CPU board to generate the required reset signal and is triggered from the RESET switch and the power-on-reset circuit. Refer to the RZ/T2M Group User's Manual: Hardware for details regarding the reset signal timing requirements, and the CPU board schematics for information regarding the reset circuitry in use on the board.

5.2 Clock Circuit

A clock circuit is fitted to the CPU board to generate the required clock signal to drive the MPU, and associated peripherals. Refer to the RZ/T2M Group Hardware Manual and the RL78/G1C hardware manual for details regarding the clock signal requirements, and the CPU board schematics for information regarding the clock circuitry in use on the CPU board. Details of the oscillators fitted to the board are listed in **Table 5-1**: Crystal below.

Table 5-1: Crystal

Crystal	Function	Default Placement	Frequency	Device Package
X1	Main MPU crystal for RZ/T2M (via clock generator (IC24))	Fitted	25MHz	Encapsulated, SMT
X2	Main MCU crystal for RL78/G1C	Fitted	12MHz	Encapsulated, SMT
X3	Main MPU crystal for RZ/T2M (MPU direct)	Fitted	25MHz	Encapsulated, SMT

5.3 Switches

There are four push switches and four DIP switches located on the CPU board. The function of each switch and its connection is shown in **Table 5-2 and Table 5-3**. For further information regarding switch connectivity, refer to the CPU board schematics.

Table 5-2: Push Switch Connections

Switch	Function	MPU	
		Port	Pin
S3	When pressed, the microprocessor is reset.	RES#	T5
SW1	Connects to IRQ2 for user controls.	P10_5	T13
SW2	Connects to IRQ7 for user controls.	P16_3	K16
NMI	Connects to an NMI input for user controls.	P16_2	L19

Table 5-3: DIP Switch Connections

Switch	Function	MPU	
		Port	Pin
SW3-1	Connects to P11_0 for user controls.	P11_0	Y18
SW3-2	Connects to P11_3 for user controls.	P11_3	T15
SW3-3	Connects to P11_4 for user controls.	P11_4	V17
SW3-4	Connects to P11_6 for user controls.	P11_6	R13
SW3-5	Connects to P10_6 for user controls.	P10_6	T12
SW3-6	Connects to P13_2 for user controls.	P13_2	P16
SW3-7	Connects to P13_7 for user controls.	P13_7	N15
SW3-8	Connects to P14_1 for user controls.	P14_1	U20
SW4-1	Refer to section 6.3 for the setting contents.	P04_5	N1
SW4-2	Refer to section 6.3 for the setting contents.	P04_6	M5
SW4-3	Refer to section 6.3 for the setting contents.	P04_7	N2
SW4-4	Refer to section 6.3 for the setting contents.	P17_0	J15
SW4-5	Refer to section 6.3 for the setting contents.	P02_1	F1
SW5-3	Refer to section 6 for the setting contents.	P18_1	G19
SW5-4	Refer to section 6 for the setting contents.	P18_1	G19
SW5-5	Refer to section 6 for the setting contents.	P17_7	G20
SW5-6	Refer to section 6 for the setting contents.	P17_7	G20
SW5-7	Refer to section 6 for the setting contents.	P17_7	G20
SW5-8	Refer to section 6 for the setting contents.	P17_6	J18
SW5-9	Refer to section 6 for the setting contents.	P17_6	J18
SW5-10	Refer to section 6 for the setting contents.	P17_6	J18
SW6-1	Refer to section 6 for the setting contents.	-	-
SW6-3	Refer to section 6 for the setting contents.	P22_1	C7
SW6-4	Refer to section 6 for the setting contents.	P22_1	C7
SW6-5	Refer to section 6 for the setting contents.	P18_0	H16
SW6-6	Refer to section 6 for the setting contents.	P18_0	H16
SW6-7	Refer to section 6 for the setting contents.	P18_3	G18
SW6-8	Refer to section 6 for the setting contents.	P18_3	G18
SW6-9	Refer to section 6 for the setting contents.	P05_2	P3
SW6-10	Refer to section 6 for the setting contents.	P05_2	P3

5.4 LEDs

There are 20 LEDs on the RSK+ board. The function of each LED, its colour, and its connections are shown in **Table 5-4**.

Table 5-4: LED Connections

LED	Colour	Function	MPU	
			Port	Pin
POWER	Green	Indicates the status of the 3.3V power rail.	-	-
LED0	Green	User operated LED.	P19_6	D18
LED1	Yellow	User operated LED.	P19_4	C20
LED2	Red	User operated LED.	P20_0	B20
LED3	Red	User operated LED.	P23_4	C5
LED4	Yellow	Indicates the status of the J-Link® OB.	-	-
ETH_LED0	Green	EtherCAT LED(LEDRUN)	P20_2	A10
ETH_LED1	Red	EtherCAT LED(LEDERR)	P20_3	C9
ETH_LED2	Green	EtherCAT LED(LINKACT0)	P20_1	C11
ETH_LED3	Green	EtherCAT LED(LINKACT1)	P20_4	B10
ETH_LED4	Red	EtherCAT LED	P19_7	G15
ETH_LED5	Green	EtherCAT LED(LINKACT2)	P21_0	A9
ETH_LED6	Red	EtherCAT LED	P08_2	V6
ETH_LED7	Yellow Green	EtherCAT LED	P19_3	H15
ETHERNET Connector (ETH0)	Green	Ethernet LED(Link)	-	-
ETHERNET Connector (ETH0)	Yellow	Ethernet LED(Activity)	-	-
ETHERNET Connector (ETH1)	Green	Ethernet LED(Link)	-	-
ETHERNET Connector (ETH1)	Yellow	Ethernet LED(Activity)	-	-
ETHERNET Connector (ETH2)	Green	Ethernet LED(Link)	-	-
ETHERNET Connector (ETH2)	Yellow	Ethernet LED(Activity)	-	-

5.5 Potentiometer

A single-turn potentiometer is connected as a potential divider to analog input AN115, pin C12. The potentiometer can be used to create a voltage between VCC18_ADC1 and GROUND.
Refer to the maker site for specification of the potentiometer (PIHER with part number N6L50T7S-103R).

The potentiometer offers an easy method of supplying a variable analog input to the microprocessor. It does not necessarily reflect the accuracy of the controller's ADC. Refer to the RZ/T2M Group User's Manual: Hardware for further details.

5.6 Pmod™

The RSK+ board is equipped with connectors for Digilent Pmod™ interface. Please connect the Pmod™ Peripheral module that is compatible with the PMOD connector.

The Digilent Pmod™ Compatible headers use an SPI interface, an I²C interface and a UART interface. **Figure 5-1** below shows Digilent Pmod™ Compatible Header Pin Numbering. Connection information for the Digilent Pmod™ Compatible header is provided in **Table 5-5 and Table 5-6** below.

Please note that the connector numbering adheres to the Digilent Pmod™ standard and is different from all other connectors on the RSK+ designs. Details can be found in the Digilent Pmod™ Interface Specification.

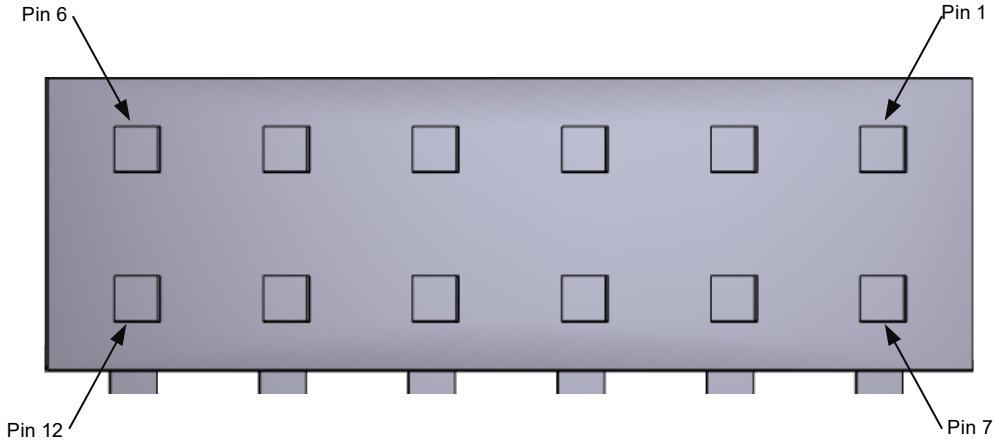

Figure 5-1: Digilent Pmod™ Compatible Header Pin Numbering

Table 5-5: Pmod™ Header (J25) Connections

Digilent Pmod™ Compatible Header Connections							
Pin	Circuit Net Name	MPU		Pin	Circuit Net Name	MPU	
		Port	Pin			Port	Pin
1	CTS3#	P17_4	J16	7	IRQ3	P19_2	D19
2	SCI_TXD	P18_0	H16	8	P16_7	P16_7	J19
3	SCI_RXD	P17_7	G20	9	P17_0_MDD	P17_0	J15
4	SCI_RTS	P18_1	G19	10	P17_1	P17_1	J20
5	GROUND	-	-	11	GROUND	-	-
6	3.3V	-	-	12	3.3V	-	-

Table 5-6: Pmod™ Header (J26) Connections

Digilent Pmod™ Compatible Header Connections							
Pin	Circuit Net Name	MPU		Pin	Circuit Net Name	MPU	
		Port	Pin			Port	Pin
1	SSL20	P18_7	F18	7	IRQ9	P17_2	H20
2	MOSI2	P18_5	E20	8	P23_6	P23_6	A2
3*	MISO2 I2C_SCL_A	P18_6 P22_6	E19 E7	9	P08_3	P08_3	T6
4*	RSPCK2 I2C_SDA_A	P18_4 P22_7	F19 C6	10	P19_1	P19_1	E18
5	GROUND	-	-	11	GROUND	-	-
6*	3.3V 5.0V	-	-	12	3.3V 5.0V	-	-

*: It is necessary to set the solder bridge jumper to change the function. Refer to section 6.2 for the required modifications.

5.7 Grove®

The RSK+ board is equipped with connectors for Grove® interface. Please connect the Grove® module that is compatible with connector.
The Grove® compatible headers use an I²C interface and an analog interface. **Figure 5-2** below shows Grove® Compatible Header Pin Numbering. Connection information for the Grove® Compatible header is provided in **Table 5-7 and Table 5-8** below.

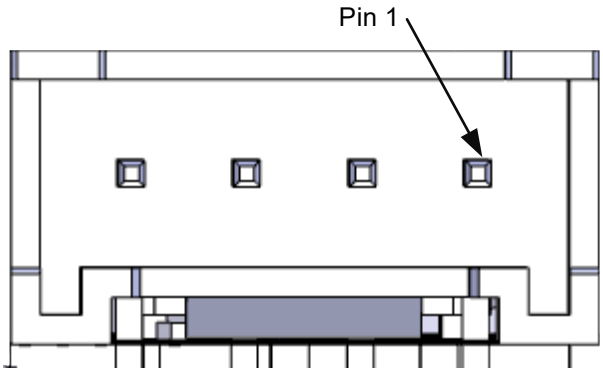

Figure 5-2: Grove® Compatible Header Pin Numbering

Table 5-7: Grove® Header (J27) Connections

Grove® Compatible Header Connections			
Pin	**Circuit Net Name**	**MPU**	
		Port	**Pin**
1	I2C_SCL_A	P22_6	E7
2	I2C_SDA_A	P22_7	C6
3	3.3V	-	-
4	GROUND	-	-

Table 5-8: Grove® Header (J28) Connections

Grove® Compatible Header Connections			
Pin	**Circuit Net Name**	**MPU**	
		Port	**Pin**
1	ADC_AN101	AN101	B16
2	ADC_AN102	AN102	E13
3	3.3V	-	-
4	GROUND	-	-

5.8 QWIIC®

The RSK+ board is equipped with connectors for QWIIC® interface. Please connect the QWIIC® products that is compatible with connector.
The QWIIC® compatible headers use an I²C interface. **Figure 5-3** below shows QWIIC® Compatible Header Pin Numbering. Connection information for the QWIIC® Compatible header is provided in Table 5-9 below.

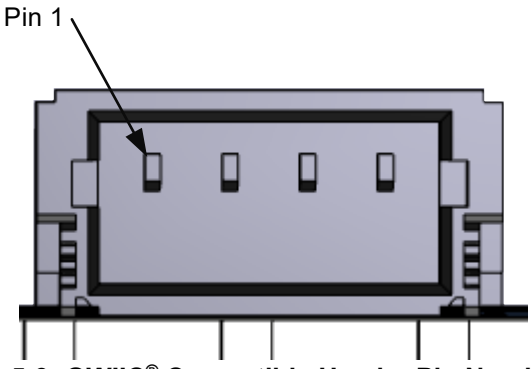

Figure 5-3: QWIIC® Compatible Header Pin Numbering

Table 5-9: QWIIC® Header (J30) Connections

QWIIC® Compatible Header Connections			
Pin	**Circuit Net Name**	**MPU**	
		Port	**Pin**
1	GROUND	-	-
2	3.3V	-	-
3	I2C_SDA_A	P22_7	C6
4	I2C_SCL_A	P22_6	E7

5.9 mikroBUS™

The RSK+ board is equipped with connectors for mikroBUS™ interface. Please connect the mikroBUS™ products that is compatible with connector.
The mikroBUS™ compatible headers use analog interface, SPI interface, UART interface, I^2C interface, PWM and interrupt. Connection information for the mikroBUS™ Compatible header is provided in **Table 5-10 and Table 5-11**below.

Table 5-10: mikroBUS™ Header (J21) Connections

mikroBUS™ Compatible Header Connections			
Pin	**Circuit Net Name**	**MPU**	
		Port	**Pin**
1	ADC_AN100	AN100	F13
2	MB_RST#	P18_3	G18
3	SSL20	P18_7	F18
4	RSPCK2	P18_4	F19
5	MISO2	P18_6	E19
6	MOSI2	P18_5	E20
7	3.3V	-	-
8	GROUND	-	-

Table 5-11: mikro™ BUS Header (J22) Connections

mikroBUS™ Compatible Header Connections			
Pin	**Circuit Net Name**	**MPU**	
		Port	**Pin**
1	MIK_PWM	P17_6	J18
2	IRQ11_ENCIF9_WAIT#	P03_3	K3
3	SCI_RXD	P17_7	G20
4	SCI_TXD	P18_0	H16
5	I2C_SCL_A	P22_6	E7
6	I2C_SDA_A	P22_7	C6
7	5.0V	-	-
8	GROUND	-	-

5.10 USB Serial Port

A USB serial port is implemented in a Renesas low power microcontroller (RL78/G1C) and is connected to the RZ/T2M Serial Communications Interface (SCI) module. Connections between the USB to Serial converter and the microprocessor are listed in **Table 5-12** below.

Table 5-12: Serial Port Connections

Signal Name	Function	MPU	
		Port	Pin
UART_USB_TX	SCI0 Transmit Signal.	P16_5	K19
UART_USB_RX	SCI0 Receive Signal.	P16_6	K18

When the CPU board is first connected to a PC running Windows™ with the USB/Serial connection, the PC will look for a driver. Use the driver that is installed as standard on your PC.
If you do not have the driver, please download the driver installer from the following URL.
https://www.renesas.com/document/rsk-usb-serial-driver?language=en

5.11 Controller Area Network (CAN)

A CAN transceiver IC (U10) is fitted to the RSK+ board and connected to the CAN MPU peripheral. For further details regarding the CAN protocol and supported modes of operation, please refer to the RZ/T2M Group User's Manual: Hardware. Connection information for the CAN interface header is provided in **Table 5-13**. The details of connecting to the connected device and MPU are shown in **Table 5-14** below.

Table 5-13: CAN Interface Header (J33) Connections

CAN Interface Header Connections	
Pin	**Circuit Net Name**
1	CAN_H
2	CAN_L
3	GROUND

Table 5-14: CAN Connections

CAN Signal	Function	MPU	
		Port	Pin
CAN_TX	CAN Data Transmission.	P05_3	P2
CAN_RX_OB	CAN Data Reception.	P05_2	P3
CAN_RX_JA5 *1			

*1: This connection is a not available in the default RSK+ configuration - refer to section 6 for the required modifications.

5.12 Ethernet

When running any Ethernet software, a unique MAC address should be used. A unique Renesas allocated MAC address is attached to the PCB as a sticker and should always be used with this device to ensure full compatibility when using other Renesas hardware on a common Ethernet connection.

Three Ethernet PHY ICs are fitted to the CPU board and are connected to the MPU Ethernet peripherals. The RZ/T2M MPU supports half and full duplex, 10Mb/s and 100Mb/s and 1000Mb/s transmission and reception. Refer to section 5.4 Ethernet LEDs. The connections for the Ethernet controller are listed in **Table 5-15, Table 5-16, Table 5-17, Table 5-18, Table 5-19** below.
Note that Ethernet port 2 cannot be used at the same time as SDRAM.

Table 5-15: Ethernet Connections (ETH0)

Ethernet signal	Function	MPU	
		Port	Pin
ETH0_TXCLK	RGMII: Transmit clock output	P09_7	R9
ETH0_TXEN	RGMII: Transmit data enable / Transmit data error	P10_0	W7
ETH0_TXD0	RGMII: Transmit data0	P09_6	Y6
ETH0_TXD1	RGMII: Transmit data1	P09_5	T9
ETH0_TXD2	RGMII: Transmit data2	P09_4	R8
ETH0_TXD3	RGMII: Transmit data3	P09_3	W6
ETH0_RXCLK	RGMII: Receive clock input	P08_6	V7
ETH0_RXDV	RGMII: Receive data valid / Receive data error	P08_5	Y3
ETH0_RXD0	RGMII: Receive data0	P10_1	Y7
ETH0_RXD1	RGMII: Receive data1	P10_2	V8
ETH0_RXD2	RGMII: Receive data2	P10_3	V9
ETH0_RXD3	RGMII: Receive data3	P08_4	W4
ETH0_REFCLK	Outputs 25MHz clock for EtherPHY0	P09_1	T8

Table 5-16: Ethernet Connections (ETH1)

Ethernet signal	Function	MPU	
		Port	Pin
ETH1_TXCLK	RGMII: Transmit clock output	P06_4	U1
ETH1_TXEN	RGMII: Transmit data enable / Transmit data error	P06_5	T3
ETH1_TXD0	RGMII: Transmit data0	P06_3	P5
ETH1_TXD1	RGMII: Transmit data1	P06_2	T2
ETH1_TXD2	RGMII: Transmit data2	P05_7	P6
ETH1_TXD3	RGMII: Transmit data3	P06_0	T1
ETH1_RXCLK	RGMII: Receive clock input	P07_3	U3
ETH1_RXDV	RGMII: Receive data valid / Receive data error	P07_2	W1
ETH1_RXD0	RGMII: Receive data0	P06_6	U2
ETH1_RXD1	RGMII: Receive data1	P06_7	V1
ETH1_RXD2	RGMII: Receive data2	P07_0	V2
ETH1_RXD3	RGMII: Receive data3	P07_1	R5
ETH1_REFCLK	Outputs 25MHz clock for EtherPHY1	P06_1	R3

Table 5-17: Ethernet Connections (ETH2)

Ethernet signal	Function	MPU	
		Port	Pin
ETH2_TXCLK	RGMII: Transmit clock output	P00_6	D3
ETH2_TXEN	RGMII: Transmit data enable / Transmit data error	P00_2	B1
ETH2_TXD0	RGMII: Transmit data0	P01_5	F3
ETH2_TXD1	RGMII: Transmit data1	P01_4	H5
ETH2_TXD2	RGMII: Transmit data2	P01_3	D1
ETH2_TXD3	RGMII: Transmit data3	P01_2	D2
ETH2_RXCLK	RGMII: Receive clock input	P24_1	C3
ETH2_RXDV	RGMII: Receive data valid / Receive data error	P00_1	F5
ETH2_RXD0	RGMII: Receive data0	P23_7	B3
ETH2_RXD1	RGMII: Receive data1	P24_0	C4
ETH2_RXD2	RGMII: Receive data2	P24_2	E5
ETH2_RXD3	RGMII: Receive data3	P00_0	B2
ETH2_REFCLK	Outputs 25MHz clock for EtherPHY2	P00_3	C2

Table 5-18: Ethernet Connections (ETH0/ETH1/ETH2)

Ethernet signal	Function	MPU	
		Port	Pin
ETH_MDIO	Management data I/O	P09_0	T7
ETH2_MDIO	Management data I/O	P01_0	E3
ETH_MDC	Management data clock	P08_7	W5
ETH2_MDC	Management data clock	P01_1	H6

Table 5-19: Default PHY setting

Default PHY setting items	Default PHY setting contents
PHY Address	ETH0 (IC35): = 0 ETH1 (IC31): = 1 ETH2 (IC16): = 2
MAC Interface	RGMII
Isolate	Disable
Speed	Depends auto negotiation
Duplex	Full-Duplex
Auto negotiation	Enable

5.13 Ethernet Switch (ETHSW)

The CPU board has an Ethernet Switch (ETHSW) and is connected to the ETHSW module of the microprocessor. The ETHSW connections to and from the MPU are shown in **Table 5-15, Table 5-16, Table 5-17, Table 5-18, Table 5-20** below.
Note that ETHSW port 2 cannot be used at the same time as SDRAM.

Table 5-20: Ethernet Connections (ETHSW0/ETHSW1/ETHSW2)

Ethernet signal	Function	MPU	
		Port	Pin
ETHSW_LPI0	Port0 MAC status	P08_0	V5
ETHSW_LPI1	Port0 MAC status	P01_7	F2
ETHSW_LPI2	Port0 MAC status	P02_0	J6
ETHSW_PTPOUT0	Ethernet switch timer pulse	P08_3	T6
ETHSW_PTPOUT1	Ethernet switch timer pulse	P02_1	F1
ETHSW_PTPOUT2	Ethernet switch timer pulse	P13_2	P16
ETHSW_PTPOUT3	Ethernet switch timer pulse	P21_0	A9
ETHSW_TDMAOUT0	Ethernet switch TDMA timer	P02_2	J5
ETHSW_TDMAOUT1	Ethernet switch TDMA timer	P20_2	A10
ETHSW_TDMAOUT2	Ethernet switch TDMA timer	P20_3	C9
ETHSW_TDMAOUT3	Ethernet switch TDMA timer	P20_4	B10
ETH0_LINK	Ethernet switch PHY link status	P10_4	R11
ETH1_LINK	Ethernet switch PHY link status	P05_5	R1
ETH2_LINK	Ethernet switch PHY link status	P00_5	G5

5.14 EtherCAT Slave Controller (ESC)

To run the EtherCAT slave controller software, the EtherCAT ID number is required. Please use SW3 as necessary.

The CPU board has an EtherCAT slave controller (ESC) and is connected to the ESC module of the microprocessor. EtherCAT status LEDs are listed in section 5.4. The EtherCAT connections to and from the MPU are shown in **Table 5-15, Table 5-16, Table 5-17, Table 5-18, Table 5-21** below.
Note that ESC port 2 cannot be used at the same time as SDRAM.

Table 5-21: Ethernet Connections (ESC0/ESC1/ESC2)

Ethernet signal	Function	MPU	
		Port	Pin
ESC_LEDRUN	EtherCAT RUN LED signal output port	P20_2	A10
ESC_IRQ	EtherCAT IRQ signal output port	P17_0	J15
ESC_LEDERR	EtherCAT Error LED signal output port	P20_3	C9
ESC_LINKACT0	EtherCAT link / Activity LED signal output port	P20_1	C11
ESC_LINKACT1	EtherCAT link / Activity LED signal output port	P20_4	B10
ESC_LINKACT2	EtherCAT link / Activity LED signal output port	P21_0	A9
ESC_SYNC0	EtherCAT SYNC0 signal output port	P13_6	R18
ESC_SYNC1	EtherCAT SYNC1 signal output port	P13_6	R18
ESC_LATCH0	EtherCAT LATCH0 signal input port	P13_5	N16
ESC_LATCH1	EtherCAT LATCH1 signal input port	P13_5	N16
ESC_RESETOUT#	EtherCAT reset signal output port	P20_7	E10
EEPROM_SCL	EtherCAT EEPROM I^2C clock output port	P20_5	F10
EEPROM_SDA	EtherCAT EEPROM I^2C data signal I/O port	P20_6	C10
ETH0_LINK	EtherCAT PHY0 link status signal input port	P10_4	R11
ETH1_LINK	EtherCAT PHY1 link status signal input port	P05_5	R1
ETH2_LINK	EtherCAT PHY2 link status signal input port	P00_5	G5

5.15 Universal Serial Bus (USB)

This CPU board is fitted with a USB Host socket (type A, CN10) and a Function socket (type Mini B, CN11). USB module is connected to the Host and Function socket and can operate as either a Host or Function device. However, they cannot be used at the same time. The connection for the USB module is shown in **Table 5-22** below.

Table 5-22: USB Module Connections

USB Signal	Function	MPU	
		Port	Pin
USB_DP	D+ I/O pin of the USB on-chip transceiver	USB_DP	Y14
USB_DM	D– I/O pin of the USB on-chip transceiver	USB_DM	Y13
USB_VBUSIN	VBUS (5V) supply enable signal for external power supply chip	P07_4	W2
USB_VBUSEN	Outputs the VBUS power enable signal for USB.	P19_0	D20
USB_OVRCUR	External overcurrent detection signal B	P17_5	H18

5.16 External Bus

The RZ/T2M features an external data bus, which is connected to various devices on the CPU board. Details of the devices connected to the external data bus are listed in **Table 5-23** below. Further details of the devices connected to the external bus can be found in the board schematics.

Table 5-23: External Bus Address Space

Chip Select	Device Name	Device Description	Address Space
CS0	IC22	256Mbit NOR Flash	70000000h – 71FFFFFFh (32Mbyte)
CS2	-	Unused	74000000h – 77FFFFFFh (64Mbyte)
CS3	IC23	256Mbit SDRAM	78000000h – 79FFFFFFh (32Mbyte)
CS3(BSC_CS3#_33)	JA3-A	Application Header	78000000h – 7BFFFFFFh (64Mbyte)
CS5	JA3-A	Application Header	7C000000h – 7FFFFFFFh (64Mbyte)

5.17 Expanded Serial Peripheral Interface (xSPI)

The RZ/T2M features two Expanded Serial Peripheral Interface modules (xSPI). The extended serial peripheral interface is connected to the device on the CPU board. Details of the devices connected to the extended serial peripheral interface are shown in **Table 5-24** below. Further details of the devices connected to the extended serial peripheral interface can be found in the board schematics.

Table 5-24: Expanded Serial Interface (xSPI) Address Space

Chip Select	Device Name	Device Description	Address Space
XSPI0_CS0*[1]	IC19	512Mbit Octa Flash	60000000h – 63FFFFFFh (64Mbyte)
XSPI0_CS0	IC21	512Mbit Serial Flash	60000000h – 63FFFFFFh (64Mbyte)
XSPI0_CS1	-	Unused	64000000h – 67FFFFFFh (64Mbyte)
XSPI1_CS0	IC41	64Mbit Hyper RAM	68000000h – 687FFFFFh (8Mbyte)
XSPI1_CS1	-	Unused	6C000000h – 6FFFFFFFh (64Mbyte)

*[1]: This connection is a not available in the default RSK+ configuration - refer to section 6 for the required modifications.

5.18 I²C Bus (Inter-IC Bus)

The RZ/T2M features three I²C (Inter-IC Bus) interface modules. Channel 0 of the IIC is connected to a 16Kbit EEPROM. Channel 0 of the IIC is also multiplexed with I²C for EtherCAT and can also be used as EEPROM for EtherCAT. Channel 1 of the IIC is connected to Pmod™ and Grove®, QWIIC®, mikroBUS™, Application Headers. **Table 5-25** below details the connected device, and their connection to the MPU.

Table 5-25: I²C BUS Port Connections

Signal Name	Function	MPU	
		Port	Pin
EEPROM_SCL (RIIC0)	CLOCK	P20_5	F10
EEPROM_SDA (RIIC0)	DATA	P20_6	C10
I2C_SCL_A (RIIC1)	CLOCK	P22_6	E7
I2C_SDA_A (RIIC1)	DATA	P22_7	C6

5.19 RS485 Interface

A RS485 transceiver IC is fitted to the RSK+ board and connected to the SCI MPU peripheral. Connection information for the RS485 Interface header is provided in **Table 5-26 below.** The details of connecting to the connected device and MPU are shown in **Table 5-27** below.

Table 5-26: RS485 Interface Header (CN12) Connections

RS485 Interface Header Connections			
Pin	**Circuit Net Name**	**Pin**	**Circuit Net Name**
1	NC	2	NC
3	RS485_B	4	RS485_Y
5	RS485_Z	6	RS485_A
7	NC	8	NC
9	NC	10	NC

Table 5-27: RS485 Port Connections

Signal Name	Function	MPU	
		Port	Pin
RS485_RXD*1	SCI3 Receive Signal	P17_7	G20
RS485_DE*1	SCI3 Driver Enable Signal	P04_5	N1
SCI_TXD	SCI3 Transmit Signal	P18_0	H16

*1: This connection is a not available in the default RSK+ configuration - refer to section 6 for the required modifications.

6. Configuration

6.1 Modifying the RSK+

This section lists the option links that are used to modify the way CPU board operates in order to access different configurations. Configurations are made by modifying link resistors or headers with movable jumpers or by configuration DIP switches.

A link resistor is a 0Ω surface mount resistor, which is used to short or isolate parts of a circuit. Option links are listed in the following sections, detailing their function when fitted or removed. **Bold, blue text** indicates the default configuration that the CPU board is supplied with. Refer to the component placement diagram (section 3) to locate the option links, jumpers and DIP switches.

When removing soldered components, always ensure that the CPU board is not exposed to a soldering iron for intervals greater than 5 seconds. This is to avoid damage to nearby components mounted on the board.

When modifying a link resistor, always check the related option links to ensure there is no possible signal contention or short circuits. Because many of the MPU's pins are multiplexed, some of the peripherals must be used exclusively. Refer to the RZ/T2M Group User's Manual: Hardware and CPU board schematics for further information.

6.2 Jumper Settings

Three types of jumpers are provided on the CPU board.
1. Solder bridge
2. Trace cut
3. Traditional pin header jumpers

The following sections describe each type and their default configuration.

6.2.1 Solder Bridge

A **solder-bridge** jumper is provided with two isolated pads that may be joined together by one of three methods:
- Solder may be applied to both pads to develop a bulge on each and the bulges joined by touching a soldering iron across the two pads.
- A small wire may be placed across the two pads and soldered in place.
- A SMD resistor, size 0805, 0603, or 0402, may be placed across the two pads and soldered in place. A zero-ohm resistor shorts the pads together.

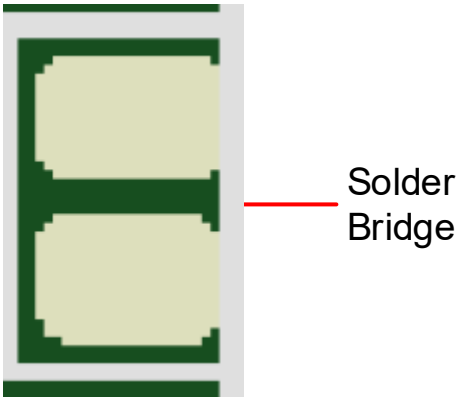

Figure 6-1: Solder Bridge

6.2.2 Trace Cut

A trace-cut jumper is provided with a narrow copper trace connecting its pads. The silk screen overlay printing around a trace-cut jumper is a solid box. To isolate the pads, cut the trace between pads adjacent to each pad, then remove the connecting copper foil either mechanically or with the assistance of heat. Once the etched copper trace is removed, the trace-cut jumper is turned into a solder-bridge jumper for any later changes.

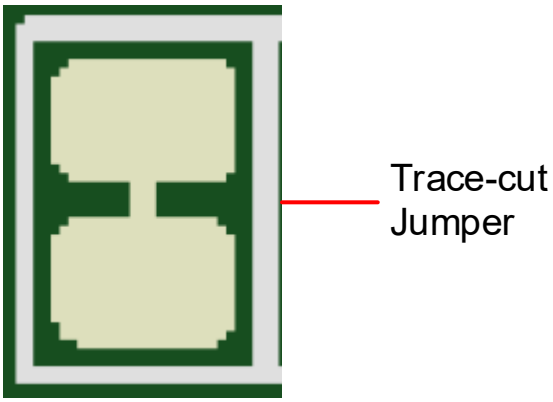

Figure 6-2: Trace Cut

6.2.3 Default Solder Bridge Jumper and Trace Cut Settings

The following table describes the default settings for solder bridge jumper and trace cut on the CPU board.

Table 6-1: Default Solder Bridge Jumper and Trace Cut Settings

Reference	Jumper Position	Explanation
E1	**Open**	**When using the Pmod™ module with a 3.3V power supply. (J26)**
	Closed	When using the Pmod™ module with a 5.0V power supply. (J26) Cannot be closed at the same time as E25.
E2	**Open**	**When the Pmod™ module of the I²C interface is not used. (J26)**
	Closed	When using the Pmod™ module of the I²C interface. (J26) Cannot be closed at the same time as E23.
E3	**Open**	**When the Pmod™ module of the I²C interface is not used. (J26)**
	Closed	When using the Pmod™ module of the I²C interface. (J26) Cannot be closed at the same time as E24.
E4	**Closed**	**When supplying 3.3V to the J-Link® OB circuit**
E23	Open	When the Pmod™ module of the SPI interface is not used. (J26)
	Closed	**When using the Pmod™ module of the SPI interface. (J26) Cannot be closed at the same time as E2.**
E24	Open	When the Pmod™ module of the SPI interface is not used. (J26)
	Closed	**When using the Pmod™ module of the SPI interface. (J26) Cannot be closed at the same time as E3.**
E25	Open	When using the Pmod™ module with a 5V power supply.
	Closed	**When using the Pmod™ module with a 3.3V power supply. Cannot be closed at the same time as E1.**
E30	**Closed**	**When connecting to emulator.**
E32	**Closed**	**When using push switch of NMI.**
E46	**Open**	**When the external clock is not input from the application header (JA2-A).**
	Closed	When inputting the external clock from the application header (JA2-A).

6.2.4 Traditional Pin Header Jumpers

These jumpers are traditional small pitch jumpers that require an external shunt to open/close them. The following table describes the default settings for traditional pin header jumpers on the CPU board.

Table 6-2: Default Pin Header Jumper Settings

Reference	Jumper Position	Explanation
CN8	Short 1-2	When using Octa Flash
	Short 2-3	**When using QSPI Serial Flash**
CN17	Short 1-2	When using VCC1833_2 domain at 3.3V
	Short 2-3	**When using VCC1833_2 domain at 1.8V**
CN18	**Short 1-2**	**When using 3 ports in the same PHY mode**
	Short 2-3	When ports 0 and 1 use the same PHY mode and port 2 uses different PHY modes
CN19	**Short 1-2**	**When using 3 ports in the same PHY mode**
	Short 2-3	When ports 0 and 1 use the same PHY mode and port 2 uses different PHY modes
CN20	**Short 1-2**	**When using 3 ports in the same PHY mode**
	Short 2-3	When ports 0 and 1 use the same PHY mode and port 2 uses different PHY modes
CN21	**Short 1-2**	**When using the RS485 transmission method in full duplex**
	Short 2-3	When using the RS485 transmission method in half duplex
CN22	**Short 1-2**	**When using the RS485 transmission method in full duplex**
	Short 2-3	When using the RS485 transmission method in half duplex
CN23	**Short 1-2**	**When not using CS5#**
	Short 2-3	When using CS5#
J9	**Open**	**When using the J-Link® OB**
	Short	When using the external emulator or not using the emulator

6.3 MPU Operating Modes

Table 6-3 and Table 6-4 and Table 6-5 below details the option links associated with configuring the MPU Operating Modes.

Table 6-3: MPU Operating Modes Switch Settings (1)

SW4-1 (MD0)	SW4-2 (MD1)	SW4-3 (MD2)	Explanation
ON	**ON**	**ON**	**xSPI0 boot mode (x1 boot Serial flash)**
OFF	ON	ON	xSPI0 boot mode (x8 boot Serial flash) *1
ON	OFF	ON	16-bit bus boot mode (NOR flash)
OFF	OFF	ON	32-bit bus boot mode (NOR flash) *1
ON	ON	OFF	xSPI1 boot mode (x1 boot Serial flash) *1
OFF	ON	OFF	SCI (UART) boot mode
ON	OFF	OFF	USB boot mode
OFF	OFF	OFF	Reserved (setting prohibited)

*1: Not supported on this board.

Table 6-4: MPU Operating Modes Switch Settings (2)

SW4-4 (MDD)	Explanation
ON	**JTAG Authentication by Hash is disabled.**
OFF	JTAG Authentication by Hash mode

Table 6-5: MPU Operating Modes Switch Settings (3)

SW4-5 (MDW)	Explanation
ON	ACTM 0 wait Valid for CPU operating frequency equal to or less than 400MHz
OFF	**ACTM 1 wait**

6.4 Emulator Configuration

6.4.1 External Emulator

Table 6-6 and Table 6-7 below details the function of the option links associated with External Emulator Configuration.

Table 6-6: External Emulator Configuration Option Links (1)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
TMS	H3	P02_6	**TMS**	**-**	**-**	**J20.2**	**-**	**-**
						CN9.17	**-**	**-**
						J13.2	**-**	**-**
						U7.30	**R35**	**-**
						CN2.3	**-**	**-**
TCK	J2	P02_7	**TCK**	**-**	**-**	**J20.4**	**-**	**-**
						CN9.15	**-**	**-**
						J13.4	**-**	**-**
						U7.40	**R23**	**-**
						CN2.4	**-**	**-**
TDO	G3	P02_4	**TDO**	**-**	**-**	**J20.6**	**-**	**-**
						CN9.11	**-**	**-**
						J13.6	**-**	**-**
						U7.23	**-**	**-**
TDI	H2	P02_5	**TDI**	**-**	**-**	**J20.8**	**-**	**-**
						CN9.19	**-**	**-**
						J13.8	**-**	**-**
						U7.17	**-**	**-**
						CN2.2	**-**	**-**
TRST#	G2	-	**POWER_RESET#**	**-**	**-**	**IC4.2**	**-**	**-**
						IC38.11	**-**	**-**
			TRST_OUT#	**-**	**-**	**J20.16**	**-**	**-**
						CN9.21	**-**	**-**
RESET#	T5	-	**POWER_RESET#**	**-**	**-**	**IC4.2**	**-**	**-**
						IC38.11	**-**	**-**
			RESET_SW#	**-**	**-**	**S3**	**-**	**-**
						U7.28	**-**	**-**
						J13.10	**-**	**-**
						J20.10	**-**	**-**
						CN9.9	**-**	**-**
BSC_D09_ TRACE_CLK	F9	P22_2	BSC_D09	IC28.16 (SW6-1 = ON)	-	IC22.F3	-	-
						IC23.44	-	-
						JA3-A.30	-	-
			TRACE_CLK	**IC28.17 (SW6-1 = OFF)**	**-**	**CN9.6**	**-**	**-**
BSC_D08_ TRACE_CTL	C7	P22_1	BSC_D08	IC28.42 (SW6-1 = ON)	-	IC22.H2	-	-
						IC23.42	-	-
						JA3-A.29	-	-
			M2_POE	IC28.41 (SW6-1 = OFF) SW6-4 = ON	SW6-3 = OFF	JA5-A.16	-	-
			TRACE_CTL	**IC28.41 (SW6-1 = OFF) SW6-3 = ON**	**SW6-4 = OFF**	**CN9.36**	**-**	**-**
BSC_D07_ TRACE_D7	B6	P22_0	BSC_D07	IC28.11 (SW6-1 = ON)	-	IC22.G7	-	-
						IC23.13	-	-
						JA3-A.24	-	-
			TRACE_D7	**IC28.12 (SW6-1 = OFF)**	**-**	**CN9.16**	**-**	**-**
						CN3.8	**-**	**-**

Table 6-7: External Emulator Configuration Option Links (2)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
BSC_D06_ TRACE_D6	B7	P21_7	BSC_D06	IC28.47 (SW6-1 = ON)	-	IC22.E6	-	-
						IC23.11	-	-
						JA3-A.23	-	-
			TRACE_D6	**IC28.46 (SW6-1 = OFF)**	-	**CN9.18**	-	-
						CN3.7	-	-
BSC_A10_M	K1	P03_7	BSC_A10	IC29.16 (SW6-1 = ON)	-	IC22.C6	-	-
						IC23.34	-	-
						JA3-A.11	-	-
			TRACE_D5	**IC29.17 (SW6-1 = OFF)**	-	**CN9.20**	-	-
BSC_D04_ TRACE_D4	A7	P21_5	BSC_D04	IC28.50 (SW6-1 = ON)	-	IC22.F5	-	-
						IC23.8	-	-
						JA3-A.21	-	-
			TRACE_D4	**IC28.49 (SW6-1 = OFF)**	-	**CN9.22**	-	-
						CN3.13	-	-
BSC_D03_ TRACE_D3	A6	P21_4	BSC_D03	IC28.5 (SW6-1 = ON)	-	IC22.F4	-	-
						IC23.7	-	-
						JA3-A.20	-	-
			TRACE_D3	**IC28.6 (SW6-1 = OFF)**	-	**CN9.24**	-	-
						CN3.16	-	-
BSC_D02_ TRACE_D2	B8	P21_3	BSC_D02	IC28.53 (SW6-1 = ON)	-	IC22.H3	-	-
						IC23.5	-	-
						JA3-A.19	-	-
			TRACE_D2	**IC28.52 (SW6-1 = OFF)**	-	**CN9.26**	-	-
						CN3.15	-	-
BSC_D01_ TRACE_D1	C8	P21_2	BSC_D01	IC28.2 (SW6-1 = ON)	-	IC22.E3	-	-
						IC23.4	-	-
						JA3-A.18	-	-
			TRACE_D1	**IC28.3 (SW6-1 = OFF)**	-	**CN9.28**	-	-
						CN3.18	-	-
BSC_D00_ TRACE_D0	B9	P21_1	BSC_D00	IC28.56 (SW6-1 = ON)	-	IC22.G2	-	-
						IC23.2	-	-
						JA3-A.17	-	-
			TRACE_D0	**IC28.55 (SW6-1 = OFF)**	-	**CN9.38**	-	-
						CN3.17	-	-

Table 6-8 and Table 6-9 below details the function of the switches associated with the External Emulator.

Table 6-8: External Emulator Configuration Switch Settings (1)

SW6-1	Explanation
ON	Enable the external bus signal.
OFF	**Enables signals other than the external bus. (CAN, Emulator, I²C, etc.)**

Table 6-9: External Emulator Configuration Switch Settings (2)

SW6-4	SW6-3	Explanation
ON	OFF	Enable the "M2_POE" signal.
OFF	**ON**	**Enable the "TRACE_CTL" signal.**

Table 6-10 below details the function of the jumpers associated with the External Emulator.

Table 6-10: External Emulator Configuration Jumper Settings

Reference	Jumper Position	Explanation
J9	Short	Enable the External Emulator.
	Open	**Enable the J-Link® OB.**

6.4.2 J-Link® OB

Table 6-11 below details the function of the option links associated with J-Link® OB Configuration.

Table 6-11: J-Link® OB Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
TMS	H3	P02_6	TMS	-	-	J20.2	-	-
						CN9.17	-	-
						J13.2	-	-
						U7.30	R35	-
						CN2.3	-	-
TCK	J2	P02_7	TCK	-	-	J20.4	-	-
						CN9.15	-	-
						J13.4	-	-
						U7.40	R23	-
						CN2.4	-	-
TDO	G3	P02_4	TDO	-	-	J20.6	-	-
						CN9.11	-	-
						J13.6	-	-
						U7.23	-	-
TDI	H2	P02_5	TDI	-	-	J20.8	-	-
						CN9.19	-	-
						J13.8	-	-
						U7.17	-	-
						CN2.2	-	-
TRST#	G2	-	POWER_RESET#	-	-	IC4.2	-	-
						IC38.11	-	-
			TRST_OUT#	-	-	J20.16	-	-
						CN9.21	-	-
RESET#	T5	-	POWER_RESET#	-	-	IC4.2	-	-
						IC38.11	-	-
			RESET_SW#	-	-	S3	-	-
						U7.28	-	-
						J13.10	-	-
						J20.10	-	-
						CN9.9	-	-

Table 6-12 below details the function of the jumpers associated with the J-Link® OB.

Table 6-12: J-Link® OB Configuration Jumper Settings

Reference	Jumper Position	Explanation
J9	Short	Enable the External Emulator.
	Open	**Enable the J-Link® OB.**

6.5 Power Supply Configuration

Table 6-13 below details the function of the option links associated with Power Supply Configuration.

Table 6-13: Power Supply Configuration Option Links

Reference	Explanation	Fit	DNF
5.0V	**Connect 5V Power rail to 5.0V.**	-	-
CON_5V	**Connect 5V Power rail to CON_5V.**	**R133**	-
3.3V	**Connect 3.3V Power rail to 3.3V.**	-	-
CON_3V3	**Connect 3.3V Power rail to CON_3V3.**	**R134**	-
+3V3JLOB	**Connect 3.3V Power rail to +3V3JLOB.**	**E4**	-
1.8V	**Connect 1.8V Power rail to 1.8V.**	-	-
VCC11_RZCORE	**Connect 1.1V Power rail to VCC11_RZCORE.**	-	-
ETH_VDD10	**Connect 1.0V Power rail to ETH_VDD10.**	-	-
ETH_VDD25	**Connect 2.5V Power rail to ETH_VDD25.**	-	-
VCC1833_0	**Connect 1.8V Power rail to VCC1833_0.**	-	-
VCC1833_1	**Connect 1.8V Power rail to VCC1833_1.**	-	-
VCC1833_2	Connect 3.3V Power rail to VCC1833_2.	CN17 (1-2 pin short)	-
	Connect 1.8V Power rail to VCC1833_2.	**CN17 (2-3 pin short)**	-
VCC1833_3	**Connect 1.8V Power rail to VCC1833_3.**	-	-
VCC1833_4	**Connect 1.8V Power rail to VCC1833_4.**	-	-
VCC18_PLL0	**Connect 1.8V Power rail to VCC18_PLL0.**	-	-
VCC18_PLL1	**Connect 1.8V Power rail to VCC18_PLL1.**	-	-
VCC18_TSU	**Connect 1.8V Power rail to VCC18_TSU.**	-	-
VCC18_ADC0	**Connect 1.8V Power rail to VCC18_ADC0.**	**R158**	-
VCC18_ADC1	**Connect 1.8V Power rail to VCC18_ADC1.**	**R159**	-

Table 6-14 below details the function of the jumpers associated with the Power Supply.

Table 6-14: Power Supply Configuration Jumper Settings

Reference	Jumper Position	Explanation
CN17	Shorted Pin 1-2	Connect 3.3V Power rail to VCC1833_2. (When using SDRAM)
	Shorted Pin 2-3	**Connect 1.8V Power rail to VCC1833_2. (When using Ethernet port 2)**

6.6 Clock Configuration

Table 6-15 below details the function of the option links associated with Clock Configuration.

Table 6-15: Clock Configuration Option Links

Reference	Explanation	Solder, FIT	De-solder, DNF
XIN, XOUT	Connect 25MHz crystal (X3) to RZ/T2M.	R242, R244	R288
EXTCLKIN	**Connect 25MHz crystal (X1) via a clock generator (IC24) to RZ/T2M.**	**R160, R245**	**E46, R246**
	Connect JA2-A.2 to RZ/T2M.	E46	R245, R246

6.7 Analog Power & ADC Configuration

Table 6-16 below details the function of the option links associated with Analog Power & ADC Configuration.

Table 6-16: Analog Power & ADC Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
ADC_AN000	B17	-	**ADC_AN000**	**-**	**-**	**JA1-A.9**	**-**	**-**
ADC_AN001	C16	-	**ADC_AN001**	**-**	**-**	**JA1-A.10**	**-**	**-**
ADC_AN002	A18	-	**ADC_AN002**	**-**	**-**	**JA1-A.11**	**-**	**-**
ADC_AN003	E16	-	**ADC_AN003**	**-**	**-**	**JA1-A.12**	**-**	**-**
ADC_AN004	A19	-	**ADC_AN004**	**-**	**-**	**JA5-A.1**	**-**	**-**
ADC_AN005	C17	-	**ADC_AN005**	**-**	**-**	**JA5-A.2**	**-**	**-**
ADC_AN006	B18	-	**ADC_AN006**	**-**	**-**	**JA5-A.3**	**-**	**-**
ADC_AN007	B19	-	**ADC_AN007**	**-**	**-**	**JA5-A.4**	**-**	**-**
ADC_AN100	F13	-	**ADC_AN100**	**-**	**-**	**J21.1**	**-**	**-**
ADC_AN101	B16	-	**ADC_AN101**	**-**	**-**	**J28.1**	**-**	**-**
ADC_AN102	E13	-	**ADC_AN102**	**-**	**-**	**J28.2**	**-**	**-**
ADC_AN115	C12	-	**ADC_AN115**	**-**	**-**	**R5**	**-**	**-**
VCC18_ADC0	F14	-	**VCC18_ADC0**	**L11**	**-**	**-**	**-**	**-**
			CON_AVCC	R140	-	-	-	-
VCC18_ADC1	F11	-	**VCC18_ADC1**	**L12**	**-**	**-**	**-**	**-**
VREFH0	C15	-	**VCC18_ADC0**	**L11, R158**	**R143, R140**	**-**	**-**	**-**
			CON_AVREF	R143	R158, **R140**	-	-	-
			CON_AVCC	R140, **R158**	**R143**	-		
VREFH1	C14	-	**VCC18_ADC1**	**L12, R159**	**-**	**-**	**-**	**-**

6.8 External BUS & NOR Flash Configuration

Table 6-17, Table 6-18, Table 6-19, Table 6-20 below details the function of the option links associated with External BUS & NOR Flash Configuration.

Table 6-17: External BUS & NOR Flash Configuration Option Links (1)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
BSC_A25_M	Y2	P08_1	BSC_A25	IC12.42 (SW6-1 = ON)	-	IC22.F8	-	-
BSC_A24_ETHSW_LPI0	V5	P08_0	BSC_A24	IC12.11 (SW6-1 = ON)	-	IC22.B5	-	-
			ETHSW_LPI0	**IC12.12 (SW6-1 = OFF)**	**-**	**CN2.1**	**-**	**-**
BSC_A23_M	W3	P07_7	BSC_A23	IC12.47 (SW6-1 = ON)	-	IC22.D8	-	-
BSC_A22_M	R6	P07_6	BSC_A22	IC12.8 (SW6-1 = ON)	-	IC22.C8	-	-
						JA3-A.43	-	-
BSC_A21_M	V4	P07_5	BSC_A21	IC12.50 (SW6-1 = ON)	-	IC22.C5	-	-
						JA3-A.42	-	-
BSC_A20_ENCIF0	E2	P01_6	BSC_A20	IC12.5 (SW6-1 = ON)	-	IC22.B6	-	-
						JA3-A.41	-	-
			ENCIF0	**IC12.6 (SW6-1 = OFF)**	**-**	**CN1.1**	**-**	**-**
BSC_A19_ADTRG	F2	P01_7	BSC_A19	IC12.53 (SW6-1 = ON)	-	IC22.C3	-	-
						JA3-A.40	-	-
			ADTRG_ENCIF_RSPCK	**IC12.52 (SW6-1 = OFF)**	**-**	**CN1.2**	**-**	**-**
						JA1-A.8	**-**	**-**
BSC_A18_ENCIF2	J6	P02_0	BSC_A18	IC12.2 (SW6-1 = ON)	-	IC22.D3	-	-
						JA3-A.39	-	-
			ENCIF2	**IC12.3 (SW6-1 = OFF)**	**-**	**CN1.3**	**-**	**-**
BSC_A17_MDW	F1	P02_1	BSC_A17	IC12.56 (SW6-1 = ON)	-	IC22.E8	-	-
						JA3-A.38	-	-
			BSC_A17_MDW	**-**	**-**	**SW4.5**	**IC14.9**	**-**
BSC_A16_M2_ENCZ	J5	P02_2	BSC_A16	IC29.25 (SW6-1 = ON)	-	IC22.B8	-	-
						JA3-A.37	-	-
			M2_ENCZ	**IC29.26 (SW6-1 = OFF)**	**-**	**CN1.4**	**-**	**-**
						JA5-A.9	**-**	**-**
BSC_A15_ENCIF4	G1	P02_3	BSC_A15	IC29.33 (SW6-1 = ON)	-	IC22.D7	-	-
						IC23.21	-	-
						JA3-A.16	-	-
			ENCIF4	**IC29.32 (SW6-1 = OFF)**	**-**	**CN1.6**	**-**	**-**
BSC_A14_ENCIF8	K6	P03_0	BSC_A14	IC29.22 (SW6-1 = ON)	-	IC22.C7	-	-
						IC23.20	-	-
						JA3-A.15	-	-
			ENCIF8	**IC29.23 (SW6-1 = OFF)**	**-**	**CN1.11**	**-**	**-**
BSC_A13_M	J3	P03_2	BSC_A13	IC29.36 (SW6-1 = ON)	-	IC22.B7	-	-
						IC23.36	-	-
						JA3-A.14	-	-
BSC_A12_M1_TOG	K2	P03_5	BSC_A12	IC29.19 (SW6-1 = ON)	-	IC22.A7	-	-
						IC23.35	-	-
						JA3-A.13	-	-
			M1_TOG	**IC29.20 (SW6-1 = OFF)**	**-**	**JA6.13**	**-**	**-**

Table 6-18: External BUS & NOR Flash Configuration Option Links (2)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
BSC_A11_M1_UP	L3	P03_6	BSC_A11	IC29.39 (SW6-1 = ON)	-	IC22.D6	-	-
						IC23.22	-	-
						JA3-A.12	-	-
			M1_UP	**IC29.38 (SW6-1 = OFF)**	**SW5-10 = OFF**	**CN3.14**	**-**	**-**
						JA2-A.13	**-**	**-**
BSC_A10_M	K1	P03_7	BSC_A10	IC29.16 (SW6-1 = ON)	-	IC22.C6	-	-
						IC23.34	-	-
						JA3-A.11	-	-
			TRACE_D5	**IC29.17 (SW6-1 = OFF)**	**-**	**CN9.20**	**-**	**-**
BSC_A09_M	L2	P04_0	BSC_A09	IC29.42 (SW6-1 = ON)	-	IC22.A6	-	-
						IC23.33	-	-
						JA3-A.10	-	-
BSC_A08_M	L5	P04_4	BSC_A08	IC29.11 (SW6-1 = ON)	-	IC22.A2	-	-
						IC23.32	-	-
						JA3-A.9	-	-
			ENCIF10	**IC29.12 (SW6-1 = OFF)**	**-**	**CN1.13**	**-**	**-**
BSC_A07_MD0_RS485_DE	N1	P04_5	BSC_A07	IC29.47 (SW6-1 = ON)	-	IC22.B2	-	-
						IC23.31	-	-
						JA3-A.8	-	-
			RS485_DE	**IC29.46 (SW6-1 = OFF)**	**-**	**IC27.5**	**-**	**-**
			BSC_A07_MD0_ RS485_DE	**-**	**-**	**SW4.1**	**IC14.18**	**-**
BSC_A06_MD1	M5	P04_6	BSC_A06	IC29.8 (SW6-1 = ON)	-	IC22.C2	-	-
						IC23.30	-	-
						JA3-A.7	-	-
			BSC_A06_MD1	**-**	**-**	**SW4.2**	**IC14.16**	**-**
BSC_A05_MD2	N2	P04_7	BSC_A05	IC29.50 (SW6-1 = ON)	-	IC22.D2	-	-
						IC23.29	-	-
						JA3-A.6	-	-
			BSC_A05_MD2	**-**	**-**	**SW4.3**	**IC14.14**	**-**
BSC_A04_M	M6	P05_0	BSC_A04	IC29.5 (SW6-1 = ON)	-	IC22.B1	-	-
						IC23.26	-	-
						JA3-A.5	-	-
BSC_A03_ENCIF12	N3	P05_1	BSC_A03	IC29.53 (SW6-1 = ON)	-	IC22.C1	-	-
						IC23.25	-	-
						JA3-A.4	-	-
			ENCIF12	**IC29.52 (SW6-1 = OFF)**	**-**	**CN1.16**	**-**	**-**
BSC_A02_CAN_RX	P3	P05_2	BSC_A02	IC29.2 (SW6-1 = ON)	-	IC22.D1	-	-
						IC23.24	-	-
						JA3-A.3	-	-
			CAN_RX	**IC29.3 (SW6-1 = OFF)**	**-**	**CN1.17**	**-**	**-**
			CAN_RX_JA5	IC29.3 (SW6-1 = OFF), SW6-9 =ON	SW6-10 = OFF	JA5-A.6	-	-
			CAN_RX_OB	IC29.3 (SW6-1 = OFF), SW6-10 = ON	SW6-9 = OFF	U10.4	-	-

Table 6-19: External BUS & NOR Flash Configuration Option Links (3)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
BSC_A01_CAN_TX	P2	P05_3	BSC_A01	IC29.56 (SW6-1 = ON)	-	IC22.E1	-	-
						IC23.23	-	-
						JA3-A.2	-	-
			CAN_TX	**IC29.55 (SW6-1 = OFF)**	**-**	**CN1.18**	**-**	**-**
						JA5-A.5	**-**	**-**
						U10.1	**-**	**-**
BSC_D15_M	A3	P23_0	BSC_D15	IC28.25 (SW6-1 = ON)	-	IC22.F7	-	-
						IC23.53	-	-
						JA3-A.36	-	-
BSC_D14_SDA1	C6	P22_7	BSC_D14	IC28.33 (SW6-1 = ON)	-	IC22.H7	-	-
						IC23.51	-	-
						JA3-A.35	-	-
			I2C_SDA_A	**IC28.32 (SW6-1 = OFF)**	-	**J27.2**	**-**	**-**
						J30.3	**-**	**-**
						J22.6	**-**	**-**
						JA1-A.25	**-**	**-**
						J26.4	**E3**	**E24**
BSC_D13_SCL1	E7	P22_6	BSC_D13	IC28.22 (SW6-1 = ON)	-	IC22.F6	-	-
						IC23.50	-	-
						JA3-A.34	-	-
			I2C_SCL_A	**IC28.23 (SW6-1 = OFF)**	**-**	**J27.1**	**-**	**-**
						J30.4	**-**	**-**
						J22.5	**-**	**-**
						JA1-A.26	**-**	**-**
						J26.3	**E2**	**E23**
BSC_D12_M	B5	P22_5	BSC_D12	IC28.36 (SW6-1 = ON)	-	IC22.G6	-	-
						IC23.48	-	-
						JA3-A.33	-	-
BSC_D11_M	E8	P22_4	BSC_D11	IC28.19 (SW6-1 = ON)	-	IC22.H4	-	-
						IC23.47	-	-
						JA3-A.32	-	-
BSC_D10_ENCIF11	A4	P22_3	BSC_D10	IC28.39 (SW6-1 = ON)	-	IC22.G3	-	-
						IC23.45	-	-
						JA3-A.31	-	-
			ENCIF11	**IC28.38 (SW6-1 = OFF)**	**-**	**CN1.14**	**-**	**-**
BSC_D09_TRACE_CLK	F9	P22_2	BSC_D09	IC28.16 (SW6-1 = ON)	-	IC22.F3	-	-
						IC23.44	-	-
						JA3-A.30	-	-
			TRACE_CLK	**IC28.17 (SW6-1 = OFF)**	**-**	**CN9.6**	**-**	**-**
BSC_D08_TRACE_CTL	C7	P22_1	BSC_D08	IC28.42 (SW6-1 = ON)	-	IC22.H2	-	-
						IC23.42	-	-
						JA3-A.29	-	-
			M2_POE	IC28.41 (SW6-1 = OFF) SW6-4 = ON	SW6-3 = OFF	JA5-A.16	-	-
			TRACE_CTL	IC28.41 (SW6-1 = OFF) SW6-3 = ON	SW6-4 = OFF	CN9.36	-	-
BSC_D07_TRACE_D7	B6	P22_0	BSC_D07	IC28.11 (SW6-1 = ON)	-	IC22.G7	-	-
						IC23.13	-	-
						JA3-A.24	-	-
			TRACE_D7	**IC28.12 (SW6-1 = OFF)**	**-**	**CN9.16**	**-**	**-**
						CN3.8	**-**	**-**
BSC_D06_TRACE_D6	B7	P21_7	BSC_D06	IC28.47 (SW6-1 = ON)	-	IC22.E6	-	-
						IC23.11	-	-
						JA3-A.23	-	-
			TRACE_D6	**IC28.46 (SW6-1 = OFF)**	**-**	**CN9.18**	**-**	**-**
						CN3.7	**-**	**-**

Table 6-20: External BUS & NOR Flash Configuration Option Links (4)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
BSC_D05_GTIOC16B	E9	P21_6	BSC_D05	IC28.8 (SW6-1 = ON)	-	IC22.H6	-	-
						IC23.10	-	-
						JA3-A.22	-	-
			GTIOC16B	**IC28.9 (SW6-1 = OFF)**	**-**	**CN2.6**	**-**	**-**
BSC_D04_TRACE_D4	A7	P21_5	BSC_D04	IC28.50 (SW6-1 = ON)	-	IC22.F5	-	-
						IC23.8	-	-
						JA3-A.21	-	-
			TRACE_D4	**IC28.49 (SW6-1 = OFF)**	**-**	**CN9.22**	**-**	**-**
						CN3.13	**-**	**-**
BSC_D03_TRACE_D3	A6	P21_4	BSC_D03	IC28.5 (SW6-1 = ON)	-	IC22.F4	-	-
						IC23.7	-	-
						JA3-A.20	-	-
			TRACE_D3	**IC28.6 (SW6-1 = OFF)**	**-**	**CN9.24**	**-**	**-**
						CN3.16	**-**	**-**
BSC_D02_TRACE_D2	B8	P21_3	BSC_D02	IC28.53 (SW6-1 = ON)	-	IC22.H3	-	-
						IC23.5	-	-
						JA3-A.19	-	-
			TRACE_D2	**IC28.52 (SW6-1 = OFF)**	**-**	**CN9.26**	**-**	**-**
						CN3.15	**-**	**-**
BSC_D01_TRACE_D1	C8	P21_2	BSC_D01	IC28.2 (SW6-1 = ON)	-	IC22.E3	-	-
						IC23.4	-	-
						JA3-A.18	-	-
			TRACE_D1	**IC28.3 (SW6-1 = OFF)**	**-**	**CN9.28**	**-**	**-**
						CN3.18	**-**	**-**
BSC_D00_TRACE_D0	B9	P21_1	BSC_D00	IC28.56 (SW6-1 = ON)	-	IC22.G2	-	-
						IC23.2	-	-
						JA3-A.17	-	-
			TRACE_D0	**IC28.55 (SW6-1 = OFF)**	**-**	**CN9.38**	**-**	**-**
						CN3.17	**-**	**-**
BSC_CS0#	M2	P04_2	**BSC_CS0#**	**-**	**-**	**IC22.F1**	**-**	**-**
BSC_RD#	M3	P04_3	**BSC_RD#**	**-**	**-**	**IC22.F2**	**-**	**-**
						JA3-A.25	**-**	**-**
BSC_DQMLL_M	E6	P23_1	BSC_DQMLL_WE0#	IC12.22 (SW6-1 = ON)	-	IC22.A5	-	-
						IC23.15	-	-
						JA3-A.48	-	-

Table 6-21 below details the function of the switches associated with the NOR Flash.

Table 6-21: External BUS & NOR Flash Configuration Switch Settings

SW6-1	Explanation
ON	Enable the external bus signal.
OFF	**Enables signals other than the external bus. (CAN, Emulator, I²C, etc.)**

6.9 External BUS & SDRAM Configuration

Table 6-22, Table 6-23, Table 6-24, Table 6-25 below details the function of the option links associated with External BUS & SDRAM Configuration.

Table 6-22: External BUS & SDRAM Configuration Option Links (1)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
BSC_A15_ENCIF4	G1	P02_3	BSC_A15	IC29.33 (SW6-1 = ON)	-	IC22.D7	-	-
						IC23.21	-	-
						JA3-A.16	-	-
			ENCIF4	**IC29.32 (SW6-1 = OFF)**	**-**	**CN1.6**	**-**	**-**
BSC_A14_ENCIF8	K6	P03_0	BSC_A14	IC29.22 (SW6-1 = ON)	-	IC22.C7	-	-
						IC23.20	-	-
						JA3-A.15	-	-
			ENCIF8	**IC29.23 (SW6-1 = OFF)**	**-**	**CN1.11**	**-**	**-**
BSC_A13_M	J3	P03_2	BSC_A13	IC29.36 (SW6-1 = ON)	-	IC22.B7	-	-
						IC23.36	-	-
						JA3-A.14	-	-
BSC_A12_M1_TOG	K2	P03_5	BSC_A12	IC29.19 (SW6-1 = ON)	-	IC22.A7	-	-
						IC23.35	-	-
						JA3-A.13	-	-
			M1_TOG	**IC29.20 (SW6-1 = OFF)**	**-**	**JA6.13**	**-**	**-**
BSC_A11_M1_UP	L3	P03_6	BSC_A11	IC29.39 (SW6-1 = ON)	-	IC22.D6	-	-
						IC23.22	-	-
						JA3-A.12	-	-
			M1_UP	**IC29.38 (SW6-1 = OFF)**	**SW5-10 = OFF**	**CN3.14**	**-**	**-**
						JA2-A.13	**-**	**-**
BSC_A10_M	K1	P03_7	BSC_A10	IC29.16 (SW6-1 = ON)	-	IC22.C6	-	-
						IC23.34	-	-
						JA3-A.11	-	-
			TRACE_D5	**IC29.17 (SW6-1 = OFF)**	**-**	**CN9.20**	**-**	**-**
BSC_A09_M	L2	P04_0	BSC_A09	IC29.42 (SW6-1 = ON)	-	IC22.A6	-	-
						IC23.33	-	-
						JA3-A.10	-	-
BSC_A08_M	L5	P04_4	BSC_A08	IC29.11 (SW6-1 = ON)	-	IC22.A2	-	-
						IC23.32	-	-
						JA3-A.9	-	-
			ENCIF10	**IC29.12 (SW6-1 = OFF)**	**-**	**CN1.13**	**-**	**-**
BSC_A07_MD0_RS485_DE	N1	P04_5	BSC_A07	IC29.47 (SW6-1 = ON)	-	IC22.B2	-	-
						IC23.31	-	-
						JA3-A.8	-	-
			RS485_DE	**IC29.46 (SW6-1 = OFF)**	**-**	**IC27.5**	**-**	**-**
			BSC_A07_MD0_RS485_DE	**-**	**-**	**SW4.1**	**IC14.18**	**-**
BSC_A06_MD1	M5	P04_6	BSC_A06	IC29.8 (SW6-1 = ON)	-	IC22.C2	-	-
						IC23.30	-	-
						JA3-A.7	-	-
			BSC_A06_MD1	**-**	**-**	**SW4.2**	**IC14.16**	**-**

Table 6-23: External BUS & SDRAM Configuration Option Links (2)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
BSC_A05_MD2	N2	P04_7	BSC_A05	IC29.50 (SW6-1 = ON)	-	IC22.D2	-	-
						IC23.29	-	-
						JA3-A.6	-	-
			BSC_A05_MD2	**-**	**-**	**SW4.3**	**IC14.14**	**-**
BSC_A04_M	M6	P05_0	BSC_A04	IC29.5 (SW6-1 = ON)	-	IC22.B1	-	-
						IC23.26	-	-
						JA3-A.5	-	-
BSC_A03_ENCIF12	N3	P05_1	BSC_A03	IC29.53 (SW6-1 = ON)	-	IC22.C1	-	-
						IC23.25	-	-
						JA3-A.4	-	-
			ENCIF12	**IC29.52 (SW6-1 = OFF)**	**-**	**CN1.16**	**-**	**-**
BSC_A02_CAN_RX	P3	P05_2	BSC_A02	IC29.2 (SW6-1 = ON)	-	IC22.D1	-	-
						IC23.24	-	-
						JA3-A.3	-	-
			CAN_RX	**IC29.3 (SW6-1 = OFF)**	**-**	**CN1.17**	**-**	**-**
			CAN_RX_JA5	IC29.3 (SW6-1 = OFF), SW6-9 =ON	SW6-10 = OFF	JA5-A.6	-	-
			CAN_RX_OB	IC29.3 (SW6-1 = OFF), SW6-10 = ON	SW6-9 = OFF	U10.4	-	-
BSC_A01_CAN_TX	P2	P05_3	BSC_A01	IC29.56 (SW6-1 = ON)	-	IC22.E1	-	-
						IC23.23	-	-
						JA3-A.2	-	-
			CAN_TX	**IC29.55 (SW6-1 = OFF)**	**-**	**CN1.18**	**-**	**-**
						JA5-A.5	**-**	**-**
						U10.1	**-**	**-**
BSC_D15_M	A3	P23_0	BSC_D15	IC28.25 (SW6-1 = ON)	-	IC22.F7	-	-
						IC23.53	-	-
						JA3-A.36	-	-
BSC_D14_SDA1	C6	P22_7	BSC_D14	IC28.33 (SW6-1 = ON)	-	IC22.H7	-	-
						IC23.51	-	-
						JA3-A.35	-	-
			I2C_SDA_A	**IC28.32 (SW6-1 = OFF)**	**-**	**J27.2**	**-**	**-**
						J30.3	**-**	**-**
						J22.6	**-**	**-**
						JA1-A.25	**-**	**-**
						J26.4	**E3**	**E24**
BSC_D13_SCL1	E7	P22_6	BSC_D13	IC28.22 (SW6-1 = ON)	-	IC22.F6	-	-
						IC23.50	-	-
						JA3-A.34	-	-
			I2C_SCL_A	**IC28.23 (SW6-1 = OFF)**	**-**	**J27.1**	**-**	**-**
						J30.4	**-**	**-**
						J22.5	**-**	**-**
						JA1-A.26	**-**	**-**
						J26.3	**E2**	**E23**
BSC_D12_M	B5	P22_5	BSC_D12	IC28.36 (SW6-1 = ON)	-	IC22.G6	-	-
						IC23.48	-	-
						JA3-A.33	-	-
BSC_D11_M	E8	P22_4	BSC_D11	IC28.19 (SW6-1 = ON)	-	IC22.H4	-	-
						IC23.47	-	-
						JA3-A.32	-	-
BSC_D10_ENCIF11	A4	P22_3	BSC_D10	IC28.39 (SW6-1 = ON)	-	IC22.G3	-	-
						IC23.45	-	-
						JA3-A.31	-	-
			ENCIF11	**IC28.38 (SW6-1 = OFF)**	**-**	**CN1.14**	**-**	**-**

Table 6-24: External BUS & SDRAM Configuration Option Links (3)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
BSC_D09_TRACE_CLK	F9	P22_2	BSC_D09	IC28.16 (SW6-1 = ON)	-	IC22.F3	-	-
						IC23.44	-	-
						JA3-A.30	-	-
			TRACE_CLK	**IC28.17 (SW6-1 = OFF)**	-	**CN9.6**	-	-
BSC_D08_TRACE_CTL	C7	P22_1	BSC_D08	IC28.42 (SW6-1 = ON)	-	IC22.H2	-	-
						IC23.42	-	-
						JA3-A.29	-	-
			M2_POE	IC28.41 (SW6-1 = OFF) SW6-4 = ON	SW6-3 = OFF	JA5-A.16	-	-
			TRACE_CTL	IC28.41 (SW6-1 = OFF) SW6-3 = ON	SW6-4 = OFF	CN9.36	-	-
BSC_D07_TRACE_D7	B6	P22_0	BSC_D07	IC28.11 (SW6-1 = ON)	-	IC22.G7	-	-
						IC23.13	-	-
						JA3-A.24	-	-
			TRACE_D7	**IC28.12 (SW6-1 = OFF)**	-	**CN9.16**	-	-
						CN3.8	-	-
BSC_D06_TRACE_D6	B7	P21_7	BSC_D06	IC28.47 (SW6-1 = ON)	-	IC22.E6	-	-
						IC23.11	-	-
						JA3-A.23	-	-
			TRACE_D6	**IC28.46 (SW6-1 = OFF)**	-	**CN9.18**	-	-
						CN3.7	-	-
BSC_D05_GTIOC16B	E9	P21_6	BSC_D05	IC28.8 (SW6-1 = ON)	-	IC22.H6	-	-
						IC23.10	-	-
						JA3-A.22	-	-
			GTIOC16B	**IC28.9 (SW6-1 = OFF)**	-	**CN2.6**	-	-
BSC_D04_TRACE_D4	A7	P21_5	BSC_D04	IC28.50 (SW6-1 = ON)	-	IC22.F5	-	-
						IC23.8	-	-
						JA3-A.21	-	-
			TRACE_D4	**IC28.49 (SW6-1 = OFF)**	-	**CN9.22**	-	-
						CN3.13	-	-
BSC_D03_TRACE_D3	A6	P21_4	BSC_D03	IC28.5 (SW6-1 = ON)	-	IC22.F4	-	-
						IC23.7	-	-
						JA3-A.20	-	-
			TRACE_D3	**IC28.6 (SW6-1 = OFF)**	-	**CN9.24**	-	-
						CN3.16	-	-
BSC_D02_TRACE_D2	B8	P21_3	BSC_D02	IC28.53 (SW6-1 = ON)	-	IC22.H3	-	-
						IC23.5	-	-
						JA3-A.19	-	-
			TRACE_D2	**IC28.52 (SW6-1 = OFF)**	-	**CN9.26**	-	-
						CN3.15	-	-
BSC_D01_TRACE_D1	C8	P21_2	BSC_D01	IC28.2 (SW6-1 = ON)	-	IC22.E3	-	-
						IC23.4	-	-
						JA3-A.18	-	-
			TRACE_D1	**IC28.3 (SW6-1 = OFF)**	-	**CN9.28**	-	-
						CN3.18	-	-
BSC_D00_TRACE_D0	B9	P21_1	BSC_D00	IC28.56 (SW6-1 = ON)	-	IC22.G2	-	-
						IC23.2	-	-
						JA3-A.17	-	-
			TRACE_D0	**IC28.55 (SW6-1 = OFF)**	-	**CN9.38**	-	-
						CN3.17	-	-
BSC_CS3#_18	N18	P14_5	**BSC_CS3#_33**	**IC13.4**	-	**IC23.19**	-	-
						JA3-A.28	-	-
BSC_RAS#_M	C1	P00_7	BSC_RAS#	IC12.16 (SW6-1 = ON)	-	IC23.18	-	-
						JA3-A.50	-	-

Table 6-25: External BUS & SDRAM Configuration Option Links (4)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
BSC_CAS#_M	E3	P01_0	BSC_CAS#	IC12.39 (SW6-1 = ON)	-	IC23.17	-	-
						JA3-A.49	-	-
			ETH2_MDIO	IC12.39 (SW6-1 = OFF), CN19 (2-3 pin short)		IC16.50	-	-
BSC_WR#_M	K5	P03_4	BSC_WR#	IC12.19 (SW6-1 = ON)	-	IC23.16	-	-
						JA3-A.26	-	-
BSC_DQMLU_M	B4	P23_2	BSC_DQMLU	IC12.36 (SW6-1 = ON)	-	IC23.39	-	-
						JA3-A.47	-	-
BSC_DQMLL_M	E6	P23_1	BSC_DQMLL_WE0#	IC12.22 (SW6-1 = ON)	-	IC22.A5	-	-
						IC23.15	-	-
						JA3-A.48	-	-
BSC_CKE_M	H6	P01_1	BSC_CKE	IC12.33 (SW6-1 = ON)	-	IC23.37	-	-
						JA3-A.46	-	-
			ETH2_MDC	IC12.32 (SW6-1 = OFF), CN18 (2-3 pin short)	-	IC16.48	-	-
BSC_CKIO_M	M1	P04_1	BSC_CKIO	IC12.25 (SW6-1 = ON) R91	-	IC23.38	-	-
						JA3-A.44	-	-

Table 6-26 below details the function of the switches associated with the SDRAM.

Table 6-26: External BUS & SDRAM Configuration Switch Settings

SW6-1	Explanation
ON	Enable the external bus signal.*1
OFF	**Enables signals other than the external bus. (CAN, Emulator, I²C, etc.)**

*1: SDRAM and Ethernet / Switch / EtherCAT port 2 cannot be used at the same time.

Table 6-27 below details the function of the jumpers associated with the SDRAM.

Table 6-27: External BUS & SDRAM Configuration Jumper Settings

Reference	Jumper Position	Explanation
CN17	Shorted Pin 1-2	Connect 3.3V Power rail to VCC1833_2. (When using SDRAM)*1
	Shorted Pin 2-3	**Connect 1.8V Power rail to VCC1833_2. (When using Ethernet port 2)**

*1: When using SDRAM, use the Ethernet switch (CN18-CN20) setting at 2-3.

6.10 CAN Configuration

Table 6-28 below details the function of the option links associated with CAN Configuration.

Table 6-28: CAN Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
BSC_A01_CAN_TX	P2	P05_3	BSC_A01	IC29.56 (SW6-1 = ON)	-	IC22.E1	-	-
						IC23.23	-	-
						JA3-A.2	-	-
			CAN_TX	**IC29.55 (SW6-1 = OFF)**	**-**	**CN1.18**	**-**	**-**
						JA5-A.5	**-**	**-**
						U10.1	**-**	**-**
BSC_A02_CAN_RX	P3	P05_2	BSC_A02	IC29.2 (SW6-1 = ON)	-	IC22.D1	-	-
						IC23.24	-	-
						JA3-A.3	-	-
			CAN_RX	**IC29.3 (SW6-1 = OFF)**	**-**	**CN1.17**	**-**	**-**
			CAN_RX_JA5	IC29.3 (SW6-1 = OFF), SW6-9 =ON	SW6-10 = OFF	JA5-A.6	-	-
			CAN_RX_OB	IC29.3 (SW6-1 = OFF), SW6-10 = ON	SW6-9 = OFF	U10.4	-	-

Table 6-29 and Table 6-30 below details the function of the switches associated with the CAN.

Table 6-29: CAN Configuration Switch Settings (1)

SW6-1	Explanation
ON	Enable the external bus signal.
OFF	**Enables signals other than the external bus. (CAN, Emulator, I²C, etc.)**

Table 6-30: CAN Configuration Switch Settings (2)

SW6-10	SW6-9	Explanation
ON	OFF	Enable the “CAN_RX_OB” signal.
OFF	ON	Enable the “CAN_RX_JA5” signal.

6.11 Ethernet Configuration

Table 6-31, Table 6-32, Table 6-33 below details the function of the option links associated with Ethernet Configuration.

Table 6-31: Ethernet Configuration Option Links (1)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
ETH0_TXCLK	R9	P09_7	ETH0_TXCLK	R103	-	IC35.37	-	-
ETH0_TXEN	W7	P10_0	ETH0_TXEN	R104	-	IC35.33	-	-
ETH0_TXD0	Y6	P09_6	ETH0_TXD0	R102	-	IC35.38	-	-
ETH0_TXD1	T9	P09_5	ETH0_TXD1	R101	-	IC35.40	-	-
ETH0_TXD2	R8	P09_4	ETH0_TXD2	R100	-	IC35.41	-	-
ETH0_TXD3	W6	P09_3	ETH0_TXD3	R99	-	IC35.42	-	-
ETH0_RXCLK	V7	P08_6	ETH0_RXCLK	-	-	IC35.32	R228	-
ETH0_RXDV	Y3	P08_5	ETH0_RXDV	-	-	IC35.30	R229	-
ETH0_RXD0	Y7	P10_1	ETH0_RXD0	-	-	IC35.29	R230	-
ETH0_RXD1	V8	P10_2	ETH0_RXD1	-	-	IC35.27	R231	-
ETH0_RXD2	V9	P10_3	ETH0_RXD2	-	-	IC35.26	R232	-
ETH0_RXD3	W4	P08_4	ETH0_RXD3	-	-	IC35.25	R233	-
ETH0_REFCLK	T8	P09_1	ETH0_REFCLK	R98	-	IC34.2	R227	-
ETH0_REFCLK_25	-	-	ETH0_REFCLK	R227	R226	IC35.63	R243	-
			ETH0_REFCLK_G*1	R226, R161	R227			

*1: In the default RSK+ configuration, ETH0_REFCLK_G signal is not connected to the XTAL1 pin of the Ethernet controller IC (IC35). If you want to connect the external clock (X1) on the RSK+ to the Ethernet controller IC, configure as shown in **Table 6-31** above.

Table 6-32: Ethernet Configuration Option Links (2)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
ETH1_TXCLK	U1	P06_4	ETH1_TXCLK	R96	-	IC31.37	-	-
ETH1_TXEN	T3	P06_5	ETH1_TXEN	R97	-	IC31.33	-	-
ETH1_TXD0	P5	P06_3	ETH1_TXD0	R95	-	IC31.38	-	-
ETH1_TXD1	T2	P06_2	ETH1_TXD1	R94	-	IC31.40	-	-
ETH1_TXD2	P6	P05_7	ETH1_TXD2	R90	-	IC31.41	-	-
ETH1_TXD3	T1	P06_0	ETH1_TXD3	R92	-	IC31.42	-	-
ETH1_RXCLK	U3	P07_3	ETH1_RXCLK	-	-	IC31.32	R205	-
ETH1_RXDV	W1	P07_2	ETH1_RXDV	-	-	IC31.30	R206	-
ETH1_RXD0	U2	P06_6	ETH1_RXD0	-	-	IC31.29	R207	-
ETH1_RXD1	V1	P06_7	ETH1_RXD1	-	-	IC31.27	R208	-
ETH1_RXD2	V2	P07_0	ETH1_RXD2	-	-	IC31.26	R209	-
ETH1_RXD3	R5	P07_1	ETH1_RXD3	-	-	IC31.25	R210	-
ETH1_REFCLK	R3	P06_1	ETH1_REFCLK	R93	-	IC30.2	R204	-
ETH1_REFCLK_25	-	-	ETH1_REFCLK	R204	R203	IC31.63	R220	-
			ETH1_REFCLK_G*1	R203, R162	R204			

*1: In the default RSK+ configuration, ETH1_REFCLK_G signal is not connected to the XTAL1 pin of the Ethernet controller IC (IC31). If you want to connect the external clock (X1) on the RSK+ to the Ethernet controller IC, configure as shown in **Table 6-32** above.

Table 6-33: Ethernet Configuration Option Links (3)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
ETH2_TXCLK	D3	P00_6	**ETH2_TXCLK**	**R85, CN23 (1-2 pin short)**	**-**	**IC16.37**	**-**	**-**
			CS5#	R85, CN23 (2-3 pin short)	-	JA3-A.27	-	R296
ETH2_TXEN	B1	P00_2	**ETH2_TXEN**	**R83**	**-**	**IC16.33**	**-**	**-**
ETH2_TXD0	F3	P01_5	**ETH2_TXD0**	**R89**	**-**	**IC16.38**	**-**	**-**
ETH2_TXD1	H5	P01_4	**ETH2_TXD1**	**R88**	**-**	**IC16.40**	**-**	**-**
ETH2_TXD2	D1	P01_3	**ETH2_TXD2**	**R87**	**-**	**IC16.41**	**-**	**-**
ETH2_TXD3	D2	P01_2	**ETH2_TXD3**	**R86**	**-**	**IC16.42**	**-**	**-**
ETH2_RXCLK	C3	P24_1	**ETH2_RXCLK**	**-**	**-**	**IC16.32**	**R105**	**-**
ETH2_RXDV	F5	P00_1	**ETH2_RXDV**	**-**	**-**	**IC16.30**	**R106**	**-**
ETH2_RXD0	B3	P23_7	**ETH2_RXD0**	**-**	**-**	**IC16.29**	**R107**	**-**
ETH2_RXD1	C4	P24_0	**ETH2_RXD1**	**-**	**-**	**IC16.27**	**R108**	**-**
ETH2_RXD2	E5	P24_2	**ETH2_RXD2**	**-**	**-**	**IC16.26**	**R109**	**-**
ETH2_RXD3	B2	P00_0	**ETH2_RXD3**	**-**	**-**	**IC16.25**	**R110**	**-**
ETH2_REFCLK	C2	P00_3	**ETH2_REFCLK**	**R84**	**-**	**IC11.2**	**R114**	**-**
ETH2_REFCLK_25	-	-	**ETH2_REFCLK**	**R114**	**R113**	**IC16.63**	**R265**	**-**
			ETH2_REFCLK_G*1	R113, R163	R114			

*1: In the default RSK+ configuration, ETH2_REFCLK_G signal is not connected to the XTAL1 pin of the Ethernet controller IC (IC16). If you want to connect the external clock (X1) on the RSK+ to the Ethernet controller IC, configure as shown in **Table 6-33** above.

Table 6-34 below details the function of the switches associated with the Ethernet.

Table 6-34: Ethernet Configuration Switch Settings

SW6-1	Explanation
ON	Enable the external bus signal and Ethernet. *1
OFF	**Enables signals other than the external bus. (CAN, Emulator, I²C, etc.)**

*1: BUS (SDRAM) and Ethernet port 2 cannot be used at the same time.

Table 6-35 and Table 6-36 below details the function of the jumpers associated with the Ethernet.

Table 6-35: Ethernet Configuration Jumper Settings (1)

Reference	Jumper Position	Explanation
CN17	Shorted Pin 1-2	Connect 3.3V Power rail to VCC1833_2. (When using SDRAM)
	Shorted Pin 2-3	**Connect 1.8V Power rail to VCC1833_2. (When using Ethernet port 2)**

Table 6-36: Ethernet Configuration Jumper Settings (2)

Reference	Jumper Position	Explanation
CN18, CN19, CN20	**Shorted Pin 1-2**	**When using 3 ports in the same PHY mode**
	Shorted Pin 2-3	When ports 0 and 1 use the same PHY mode and port 2 uses different PHY modes

*: When using VCC1833_2 at 3.3 V, use a jumper setting of 2-3.

6.12 Ethernet Switch Configuration

Table 6-31, Table 6-32, Table 6-33, Table 6-37 below details the function of the option links associated with Ethernet Switch (ETHSW) Configuration.

Table 6-37: ETHSW Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
BSC_A24_ETHSW_LPI0	V5	P08_0	BSC_A24	IC12.11 (SW6-1 = ON)	-	IC22.B5	-	-
			ETHSW_LPI0	**IC12.12 (SW6-1 = OFF)**	**-**	**CN2.1**	**-**	**-**
BSC_A19_ADTRG	F2	P01_7	BSC_A19	IC12.53 (SW6-1 = ON)	-	IC22.C3	-	-
						JA3-A.40	-	-
			ADTRG_ENCIF_RSPCK (ETHSW_LPI1)	**IC12.52 (SW6-1 = OFF)**	**-**	**CN1.2**	**-**	**-**
						JA1-A.8	**-**	**-**
BSC_A18_ENCIF2	J6	P02_0	BSC_A18	IC12.2 (SW6-1 = ON)	-	IC22.D3	-	-
						JA3-A.39	-	-
			ENCIF2 (ETHSW_LPI2)	**IC12.3 (SW6-1 = OFF)**	**-**	**CN1.3**	**-**	**-**
P08_3 (ETHSW_PTPOUT0)	T6	P08_3	**P08_3**	**-**	**-**	**J26.9**	**-**	**-**
						CN2.8	**-**	**-**
BSC_A17_MDW	F1	P02_1	BSC_A17	IC12.56 (SW6-1 = ON)	-	IC22.E8	-	-
						JA3-A.38	-	-
			BSC_A17_MDW (ETHSW_PTPOUT1)	**-**	**-**	**SW4.5**	**IC14.9**	**-**
DIP_SW6_18 (ETHSW_PTPOUT2)	P16	P13_2	**DIP_SW6_18**	**SW3-6 = OFF**	**-**	**SW3.6**	**-**	**-**
ETH_LED5 (ETHSW_PTPOUT3)	A9	P21_0	**ETH_LED5**	**-**	**-**	**ETH_LED5.A**	**R13**	**-**
						CN3.4	**-**	**-**
BSC_A16_M2_ENCZ	J5	P02_2	BSC_A16	IC29.25 (SW6-1 = ON)	-	IC22.B8	-	-
						JA3-A.37	-	-
			M2_ENCZ (ETHSW_TDMAOUT0)	**IC29.26 (SW6-1 = OFF)**	**-**	**CN1.4**	**-**	**-**
						JA5-A.9	**-**	**-**
ETH_LED0_MDV1 (ETHSW_TDMAOUT1)	A10	P20_2	**ETH_LED0_MDV1**	**-**	**-**	**ETH_LED0.A**	**R6**	**-**
ETH_LED1_MDV2 (ETHSW_TDMAOUT2)	C9	P20_3	**ETH_LED1_MDV2**	**-**	**-**	**ETH_LED1.A**	**R7**	**-**
						IC14.7	**-**	**-**
ETH_LED3_MDV3 (ETHSW_TDMAOUT3)	B10	P20_4	**ETH_LED3_MDV3**	**-**	**-**	**ETH_LED3.A**	**R11**	**-**
ETH0_LINK	R11	P10_4	**ETH0_LINK**	**IC36.4**	**-**	**IC35.59**	**-**	**-**
ETH1_LINK	R1	P05_5	**ETH1_LINK**	**IC32.4**	**-**	**IC31.59**	**-**	**-**
ETH2_LINK	G5	P00_5	**ETH2_LINK**	**IC17.4**	**-**	**IC16.59**	**-**	**-**

Table 6-38 below details the function of the switches associated with the ETHSW.

Table 6-38: ETHSW Configuration Switch Settings

SW6-1	Explanation
ON	Enable the external bus signal. *1
OFF	**Enables signals other than the external bus. (CAN, Emulator, I²C, ETHSW, etc.)**

*1: BUS (SDRAM) and ETHSW port 2 cannot be used at the same time.

Table 6-39 and Table 6-40 below details the function of the jumpers associated with the ETHSW.

Table 6-39: ETHSW Configuration Jumper Settings (1)

Reference	Jumper Position	Explanation
CN17	Shorted Pin 1-2	Connect 3.3V Power rail to VCC1833_2. (When using SDRAM)
	Shorted Pin 2-3	**Connect 1.8V Power rail to VCC1833_2. (When using Ethernet port 2)**

Table 6-40: ETHSW Configuration Jumper Settings (2)

Reference	Jumper Position	Explanation
CN18, CN19, CN20	**Shorted Pin 1-2**	**When using 3 ports in the same PHY mode**
	Shorted Pin 2-3	When ports 0 and 1 use the same PHY mode and port 2 uses different PHY modes

*: When using VCC1833_2 at 3.3 V, use a jumper setting of 2-3.

6.13 EtherCAT Slave Controller Configuration

Table 6-31, Table 6-32, Table 6-33, Table 6-41 below details the function of the option links associated with EtherCAT Slave Controller (ESC) Configuration.

Table 6-41: ESC Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
ETH_LED0_MDV1 (ESC_LEDRUN)	A10	P20_2	ETH_LED0_MDV1	-	-	ETH_LED0.A	R6	-
ETH_LED1_MDV2 (ESC_LEDERR)	C9	P20_3	ETH_LED1_MDV2	-	-	ETH_LED1.A	R7	-
						IC14.7	-	-
ETH_LED2_MDV0 (ESC_LINKACT0)	C11	P20_1	ETH_LED2_MDV0	-	-	ETH_LED2.A	R8	-
ETH_LED3_MDV3 (ESC_LINKACT1)	B10	P20_4	ETH_LED3_MDV3	-	-	ETH_LED3.A	R11	-
ETH_LED5 (ESC_LINKACT2)	A9	P21_0	ETH_LED5	-	-	ETH_LED5.A	R13	-
						CN3.4	-	-
M1_TRDCLK_18 (ESC_SYNC0, ESC_SYNC1)	R18	P13_6	M1_TRDCLK_33	IC42.8	-	JA2-A.26	-	-
M1_TRCCLK_18 (ESC_LATCH0, ESC_LATCH1)	N16	P13_5	M1_TRCCLK_33	IC42.9	-	JA2-A.25	-	-
ESC_RESETOUT#	E10	P20_7	ETH_RESET#_18	-	-	IC35.42	-	-
			ESC_RESETOUT#	-	-	CN3.3	-	-
						IC35.53	-	-
						IC31.53	-	-
						IC16.53	CN20 (1-2 pin short)	-
ESC_B_RESETOUT#	F7	P23_7	ESC_B_RESETOUT#	-	-	IC16.53	CN20 (2-3 pin short)	-
ETH0_LINK (ESC_PHYLINK0)	R11	P10_4	ETH0_LINK	IC36.4	-	IC35.59	-	-
ETH1_LINK (ESC_PHYLINK1)	R1	P05_5	ETH1_LINK	IC32.4	-	IC31.59	-	-
ETH2_LINK (ESC_PHYLINK0)	G5	P00_5	ETH2_LINK	IC17.4	-	IC16.59	-	-

Table 6-42 below details the function of the switches associated with the ESC.

Table 6-42: ESC Configuration Switch Settings

SW6-1	Explanation
ON	Enable the external bus signal. *1
OFF	**Enables signals other than the external bus. (CAN, Emulator, I²C, etc.)**

*1: BUS (SDRAM) and ESC port 2 cannot be used at the same time.

Table 6-43 and Table 6-44 below details the function of the jumpers associated with the ESC.

Table 6-43: ESC Configuration Jumper Settings (1)

Reference	Jumper Position	Explanation
CN17	Shorted Pin 1-2	Connect 3.3V Power rail to VCC1833_2. (When using SDRAM)
	Shorted Pin 2-3	**Connect 1.8V Power rail to VCC1833_2. (When using Ethernet port 2)**

Table 6-44: ESC Configuration Jumper Settings (2)

Reference	Jumper Position	Explanation
CN18, CN19, CN20	**Shorted Pin 1-2**	**When using 3 ports in the same PHY mode**
	Shorted Pin 2-3	When ports 0 and 1 use the same PHY mode and port 2 uses different PHY modes

*: When using VCC1833_2 at 3.3 V, use a jumper setting of 2-3.

6.14 General I/O & LED Configuration

Table 6-45 below details the function of the option links associated with General I/O & LED Configuration.

Table 6-45: General I/O & LED Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
RLED0_M2_UN	D18	P19_6	**RLED0**	**R201**	**R202**	**LED0.A**	**R43**	**-**
			M2_UN	R202	R201	JA5-A.20	-	-
RLED1_M2_VP	C20	P19_4	**RLED1**	**R199**	**R200**	**LED1.A**	**R44**	**-**
			M2_VP	R200	R199	JA5-A.21	-	-
RLED2_M2_WN	B20	P20_0	**RLED2**	**R197**	**R198**	**LED2.A**	**R46**	**-**
			M2_WN	R198	R197	JA5-A.24	-	-
RLED3_ M2_TRDCLK_ CS5#	C5	P23_4	**RLED3**	**R195**	**R196, R296**	**LED3.A**	**R47**	**-**
			M2_TRDCLK	R196	R195, R296	JA5-A.18	-	-
			CS5#	R296	R195, R196	JA3-A.27	-	-
ETH_LED0_MDV1	A10	P20_2	**ETH_LED0_MDV1**	**-**	**-**	**ETH_LED0.A**	**R6**	**-**
ETH_LED1_MDV2	C9	P20_3	**ETH_LED1_MDV2**	**-**	**-**	**ETH_LED1.A**	**R7**	**-**
						IC14.7	**-**	**-**
ETH_LED2_MDV0	C11	P20_1	**ETH_LED2_MDV0**	**-**	**-**	**ETH_LED2.A**	**R8**	**-**
ETH_LED3_MDV3	B10	P20_4	**ETH_LED3_MDV3**	**-**	**-**	**ETH_LED3.A**	**R11**	**-**
ETH_LED4	G15	P19_7	**ETH_LED4**	**-**	**-**	**ETH_LED4.A**	**CN4(short), R12**	**-**
						JA5-A.23	**-**	**-**
ETH_LED5	A9	P21_0	**ETH_LED5**	**-**	**-**	**ETH_LED5.A**	**R13**	**-**
						CN3.4	**-**	**-**
LED_LED6	V6	P08_2	**LED_LED6**	**-**	**-**	**ETH_LED6.A**	**R14**	**-**
						CN2.7	**-**	**-**
M2_UP_LED7	H15	P19_3	**M2_UP_LED7**	**-**	**-**	**ETH_LED7.A**	**R15**	**-**
						JA5-A.19	**-**	**-**

6.15 I²C & EEPROM Configuration

Table 6-46 below detail the function of the option links associated with I²C & EEPROM Configuration.

Table 6-46: I²C & EEPROM Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
EEPROM_SCL	F10	P20_5	**EEPROM_SCL**	**-**	**-**	**IC20.6**	**-**	**-**
						CN3.5	**-**	**-**
EEPROM_SDA	C10	P20_6	**EEPROM_SDA**	**-**	**-**	**IC20.5**	**-**	**-**
						CN3.6	**-**	**-**

6.16 IRQ & Switch Configuration

Table 6-47, Table 6-48, Table 6-49 below details the function of the option links associated with IRQ & Switch Configuration.

Table 6-47: IRQ & Switch Configuration Option Links (1)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
BSC_A01_CAN_TX	P2	P05_3	BSC_A01	IC29.56 (SW6-1 = ON)	-	IC22.E1	-	-
						IC23.23	-	-
						JA3-A.2	-	-
			CAN_TX	**IC29.55 (SW6-1 = OFF)**	-	**CN1.18**	-	-
						JA5-A.5	-	-
						U10.1	-	-
BSC_A16_M2_ENCZ	J5	P02_2	BSC_A16	IC29.25 (SW6-1 = ON)	-	IC22.B8	-	-
						JA3-A.37		
BSC_A02_CAN_RX	P3	P05_2	BSC_A02	IC29.2 (SW6-1 = ON)	-	IC22.D1	-	-
						IC23.24	-	-
						JA3-A.3	-	-
			CAN_RX	**IC29.3 (SW6-1 = OFF)**	-	**CN1.17**	-	-
			CAN_RX_JA5	IC29.3 (SW6-1 = OFF), SW6-9 =ON	SW6-10 = OFF	JA5-A.6	-	-
			CAN_RX_OB	IC29.3 (SW6-1 = OFF), SW6-10 = ON	SW6-9 = OFF	U10.4	-	-
ETH2_INT#	G6	P00_4	**ETH2_INT#**	-	-	**IC16.51**	-	-
ETH1_INT#	R2	P05_6	**ETH1_INT#**	-	-	**IC31.51**	-	-
IRQ11_ENCIF9_WAIT#	K3	P03_3	**IRQ11_ENCIF9_WAIT#**	-	-	**J22.2**	-	-
						CN1.12	-	-
						JA3-A.45	-	-
ETH0_LINK	R11	P10_4	**ETH0_LINK**	**IC36.4**	-	**IC35.59**	-	-
P18_1	G19	P18_1	SCI_RTS	SW5-3 = ON	SW5-4 = OFF	J25.4	-	-
			M1_UN	SW5-4 = ON	SW5-3 = OFF	JA2-A.14	-	-
IRQ9	H20	P17_2	**IRQ9**	-	-	**J26.7**	-	-
BSC_A11_M1_UP	L3	P03_6	BSC_A11	IC29.39 (SW6-1 = ON)	-	IC22.D6	-	-
						IC23.22	-	-
						JA3-A.12	-	-
			M1_UP	**IC29.38 (SW6-1 = OFF)**	**SW5-10 = OFF**	**CN3.14**	-	-
						JA2-A.13		
BSC_A12_M1_TOG	K2	P03_5	BSC_A12	IC29.19 (SW6-1 = ON)	-	IC22.A7	-	-
						IC23.35	-	-
						JA3-A.13	-	-
			M1_TOG	**IC29.20 (SW6-1 = OFF)**	-	**JA6.13**	-	-
DIP_SW6_18	P16	P13_2	**DIP_SW6_18**	**SW3.6 = OFF**	-	**SW3.6**	-	-
IRQ3	D19	P19_2	**IRQ3**	-	-	**J25.7**	-	-
						JA1-A.23	-	-
P18_3	G18	P18_3	MB_RST#	SW6-8 = ON	SW6-7 = OFF	J21.2	-	-
			M1_WN	SW6-7 = ON	SW6-8 = OFF	JA2-A.18	-	-
ETH0_INT#	Y5	P09_2	**ETH0_INT#**	-	-	**IC35.51**	-	-
NMI_18	L19	P16_2	**NMI_18**	-	-	**NMI**	**E32**	-
SW1	T13	P10_5	**SW1**	-	-	**SW1**	-	-
SW2	K16	P16_3	**SW2**	-	-	**SW2**	-	-

Table 6-48: IRQ & Switch Configuration Option Links (2)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
RESET#	T5	-	POWER_RESET#	-	-	IC4.2	-	-
						IC38.11	-	-
			RESET_SW#	-	-	S3	-	-
						U7.28	-	-
						J13.10	-	-
						J20.10	-	-
						CN9.9	-	-
DIP_SW1_18	Y18	P11_0	DIP_SW1_18	-	-	SW3.1	-	-
DIP_SW2_18	T15	P11_3	DIP_SW2_18	-	-	SW3.2	-	-
DIP_SW3_18	V17	P11_4	DIP_SW3_18	-	-	SW3.3	-	-
DIP_SW4_18	R13	P11_6	DIP_SW4_18	-	-	SW3.4	-	-
DIP_SW5_18	T12	P10_6	DIP_SW5_18	-	-	SW3.5	-	-
DIP_SW6_18	P16	P13_2	DIP_SW6_18	-	-	SW3.6	-	-
DIP_SW7_18	N15	P13_7	DIP_SW7_18	-	-	SW3.7	-	-
DIP_SW8_18	U20	P14_1	DIP_SW8_18	-	-	SW3.8	-	-
BSC_A07_MD0_RS485_DE	N1	P04_5	BSC_A07	IC29.47 (SW6-1 = ON)	-	IC22.B2	-	-
						IC23.31	-	-
						JA3-A.8	-	-
			RS485_DE	IC29.46 (SW6-1 = OFF)	-	IC27.5	-	-
			BSC_A07_MD0_ RS485_DE	-	-	SW4.1	IC14.18	-
BSC_A06_MD1	M5	P04_6	BSC_A06	IC29.8 (SW6-1 = ON)	-	IC22.C2	-	-
						IC23.30	-	-
						JA3-A.7	-	-
			BSC_A06_MD1	-	-	SW4.2	IC14.16	-
BSC_A05_MD2	N2	P04_7	BSC_A05	IC29.50 (SW6-1 = ON)	-	IC22.D2	-	-
						IC23.29	-	-
						JA3-A.6	-	-
			BSC_A05_MD2	-	-	SW4.3	IC14.14	-
P17_0_MDD	J15	P17_0	P17_0_MDD	-	-	J25.9	-	-
						SW4.4	IC14.12	-
BSC_A17_MDW	F1	P02_1	BSC_A17	IC12.1 (SW6-1 = ON)	-	IC22.E8	-	-
						JA3-A.38	-	-
			BSC_A17_MDW	-	-	SW4.5	IC14.9	-
P17_7	G20	P17_7	SCI_RXD	SW5-5 = ON	SW5-6 = OFF SW5-7 = OFF	J22.3	-	-
						J25.3	-	-
						JA2-A.8	-	-
			RS485_RXD	SW5-6 = ON	SW5-5 = OFF SW5-7 = OFF	IC27.3	-	-
			M1_VP	SW5-7 = ON	SW5-5 = OFF SW5-6 = OFF	JA2-A.15	-	-
P17_6	J18	P17_6	MIK_PWM	SW5-8 = ON	SW5-9 = OFF SW5-10 = OFF	J22.1	-	-
			SCK3	SW5-9 = ON	SW5-8 = OFF SW5-10 = OFF	JA2-A.10	-	-
			M1_UP*1	SW5-10 = ON	SW5-8 = OFF SW5-9 = OFF	CN3.14	-	-
						JA2-A.13	-	-

*1: When using the J18 pin of RZ/T2M as M1_UP, set as follows.

- SW5-8, 9 = "OFF"
- SW5-10 = "ON"
- SW6-1 = "ON"
- Set P03_6 of RZ/T2M as an Hi-Z port.

Table 6-49: IRQ & Switch Configuration Option Links (3)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P18_0	H16	P18_0	SCI_TXD	SW6-6 = ON	SW6-5 = OFF	J22.4	-	-
						J25.2	-	-
						JA2-A.6	-	-
						IC27.6	-	-
			M1_VN	SW6-5 = ON	SW6-6 = OFF	JA2-A.16	-	-
BSC_D08_TRACE_CTL	C7	P22_1	BSC_D08	IC28.42 (SW6-1 = ON)	-	IC22.H2	-	-
						IC23.42	-	-
						JA3-A.29	-	-
			M2_POE	IC28.41 (SW6-1 = OFF) SW6-4 = ON	SW6-3 = OFF	JA5-A.16	-	-
			TRACE_CTL	IC28.41 (SW6-1 = OFF) SW6-3 = ON	SW6-4 = OFF	CN9.36	-	-

6.17 MTU & POE & Timer Configuration

Table 6-50, Table 6-51 below details the function of the option links associated with MTU & POE & Timer Configuration.

Table 6-50: MTU & POE & Timer Configuration Option Links (1)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
BSC_A11_M1_UP	L3	P03_6	BSC_A11	IC29.39 (SW6-1 = ON)	-	IC22.D6	-	-
						IC23.22	-	-
						JA3-A.12	-	-
			M1_UP	**IC29.38 (SW6-1 = OFF)**	**SW5-10 = OFF**	**CN3.14**	**-**	**-**
						JA2-A.13	**-**	**-**
P18_1	G19	P18_1	SCI_RTS	SW5-3 = ON	SW5-4 = OFF	J25.4	-	-
			M1_UN	SW5-4 = ON	SW5-3 = OFF	JA2-A.14	-	-
P17_7	G20	P17_7	SCI_RXD	SW5-5 = ON	SW5-6 = OFF SW5-7 = OFF	J22.3	-	-
						J25.3	-	-
						JA2-A.8	-	-
			RS485_RXD	SW5-6 = ON	SW5-5 = OFF SW5-7 = OFF	IC27.3	-	-
			M1_VP	SW5-7 = ON	SW5-5 = OFF SW5-6 = OFF	JA2-A.15	-	-
P18_0	H16	P18_0	SCI_TXD	SW6-6 = ON	SW6-5 = OFF	J22.4	-	-
						J25.2	-	-
						JA2-A.6	-	-
						IC27.6	-	-
			M1_VN	SW6-5 = ON	SW6-6 = OFF	JA2-A.16	-	-
M1_WP	F20	P18_2	**M1_WP**	**-**	**-**	**JA2-A.17**	**-**	**-**
P18_3	G18	P18_3	MB_RST#	SW6-8 = ON	SW6-7 = OFF	J21.2	-	-
			M1_WN	SW6-7 = ON	SW6-8 = OFF	JA2-A.18	-	-
MTIOC1A_18	V16	P11_1	**MTIOC1A_33**	**IC42.10**	**-**	**JA2-A.23**	**-**	**-**
ENCIF5	H19	P17_3	**ENCIF5**	**-**	**-**	**CN1.7**	**-**	**-**
						JA2-A.24	**-**	**-**
M1_TRCCLK_18	N16	P13_5	**M1_TRCCLK_33**	**IC42.9**	**-**	**JA2-A.25**	**-**	**-**
M1_TRDCLK_18	R18	P13_6	**M1_TRDCLK_33**	**IC42.8**	**-**	**JA2-A.26**	**-**	**-**
BSC_A16_M2_ENCZ	J5	P02_2	BSC_A16	IC29.25 (SW6-1 = ON)	-	IC22.B8	-	-
						JA3-A.37	-	-
			M2_ENCZ	**IC29.26 (SW6-1 = OFF)**	**-**	**CN1.4**	**-**	**-**
						JA5-A.9	**-**	**-**
BSC_D08_TRACE_CTL	C7	P22_1	BSC_D08	IC28.42 (SW6-1 = ON)	-	IC22.H2	-	-
						IC23.42	-	-
						JA3-A.29	-	-
			M2_POE	IC28.41 (SW6-1 = OFF) SW6-4 = ON	SW6-3 = OFF	JA5-A.16	-	-
			TRACE_CTL	IC28.41 (SW6-1 = OFF) SW6-3 = ON	SW6-4 = OFF	CN9.36	-	-
JA5_17	F8	P23_3	**JA5_17**	**-**	**-**	**JA5-A.17**	**-**	**-**
RLED3_ M2_TRDCLK_ CS5#	C5	P23_4	**RLED3**	**R195**	**R196, R296**	**LED3.A**	**R47**	**-**
			M2_TRDCLK	R196	R195, R296	JA5-A.18	-	-
			CS5#	R296	R195, R196	JA3-A.27	-	-
RLED3_M2_TRDCLK	C5	P23_4	**RLED3**	**R195**	**R196**	**LED3.A**	**R47**	**-**
			M2_TRDCLK	R196	R195	JA5-A.18	-	-
M2_UP_LED7	H15	P19_3	**M2_UP_LED7**	**R15**	**-**	**ETH_LED7.A**	**R15**	**-**
				-	-	**JA5-A.19**	-	-
RLED0_M2_UN	D18	P19_6	**RLED0**	**R201**	**R202**	**LED0.A**	**R43**	**-**
			M2_UN	R202	R201	JA5-A.20	-	-

Table 6-51: MTU & POE & Timer Configuration Option Links (2)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
RLED1_M2_VP	C20	P19_4	**RLED1**	**R199**	**R200**	**LED1.A**	**R44**	**-**
			M2_VP	R200	R199	JA5-A.21	-	-
M2_VN	G16	P19_5	**M2_VN**	**-**	**-**	**JA5-A.22**	**-**	**-**
ETH_LED4	G15	P19_7	**ETH_LED4**	**-**	**-**	**ETH_LED4.A**	**CN4(short), R12**	**-**
						JA5-A.23	-	-
RLED2_M2_WN	B20	P20_0	**RLED2**	**R197**	**R198**	**LED2.A**	**R46**	**-**
			M2_WN	R198	R197	JA5-A.24	-	-

Table 6-52, Table 6-53, Table 6-54, Table 6-55, Table 6-56, Table 6-57 below details the function of the switches associated with the MTU & POE & Timer.

Table 6-52: MTU & POE & Timer Configuration Switch Settings (1)

SW6-1	Explanation
ON	Enable the external bus signal.
OFF	**Enables signals other than the external bus. (CAN, Emulator, I²C, etc.)**

Table 6-53: MTU & POE & Timer Configuration Switch Settings (2)

SW5-7	SW5-6	SW5-5	Explanation
ON	OFF	OFF	Enable the "M1_VP" signal.
OFF	ON	OFF	Enable the "RS485_RXD" signal.
OFF	OFF	ON	Enable the "SCI_RXD" signal.

Table 6-54: MTU & POE & Timer Configuration Switch Settings (3)

SW5-4	SW5-3	Explanation
ON	OFF	Enable the "M1_UN" signal.
OFF	ON	Enable the "SCI_RTS" signal.

Table 6-55: MTU & POE & Timer Configuration Switch Settings (4)

SW6-8	SW6-7	Explanation
ON	OFF	Enable the "MB_RST#" signal.
OFF	ON	Enable the "M1_WN" signal.

Table 6-56: MTU & POE & Timer Configuration Switch Settings (5)

SW6-6	SW6-5	Explanation
ON	OFF	Enable the "SCI_TXD" signal.
OFF	ON	Enable the "M1_VN" signal.

Table 6-57: MTU & POE & Timer Configuration Switch Settings (6)

SW6-4	SW6-3	Explanation
ON	OFF	Enable the "M2_POE" signal.
OFF	ON	Enable the "TRACE_CTL" signal.

6.18 GPT & POEG & Timer Configuration

Table 6-58 below details the function of the option links associated with GPT & POEG & Timer Configuration.

Table 6-58: GPT & POEG & Timer Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
BSC_A11_M1_UP	L3	P03_6	BSC_A11	IC29.39 (SW6-1 = ON)	-	IC22.D6	-	-
						IC23.22	-	-
						JA3-A.12	-	-
			M1_UP	**IC29.38 (SW6-1 = OFF)**	**SW5-10 = OFF**	**CN3.14**	**-**	**-**
						JA2-A.13	**-**	**-**
P18_1	G19	P18_1	SCI_RTS	SW5-3 = ON	SW5-4 = OFF	J25.4	-	-
			M1_UN	SW5-4 = ON	SW5-3 = OFF	JA2-A.14	-	-
P17_7	G20	P17_7	SCI_RXD	SW5-5 = ON	SW5-6 = OFF SW5-7 = OFF	J22.3	-	-
						J25.3	-	-
						JA2-A.8	-	-
			RS485_RXD	SW5-6 = ON	SW5-5 = OFF SW5-7 = OFF	IC27.3	-	-
			M1_VP	SW5-7 = ON	SW5-5 = OFF SW5-6 = OFF	JA2-A.15	-	-
P18_0	H16	P18_0	SCI_TXD	SW6-6 = ON	SW6-5 = OFF	J22.4	-	-
						J25.2	-	-
						JA2-A.6	-	-
						IC27.6	-	-
			M1_VN	SW6-5 = ON	SW6-6 = OFF	JA2-A.16	-	-
M1_WP	F20	P18_2	**M1_WP**	**-**	**-**	**JA2-A.17**	**-**	**-**
P18_3	G18	P18_3	MB_RST#	SW6-8 = ON	SW6-7 = OFF	J21.2	-	-
			M1_WN	SW6-7 = ON	SW6-8 = OFF	JA2-A.18	-	-
MTIOC1A_18	V16	P11_1	**MTIOC1A_33**	**IC42.10**	**-**	**JA2-A.23**	**-**	**-**
ENCIF5	H19	P17_3	**ENCIF5**	**-**	**-**	**CN1.7**	**-**	**-**
						JA2-A.24	**-**	**-**
BSC_A16_M2_ENCZ	J5	P02_2	BSC_A16	IC29.25 (SW6-1 = ON)	-	IC22.B8	-	-
						JA3-A.37	-	-
			M2_ENCZ	**IC29.26 (SW6-1 = OFF)**	**-**	**CN1.4**	**-**	**-**
						JA5-A.9	**-**	**-**
BSC_D08_TRACE_CTL	C7	P22_1	BSC_D08	IC28.42 (SW6-1 = ON)	-	IC22.H2	-	-
						IC23.42	-	-
						JA3-A.29	-	-
			M2_POE	IC28.41 (SW6-1 = OFF) SW6-4 = ON	SW6-3 = OFF	JA5-A.16	-	-
			TRACE_CTL	IC28.41 (SW6-1 = OFF) SW6-3 = ON	SW6-4 = OFF	CN9.36	-	-
M2_UP_LED7	H15	P19_3	**M2_UP_LED7**	**R15**	**-**	**ETH_LED7.A**	**R15**	**-**
				-	-	**JA5-A.19**	-	-
RLED0_M2_UN	D18	P19_6	**RLED0**	**R201**	**R202**	**LED0.A**	**R43**	**-**
			M2_UN	R202	R201	JA5-A.20	-	-
RLED1_M2_VP	C20	P19_4	**RLED1**	**R199**	**R200**	**LED1.A**	**R44**	**-**
			M2_VP	R200	R199	JA5-A.21	-	-
M2_VN	G16	P19_5	**M2_VN**	**-**	**-**	**JA5-A.22**	**-**	**-**
ETH_LED4	G15	P19_7	**ETH_LED4**	**-**	**-**	**ETH_LED4.A**	**CN4(short), R12**	**-**
						JA5-A.23	-	-
RLED2_M2_WN	B20	P20_0	**RLED2**	**R197**	**R198**	**LED2.A**	**R46**	**-**
			M2_WN	R198	R197	JA5-A.24	-	-

Table 6-59, Table 6-60, Table 6-61, Table 6-62, Table 6-63, Table 6-64 below details the function of the switches associated with the GPT & POEG & Timer.

Table 6-59: GPT & POEG & Timer Configuration Switch Settings (1)

SW6-1	Explanation
ON	Enable the external bus signal.
OFF	**Enables signals other than the external bus. (CAN, Emulator, I²C, etc.)**

Table 6-60: GPT & POEG & Timer Configuration Switch Settings (2)

SW5-7	SW5-6	SW5-5	Explanation
ON	OFF	OFF	Enable the "M1_VP" signal.
OFF	ON	OFF	Enable the "RS485_RXD" signal.
OFF	OFF	ON	Enable the "SCI_RXD" signal.

Table 6-61: GPT & POEG & Timer Configuration Switch Settings (3)

SW5-4	SW5-3	Explanation
ON	OFF	Enable the "M1_UN" signal.
OFF	ON	Enable the "SCI_RTS" signal.

Table 6-62: GPT & POEG & Timer Configuration Switch Settings (4)

SW6-8	SW6-7	Explanation
ON	OFF	Enable the "MB_RST#" signal.
OFF	ON	Enable the "M1_WN" signal.

Table 6-63: GPT & POEG & Timer Configuration Switch Settings (5)

SW6-6	SW6-5	Explanation
ON	OFF	Enable the "SCI_TXD" signal.
OFF	ON	Enable the "M1_VN" signal.

Table 6-64: GPT & POEG & Timer Configuration Switch Settings (6)

SW6-4	SW6-3	Explanation
ON	OFF	Enable the "M2_POE" signal.
OFF	ON	Enable the "TRACE_CTL" signal.

6.19 PMOD (UART) Configuration

Table 6-65 below details the function of the option links associated with PMOD (UART) Configuration.

Table 6-65: PMOD (UART) Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
CTS3#	J16	P17_4	CTS3#	-	-	J25.1	-	-
						CN1.8	-	-
P18_0	H16	P18_0	SCI_TXD	SW6-6 = ON	SW6-5 = OFF	J22.4	-	-
						J25.2	-	-
						JA2-A.6	-	-
						IC27.6	-	-
			M1_VN	SW6-5 = ON	SW6-6 = OFF	JA2-A.16	-	-
P17_7	G20	P17_7	SCI_RXD	SW5-5 = ON	SW5-6 = OFF SW5-7 = OFF	J22.3	-	-
						J25.3	-	-
						JA2-A.8	-	-
			RS485_RXD	SW5-6 = ON	SW5-5 = OFF SW5-7 = OFF	IC27.3	-	-
			M1_VP	SW5-7 = ON	SW5-5 = OFF SW5-6 = OFF	JA2-A.15	-	-
P18_1	G19	P18_1	SCI_RTS	SW5-3 = ON	SW5-4 = OFF	J25.4	-	-
			M1_UN	SW5-4 = ON	SW5-3 = OFF	JA2-A.14	-	-
IRQ3	D19	P19_2	IRQ3	-	-	J25.7	-	-
						JA1-A.23	-	-
P16_7	J19	P16_7	P16_7	-	-	J25.8	-	-
P17_0_MDD	J15	P17_0	P17_0_MDD	-	-	J25.9	-	-
						SW4.4	IC14.12	-
P17_1	J20	P17_1	P17_1	-	-	J25.10	-	-

Table 6-66, Table 6-67, Table 6-68 below details the function of the switches associated with the PMOD (UART).

Table 6-66: PMOD (UART) Configuration Switch Settings (1)

SW5-4	SW5-3	Explanation
ON	OFF	Enable the "M1_UN" signal.
OFF	ON	Enable the "SCI_RTS" signal.

Table 6-67: PMOD (UART) Configuration Switch Settings (2)

SW5-7	SW5-6	SW5-5	Explanation
ON	OFF	OFF	Enable the "M1_VP" signal.
OFF	ON	OFF	Enable the "RS485_RXD" signal.
OFF	OFF	ON	Enable the "SCI_RXD" signal.

Table 6-68: PMOD (UART) Configuration Switch Settings (3)

SW6-6	SW6-5	Explanation
ON	OFF	Enable the "SCI_TXD" signal.
OFF	ON	Enable the "M1_VN" signal.

6.20 PMOD (SPI) Configuration

Table 6-69 below details the function of the option links associated with PMOD (SPI) Configuration.

Table 6-69: PMOD (SPI) Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
SSL20	F18	P18_7	SSL20	-	-	J21.3	-	-
						J26.1	-	-
MOSI2	E20	P18_5	MOSI2	-	-	J21.6	-	-
						J26.2	-	-
MISO2	E19	P18_6	MISO2	-	-	J21.5	-	-
						J26.3	E23	E2
						CN1.19	-	-
						CN2.5	-	-
RSPCK2	F19	P18_4	RSPCK2	-	-	J21.4	-	-
						J26.4	E24	E3
IRQ9	H20	P17_2	IRQ9	-	-	J26.7	-	-
P23_6	A2	P23_6	P23_6	-	-	J26.8	-	-
P08_3	T6	P08_3	P08_3	-	-	J26.9	-	-
						CN2.8	-	-
P19_1	E18	P19_1	P19_1	-	-	J26.10	-	-

6.21 PMOD (I^2C) Configuration

Table 6-70 below details the function of the option links associated with PMOD (I^2C) Configuration.

Table 6-70: PMOD (I^2C) Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
BSC_D13_SCL1	E7	P22_6	BSC_D13	IC28.22 (SW6-1 = ON)	-	IC22.F6	-	-
						IC23.50	-	-
						JA3-A.34	-	-
			I2C_SCL_A	IC28.23 (SW6-1 = OFF)	-	J27.1	-	-
						J30.4	-	-
						J22.5	-	-
						JA1-A.26	-	-
						J26.3	E2	E23
BSC_D14_SDA1	C6	P22_7	BSC_D14	IC28.33 (SW6-1 = ON)	-	IC22.H7	-	-
						IC23.51	-	-
						JA3-A.35	-	-
			I2C_SDA_A	IC28.32 (SW6-1 = OFF)	-	J27.2	-	-
						J30.3	-	-
						J22.6	-	-
						JA1-A.25	-	-
						J26.4	E3	E24
IRQ9	H20	P17_2	IRQ9	-	-	J26.7	-	-
P23_6	A2	P23_6	P23_6	-	-	J26.8	-	-
P08_3	T6	P08_3	P08_3	-	-	J26.9	-	-
						CN2.8	-	-
P19_1	E18	P19_1	P19_1	-	-	J26.10	-	-

Table 6-71 below details the function of the switches associated with the PMOD (I^2C).

Table 6-71: PMOD (I^2C) Configuration Switch Settings

SW6-1	Explanation
ON	Enable the external bus signal.
OFF	Enables signals other than the external bus. (CAN, Emulator, I^2C, etc.)

6.22 Grove® (I²C) Configuration

Table 6-72 below details the function of the option links associated with Grove® (I²C) Configuration.

Table 6-72: Grove® (I²C) Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
BSC_D13_SCL1	E7	P22_6	BSC_D13	IC28.22 (SW6-1 = ON)	-	IC22.F6	-	-
						IC23.50	-	-
						JA3-A.34	-	-
			I2C_SCL_A	IC28.23 (SW6-1 = OFF)	-	J27.1	-	-
						J30.4	-	-
						J22.5	-	-
						JA1-A.26	-	-
						J26.3	E2	E23
BSC_D14_SDA1	C6	P22_7	BSC_D14	IC28.33 (SW6-1 = ON)	-	IC22.H7	-	-
						IC23.51	-	-
						JA3-A.35	-	-
			I2C_SDA_A	IC28.32 (SW6-1 = OFF)	-	J27.2	-	-
						J30.3	-	-
						J22.6	-	-
						JA1-A.25	-	-
						J26.4	E3	E24

Table 6-73 below details the function of the switches associated with the Grove® (I²C).

Table 6-73: Grove® (I²C) Configuration Switch Settings

SW6-1	Explanation
ON	Enable the external bus signal.
OFF	Enables signals other than the external bus. (CAN, Emulator, I²C, etc.)

6.23 Grove® (Analog) Configuration

Table 6-74 below details the function of the option links associated with Grove (Analog) Configuration.

Table 6-74: Grove® (Analog) Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
ADC_AN101	B16	-	ADC_AN101	-	-	J28.1	-	-
ADC_AN102	E13	-	ADC_AN102	-	-	J28.2	-	-

6.24 QWIIC® (I²C) Configuration

Table 6-75 below details the function of the option links associated with QWIIC® (I²C) Configuration.

Table 6-75: QWIIC® (I²C) Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
BSC_D13_SCL1	E7	P22_6	BSC_D13	IC28.22 (SW6-1 = ON)	-	IC22.F6	-	-
						IC23.50	-	-
						JA3-A.34	-	-
			I2C_SCL_A	IC28.23 (SW6-1 = OFF)	-	J27.1	-	-
						J30.4	-	-
						J22.5	-	-
						JA1-A.26	-	-
						J26.3	E2	E23
BSC_D14_SDA1	C6	P22_7	BSC_D14	IC28.33 (SW6-1 = ON)	-	IC22.H7	-	-
						IC23.51	-	-
						JA3-A.35	-	-
			I2C_SDA_A	IC28.32 (SW6-1 = OFF)	-	J27.2	-	-
						J30.3	-	-
						J22.6	-	-
						JA1-A.25	-	-
						J26.4	E3	E24

Table 6-76 below details the function of the switches associated with the QWIIC® (I²C).

Table 6-76: QWIIC® (I²C) Configuration Switch Settings

SW6-1	Explanation
ON	Enable the external bus signal.
OFF	Enables signals other than the external bus. (CAN, Emulator, I²C, etc.)

6.25 mikroBUS™ Configuration

Table 6-77 below details the function of the option links associated with mikroBUS™ Configuration.

Table 6-77: mikroBUS™ Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
ADC_AN100	F13	-	**ADC_AN100**	**-**	**-**	**J21.1**	**-**	**-**
P18_3	G18	P18_3	MB_RST#	SW6-8 = ON	SW6-7 = OFF	J21.2	-	-
			M1_WN	SW6-7 = ON	SW6-8 = OFF	JA2-A.18	-	-
SSL20	F18	P18_7	**SSL20**	**-**	**-**	**J21.3**	**-**	**-**
						J26.1	**-**	**-**
RSPCK2	F19	P18_4	**RSPCK2**	**-**	**-**	**J21.4**	**-**	**-**
						J26.4	**E24**	**E3**
MISO2	E19	P18_6	**MISO2**	**-**	**-**	**J21.5**	**-**	**-**
						J26.3	**E23**	**E2**
						CN1.19	**-**	**-**
						CN2.5	**-**	**-**
MOSI2	E20	P18_5	**MOSI2**	**-**	**-**	**J21.6**	**-**	**-**
						J26.2	**-**	**-**
P17_6	J18	P17_6	MIK_PWM	SW5-8 = ON	SW5-9 = OFF SW5-10 = OFF	J22.1	-	-
			SCK3	SW5-9 = ON	SW5-8 = OFF SW5-10 = OFF	JA2-A.10	-	-
			M1_UP*1	SW5-10 = ON	SW5-8 = OFF SW5-9 = OFF	CN3.14	-	-
						JA2-A.13	-	-
IRQ11_ENCIF9_ WAIT#	K3	P03_3	**IRQ11_ENCIF9_WAIT#**	**-**	**-**	**J22.2**	**-**	**-**
						CN1.12	**-**	**-**
						JA3-A.45	**-**	**-**
P17_7	G20	P17_7	SCI_RXD	SW5-5 = ON	SW5-6 = OFF SW5-7 = OFF	J22.3	-	-
						J25.3	-	-
						JA2-A.8	-	-
			RS485_RXD	SW5-6 = ON	SW5-5 = OFF SW5-7 = OFF	IC27.3	-	-
			M1_VP	SW5-7 = ON	SW5-5 = OFF SW5-6 = OFF	JA2-A.15	-	-
P18_0	H16	P18_0	SCI_TXD	SW6-6 = ON	SW6-5 = OFF	J22.4	-	-
						J25.2	-	-
						JA2-A.6	-	-
						IC27.6	-	-
			M1_VN	SW6-5 = ON	SW6-6 = OFF	JA2-A.16	-	-
BSC_D13_SCL1	E7	P22_6	BSC_D13	IC28.22 (SW6-1 = ON)	-	IC22.F6	-	-
						IC23.50	-	-
						JA3-A.34	-	-
			I2C_SCL_A	**IC28.23 (SW6-1 = OFF)**	**-**	**J27.1**	**-**	**-**
						J30.4	**-**	**-**
						J22.5	**-**	**-**
						JA1-A.26	**-**	**-**
						J26.3	**E2**	**E23**
BSC_D14_ SDA1	C6	P22_7	BSC_D14	IC28.33 (SW6-1 = ON)	-	IC22.H7	-	-
						IC23.51	-	-
						JA3-A.35	-	-
			I2C_SDA_A	**IC28.32 (SW6-1 = OFF)**	**-**	**J27.2**	**-**	**-**
						J30.3	**-**	**-**
						J22.6	**-**	**-**
						JA1-A.25	**-**	**-**
						J26.4	**E3**	**E24**

*1: When using the J18 pin of RZ/T2M as M1_UP, set as follows.

- SW5-8, 9 = "OFF"
- SW5-10 = "ON"
- SW6-1 = "ON"
- Set P03_6 of RZ/T2M as an Hi-Z port.

Table 6-78, Table 6-79, Table 6-80, Table 6-81, Table 6-82 below details the function of the switches associated with the mikroBUS™.

Table 6-78: mikroBUS™ Configuration Switch Settings (1)

SW6-1	Explanation
ON	Enable the external bus signal.
OFF	**Enables signals other than the external bus. (CAN, Emulator, I²C, etc.)**

Table 6-79: mikroBUS™ Configuration Switch Settings (2)

SW5-10	SW5-9	SW5-8	Explanation
ON	OFF	OFF	Enable the "M1_UP" signal.
OFF	ON	OFF	Enable the "SCK3" signal.
OFF	OFF	ON	Enable the " MIK_PWM" signal.

Table 6-80: mikroBUS™ Configuration Switch Settings (3)

SW5-7	SW5-6	SW5-5	Explanation
ON	OFF	OFF	Enable the "M1_VP" signal.
OFF	ON	OFF	Enable the "RS485_RXD" signal.
OFF	OFF	ON	Enable the "SCI_RXD" signal.

Table 6-81: mikroBUS™ Configuration Switch Settings (4)

SW6-8	SW6-7	Explanation
ON	OFF	Enable the "MB_RST#" signal.
OFF	ON	Enable the "M1_WN" signal.

Table 6-82: mikroBUS™ BUS Configuration Switch Settings (5)

SW6-6	SW6-5	Explanation
ON	OFF	Enable the "SCI_TXD" signal.
OFF	ON	Enable the "M1_VN" signal.

6.26 xSPI & QSPI & Octa Flash Configuration

Table 6-83 below details the function of the option links associated with xSPI & QSPI & Octa Flash Configuration.

Table 6-83: xSPI & QSPI & Octa Flash Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
XSPI0_CKP	P18	P14_6	**XSPI0_CKP**	**R4**	**-**	**IC19.B2**	**-**	**-**
						IC21.16	**-**	**-**
XSPI0_CS0	M19	P15_7	**OSPI_CS**	**CN8 (1-2 pin short)**	**-**	**IC19.C2**	**-**	**-**
			QSPI_CS	CN8 (2-3 pin short)	-	IC21.7	-	-
XSPI0_RESET0	L18	P16_1	**XSPI0_RESET0**	**-**	**-**	**IC19.A4**	**-**	**-**
						IC21.3	**-**	**-**
XSPI0_DS	R19	P14_4	**XSPI0_DS**	**-**	**-**	**IC19.C3**	**-**	**-**
XSPI0_ECS#	M16	P14_2	**XSPI0_ECS#**	**-**	**-**	**IC19.A5**	**-**	**-**
XSPI0_IO7	K15	P15_6	**XSPI0_IO7**	**-**	**-**	**IC19.E1**	**-**	**-**
XSPI0_IO6	N20	P15_5	**XSPI0_IO6**	**-**	**-**	**IC19.E2**	**-**	**-**
XSPI0_IO5	N19	P15_4	**XSPI0_IO5**	**-**	**-**	**IC19.E3**	**-**	**-**
XSPI0_IO4	M18	P15_3	**XSPI0_IO4**	**-**	**-**	**IC19.D5**	**-**	**-**
XSPI0_IO3	P20	P15_2	**XSPI0_IO3**	**-**	**-**	**IC19.D4**	**-**	**-**
						IC21.1	**-**	**-**
XSPI0_IO2	L16	P15_1	**XSPI0_IO2**	**-**	**-**	**IC19.C4**	**-**	**-**
						IC21.9	**-**	**-**
XSPI0_IO1	M15	P15_0	**XSPI0_IO1**	**-**	**-**	**IC19.D2**	**-**	**-**
						IC21.8	**-**	**-**
XSPI0_IO0	P19	P14_7	**XSPI0_IO0**	**-**	**-**	**IC19.D3**	**-**	**-**
						IC21.15	**-**	**-**

Table 6-84 below details the function of the jumpers associated with the xSPI & QSPI & Octa Flash.

Table 6-84: xSPI & QSPI & Octa Flash Configuration Jumper Settings

Reference	Jumper Position	Explanation
CN8	Shorted Pin 1-2	Enable Octa Flash (IC19).
	Shorted Pin 2-3	**Enable QSPI Serial Flash (IC21).**

6.27 xSPI & HyperRAM Configuration

Table 6-85 below details the function of the option links associated with xSPI & HyperRAM Configuration.

Table 6-85: xSPI & HyperRAM Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
HYRAM_CKP	U19	P13_3	HYRAM_CKP	R2	-	IC41.B2	-	-
HYRAM_CKN	V20	P13_4	HYRAM_CKN	R3	-	IC41.B1	-	-
HYRAM_CS0	T18	P13_1	HYRAM_CS0	-	-	IC41.A3	-	-
HYRAM_RESET0	U18	P12_4	HYRAM_RESET0	-	-	IC41.A4	-	-
HYPER_DS	Y19	P11_7	HYPER_DS	-	-	IC41.C3	-	-
HYRAM_IO7	V18	P12_0	HYRAM_IO7	-	-	IC41.E1	-	-
HYRAM_IO6	T16	P12_1	HYRAM_IO6	-	-	IC41.E2	-	-
HYRAM_IO5	W19	P12_2	HYRAM_IO5	-	-	IC41.E3	-	-
HYRAM_IO4	R16	P12_3	HYRAM_IO4	-	-	IC41.D5	-	-
HYRAM_IO3	R15	P12_5	HYRAM_IO3	-	-	IC41.D4	-	-
HYRAM_IO2	V19	P12_6	HYRAM_IO2	-	-	IC41.C4	-	-
HYRAM_IO1	P15	P12_7	HYRAM_IO1	-	-	IC41.D2	-	-
HYRAM_IO0	W20	P13_0	HYRAM_IO0	-	-	IC41.D3	-	-

6.28 Serial & USB to Serial Configuration

Table 6-86 below details the function of the option links associated with Serial & USB to Serial Configuration.

Table 6-86: Serial & USB to Serial Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
CTS3#	J16	P17_4	CTS3#	-	-	J25.1	-	-
						CN1.8	-	-
P18_0	H16	P18_0	SCI_TXD	SW6-6 = ON	SW6-5 = OFF	J22.4	-	-
						J25.2	-	-
						JA2-A.6	-	-
						IC27.6	-	-
			M1_VN	SW6-5 = ON	SW6-6 = OFF	JA2-A.16	-	-
P17_7	G20	P17_7	SCI_RXD	SW5-5 = ON	SW5-6 = OFF SW5-7 = OFF	J22.3	-	-
						J25.3	-	-
						JA2-A.8	-	-
			RS485_RXD	SW5-6 = ON	SW5-5 = OFF SW5-7 = OFF	IC27.3	-	-
			M1_VP	SW5-7 = ON	SW5-5 = OFF SW5-6 = OFF	JA2-A.15	-	-
P18_1	G19	P18_1	SCI_RTS	SW5-3 = ON	SW5-4 = OFF	J25.4	-	-
			M1_UN	SW5-4 = ON	SW5-3 = OFF	JA2-A.14	-	-
UART_USB_TX	K19	P16_5	UART_USB_TX	IC39	-	IC38.15	IC39.1	-
UART_USB_RX	K18	P16_6	UART_USB_RX	IC40	-	IC38.16	IC39.6	-

Table 6-87, Table 6-88, Table 6-89 below details the function of the switches associated with the Serial & USB to Serial.

Table 6-87: Serial & USB to Serial Configuration Switch Settings (1)

SW5-7	SW5-6	SW5-5	Explanation
ON	OFF	OFF	Enable the "M1_VP" signal.
OFF	ON	OFF	Enable the "RS485_RXD" signal.
OFF	OFF	ON	Enable the "SCI_RXD" signal.

Table 6-88: Serial & USB to Serial Configuration Switch Settings (2)

SW5-4	SW5-3	Explanation
ON	OFF	Enable the "M1_UN" signal.
OFF	ON	Enable the "SCI_RTS" signal.

Table 6-89: Serial & USB to Serial Configuration Switch Settings (3)

SW6-6	SW6-5	Explanation
ON	OFF	Enable the "SCI_TXD" signal.
OFF	ON	Enable the "M1_VN" signal.

6.29 Serial & RS485 Configuration

Table 6-90 below details the function of the option links associated with Serial & RS485 Configuration.

Table 6-90: Serial & RS485 Configuration Option Links (1)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P18_0	H16	P18_0	SCI_TXD	SW6-6 = ON	SW6-5 = OFF	J22.4	-	-
						J25.2	-	-
						JA2-A.6	-	-
						IC27.6	-	-
			M1_VN	SW6-5 = ON	SW6-6 = OFF	JA2-A.16	-	-
P17_7	G20	P17_7	SCI_RXD	SW5-5 = ON	SW5-6 = OFF SW5-7 = OFF	J22.3	-	-
						J25.3	-	-
						JA2-A.8	-	-
			RS485_RXD	SW5-6 = ON	SW5-5 = OFF SW5-7 = OFF	IC27.3	-	-
			M1_VP	SW5-7 = ON	SW5-5 = OFF SW5-6 = OFF	JA2-A.15	-	-
BSC_A07_MD0_ RS485_DE	N1	P04_5	BSC_A07	IC29.47 (SW6-1 = ON)	-	IC22.B2	-	-
						IC23.31	-	-
						JA3-A.8	-	-
			RS485_DE	**IC29.46 (SW6-1 = OFF)**	**-**	**IC27.5**	**-**	**-**
			BSC_A07_MD0_ RS485_DE	**-**	**-**	**SW4.1**	**IC14.18**	**-**

Table 6-91: Serial & RS485 Configuration Option Links (2)

Reference	Setting	Explanation
R193	**Fit**	**Enable termination resistor R194 (130Ω) for RS485 receive signal** *1
	DNF	Disable termination resistor R194 (130Ω) for RS485 receive signal *1

*1: Configure according to the usage of this board and connection destination.

Table 6-92, Table 6-93, Table 6-94 below details the function of the switches associated with the Serial & RS485.

Table 6-92: Serial & RS485 Configuration Switch Settings (1)

SW6-1	Explanation
ON	Enable the external bus signal.
OFF	**Enables signals other than the external bus. (CAN, Emulator, I²C, etc.)**

Table 6-93: Serial & RS485 Configuration Switch Settings (2)

SW5-7	SW5-6	SW5-5	Explanation
ON	OFF	OFF	Enable the "M1_VP" signal.
OFF	ON	OFF	Enable the "RS485_RXD" signal.
OFF	OFF	ON	Enable the "SCI_RXD" signal.

Table 6-94: Serial & RS485 Configuration Switch Settings (3)

SW6-6	SW6-5	Explanation
ON	OFF	Enable the "SCI_TXD" signal.
OFF	ON	Enable the "M1_VN" signal.

Table 6-95 below details the function of the jumpers associated with the Serial & RS485.

Table 6-95: Serial & RS485 Configuration Jumper Settings

Reference	Jumper Position	Explanation
CN21	**Shorted Pin 1-2**	**Full duplex**
	Shorted Pin 2-3	Half duplex
CN22	**Shorted Pin 1-2**	**Full duplex**
	Shorted Pin 2-3	Half duplex

6.30 USB Configuration

Table 6-96 below details the function of the option links associated with the USB Configuration.

Table 6-96: USB Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
USB_VBUSEN_MDV4	D20	P19_0	USB_VBUSEN_MDV4	-	-	IC25.3	-	-
						IC14.5	-	-
USB_OVRCUR	H18	P17_5	USB_OVRCUR	-	-	IC25.8	-	-
						CN1.9	-	-
USB_VBUSIN	W2	P07_4	USB_VBUSIN	R181	-	CN10.1	-	-
						CN11.1	-	-
						IC25.7	-	-
USB_DP	Y14	-	USB_DP	-	-	CN10.3	-	-
						CN11.3	-	-
USB_DM	Y13	-	USB_DM	-	-	CN10.2	-	-
						CN11.2	-	-

7. Headers

7.1 Application Headers

This RSK+ board is fitted with application headers, which can be used to connect compatible Renesas application devices or as easy access to MPU pins.

Table 7-1 below lists the connections of the application header, JA1-A.

Table 7-1: Application Header JA1-A Connections

Application Header JA1-A					
Pin	**Header Name** **Circuit Net Name**	**MPU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MPU Pin**
1	5V CON_5V	-	2	0V GROUND	-
3	3V3 CON_3V3	-	4	0V GROUND	-
5	AVCC CON_AVCC	F14	6	AVSS CON_AVSS	-
7	AVREF CON-AVREF	C15	8	ADTRG ADTRG_ENCIF_RSPCK	F2
9	ADC0 ADC_AN000	B17	10	ADC1 ADC_AN001	C16
11	ADC2 ADC_AN002	A18	12	ADC3 ADC_AN003	E16
13	DAC0 NC	NC	14	DAC1 NC	NC
15	IO_0 NC	NC	16	IO_1 NC	NC
17	IO_2 NC	NC	18	IO_3 NC	NC
19	IO_4 NC	NC	20	IO_5 NC	NC
21	IO_6 NC	NC	22	IO_7 NC	NC
23	IRQd / IRQAEC / M2_HSIN0 IRQ3	D19 / NC / NC	24	IIC_EX NC	NC
25	IIC_SDA I2C_SDA_A	C6	26	IIC_SCL I2C_SCL_A	E7

Table 7-2 below lists the connections of the application header, JA2-A.

Table 7-2: Application Header JA2-A Connections

Application Header JA2-A					
Pin	Header Name Circuit Net Name	MPU Pin	Pin	Header Name Circuit Net Name	MPU Pin
1	RESET RESET#	T5	2	EXTAL CON_EXTAL	Y9
3	NMI NC	NC	4	Vss1 GROUND	-
5	WDT_OVF NC	NC	6	SCIaTX SCI_TXD	H16
7	IRQa / WKUP / M1_HSIN0 NC	NC	8	SCIaRX SCI_RXD	G19
9	IRQb / M1_HSIN1 NC	NC	10	SCIaCK SCK3	J18
11	M1_UD NC	NC	12	CTSaRTSa NC	NC
13	M1_UP M1_UP	J18*1, L3*2	14	M1_UN M1_UN	G19
15	M1_VP M1_VP	G20	16	M1_VN M1_VN	H16
17	M1_WP M1_WP	F20	18	M1_WN M1_WN	G18
19	TimerOut0 NC	NC	20	TimerOut1 NC	NC
21	TimerIn0 NC	NC	22	TimerIn1 NC	NC
23	IRQc / M1_EncZ / M1_HSIN2 MTIOC1A_33	NC / V16 / V16	24	M1_POE ENCIF5	H19
25	M1_TRCCLK M1_TRCCLK_33	N16	26	M1_TRDCLK M1_TRDCLK_33	R18

*1: When using the J18 pin of RZ/T2M, set as follows.
- SW5-8, 9 = "OFF"
- SW5-10 = "ON"
- SW6-1 = "ON"
- Set P03_6 of RZ/T2M as an Hi-Z port.

*2: When using the L3 pin of RZ/T2M, set as follows.
- SW5-8, 9 = "Don't care"
- SW5-10 = "OFF"
- SW6-1 = "OFF"

Table 7-3 below lists the connections of the BUS application header, JA3-A.

Table 7-3: Application Header JA3-A Connections

Application Header JA3-A (Bus)					
Pin	**Header Name** **Circuit Net Name**	**MPU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MPU Pin**
1	A0 BSC_A00_33	N5	2	A1 BSC_A01	P2
3	A2 BSC_A02	P3	4	A3 BSC_A03	N3
5	A4 BSC_A04	M6	6	A5 BSC_A05	N2
7	A6 BSC_A06	M5	8	A7 BSC_A07	N1
9	A8 BSC_A08	L5	10	A9 BSC_A09	L2
11	A10 BSC_A10	K1	12	A11 BSC_A11	L3
13	A12 BSC_A12	K2	14	A13 BSC_A13	J3
15	A14 BSC_A14	K6	16	A15 BSC_A15	G1
17	D0 BSC_D00	B9	18	D1 BSC_D01	C8
19	D2 BSC_D02	B8	20	D3 BSC_D03	A6
21	D4 BSC_D04	A7	22	D5 BSC_D05	E9
23	D6 BSC_D06	B7	24	D7 BSC_D07	B6
25	RDn BSC_RD#	M3	26	WR / SDWE BSC_WR#	K5
27	CSa CS5#	C5*2, D3*3	28	CSb *1 BSC_CS3#_33	N18
29	D8 BSC_D08	C7	30	D9 BSC_D09	F9
31	D10 BSC_D10	A4	32	D11 BSC_D11	E8
33	D12 BSC_D12	B5	34	D13 BSC_D13	E7
35	D14 BSC_D14	C6	36	D15 BSC_D15	A3
37	A16 BSC_A16	J5	38	A17 BSC_A17	F1
39	A18 BSC_A18	J6	40	A19 BSC_A19	F2
41	A20 BSC_A20	E2	42	A21 BSC_A21	V4
43	A22 BSC_A22	R6	44	SDCLK BSC_CKIO	M1
45	CSc / Wait NC	NC	46	ALE / SDCKE BSC_CKE	H6
47	HWRn / DQMH BSC_DQMLU	B4	48	LWRn / DQML BSC_DQMLL_WE0#	E6
49	CAS BSC_CAS#	E3	50	RAS BSC_RAS#	C1

*1: The chip select signal assigned on this board can also be used as a SDRAM chip select.
*2: When using the C5 pin of RZ/T2M, fit R296.
*3: When using the D3 pin of RZ/T2M, short the 2-3 pin of CN23.

Table 7-4 below lists the connections of the application header, JA5-A.

Table 7-4: Application Header JA5-A Connections

Application Header JA5-A					
Pin	**Header Name** **Circuit Net Name**	**MPU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MPU Pin**
1	ADC4 ADC_AN004	A19	2	ADC5 ADC_AN005	C17
3	ADC6 ADC_AN006	B18	4	ADC7 ADC_AN007	B19
5	CAN1TX CAN_TX	P2	6	CAN1RX CAN_RX_JA5	P3
7	CAN2TX NC	NC	8	CAN2RX NC	NC
9	IRQe / M2_EncZ / M2HSIN1 M2_ENCZ	J5 / J5 / J5	10	IRQf / M2_HSIN2 NC	NC
11	M2_UD NC	NC	12	M2_Uin NC	NC
13	M2_Vin NC	NC	14	M2_Win NC	NC
15	M2_Toggle NC	NC	16	M2_POE M2_POE	C7
17	M2_TRCCLK JA5_17	F8	18	M2_TRDCLK M2_TRDCLK	C5
19	M2_UP M2_UP_LED7	H15	20	M2_Un M2_UN	D18
21	M2_VP M2_VP	C20	22	M2_Vn M2_VN	G16
23	M2_WP ETH_LED4	G15	24	M2_Wn M2_WN	B20

Table 7-5 below lists the connections of the application header, JA6.

Table 7-5: Application Header JA6 Connections

Application Header JA6					
Pin	**Header Name** **Circuit Net Name**	**MPU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MPU Pin**
1	DREQ NC	NC	2	DACK NC	NC
3	TEND NC	NC	4	STBYn NC	NC
5	RS232TX NC	NC	6	RS232RX NC	NC
7	SCIbRX NC	NC	8	SCIbTX NC	NC
9	SCIcTX NC	NC	10	SCIbCK NC	NC
11	SCIcCK NC	NC	12	SCIcRX NC	NC
13	M1_Toggle M1_TOG	K2	14	M1_Uin NC	NC
15	M1_Vin NC	NC	16	M1_Win NC	NC
17	EXT_USB_VBUS NC	NC	18	Reserved NC	NC
19	EXT_USB_BATT NC	NC	20	Reserved NC	NC
21	EXT_USB_CHG NC	NC	22	Reserved NC	NC
23	Unregulated_VCC NC	-	24	Vss GROUND	-

7.2 Pin Headers

This RSK+ board is equipped with a header that connects specific MPU pins separately from the application headers.

Table 7-6 below lists the connections of the Pin header, CN1. The encoder interface signal of the MPU is connected to the Pin header, CN1.

Table 7-6: Pin Header CN1 Connections

Pin Header CN1					
Pin	**Circuit Net Name**	**MPU Pin**	**Pin**	**Circuit Net Name**	**MPU Pin**
1	ENCIF0	E2	2	ADTRG_ENCIF_RSPCK	F2
3	ENCIF2	J6	4	M2_ENCZ	J5
5	GROUND	-	6	ENCIF4	G1
7	ENCIF5	H19	8	CTS3#	J16
9	USB_OVRCUR	H18	10	GROUND	-
11	ENCIF8	K6	12	IRQ11_ENCIF9_WAIT#	K3
13	ENCIF10	L5	14	ENCIF11	A4
15	3.3V	-	16	ENCIF12	N3
17	CAN_RX	P3	18	CAN_TX	P2
19	MISO2	E19	20	5.0V	-

Table 7-7 below lists the connections of the Pin header, CN2.

Table 7-7: Pin Header CN2 Connections

Pin Header CN2					
Pin	**Circuit Net Name**	**MPU Pin**	**Pin**	**Circuit Net Name**	**MPU Pin**
1	ETHSW_LPI0	V5	2	TDI	H2
3	TMS	H3	4	TCK	J2
5	MISO2	E19	6	GTIOC16B	E9
7	LED_LED6	V6	8	P08_3	T6

Table 7-8 below lists the connections of the Pin header, CN3. The ΔΣ interface signal of the MPU is connected to the Pin header, CN3.

Table 7-8: Pin Header CN3 Connections

Pin Header CN3					
Pin	**Circuit Net Name**	**MPU Pin**	**Pin**	**Circuit Net Name**	**MPU Pin**
1	5.0V	-	2	3.3V	-
3	ESC_RESETOUT# (MCLK5)	E10	4	ETH_LED5 (MDAT5)	A9
5	EEPROM_SCL (MCLK4)	F10	6	EEPROM_SDA (MDAT4)	C10
7	TRACE_D6 (MCLK3)	B7	8	TRACE_D7 (MDAT3)	B6
9	GROUND	-	10	GROUND	-
11	5.0V	-	12	3.3V	-
13	TRACE_D4 (MCLK2)	A7	14	M1_UP (MDAT2)	J18, L3
15	TRACE_D2 (MCLK1)	B8	16	TRACE_D3 (MDAT1)	A6
17	TRACE_D0 (MCLK0)	B9	18	TRACE_D1 (MDAT0)	C8
19	GROUND	-	20	GROUND	-

8. Code Development

8.1 Overview

There are several ways to debug the code for this device:
Connect CPU Board to PC through SEGGER development tool J-Link® OB that is mounted on CPU Board.
Connect CPU Board to PC through each emulator.
Refer to the manufacturer's website for more details about each emulator.

8.2 Mode Support

The MPU supports various boot modes configured with RSK+ board. Details of the modifications required can be found in section 6.3. All other MPU operating modes are configured within the MPU's registers, which are listed in the RZ/T2M Group User's Manual: Hardware.

Only ever change the MPU operating mode whilst the RSK+ is turned off; otherwise, the MPU may become damaged as a result.

8.3 Address Space

For the MPU address space details, refer to the 'Address Space' section of RZ/T2M Group User's Manual: Hardware.

9. Additional Information

Technical Support

For information about the RZ/T2M Group microprocessors refer to the RZ/T2M Group Hardware Manual.

General information on Renesas microprocessors can be found on the Renesas website at:
https://www.renesas.com/

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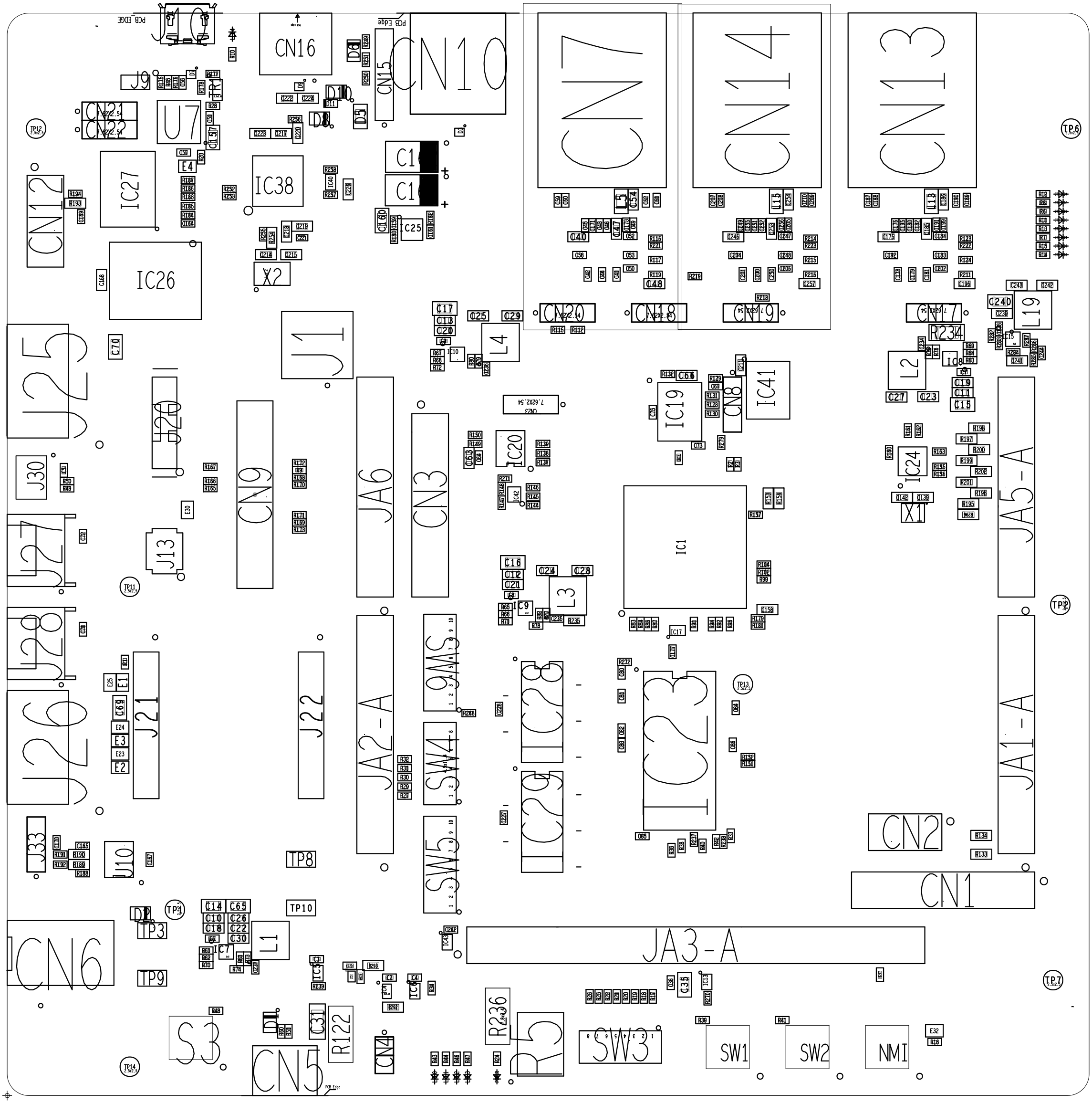
10. Appendix

Details on the placement of individual components on the board are shown on the next page.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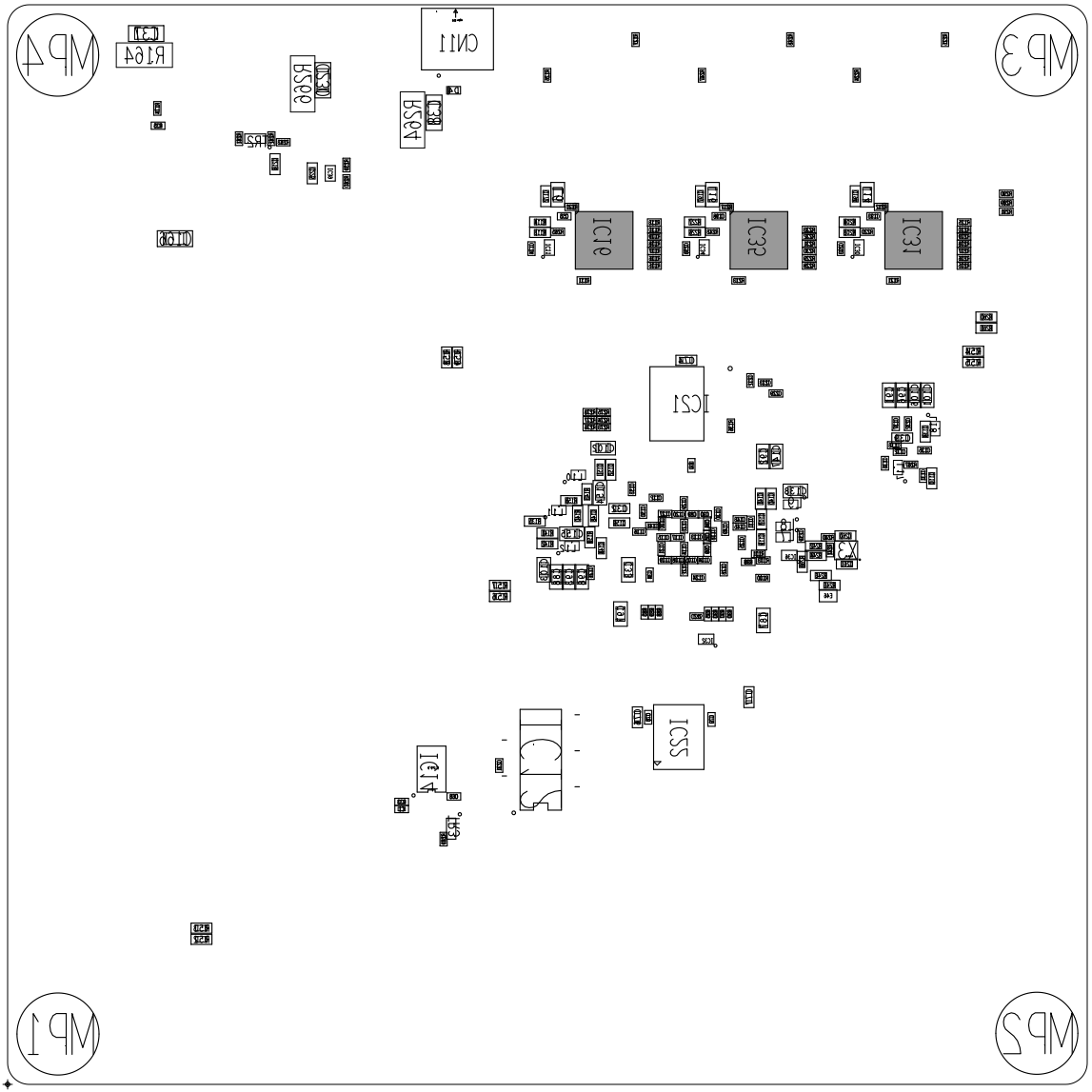
CN16
CN10
CN7
CN14
CN13
J9
CN21
CN22
U7
CN15
IC27
IC38
CN12
IC25
IC26
X2
CN20
CN18
CN19
CN17
J1
L4
L19
R234
J25
J26
CN9
JA6
CN3
IC10
IC19
CN8
IC41
L2
IC20
IC24
IC1
X1
J30
J13
J27
JA5-A
C16
C12
C21
C24
C28
L3
IC9
J28
J21
J22
JA2-A
SW6
SW4
SW5
IC28
IC26
IC23
JA1-A
J33
J10
TP8
CN2
CN1
TP10
TP3
L1
IC7
JA3-A
CN6
TP9
R236
S3
CN5
R122
CN4
R5
SW3
SW1
SW2
NMI


MP4
MP3
MP1
MP2
CN11
IC21
IC22
IC31
IC32
IC33

REVISION HISTORY	RZ/T2M Group Renesas Starter Kit+ For RZ/T2M User's Manual

Rev.	Date	Description	
		Page	Summary
1.00	Apr 20, 2022	—	First Edition issued
1.01	Sep 20, 2022	15 17 38	Change Default Enable of CLK in Figure 4-1 Change X1 to Fitted in Table 5-1 Change default configuration in Table 6-15
1.02	Dec 22, 2022	10 47 72	Correct I2C EEPROM description in Table 1-1 Correct SW6-1 setting of P01_0 in Table 6-25 Add Table 6-91 as description of R193. Along with this, correct title of Table 6-90, and the table number in Chapter 6 has been shifted by one.

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