

MOSFET – P-Channel, POWERTRENCH® -60 V, -13.5 A, 100 mΩ

FDMC5614P, FDMC5614P-L701

General Description

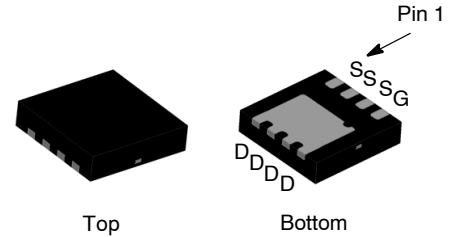
This P-Channel MOSFET is a rugged gate version of onsemi's advanced POWERTRENCH process. It has been optimized for power management applications requiring a wide range of gate drive voltage ratings (4.5 V – 20 V).

Features

- Max $r_{DS(on)}$ = 100 mΩ at $V_{GS} = -10$ V, $I_D = -5.7$ A
- Max $r_{DS(on)}$ = 135 mΩ at $V_{GS} = -4.5$ V, $I_D = -4.4$ A
- Low Gate Charge
- Fast Switching Speed
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$
- High Power and Current Handling Capability
- These Devices are Pb-Free and are RoHS Compliant

Applications

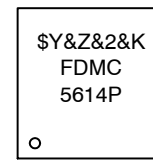
- Power Management
- Load Switch
- Battery Protection



WDFN8 3.3x3.3, 0.65P
 CASE 511DQ

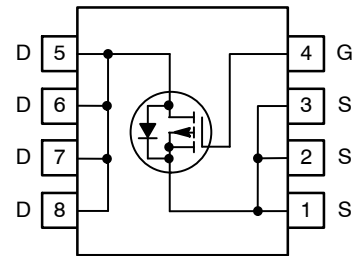
FDMC5614P, FDMC5614P-L701

MARKING DIAGRAM



- \$Y = Logo
- &Z = Assembly Location
- &2 = Date Code (Year and Week)
- &K = Lot Run Traceability Code
- FDMC = Specific Device Code
- 5614P = Specific Device Code

PIN ASSIGNMENT



P-Channel MOSFET

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

FDMC5614P, FDMC5614P-L701

MOSFET MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

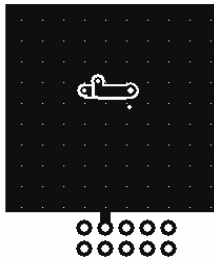
Symbol	Parameter		Rating	Unit	
V_{DS}	Drain to Source Voltage		-60	V	
V_{GS}	Gate to Source Voltage		± 20	V	
I_D	Drain Current	Continuous (Package Limited)	$T_C = 25^\circ\text{C}$	-13.5	A
		Continuous (Silicon Limited)	$T_C = 25^\circ\text{C}$	-14	
		Continuous (Note 1a)	$T_A = 25^\circ\text{C}$	-5.7	
		Pulsed		-23	
P_D	Power Dissipation		$T_C = 25^\circ\text{C}$	42	W
	Power Dissipation (Note 1a)		$T_A = 25^\circ\text{C}$	2.1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to + 150	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

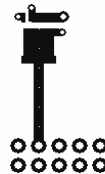
THERMAL CHARACTERISTICS

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.0	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	60	

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.
 - $R_{\theta JA} = 60^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper, 1.5' x 1.5' x 0.062' thick PCB.
 - $R_{\theta JA} = 135^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.



a. $60^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



b. $135^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

FDMC5614P, FDMC5614P-L701

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250 \mu\text{A}$, $V_{GS} = 0 \text{ V}$	-60	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$, referenced to 25°C	-	-54	-	mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -48 \text{ V}$, $V_{GS} = 0 \text{ V}$	-	-	-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0 \text{ V}$	-	-	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -250 \mu\text{A}$	-1.0	-1.95	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$, referenced to 25°C	-	4.7	-	mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10 \text{ V}$, $I_D = -5.7 \text{ A}$	-	84	100	m Ω
		$V_{GS} = -4.5 \text{ V}$, $I_D = -4.4 \text{ A}$	-	108	135	
		$V_{GS} = -10 \text{ V}$, $I_D = -5.7 \text{ A}$, $T_J = 125^\circ\text{C}$	-	140	168	
g_{FS}	Forward Transconductance	$V_{DS} = -15 \text{ V}$, $I_D = -5.7 \text{ A}$	-	11	-	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = -30 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	-	795	1055	pF
C_{oss}	Output Capacitance		-	140	185	pF
C_{rss}	Reverse Transfer Capacitance		-	60	90	pF

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -30 \text{ V}$, $I_D = -1.0 \text{ A}$, $V_{GS} = -10 \text{ V}$, $R_{GEN} = 6 \Omega$	-	10	21	ns
t_r	Rise Time		-	11	23	ns
$t_{d(off)}$	Turn-Off Delay Time		-	32	65	ns
t_f	Fall Time		-	11	22	ns
$Q_{g(TOT)}$	Total Gate Charge at 10 V	$V_{GS} = -10 \text{ V}$, $V_{DD} = -30 \text{ V}$, $I_D = -5.7 \text{ A}$	-	15	20	nC
Q_{gs}	Gate to Source Gate Charge		-	1.6	2.1	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	2.7	3.5	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}$, $I_S = -3.2 \text{ A}$	-	-0.8	-1.2	V
t_{rr}	Reverse Recovery Time	$I_F = -3.2 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$	-	-	36	ns
Q_{rr}	Reverse Recovery Charge		-	-	29	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

FDMC5614P, FDMC5614P-L701

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

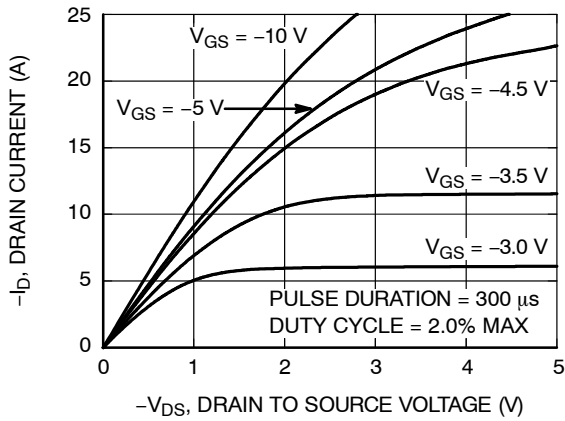


Figure 1. On Region Characteristics

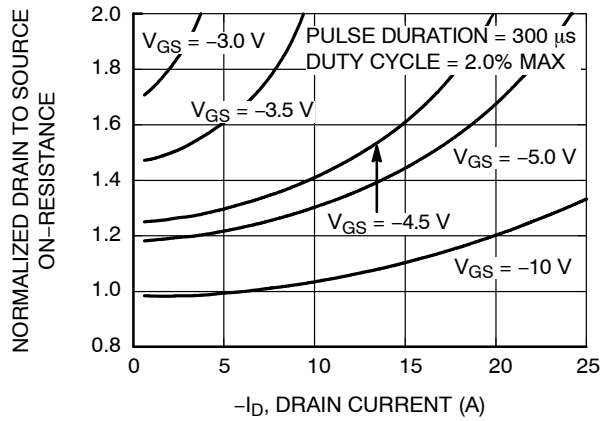


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

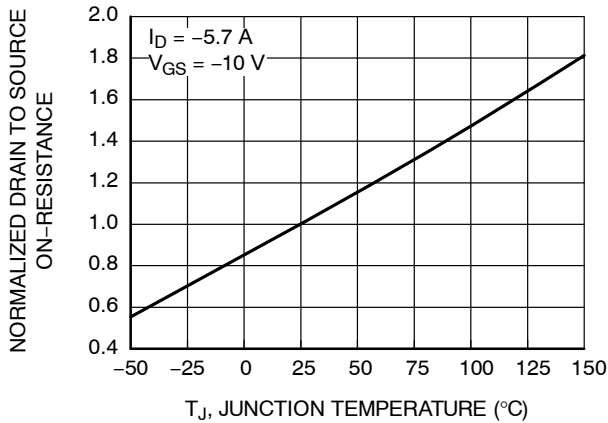


Figure 3. Normalized On Resistance vs. Junction Temperature

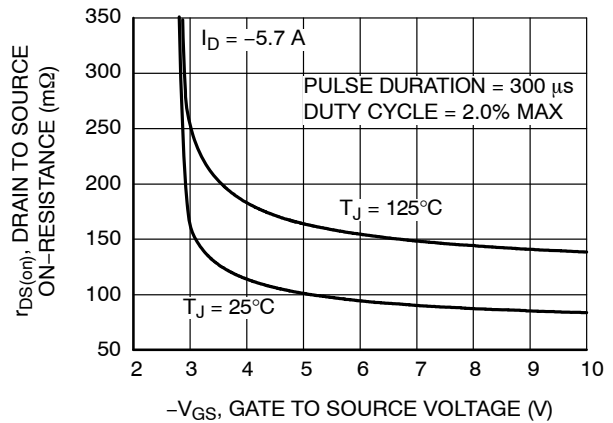


Figure 4. On-Resistance vs. Gate to Source Voltage

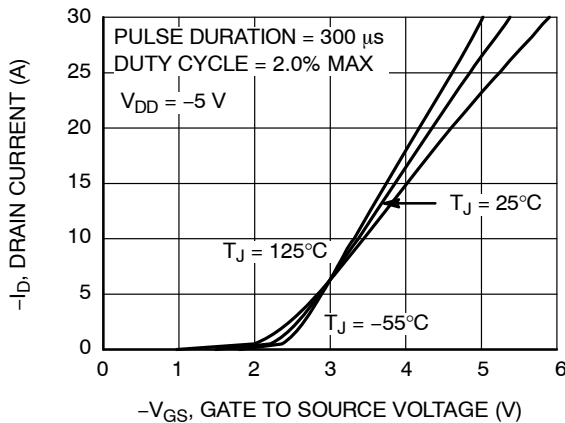


Figure 5. Transfer Characteristics

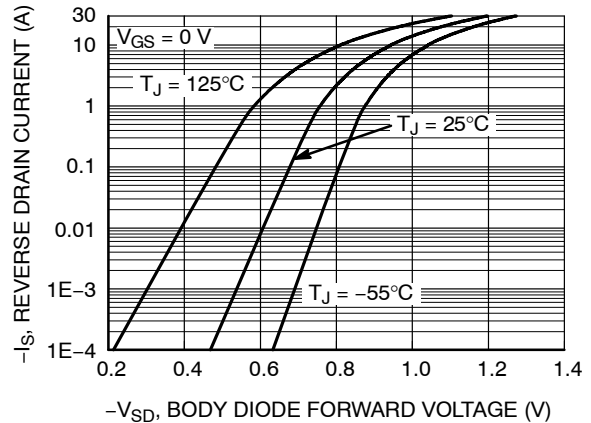


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

FDMC5614P, FDMC5614P-L701

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

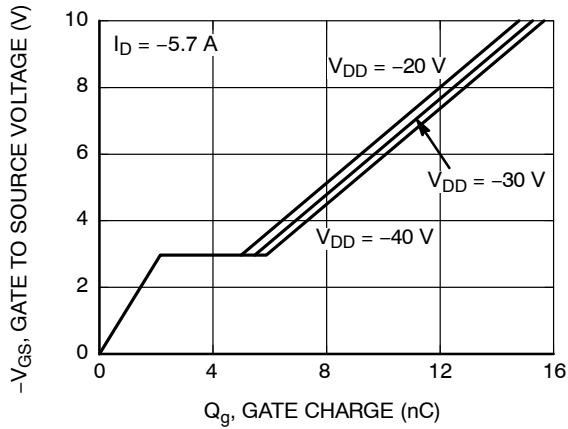


Figure 7. Gate Charge Characteristics

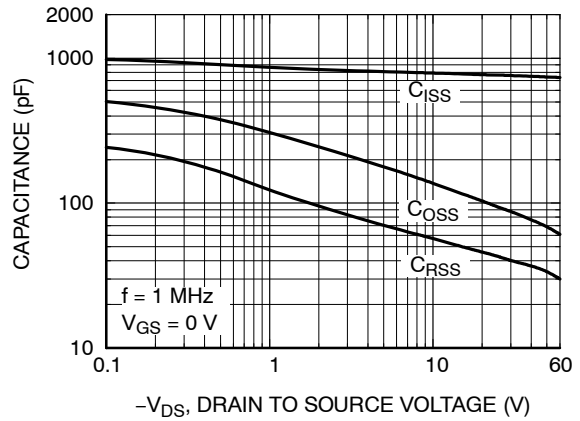


Figure 8. Capacitance vs. Drain to Source Voltage

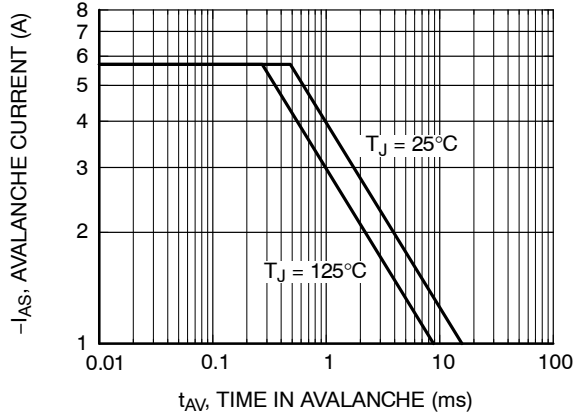


Figure 9. Unclamped Inductive Switching Capability

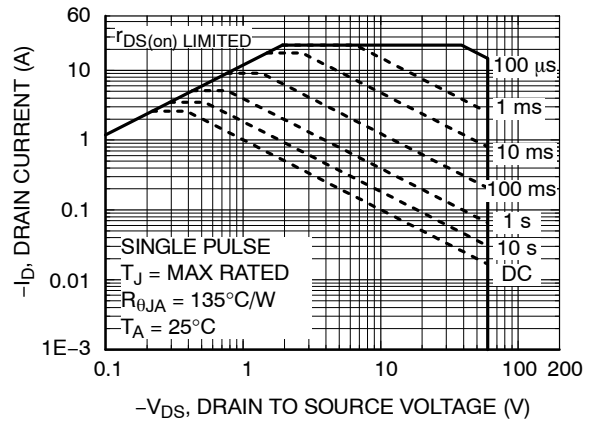


Figure 10. Forward Bias Safe Operating Area

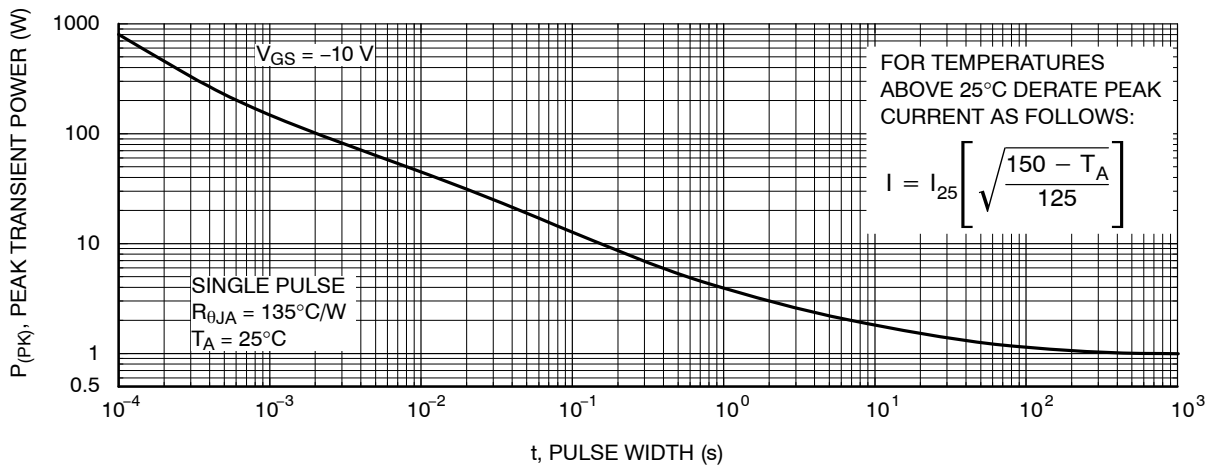


Figure 11. Single Pulse Maximum Power Dissipation

FDMC5614P, FDMC5614P-L701

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

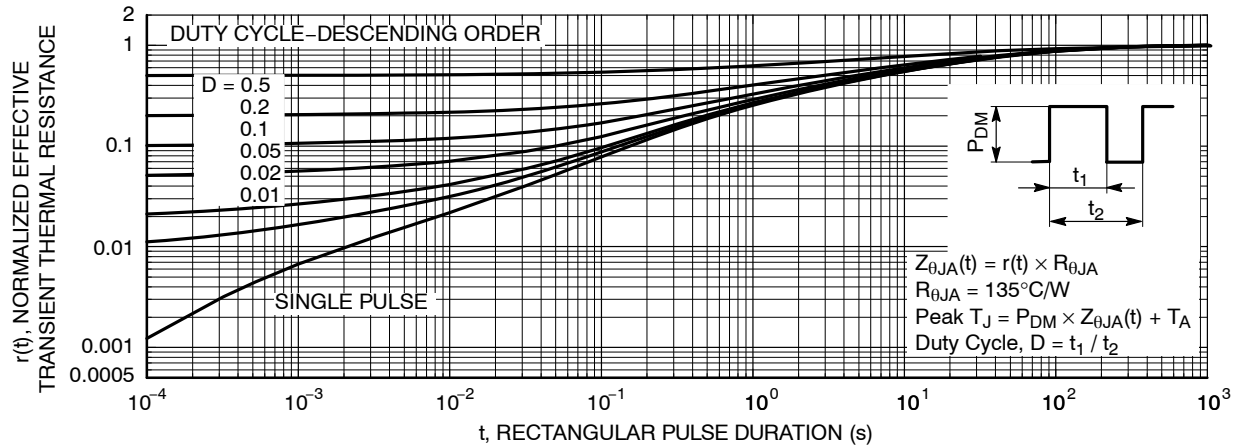


Figure 12. Transient Thermal Response Curve

ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping [†]
FDMC5614P	FDMC5614P	WDFN8 3.3x3.3, 0.65P Power 33 (Pb-Free)	7"	8 mm	3000 / Tape & Reel
FDMC5614P-L701	FDMC5614P	WDFN8 3.3x3.3, 0.65P Power 33 (Pb-Free)	7"	8 mm	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

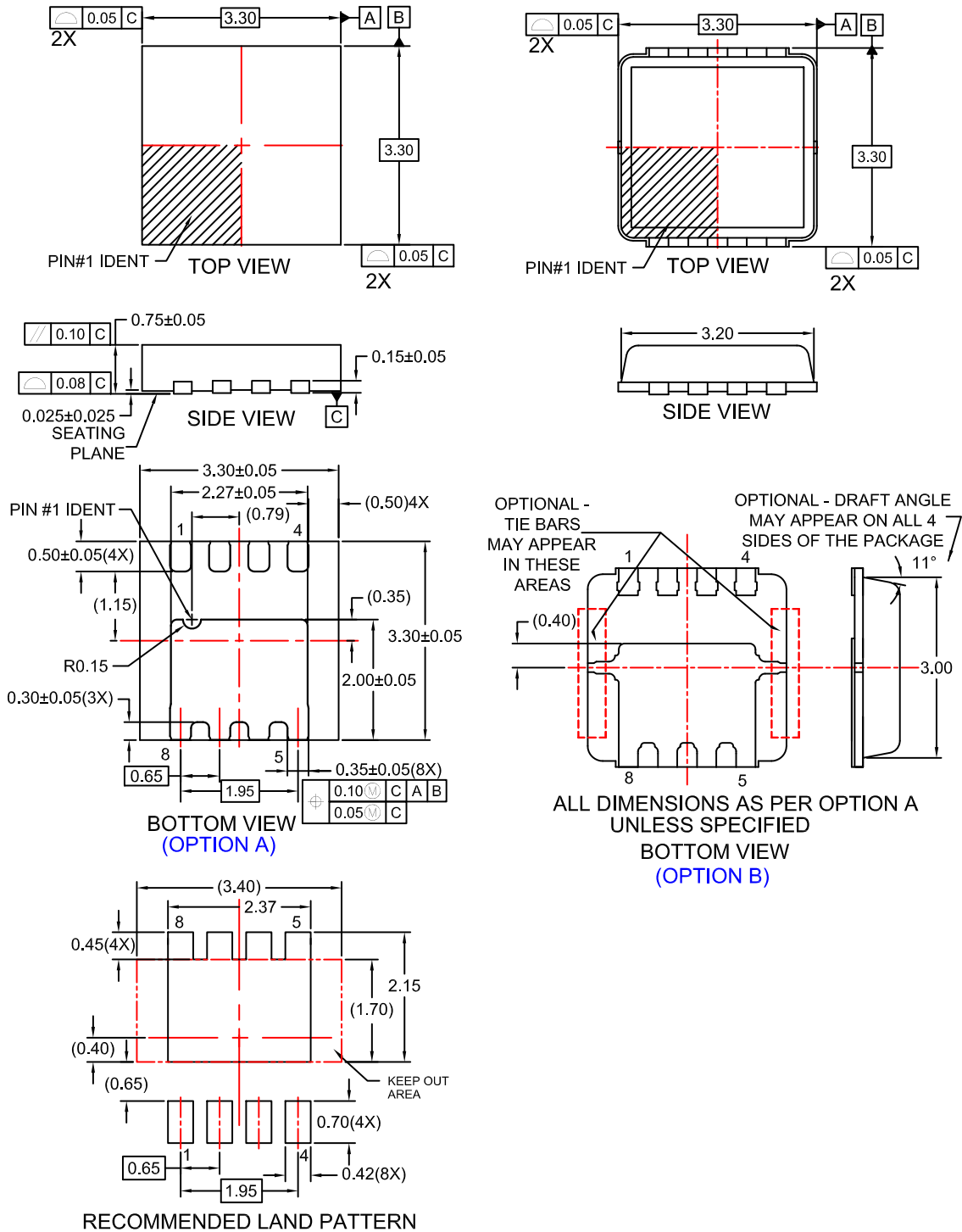
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

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WDFN8 3.3x3.3, 0.65P CASE 511DQ ISSUE O

DATE 31 OCT 2016



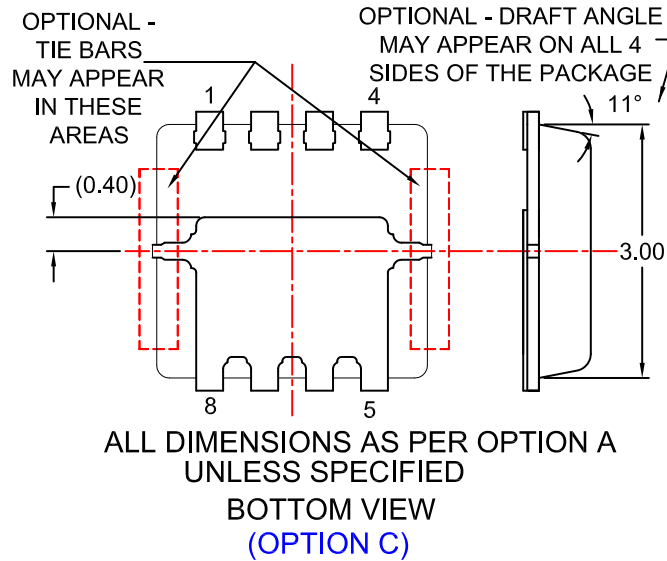
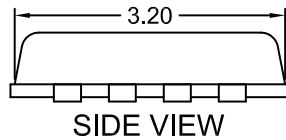
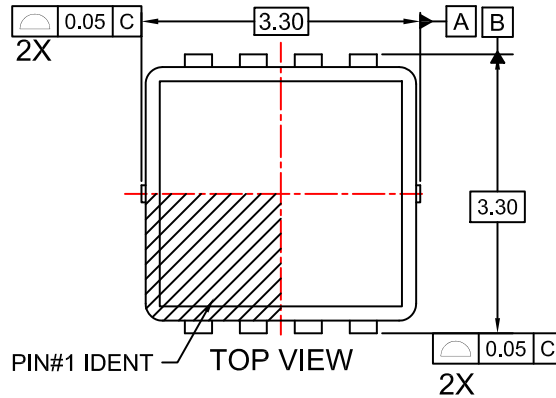
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CASE 511DQ
ISSUE O

DATE 31 OCT 2016



NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-240.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN
- E. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. BURRS OR MOLD FLASH SHALL NOT EXCEED 0.10MM.

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