SLG7NT4192

GreenPAK ™

Power Good Generator Logic

General Description

Renesas SLG7NT4192 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

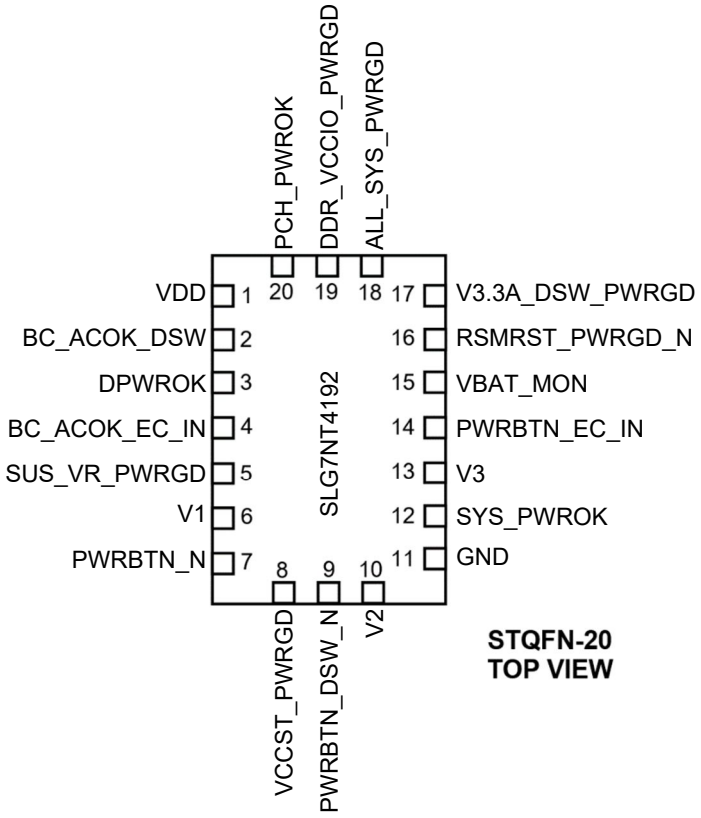
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 20 Package

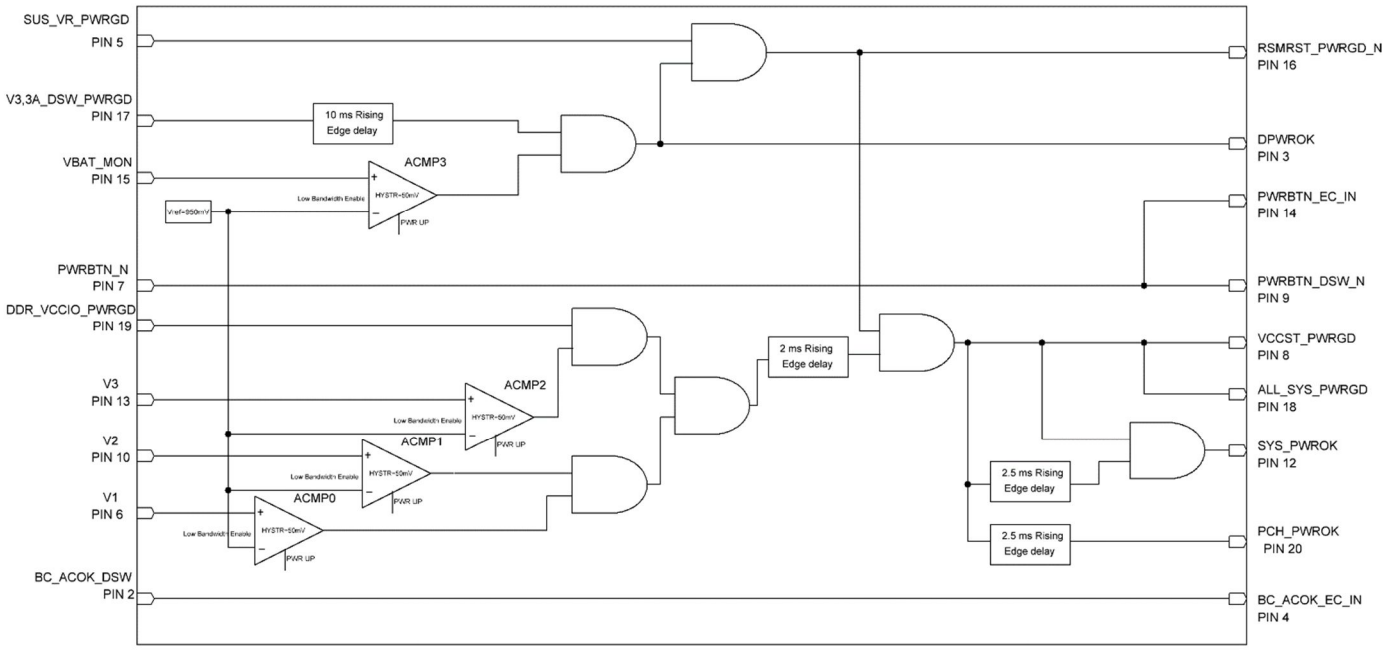
Output Summary

8 Outputs - Open Drain NMOS 1X
1 Output - Push Pull 1X

Pin Configuration



Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	BC_ACOK_DSW	Digital Input	Digital Input without Schmitt trigger	floating
3	DPWROK	Digital Output	Push Pull 1X	floating
4	BC_ACOK_EC_IN	Digital Output	Open Drain NMOS 1X	floating
5	SUS_VR_PWRGD	Digital Input	Digital Input without Schmitt trigger	floating
6	V1	Analog Input/Output	Analog Input/Output	floating
7	PWRBTN_N	Digital Input	Digital Input without Schmitt trigger	floating
8	VCCST_PWRGD	Digital Output	Open Drain NMOS 1X	floating
9	PWRBTN_DSW_N	Digital Output	Open Drain NMOS 1X	floating
10	V2	Analog Input/Output	Analog Input/Output	floating
11	GND	GND	Ground	--
12	SYS_PWROK	Digital Output	Open Drain NMOS 1X	floating
13	V3	Analog Input/Output	Analog Input/Output	floating
14	PWRBTN_EC_IN	Digital Output	Open Drain NMOS 1X	floating
15	VBAT_MON	Analog Input/Output	Analog Input/Output	floating
16	RSMRST_PWRGD_N	Digital Output	Open Drain NMOS 1X	floating
17	V3.3A_DSW_PWRGD	Digital Input	Digital Input without Schmitt trigger	floating
18	ALL_SYS_PWRGD	Digital Output	Open Drain NMOS 1X	floating
19	DDR_VCCIO_PWRGD	Digital Input	Digital Input without Schmitt trigger	floating
20	PCH_PWROK	Digital Output	Open Drain NMOS 1X	floating

Ordering Information

Part Number	Package Type
SLG7NT4192V	V=STQFN-20
SLG7NT4192VTR	VTR=STQFN-20 – Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply Voltage on VDD relative to GND		-0.5	7	V
DC Input Voltage		GND - 0.5V	VDD + 0.5V	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	8	mA
	OD 1x	--	8	
Current at Input Pin		-1.0	1.0	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

Electrical Characteristics

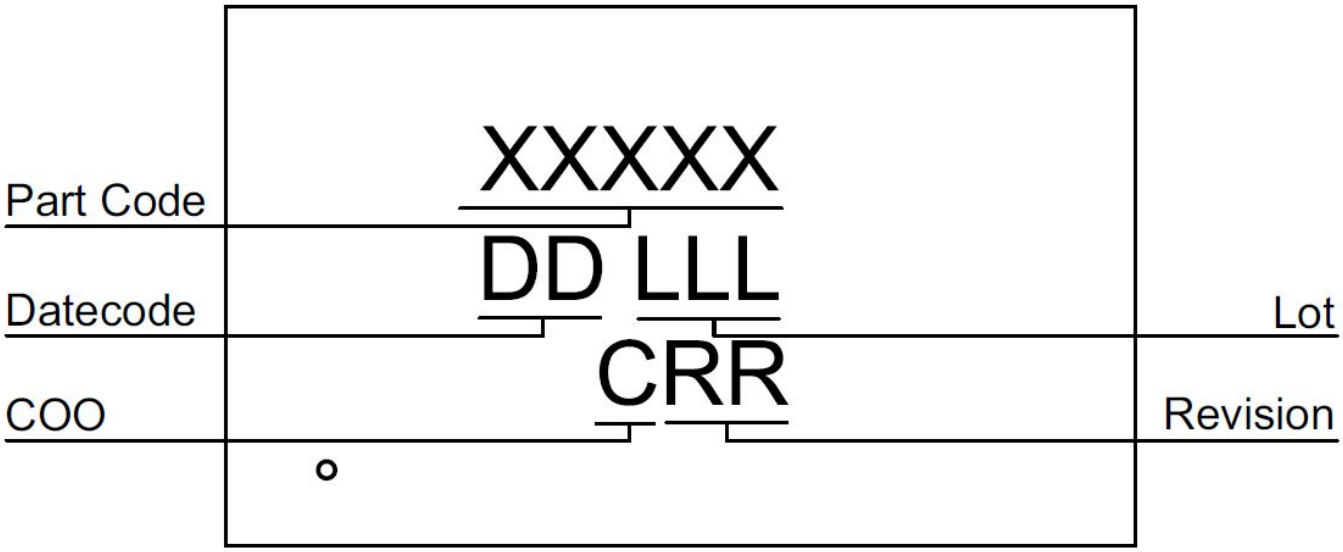
Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	3.3	3.6	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs	--	85	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	84	mA
		T_J = 110°C	--	--	40	mA
V_{IH}	HIGH-Level Input Voltage	Logic Input at VDD=1.8V	1.1	--	--	V
		Logic Input at VDD=3.3V	1.78	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input at VDD=1.8V	--	--	0.69	V
		Logic Input at VDD=3.3V	--	--	1.21	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, I_{OH}=100µA, at VDD=1.8V	1.69	1.789	--	V
		Push-Pull 1X, I_{OH}=3mA, at VDD=3.3V	2.735	3.12	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}=100µA, at VDD=1.8V	--	0.008	0.03	V
		Push-Pull 1X, I_{OL}=3mA, at VDD=3.3V	--	0.13	0.228	V
		Open Drain NMOS 1X, I_{OL}=100µA, at VDD=1.8V	--	0.005	0.02	V
		Open Drain NMOS 1X, I_{OL}=3mA, at VDD=3.3V	--	0.08	0.147	V
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, V_{OH}=VDD-0.2V, at VDD=1.8V	1.066	1.703	--	mA

		Push-Pull 1X, V_{OH}=2.4V, at VDD=3.3V	6.045	12.08	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL}=0.15V, at VDD=1.8V	0.917	1.689	--	mA
		Push-Pull 1X, V_{OL}=0.4V, at VDD=3.3V	4.875	8.244	--	mA
		Open Drain NMOS 1X, V_{OL}=0.15V, at VDD=1.8V	1.375	2.534	--	mA
		Open Drain NMOS 1X, V_{OL}=0.4V, at VDD=3.3V	7.313	12.37	--	mA
T_{DLY0}	Delay0 Time	At temperature 25°C	2.24	2.50	2.75	ms
		At temperature -40 +85°C (Note 3)	2.14	2.50	3.33	ms
T_{DLY1}	Delay1 Time	At temperature 25°C	2.24	2.50	2.75	ms
		At temperature -40 +85°C (Note 3)	2.14	2.50	3.33	ms
T_{DLY4}	Delay4 Time	At temperature 25°C	1.82	2.00	2.24	ms
		At temperature -40 +85°C (Note 3)	1.73	2.00	2.71	ms
T_{DLY5}	Delay5 Time	At temperature 25°C	8.96	10.00	10.75	ms
		At temperature -40 +85°C (Note 3)	8.54	10.00	13.03	ms
V_{ACMP0}	Analog Comparator0 Threshold Voltage	Low to High transition, at temperature 25°C	--	950	988	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	--	950	1009	mV
		High to Low transition, at temperature 25°C	911	950	--	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	871	950	--	mV
V_{ACMP1}	Analog Comparator1 Threshold Voltage	Low to High transition, at temperature 25°C	--	950	988	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	--	950	1009	mV
		High to Low transition, at temperature 25°C	911	950	--	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	871	950	--	mV
V_{ACMP2}	Analog Comparator2 Threshold Voltage	Low to High transition, at temperature 25°C	--	950	988	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	--	950	1009	mV
		High to Low transition, at temperature 25°C	911	950	--	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	871	950	--	mV

V_{ACMP3}	Analog Comparator3 Threshold Voltage	Low to High transition, at temperature 25°C	--	950	988	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	--	950	1009	mV
		High to Low transition, at temperature 25°C	911	950	--	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	871	950	--	mV
V_{HYST}	Analog Comparator Hysteresis Voltage(Note 3)	ACMP 0 at temperature 25°C	--	50	--	mV
		ACMP 0 at temperature -40 +85°C	--	50	--	mV
		ACMP 1 at temperature 25°C	--	50	--	mV
		ACMP 1 at temperature -40 +85°C	--	50	--	mV
		ACMP 2 at temperature 25°C	--	50	--	mV
		ACMP 2 at temperature -40 +85°C	--	50	--	mV
		ACMP 3 at temperature 25°C	--	50	--	mV
		ACMP 3 at temperature -40 +85°C	--	50	--	mV
T_{SU}	Startup Time	from VDD rising past 1.35 V	--	0.3	--	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.18	1.353	1.516	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.73	0.914	1.103	V

Note:
1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7, 8, 9 and 10 are connected to one side, pins 12, 13, 14, 15, 16, 17, 18, 19 and 20 to another.
3. Guaranteed by Design.

Package Top Marking



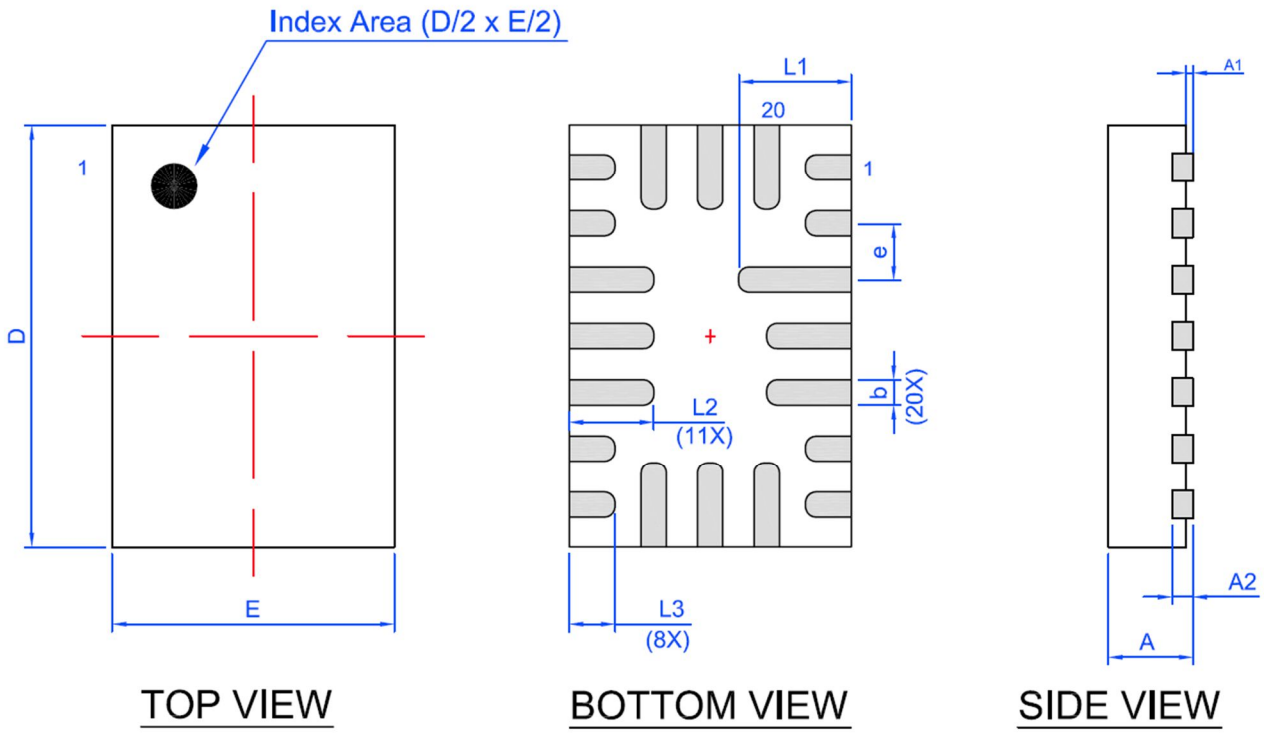
XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.06	004	L	0x47C472BA	4192V	AD	02/25/2022

The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking.

Package Drawing and Dimensions

STQFN 20L 2x3mm 0.4P COL Package
JEDEC MO-220, Variation WECE



Unit: mm

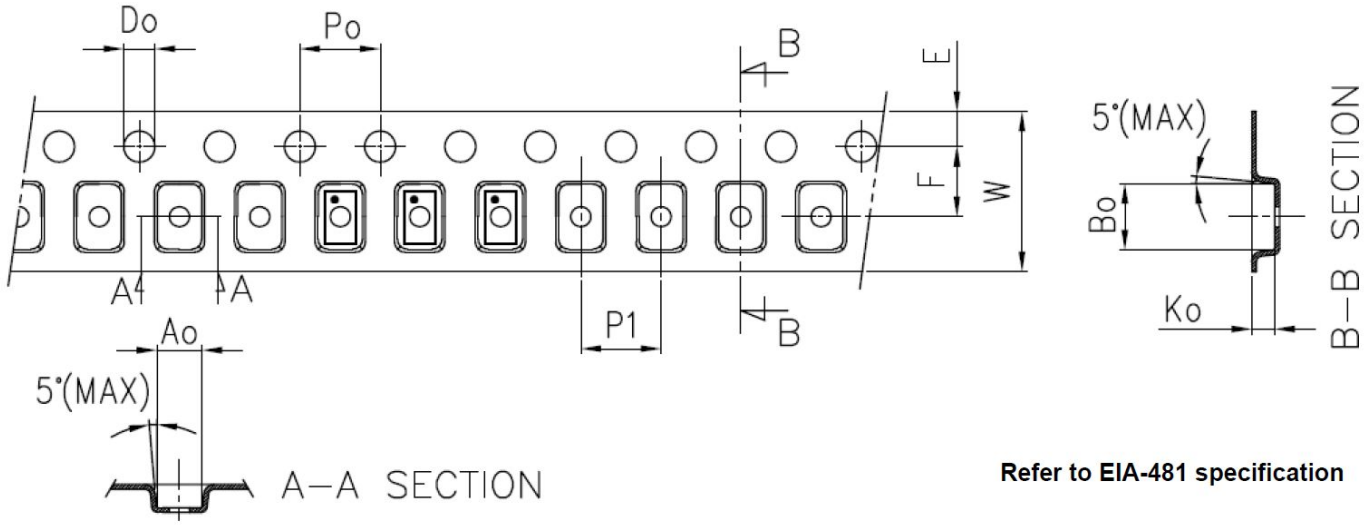
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L1	0.75	0.80	0.85
b	0.13	0.18	0.23	L2	0.55	0.60	0.65
e	0.40 BSC			L3	0.275	0.325	0.375

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 20L 2x3mm 0.4P Green	20	2x3x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3mm 0.4P Green	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

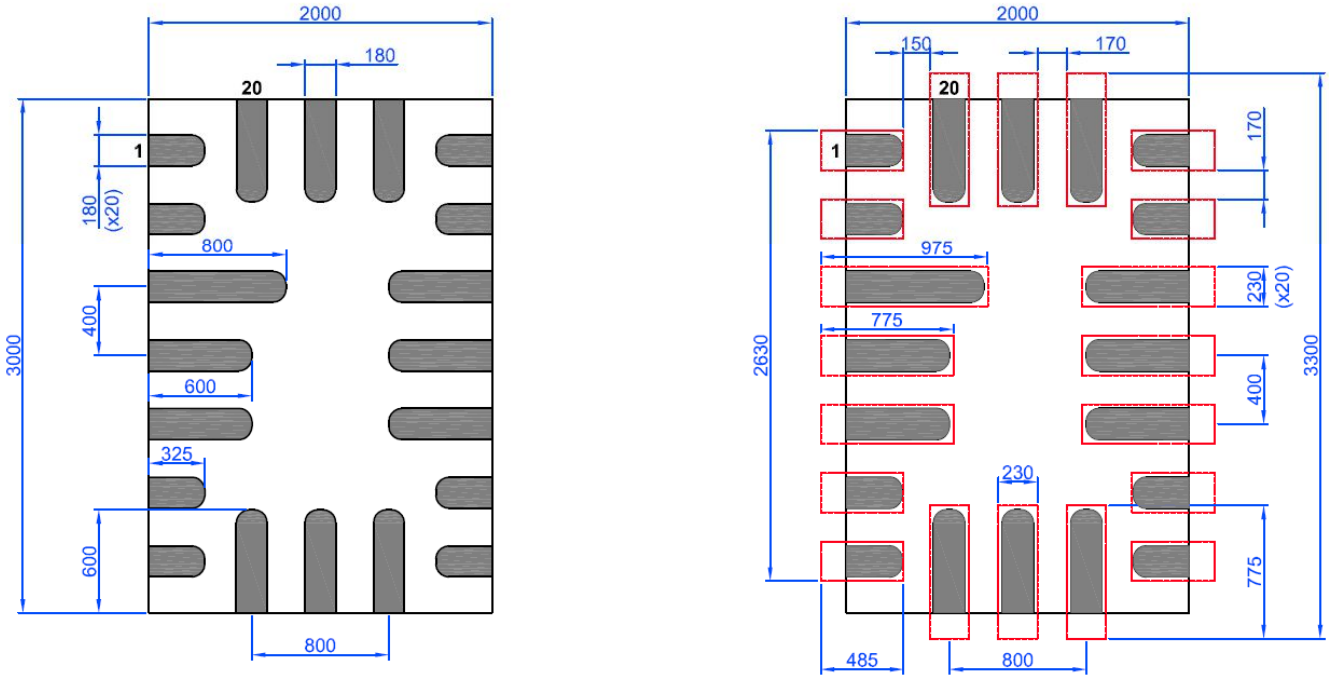
Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.3 mm^3 (nominal). More information can be found at www.jedec.org.

Recommended Land Pattern

Exposed Pad
(Top View)

Recommended Land Pattern
(Top View)

Units: µm



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