RAA489204

Industrial Grade Multi-Cell Li-Ion Battery Manager

The RAA489204 Industrial grade Li-ion battery manager IC supervises up to 14 series connected cells and is optimized to meet stringent Industrial performance, reliability, and safety requirements. The device provides all the functions expected of such a critical component in a battery management system, such as accurate cell voltage and temperature monitoring, cell balancing, and extensive system diagnostics.

In a typical configuration, a Master RAA489204 communicates to a host micro-controller through an SPI port and up to 29 additional RAA489204 devices connected together by a robust, proprietary, two-wire Daisy Chain. This communication system is highly flexible and can be implemented with capacitor isolation, transformer isolation, or a combination of both.

Three cell balancing modes are included: Manual Balance mode, Timed Balance mode, and Auto Balance mode. Auto Balance mode terminates balancing after a host-specified amount of charge has been removed from every cell.

The RAA489204 is packaged in a 64 pin TQFP and is specified for operation from -40ºC to +85ºC.

Applications

- Electric Mobility battery packs
- Backup battery and energy storage systems requiring high accuracy management and monitoring
- Portable and semi-portable equipment

Features

- Monitors and manages up to 14 cells; all standard Li-Ion cell chemistries
- Robust two-wire Daisy Chain communications system using capacitor or transformer coupling at up to 1Mbps
- High security communications protocol
- Cell voltage measurement accuracy ±10mV
- Up to six external temperature monitoring inputs
- Internal temperature monitoring with warning flag
- Two general purpose I/O pins
- Automatic sensing of position in battery stack
- Measures and performs read-back on all voltages, temperatures, and diagnostics for 112 cells in less than 10ms
- User-selectable cell measurement averaging function
- 14-bit voltage and temperature measurements
- Integrated system diagnostics for all key functions
- Watchdog shuts down device if communication is lost
- Fully tolerant to EMC and transients

Contents

1. Overview

1.1 Block Diagram

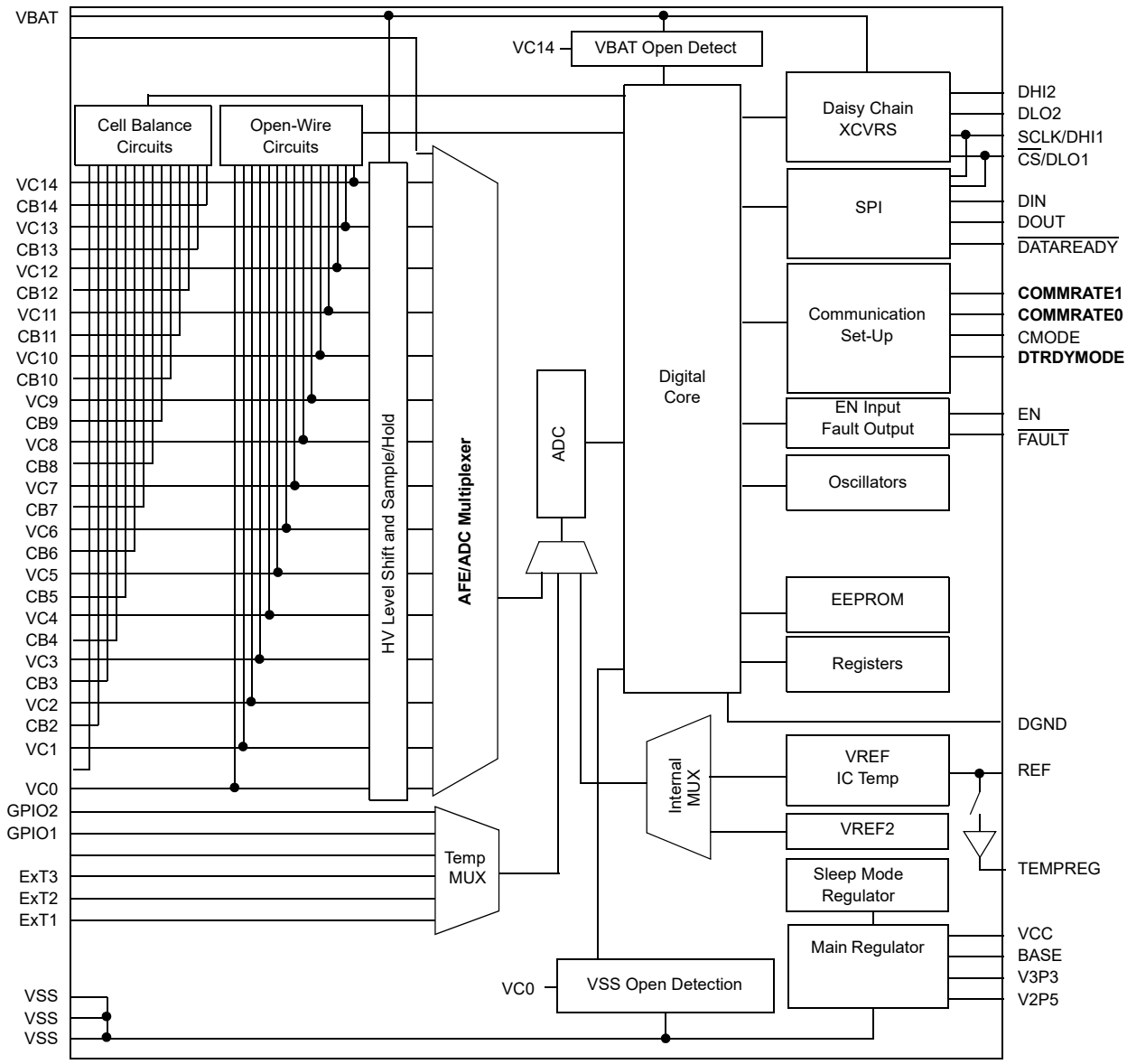


Figure 1. Block Diagram

1.2 Application Diagram

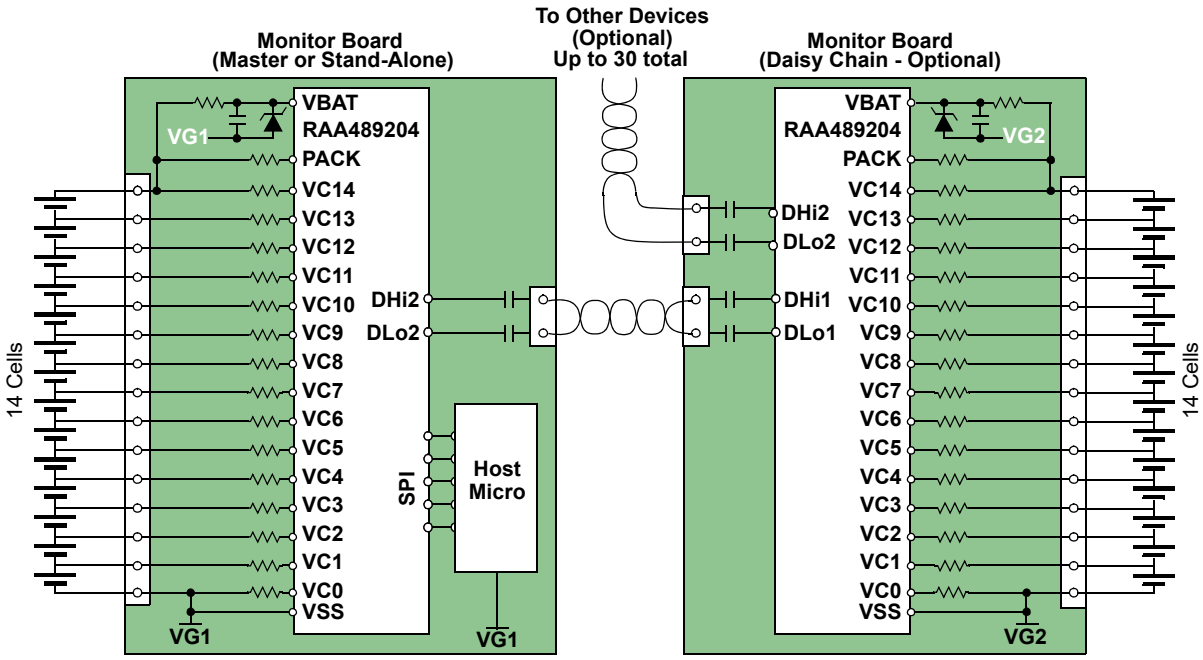
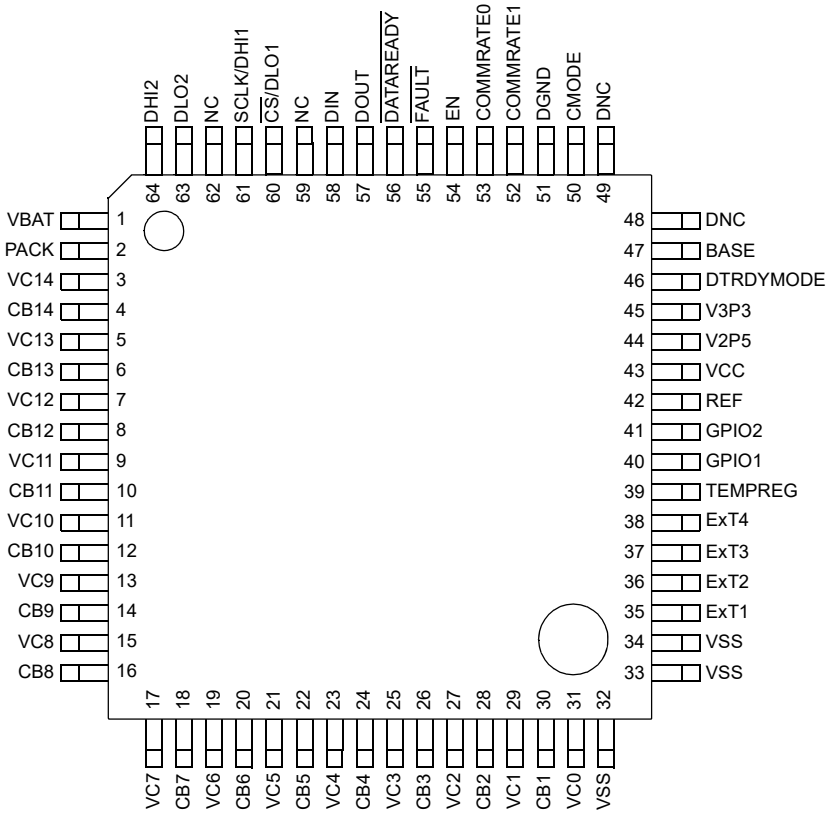


Figure 2. Typical Application

2. Pin Information

2.1 Pin Assignments



Top View

2.2 Pin Descriptions

Pin Number	Symbol	Description
1	VBAT	Main IC supply pins – 10V to 65V. Connect to the most positive terminal in the battery string.
2	PACK	Battery pack voltage input – Measures pack voltage and provides power to the AFE high voltage circuits. Connect to the most positive terminal in the battery string.
3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31	VC[14:0]	Battery cell voltage inputs – VCn connects to the positive terminal of CELLn and the negative terminal of CELLn+1. (VC14 connects only to the positive terminal of CELL14 and VC0 only connects with the negative terminal of CELL1). Recommended input range (per cell) is -5V to +5V.
4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30	CB[14:1], CB2, CB3, CB4, CB5, CB6, CB7, CB8, CB9, CB10, CB11, CB12, CB13, CB14	Cell balancing outputs – In external balancing mode, each output controls an external FET that provides a current path around the cell to provide balancing. In internal balancing mode, each output can be connected to its associated VC pin to allow balancing without the use of external FETs.
32, 33, 34	VSS	Ground – These pins connect to the most negative terminal in the battery string.
35, 36, 37, 38	ExT1, ExT2, ExT3, ExT4	External temperature monitor or general purpose analog inputs – The temperature inputs are intended for use with external resistor networks using NTC type thermistor sense elements, but can also be used as general purpose analog inputs at the discretion of the user. 0V to 2.5V input range.

Pin Number	Symbol	Description
40, 41	GPIO1, GPIO2	General purpose I/O pins – Can be used as external temperature monitor or general purpose inputs or provide output control of external circuits. As temperature inputs, they are intended for use with external resistor networks using NTC type thermistor sense elements. As general purpose analog inputs, the external circuits are implemented at the discretion of the user. GPIO pins have a 0V to 2.5V input range. As an output the GPIO1 and GPIO2 pins are controlled by register bits. 0V to 3.3V output range.
39	TEMPREG	Temperature monitor reference output – A switched 2.5V output that supplies the REF voltage to external NTC thermistor circuits to provide ratiometric ADC inputs for temperature measurement.
42	REF	2.5V voltage reference decoupling pin – Connect a 2.2µF capacitor to VSS.
43	VCC	Analog supply voltage input – Connect to V3P3 using a 33Ω resistor. Connect a 1µF capacitor to ground.
44	V2P5	Internal 2.5V digital supply decoupling pin – Connect a 1µF capacitor to DGND.
45	V3P3	3.3V digital supply voltage input – Connect the emitter of the external NPN regulator transistor to this pin. Connect a 1µF capacitor to ground.
46	DTRDYMODE	$\overline{\text{DATAREADY}}$ mode programming pin – Connect to DGND for normal $\overline{\text{DATAREADY}}$ handshake function. Connect to V3P3 for SPI Block mode data transfer function.
47	BASE	Regulator control pin – Connect the external NPN transistor base. Do not let this pin float.
50	CMODE	Communications Port 1 mode pin – Connect to V3P3 for Daisy Chain (Mid or Top stack device). Connect to GND for SPI (Daisy Chain Master or stand-alone devices).
51	DGND	Digital Ground
53, 52	COMMRATE0, COMMRATE1	Daisy Chain communications data rate setting – Connect to DGND for ‘0’ or to V3P3 for ‘1’. Data rate settings are: ‘00’ = 333kHz ‘01’ = 500kHz ‘11’ = 1MHz See Table 12.
54	EN	Enable input – Internally pulled up to V3P3 to enable the part. Tie to DGND to disable the IC. The enable logic is Internally pulled low by an open-drain function in response to an HReset command.
55	$\overline{\text{FAULT}}$	Logic fault output – Asserted Low if a fault condition exists. The logic output range is 0V to V3P3.
56	$\overline{\text{DATAREADY}}$	SPI data ready – Pin asserted Low when data is ready to be transmitted to microcontroller. The logic output range is 0V to V3P3.
57	DOUT	SPI serial data output (MISO) – The output range is 0V to V3P3.
58	DIN	SPI serial data input (MOSI)
60	$\overline{\text{CS}}$/DLO1	SPI chip-select. – (Active Low input). Daisy Chain Port 1 low connection
61	SCLK/DHI1	SPI serial clock input Daisy Chain Port 1 high connection
63, 64	DLO2, DHI2	Daisy Chain Port 2 connections
48, 49	DNC	Do not connect
59, 62	NC	No internal connections

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Voltage Relative to VSS, unless otherwise specified

Parameter	Minimum	Maximum	Unit
VBAT, PACK	-0.5	70	V
DHI1, DLO1, DHI2, DLO2	-0.5	54	V
VC0, VC1	-0.5	9	V
VC2	-0.5	18	V
VC3, VC4	-0.5	27	V
VC5, VC6	-0.5	36	V
VC7, VC8	-0.5	45	V
VC9, VC10	-0.5	63	V
VC11, VC12	-0.5	63	V
VC13, VC14	-0.5	70	V
VCn (for n = 0 to 14)	-0.5	VBAT + 0.5	V
VC5 to VC6, VC7 to VC8, VC9 to VC10, VC11 to VC12, VC13 to VC14, PACK to VBAT	-9.5	9.5	V
CBn (for n = 1 to 14)		VBAT + 0.5	V
CBn - VC(n-1) (for n = 1 to 11)	-0.5	9.0	V
VCn - CBn (for n = 12 to 14)	-0.5	9.0	V
DIN, DOUT, $\overline{\text{DATAREADY}}$, $\overline{\text{FAULT}}$, CMODE, DTRDYMODE, TEMPREG, REF, V3P3, VCC, COMM RATE n, EN, BASE, and when CMODE connected to DGN: SCLK, $\overline{\text{CS}}$,	-0.2	5.5	V
ExTn, GPIO1, GPIO2	-0.2	4.1	V
V2P5	-0.2	3.1	V

3.2 ESD Ratings

ESD Rating	Value	Unit
Human Body Model (Tested per JS-001-2017)	3500	V
Charge Device Model (Tested per JS-002-2018)	1000	V
Latch-Up (Tested per JESD-78B; Class 2, Level A)	100	mA

3.3 Thermal Information

Package Description	Thermal Resistance (Typical)	
	θ_{JA} (°C/W)	θ_{JC} (°C/W)
64 Ld TQFP Package[1][2]	43	8

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379.
2. For θ_{JC}, the case temperature location is taken at the package top center.

Parameter	Minimum	Maximum	Unit
Maximum Continuous Package Power Dissipation		400	mW
Storage Temperature	-55	+125	°C
Maximum Operating Junction Temperature		+125	°C
Pb-Free Reflow Profile	See TB493.		

3.4 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Voltages Relative to VSS, Unless Otherwise Specified			
T_A, Ambient Temperature Range	-40	+85	°C
VBAT, PACK	10	65	V
VCn, CBn (for n = 1 to 14)	-0.3	VBAT + 0.5	V
VCn - VC(n-1) (for n = 2 to 14)	-0.3	5.0	V
VC1	VC0 - 0.1	VC0 + 5.0	V
VC0	-0.1	+0.1	V
CBn - VC(n-1) (for n = 1 to 11)	-0.3	5.5	V
VCn - CBn (for n = 12 to 14)	-5.5	0.5	V
VC5, VC6	-0.3	36	V
DIN, SCLK, $\overline{CS}$, COMMRATE0, COMMRATE1, EN, DTRDYMODE, CMODE	0	3.6	V
ExT1, ExT2, ExT3, ExT4, GPIO1, GPIO2 Input Voltages	0	2.5	V
DGND	-10	10	mV

3.5 Electrical Specifications

V_{BAT} = 49V, T_A = 25°C, unless otherwise specified. Biasing set-up as in Figure 42 and Figure 43 or equivalent.

Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max[1]	Unit
Measurement Specifications						
Cell Voltage Input Measurement Range	V_{CELL}	VC(n) - VC(n-1) for design reference	-0.3		5	V
Cell Monitor Voltage Resolution	$V_{CELLRES}$	[VC(n)-VC(n-1)] LSB step size (15-bit signed number), 5V full-scale value		0.153		mV
Initial Cell Monitor Voltage Error[3]	ΔV_{CELL}	1.65V < V_{CELL} < 4.28V across -20°C to +60°C	-10		10	mV

V_{BAT} = 49V, T_A = 25°C, unless otherwise specified. Biasing set-up as in Figure 42 and Figure 43 or equivalent. **(Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max[1]	Unit
PACK Monitor Voltage Resolution	$PACK_{RES}$	ADC resolution referred to input (V_{BAT}) level. 16-bit unsigned number. Full-scale value = 78.6432V.		1.2		mV
Initial PACK Monitor Voltage Error.	ΔPACK	Measured at PACK = 23V to 60V;	-230		230	mV
External Temperature Monitoring Regulator	V_{TEMP}	$V_{TEMPREG}$ - V_{REF} (no load on $V_{TEMPREG}$),	**-20**		**20**	mV
External Temperature Output Impedance	R_{TEMP}	Output impedance at TEMPREG pin.		0.5		Ω
External Temperature and GPIO Input Pull-Up	$R_{EXTTEMP}$	Pull-up resistor to V3P3 applied to each input during measurement.		9.5		MΩ
External Temperature and GPIO Input Range	V_{EXTRNG}	Effective ExTn and GPIO input voltage range. For design reference. This is the input voltage range that does not trigger an open input condition. V_{BAT} = 49.0V	0		2.422	V
External Temperature and GPIO Input Offset	V_{EXTOFF}	V_{BAT} = 49.0V	-5		5	mV
External Temperature Input and GPIO Full Scale Error	V_{EXTG}	Absolute, V_{BAT} = 49.0V. {Measurement value} minus {Voltage measured at pin} Voltage at pin = 2.5V	-30		30	mV
		Ratiometric (relative to $V_{TEMPREG}$) V_{BAT} = 49.0V.	-30		30	mV
Internal Temperature Monitor Error	V_{INTMON}			±5		°C
Internal Temperature Monitor Resolution	T_{INTRES}	Output resolution (LSB/°K). 16-bit unsigned number		128		LSB/°K
Internal Temperature Monitor Output	T_{INT25}	Output count at +25°C		38144		Decimal
Power-Up Specifications						
Power-Up Condition Threshold	V_{POR}	V_{BAT} voltage (rising)	4.7	5.3	5.9	V
Power-Up Condition Hysteresis	V_{PORhys}			400		mV
Enable Pin Minimum Pulse Width	t_{EN}	Minimum EN low time needed to force device re-enable[2]	50			µs
Initial Power-Up Delay	t_{POR}	Time after VPOR condition (EN tied to V3P3 pin) V_{REF} = 0V to 0.95 x V_{REF} (nominal); Communication with the device is possible after this delay			26	ms
Enable Pin Power-Up Delay	t_{PUD}	Delay after EN transitions from Low to High V_{REF} = 0V to 0.95 x V_{REF} (nominal) Communication with the device is possible after this delay			13	ms

V_{BAT} = 49V, T_A = 25°C, unless otherwise specified. Biasing set-up as in Figure 42 and Figure 43 or equivalent. **(Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max[1]	Unit
Voltage Reference/Oscillator Check Delay	t_{VREF}	Time from power-on, EN pin going High, or the end of WAKEUP command to internal voltage reference check complete and start of Oscillator check		20		ms
Oscillator Check Filter Time	t_{OSCF}	Minimum duration of Oscillator fault required for detection		100		ms
Supply Current Specifications						
V_{BAT} + V_{PACK} Supply Current	I_{VBAT1}	Non-Daisy Chain configuration. EN pin = High. CMODE pin = Low. DP2 bit = 1 (upper daisy port disabled). No communications, ADC, measurement, balancing, or open-wire detection activity (stand-alone).				
		10.0V		95		µA
		49.0V		95		µA
		65V		95	135	µA
	I_{VBAT2}	Daisy Chain configuration. EN pin = High. CMODE pin = Low. DP2 = 0 (default, upper daisy port enabled). No communications, ADC, measurement, balancing, or open-wire detection activity (Master or stand-alone).				
		10V		490		µA
		49.0V		610		µA
		65V		660	800	µA
		Peak current when Daisy Chain transmitting		20		mA
	I_{VBAT3}	Daisy Chain configuration. EN pin = High, CMODE pin = High. DP2 bit = 0 (default, upper daisy port enabled). No communications, ADC, measurement, balancing, or open-wire detection activity (Mid or Top).				
		10V		860		µA
		49.0V		1100		µA
		65V		1200	1500	µA
		Peak current when Daisy Chain transmitting		20		mA
	I_{VBAT4}	Daisy Chain configuration. EN pin = High. CMODE pin = High. DP2 = 1 (optional, upper daisy port disabled). No communications, ADC, measurement, balancing, or open-wire detection activity (Top).				
		10V		490		µA
		49.0V		610		µA
		65V		660	800	µA
		Peak current when Daisy Chain transmitting		20		mA
	$I_{VBATSLEEP1}$	Sleep mode, EN = 1; CMODE pin = Low and DP2 = 0 (Device Enabled in Stand-Alone with Upper daisy port enabled) or CMODE pin = High and DP2 = don't care (Device enabled in any Daisy Chain mode).				
		10V		38		µA
		49.0V		39		µA
		65V		40		µA

V_{BAT} = 49V, T_A = 25°C, unless otherwise specified. Biasing set-up as in Figure 42 and Figure 43 or equivalent. **(Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max[1]	Unit
V_{BAT} + V_{PACK} Supply Current (Cont.)	$I_{VBATSLEEP2}$	Sleep mode EN = 1; CMODE pin = Low, DP2 = 1 (Stand-Alone with upper daisy port disabled.)		22		µA
	$I_{VBATSHDN}$	Shutdown. Device off (EN = 0)				
		10V		19		µA
		49.0V		19		µA
		65V		19	75	µA
V_{BAT} Incremental Supply Current, Balancing	$I_{VBATBAL}$	All balancing circuits on. Incremental current: Add to non-balancing V_{BAT} current. V_{BAT} = 49.0V	320	365	410	µA
Cell Input Current, Device Operating[4]	I_{VCELL}	VC0 input	-1.8	-1	-0.3	µA
		VC1 input	0.0	1	1.8	µA
		VC2, VC3, VC4, VC5, VC6, VC7, VC7, VC9, VC10, VC11, VC12, VC13 inputs	0.6	2	3.6	µA
		VC14 input	0.3	1	1.8	µA
Cell Input Current - Device off[4]	I_{VCELL_OFF}	Pins: VC0, VCn (n = 1 to 14); EN = 0; or EN =1 and in Sleep Mode.		±10		nA
V3P3 Supply Current	I_{V3P3}	Device enabled; no measurement activity, Normal mode; V_{BAT} = 65V	1.0	1.5	2.0	mA
V_{CC} Supply Current	I_{VCC}	Device enabled (EN = 1); V_{BAT} = 65V. No ADC or Daisy Chain communications active	2.4	3.5	4.5	mA
	$I_{VCCPEAK}$	V_{BAT} = 6 to 65V. Device enabled (EN = 1). Peak current when ADC active. *Note:* peak current is very short duration. Average current is not significantly affected.		6.0		mA
Supply/Reference Voltage Specifications						
V_{3P3} Regulator Voltage (Normal)	V_{3P3N}	EN = 1, load current range 0 to 5mA. V_{BAT} = 49.0V	3.25	3.35	3.45	V
V3P3 Regulator Voltage (Sleep)	V_{3P3S}	EN = 1, No load. (SLEEP) V_{BAT} = 49.0V	2.6	2.8	3.0	V
V_{REF} Reference Voltage	V_{REF}	EN = 1, no load, Pack voltage = 49.0V, +25°C, Normal mode		2.5		V
$_{VREF2}$ Second Reference Voltage	V_{REF2}	V_{BAT} = 49V	**2.488**	**2.5**	**2.512**	V
Over-Temperature Protection Specifications						
Internal Temperature Limit Threshold	T_{INTSD}	Temperature rising Auto Balance stops and scan continuous stops.		139		°C
External Temperature Limit Threshold	T_{XT}	Programmable, 0 to VREF *Note:* External temperature input voltage higher than 31/32 of Full Scale are registered as open input faults.	0		16383	Digital

V_{BAT} = 49V, T_A = 25°C, unless otherwise specified. Biasing set-up as in Figure 42 and Figure 43 or equivalent. **(Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max[1]	Unit
Fault Detection System Specifications						
Undervoltage Threshold	V_{UV}	Programmable, 0 to 8191	0		5	V
Overvoltage Threshold	V_{OV}	Programmable, 0 to 8191	0		5	V
V_{3P3} Power-Good Window	V_{3PH}	3.3V power-good window high threshold V_{BAT} = 49.0V	3.79	3.89	3.99	V
	V_{3PL}	3.3V power-good window low threshold V_{BAT} = 49.0V	2.54	2.64	2.71	V
V_{2P5} Power-Good Window	V_{2P5H}	2.5V power-good window high threshold V_{BAT} = 49.0V	2.65	2.70	2.90	V
	V_{2P5L}[3]	2.5V power-good window low threshold V_{BAT} = 49.0V	1.85	2.03	2.24	V
V_{CC} Power-Good Window	V_{VCCH}	VCC power-good window high threshold V_{BAT} = 49.0V	3.60	3.74	3.90	V
	V_{VCCL}	VCC power-good window low threshold V_{BAT} = 49.0V	2.6	2.7	2.8	V
V_{REF} Power-Good Window	V_{RPH}	V_{REF} power-good window high threshold V_{BAT} = 49.0V	2.52	2.7	2.9	V
	V_{RPL}	V_{REF} power-good window low threshold V_{BAT} = 49.0V	2.15	2.3	2.47	V
TMUX voltage when TMUX = 1 See (Table 22)		Reference Voltage (address 6h'30)		193		mV
		GPIO 1 (address 6h'27)		386		mV
		GPIO 2 (address 6h'28)		578		mV
		Ext 1 (address 6h'21)		771		mV
		Ext 2 (address 6h'22)		963		mV
		Ext 3 (address 6h'23)		1155		mV
		Ext 4 (address 6h'24)		1347		mV
		PACK/32 (address 6h'10)		1924		mV
		Internal Temperature (address 6h'20)		2116		mV
Full Scale ADC code test	$FFSP_D$	Differential measurements (Cell 1 to Cell 14) (address 6h'01 to 6h'0E)	7FE0		7FFC	Hex
	$FFSN_D$		8000		801C	Hex
	$FFSP_S$	Single ended measurements PACK voltage, IT, ExTn, GPIOn, Reference Voltage (address 6h'10 to 6h'30)	FFE0		FFFC	Hex
	$FFSN_S$		0000		001C	Hex
Cell Open-Wire Detection (See Scan Wires (Address: C4H))						
Open-Wire Current[4]	I_{OW}	VC1 to VC14; V_{BAT} = 49.0V	0.15	0.2	0.24	mA
		VC0; V_{BAT} = 49.0V	-1.26	-1.05	-0.84	mA
Open-Wire Test On Time (see Figure 62)	t_{OWON}	WSCN = 0; V_{BAT} = 49.0V	1.4	1.6	1.9	ms
		WSCN = 1; V_{BAT} = 49.0V	4.7	5.3	6.1	ms
Primary Detection Threshold, VC0	V_{F30}	Cell1 lower connection, referred to VSS; V_{BAT} = 49.0V	1.2	1.5	1.8	V

V_{BAT} = 49V, T_A = 25°C, unless otherwise specified. Biasing set-up as in Figure 42 and Figure 43 or equivalent. **(Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max[1]	Unit
Primary Detection Threshold, VC2 to VC14	V_{F31}	Through ADC, voltage delta recorded during test; V_{BAT} = 49.0V		-0.25		V
Secondary Detection 1 Threshold, VC2 to VC14	V_{F32}	VC(n) - VC(n-1); Through ADC; V_{BAT} = 49.0V	-100	-20	-20	mV
Secondary Detection 2 Threshold, VC2 to VC14	V_{F33}	VC(n) - VC(n-1); V_{BAT} = 49.0V	-360	-180	-50	mV
Secondary Detection Threshold, VC1	V_{F34}	VC1 voltage; V_{BAT} = 49.0V	0.6	0.7	0.8	V
Open V_{BAT} Fault Detection Threshold	V_{VBO1}	V_{PACK} - V_{VBAT}; V_{BAT} = 49.0V		260		mV
Open VSS Fault Detection Threshold	V_{VSSO1}	V_{VSS} - V_{VC0}; V_{BAT} = 49.0V		240		mV
Measurement Function Timing						
Cell Sample Time Skew (One Device)		Time between sample of cell1 and sample of cell14 in a Scan Voltage command.[5]		276		µs
Cell Sample Time Skew (Daisy Chain) Figure 67		Time between start of scan in Master and start of scan in Mid Daisy Chain devices for a a Scan Voltage command, 8 devices in stack, 1MHz Daisy clock.[5]		22.5		µs
		Additional Time between start of scan in Mid to Top Daisy Chain devices, 1MHz Daisy clock[5]		1		µs
Cell Sample Time skew (Eight Daisy Chain Devices)		Time between sample of cell1 and sample of Cell 112 in a Scan Voltage command[5]		300		µs
Scan Voltages Processing Time		Time from start of scan to registers loaded and ready to read. (See Figure 67 and Table 49)		589		µs
Scan Mixed Processing Time		Time from start of scan to registers loaded and ready to read. (See Figure 67 and Table 49)		665		µs
Scan Temperatures Processing Time		Time from start of scan to registers loaded and ready to read. (See Figure 67 and Table 49)		3.5		ms
Scan Wires Processing Time		Time from start of scan to registers loaded and ready to read. (See Figure 67 and Table 49)		3.5		ms
Scan All Processing Time		Time from start of scan to registers loaded and ready to read. (See Figure 67 and Table 49)		4.5		ms
Cell Balance Output Specifications						
Cell Balance Pin Output Impedance	R_{CBL}	CBn output off impedance; CB output off between CB(n) to VC(n-1): cells 1 to 11, and between CB(n) to VC(n): cells 12 to 14	2	4	5	MΩ
Cell Balance Output Current	I_{CBH1}	CBn output on. External balance mode. CB(N) - CB(N-1); (CB1 to CB11); V_{BAT} = 49.0V	-29	-25	-21	µA
	I_{CBH2}	CBn output on. External balance mode. CB(N) - CB(N-1); (CB12 to CB14); V_{BAT} = 49.0V	21	25	29	µA
Cell Balance Output Leakage in Shutdown	I_{CBSD}	EN = GND; VBAT = 49.0V	-750	0	750	nA

V_{BAT} = 49V, T_A = 25°C, unless otherwise specified. Biasing set-up as in Figure 42 and Figure 43 or equivalent. **(Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max[1]	Unit
Internal Cell Balance Output Clamp	VCBCL	I_{CB} = 100µA; V_{BAT} = 49.0V	9			V
Internal Cell Balance Switch ON-Resistance	VCBR	I_{CB} = 30mA; V_{BAT} = 49.0V; CELL1 to CELL11		9.5		Ω
		I_{CB} = 30mA; V_{BAT} = 49.0V; CELL12 to CELL14		10.1		Ω
Logic Inputs: SCLK, $\overline{CS}$, DIN						
Low Level Input Voltage	V_{IL}				0.8	V
High Level Input Voltage	V_{IH}		1.75			V
Input Hysteresis	V_{HYS}		100			mV
Input Current	I_{IN}	0V < V_{IN} < V3P3	-1		+1	µA
Input Capacitance	C_{IN}				10	pF
Logic Inputs: EN, COMMRATE 0, COMMRATE 1, CMODE						
Low Level Input Voltage	V_{IL}				0.3 × V3P3	V
High Level Input Voltage	V_{IH}		0.7 × V3P3			V
Input Hysteresis	V_{HYS}		0.05 × V3P3			V
EN Pin Input Resistance	R_{EN}	Internal Resistance between EN pin and V3P3 pin		2.5		MΩ
COMMRATE0, COMMRATE1, CMODE Pin Input Current	I_{IN}	0V < V_{IN} < V3P3	-1		+1	µA
Input Capacitance	C_{IN}				10	pF
Logic Outputs: DOUT, $\overline{FAULT}$, $\overline{DATAREADY}$						
Low Level Output Voltage	VO_L	At 3mA sink current; V_{BAT} = 49.0V			0.4	V
High Level Output Voltage	VO_H	At 3mA source current; V_{BAT} = 49.0V	V3P3 - 0.4			V
Logic Outputs: GPIO1, GPIO2 (as Output)						
Low Level Output Voltage	LVO_L	At 1mA sink current; V_{BAT} = 49.0V			0.4	V
High Level Output Voltage	LVO_H	At 1mA source current; V_{BAT} = 49.0V	V3P3 - 0.4			V
SPI Interface Timing (See Figure 3 and Figure 4)						
SCLK Clock Frequency	f_{SCLK}	V_{BAT} = 49.0V			2.0	MHz
Pulse Width of Input Spikes Suppressed	t_{IN1}	V_{BAT} = 49.0V	50		200	ns
Chip Select Lead Time	t_{LEAD}	Chip select Low to first SCLK rising edge; V_{BAT} = 49.0V	200			ns

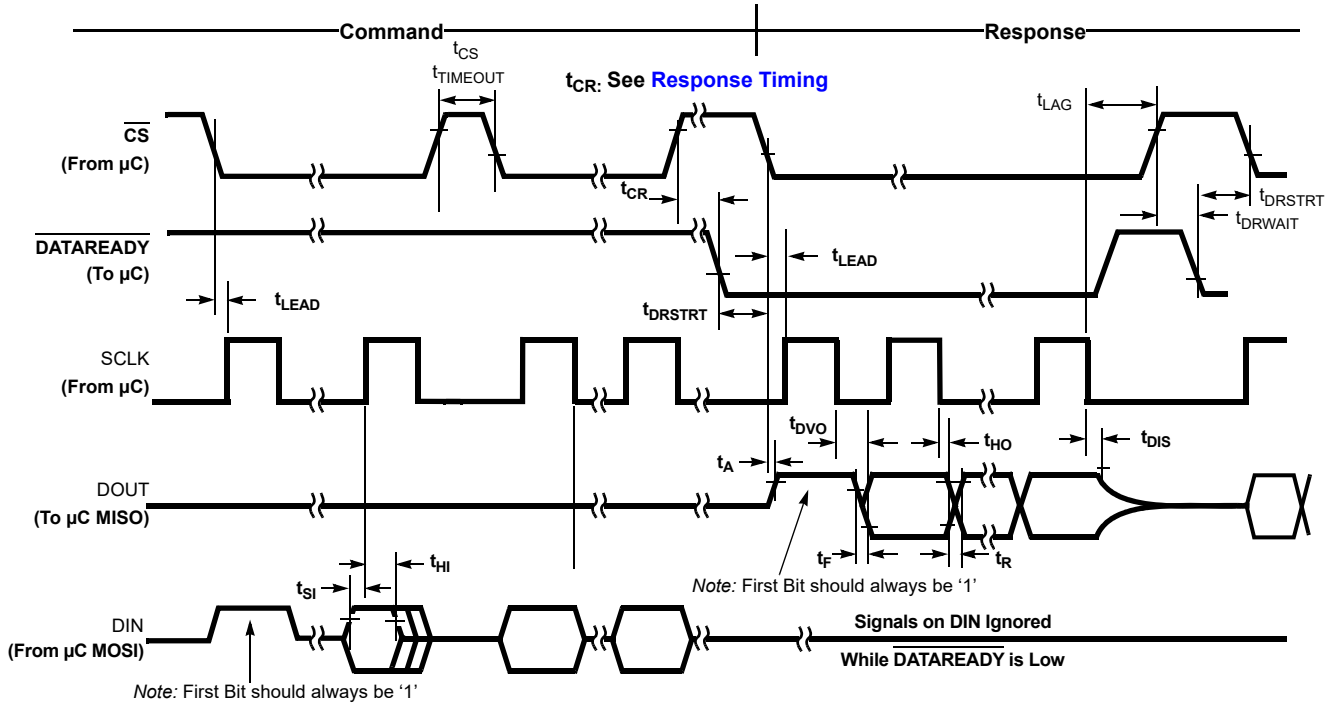
V_{BAT} = 49V, T_A = 25°C, unless otherwise specified. Biasing set-up as in Figure 42 and Figure 43 or equivalent. **(Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max[1]	Unit
Clock High Time	t_{HIGH}	V_{BAT} = 49.0V[6]	200			ns
Clock Low Time	t_{LOW}	V_{BAT} = 49.0V[6]	200			ns
DOUT Rise Time	t_R	Up to 50pF load			30	ns
DOUT Fall Time	t_F	Up to 50pF load			30	ns
Chip Select Lag Time	t_{LAG}	Falling edge of 8th SCLK clock to $\overline{CS}$ High; (Byte Mode) V_{BAT} = 49.0V	250			ns
Data Input Set-Up Time	t_{SI}	DIN valid before rising edge of SCLK; V_{BAT} = 49.0V	100			ns
Data Input Hold Time	t_{HI}	DIN to remain valid following rising edge of SCLK; V_{BAT} = 49.0V	80			ns
Slave Access Time	t_A	$\overline{CS}$ Low to DOUT active; V_{BAT} = 49.0V			200	ns
Data Output Valid Time	t_{DVO}	DOUT valid after falling edge of SCLK; V_{BAT} = 49.0V[7]			350	ns
Data Output Hold Time	t_{HO}	DOUT valid after falling edge of SCLK; V_{BAT} = 49.0V	0			ns
Chip Select High Time	t_{CS}	High time for $\overline{CS}$ between bytes (Byte Mode); V_{BAT} = 49.0V	250			ns
SPI Communications Timeout	$t_{TIMEOUT}$	Within a communication sequence, the time $\overline{CS}$ can remain High before SPI communications time out, requiring the start of a new command; V_{BAT} = 49.0V		100		µs
$\overline{DATAREADY}$ Start Time	t_{DRSTRT}	$\overline{DATAREADY}$ Low to $\overline{CS}$ Low; Microcontroller response time to start clocking data out. V_{BAT} = 49.0V	200			ns
$\overline{DATAREADY}$ Wait Time Data	t_{DRWAIT}	$\overline{CS}$ High to $\overline{DATAREADY}$ Low. Delay before the device indicates more data is ready to transmit; V_{BAT} = 49.0V			140	ns
$\overline{DATAREADY}$ Stop Time	t_{DRSTP}	Falling edge of last SCLK clock 8 to $\overline{DATAREADY}$ High (Block Mode); V_{BAT} = 49.0V	20		150	ns
$\overline{CS}$ Wait Time	t_{CSWAIT}	$\overline{DATAREADY}$ High to $\overline{CS}$ High; V_{BAT} = 49.0V; Microcontroller response time to end a data capture.	200			ns
DOUT Disable Time	t_{DIS}	DOUT disabled following the falling edge of SCLK on the last byte before CS goes High; V_{BAT} = 49.0V			240	ns
Daisy Chain Communications Interface: DHi1, DLo1, DHi2, DLo2						
Daisy Chain Clock Frequency	f_{DAISY}	COMMRATE0, COMMSRATE1 = 1, 1	880	1000	1100	kHz
		COMMRATE0, COMMSRATE1 = 0, 1	440	500	550	kHz
		COMMRATE0, COMMSRATE1 = 0, 0	290	333	364	kHz
Common-Mode Reference Voltage				$V_{BAT}/2$		V
Maximum Packet Reset Timeout				3 × $1/f_{DAISY}$		sec

1. These MIN and/or MAX values are based on characterization data and are not 100% tested.

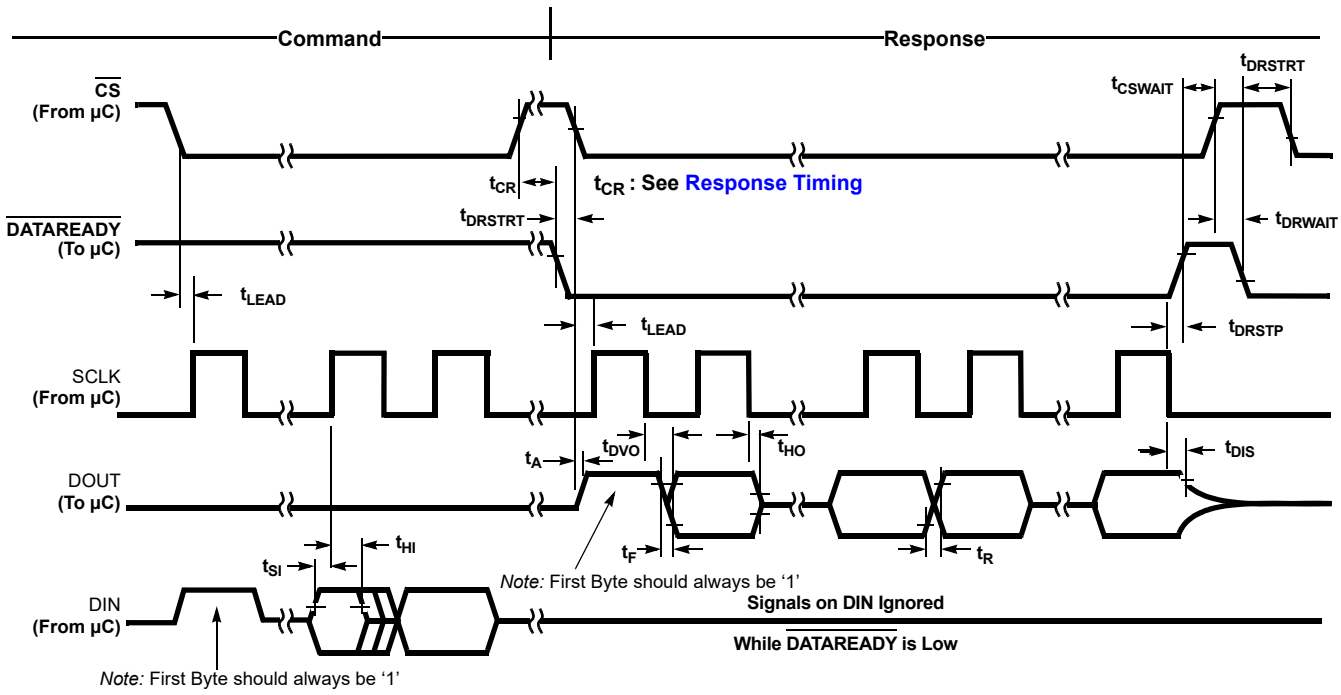
2. Compliance to data sheet limits is assured by one or more methods, including production test, characterization, and/or design.
3. Stresses can be induced in the RAA489204 during soldering or other high-temperature events that affect measurement accuracy. Initial accuracy does not include effects because of this.
4. Positive current = current into the pin.
5. Skew times are based on the designed number of internal and Daisy Chain clocks needed to perform the operation and pass the command to the stack of devices.
6. SPI SCLK and DIN inputs feature minimum pulse width filters that limit the clock rate to 2.5MHz. Contact factory for higher data rates.
7. These specifications do not include rise or fall time of SDO. Rise and fall time is dependent on the bus capacitance and the DOUT current. The DOUT current is specified above (VO_L and VO_H.) The SPI MISO setup and hold time requirements of the MCU should be met, assuming worst case bus capacitance on DOUT.

3.6 Timing Diagrams



Note: In Byte mode, the microcontroller sets $\overline{CS}$ High after eight bits of data, so the microcontroller response time (t_{LAG}) determines when $\overline{CS}$ goes High. The RAA489204 then sets $\overline{DATAREADY}$ Low in response if there are additional data bytes to transfer.

Figure 3. SPI Interface Timing (Byte Mode)



Note: In Block mode, the microcontroller waits for the RAA489204 $\overline{\text{DATAREADY}}$ signal to go High at the end of the transfer, so the delay time, t_{DRSTP}, and the microcontroller response time, t_{CSWAIT}, determine when $\overline{\text{CS}}$ goes High. The RAA489204 then sets $\overline{\text{DATAREADY}}$ Low in response if there are additional data bytes to transfer.

Figure 4. SPI Interface Timing (Block Mode)

4. Typical Performance Curves

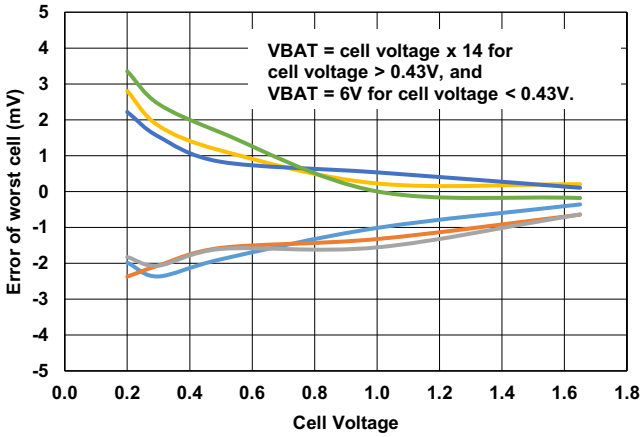


Figure 5. Max/Min Errors of Worst Cell at Low VBAT Voltages, 3 Typical Parts

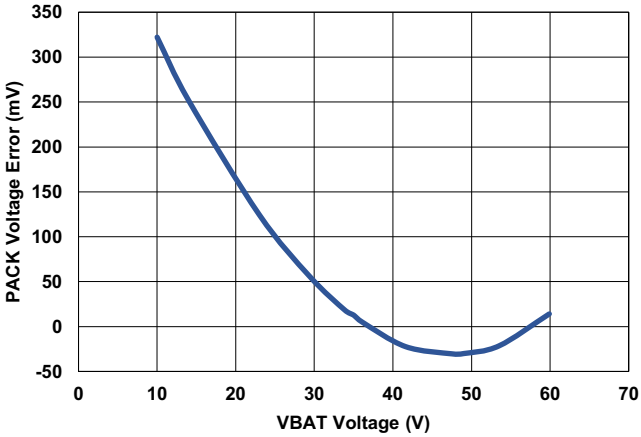


Figure 6. Pack Voltage Error, 25°C

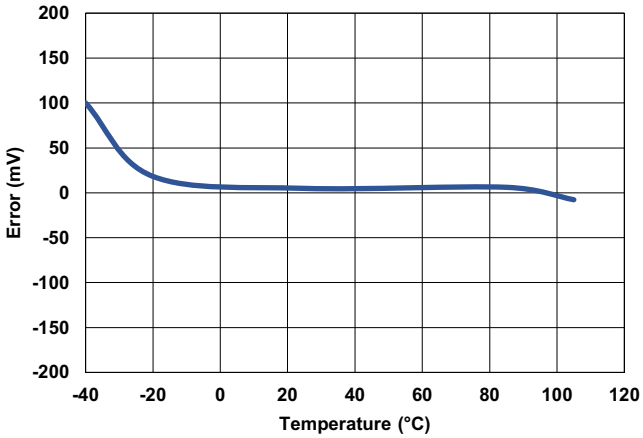


Figure 7. Pack Voltage Error, VBAT = 36V

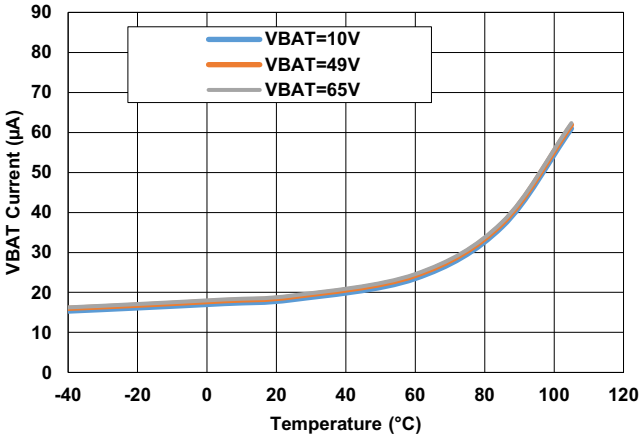


Figure 8. VBAT Sleep Current; Stand-Alone, DP2 = 1

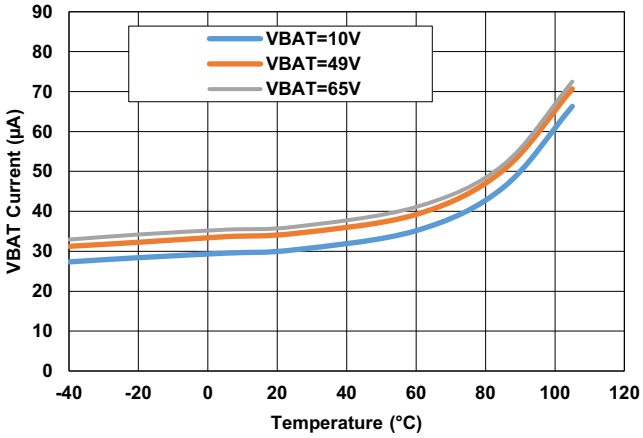


Figure 9. VBAT Sleep Current; Stand-Alone/Daisy Chain Master, DP2 = 0

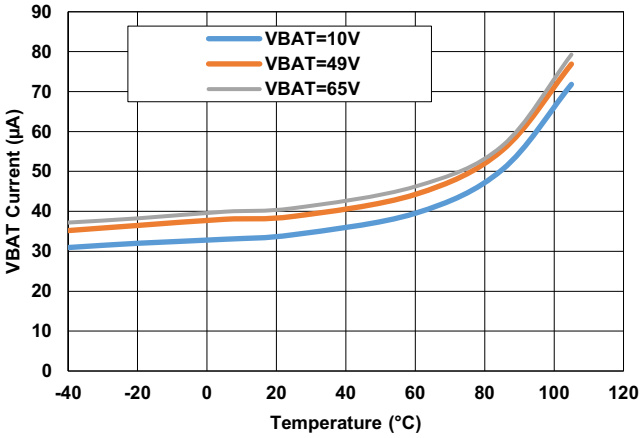


Figure 10. VBAT Sleep Current; Daisy Chain Mid/Top, DP2 = 0 or 1

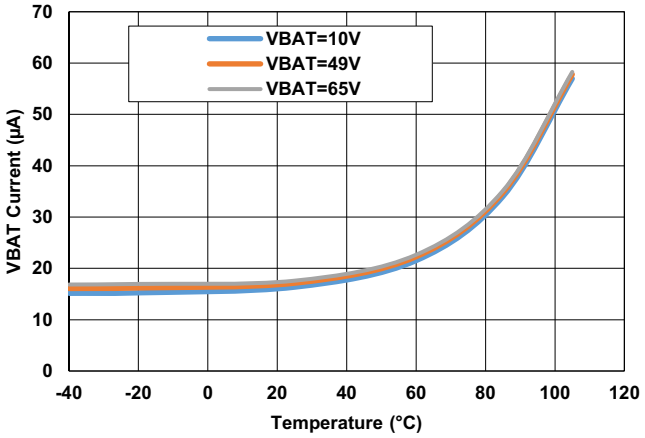


Figure 11. VBAT Shutdown Current;
Stand-Alone/Daisy Chain Master, DP2 = 0 or 1

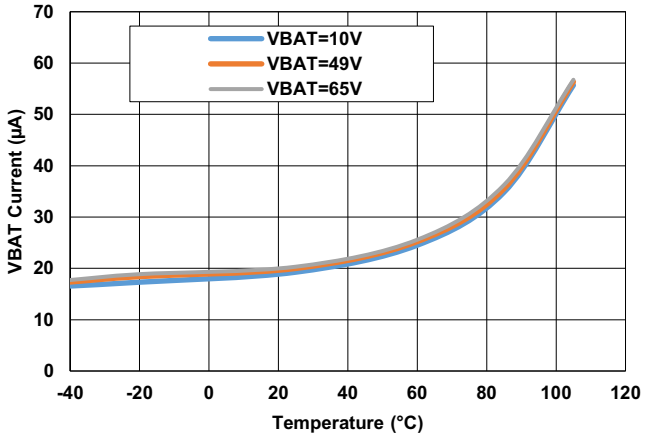


Figure 12. VBAT Shutdown Current;
Daisy Chain Mid/Top, DP2 = 0 or 1

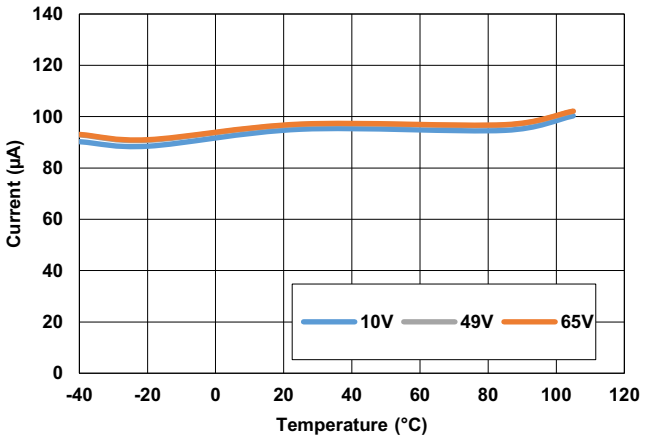


Figure 13. VBAT Supply Current;
Stand-Alone Mode

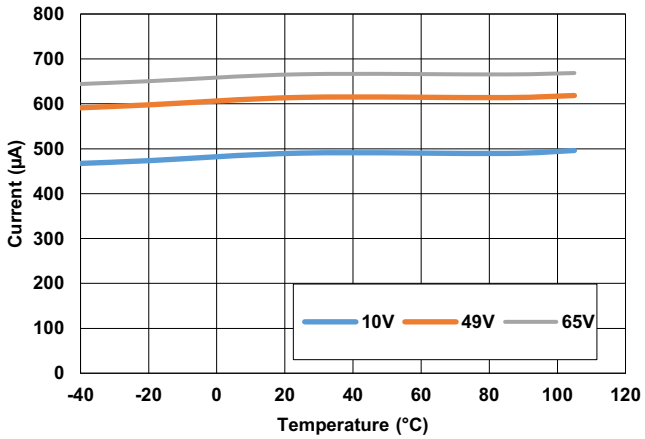


Figure 14. VBAT Supply Current;
Daisy Chain Master

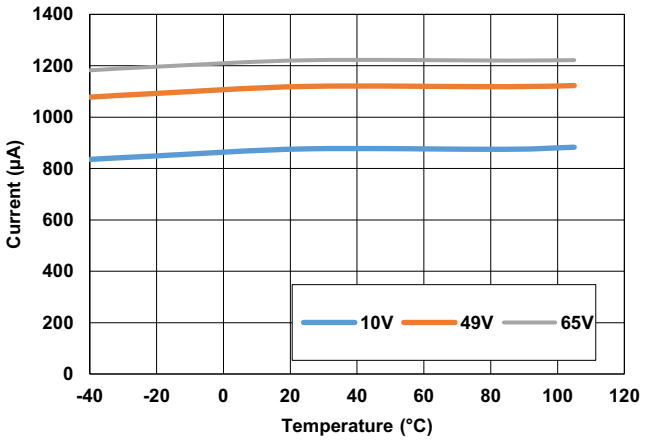


Figure 15. VBAT Supply Current;
Daisy Chain Mid

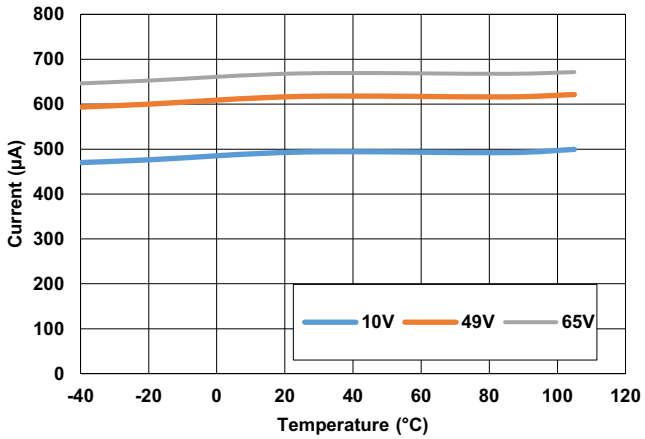


Figure 16. VBAT Supply Current;
Daisy Chain Top

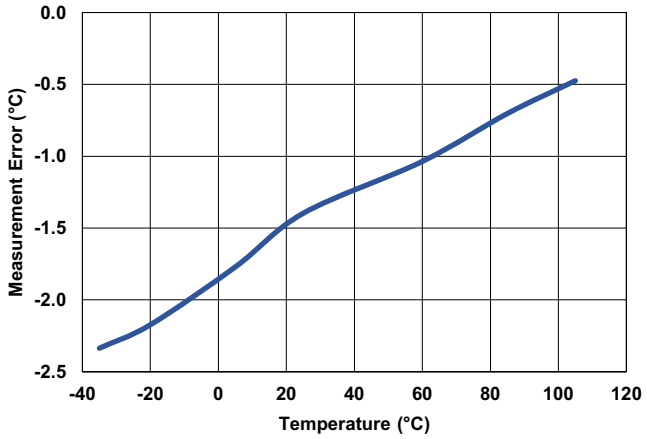


Figure 17. IC Temperature Error; VBAT = 20V to 49V

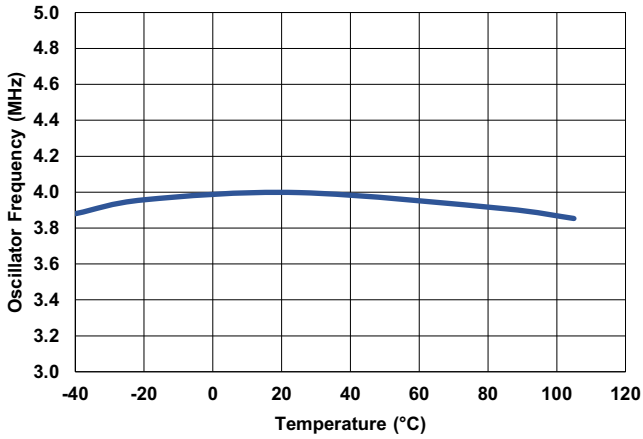


Figure 18. 4MHz Oscillator Freq; VBAT = 49V

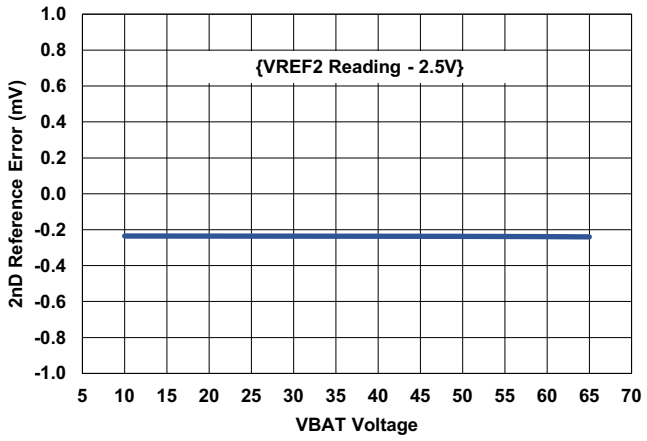


Figure 19. 2nd VREF Average Error; +25°C

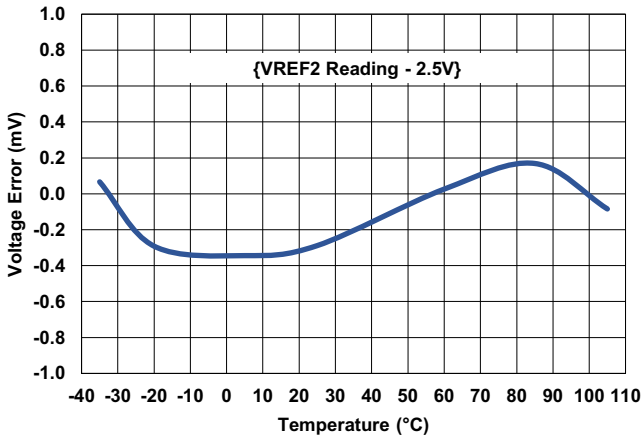


Figure 20. 2nd VREF Average Error; VBAT = 20V to 49V

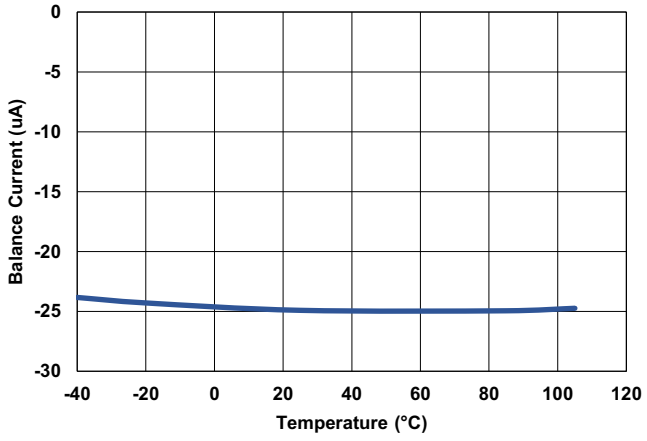


Figure 21. Cell Balance Current CB1-CB11; VBAT=49V

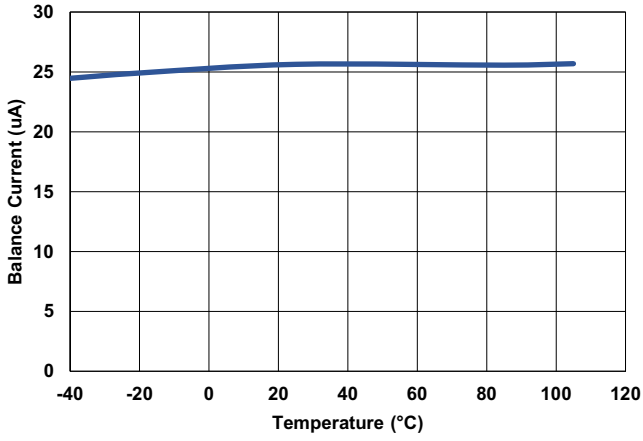


Figure 22. Cell Balance Current CB12-CB14; VBAT=49V

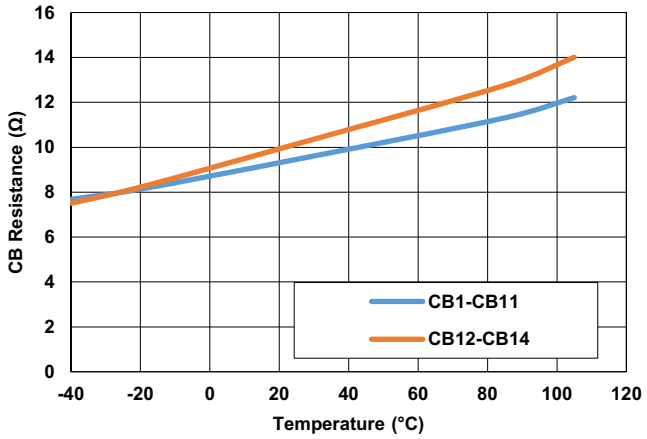


Figure 23. Internal Balance On Resistance; VBAT = 49V

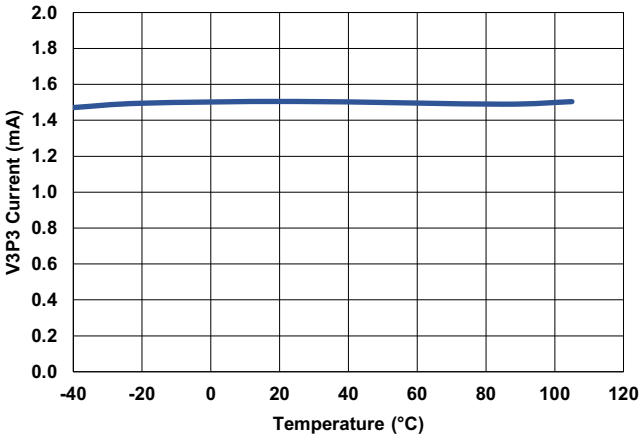


Figure 24. V3P3 Current; VBAT = 10V to 65V

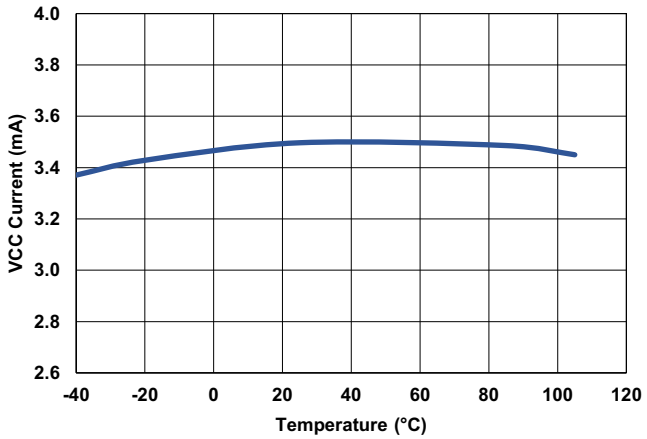


Figure 25. VCC Active Current; VBAT = 10V to 65V

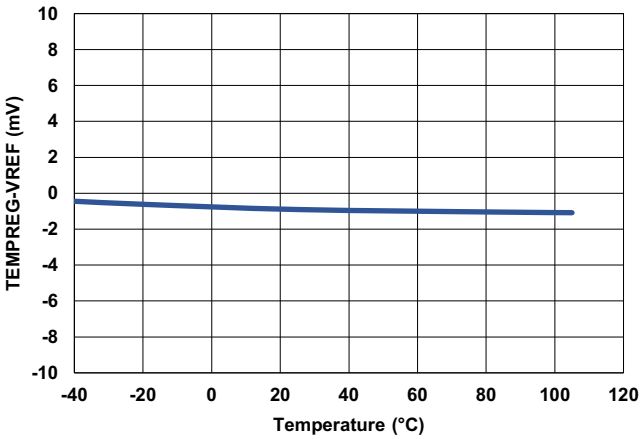


Figure 26. TEMPREG Voltage, VBAT = 10V to 65V

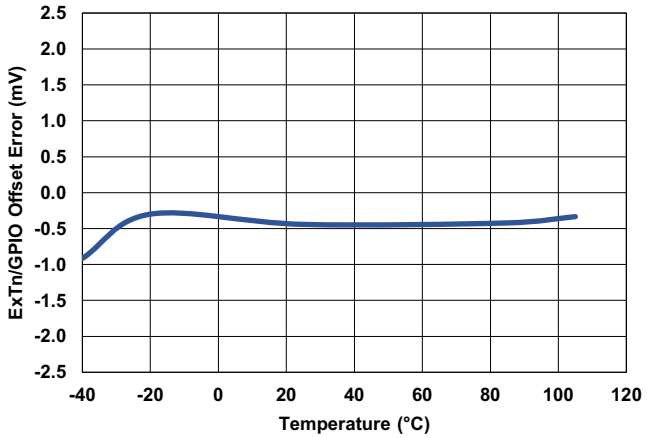


Figure 27. ExTn/GPIO Offset; VBAT = 49V

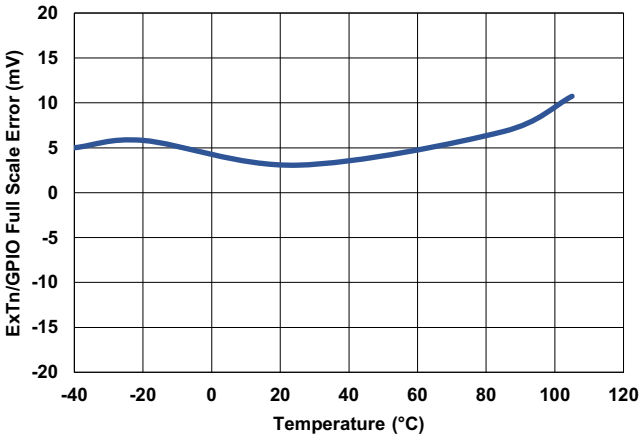


Figure 28. ExTn/GPIO Full Scale Error; VBAT = 49V

5. Device Overview

The RAA489204 is a Li-ion battery manager IC that supervises up to 14 series connected cells. Up to 30 RAA489204 devices can be connected in series to support systems with up to 420 cells using a single chain of devices. The RAA489204 provides accurate monitoring, cell balance control, and diagnostic functions. The RAA489204 includes a voltage reference, 14-bit A/D converter, and registers for control and data. An external microcontroller communicates to the RAA489204 through an SPI interface. Series-connected RAA489204 devices communicate with each other through a proprietary Daisy Chain communications interface.

The RAA489204 devices handle Daisy Chain communications differently depending on their position within the Daisy Chain. The RAA489204 at one end of the Daisy Chain acts as a Master device for communications. The Master device, also called the bottom device, occupies the first position in the Daisy Chain and communicates to a host microcontroller using an SPI interface. A single Daisy Chain port then connects the Master device to the next device in the Daisy Chain.

The device at the other end of the Daisy Chain from the Master is the Top device. The Top device has a single Daisy Chain port connection to the device below. Devices other than the Master and Top devices are Mid devices. Mid devices have two Daisy Chain port connections. The Up port connects to the device above and the Down port connects to the device below. The Master RAA489204 device is device number 1. The Top device is device number n, where n is the total number of RAA489204 devices in the Daisy Chain. The Mid devices are numbered 2 to (n-1) with device number 2 being connected to the Master device. If n = 2, there is a Master device and a Top device, with no Mid device.

When multiple RAA489204 devices are connected to a series of cells, their power supply domains are normally non-overlapping. The lower (VSS) supply of each RAA489204 nominally connects to the same potential as the upper (VBAT) supply of the RAA489204 device below.

The RAA489204 provides two multiple parameter measurement scanning modes in addition to a single parameter direct measurement capability. These scanning modes provide pseudo simultaneous measurement of all cell voltages in the stack.

The addressed device, the top device, and the bottom device act as Masters for the purposes of communications timing. All other devices are repeaters, passing data up or down the chain.

6. System Hardware Connection

6.1 Battery Connection

The first consideration in designing a battery system around the RAA489204 is the connection of the cells to the IC.

All inputs to the RAA489204 VCn pins are protected against battery voltage transients and hot plug events by RC filters. The basic input filter structure, with capacitors to the local ground, provides protection against transients and EMI for the cell inputs. These capacitors carry the loop currents produced by EMI and should be placed as close to the connector as possible. Connect the ground terminals of the capacitors directly to a solid ground plane. Do not use vias to connect these capacitors to the input signal path or to ground. Place any vias in line to the signal inputs so that the inductance of these forms a low-pass filter with the grounded capacitors.

The circuit shown in Figure 29 is a standard two stage filter arrangement on each cell input. The first stage filter provides rejection to EMC and transients while the second stage reduces any differential noise at the cell inputs. The second stage capacitors should be located close to the IC.

The resistors on the input filter also provide a current limit function during hot plug events. The RAA489204 is calibrated for use with 1kΩ series protection resistors at the VCn and PACK inputs. The VBAT connection uses a lower value input resistor to accommodate the V_{BAT} supply current of the RAA489204. As much as possible, the time constant produced by the filtering applied to VBAT should be matched to that applied to the PACK and VCn monitoring inputs, as shown in Figure 29.

The filtered battery voltage connects to the internal cell voltage monitoring system. The monitoring system comprises three basic elements; a level shifter to eliminate the cell common-mode voltage, a multiplexer to select a specific input and an analog-to-digital conversion of the cell voltage.

Each RAA489204 is calibrated over-temperature assuming an input series resistance of 1kΩ. Cell voltage measurement error data is given in Measurement Specifications for various voltage and temperature ranges. Plots showing the typical error distribution over the full input range are included in the Typical Performance Curves section.

Account for input filter time constant effects when evaluating measurement accuracy. An interaction between the RAA489204 scanning action and the input filters that results in a small but predictable scan error signature. With the component values shown in Figure 29, the scan error signature is shown in Table 1. Subtract these values from the cell voltages read out of the RAA489204.

Table 1. Scan Error Signature for Figure 29

Input	Voltage Shift Due to Input Filter (mV)
Cell 1	0
Cell 2	0.07
Cell 3	-0.18
Cell 4	-0.37
Cell 5	-0.43
Cell 6	-0.43
Cell 7	-0.42
Cell 8	-0.42
Cell 9	-0.42
Cell 10	-0.42
Cell 11	-0.42
Cell 12	-0.42
Cell 13	-0.41
Cell 14	-0.35

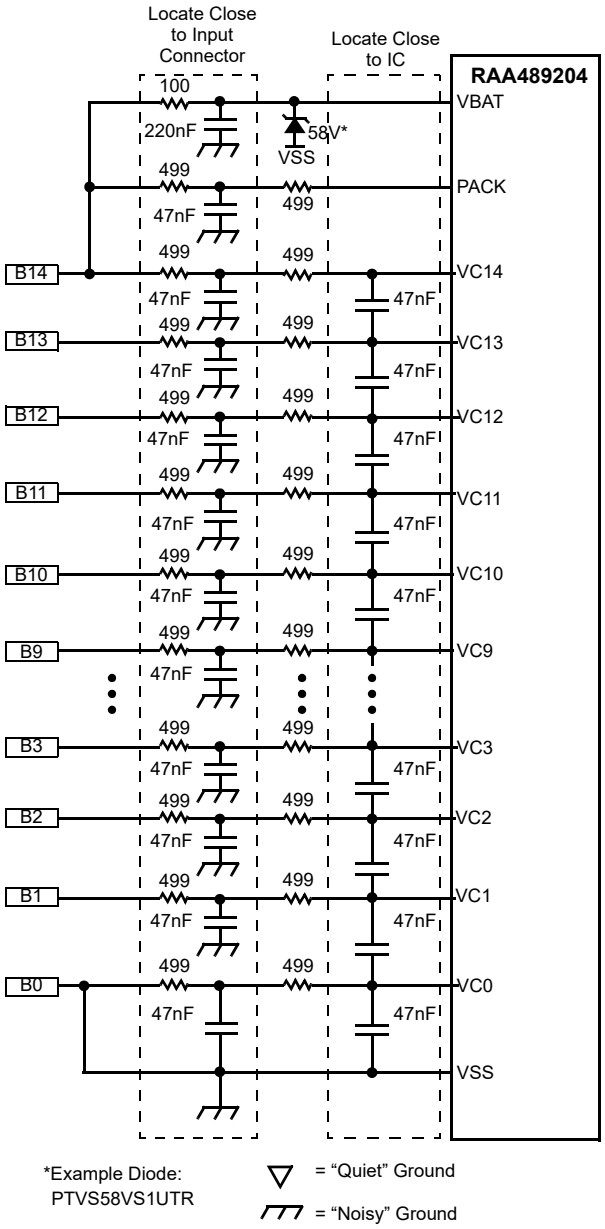


Figure 29. Typical Battery Connection Circuits

Another important consideration is the connection of cells in a stacked configuration. This primarily involves connecting the supply and ground pins at the junction of two devices. The preferred connection has four wires between the battery and the two devices, but this does pose a cost constraint. To minimize the connections, the power and monitor pins can be connected separately. This option (Option 1) is shown in Figure 30. Back-to-back diodes between the power and monitor pins keeps communications active and allow open-wire detection to work when one of the two wires opens from the battery stack. A second configuration (Option 2) has one connection wire to VC0/VSS of the upper device and one wire to VBAT/PACK/VC14 of the lower device, see Figure 31. For Option 2, additional diodes between VC0/VC1 and VC13/PACK provide supply current paths that allow the device to operate sufficiently to detect a connection fault in the case of an open battery connection.

Renesas recommends using a thicker wire to connect the supply and ground points to the battery pack. This helps minimize any IR drop related measurement errors on the top and bottom cell of each RAA489204. If a single wire is used between the battery and a common power/ground point on the board, a break in this wire would be detected as either a VSS connection issue on the upper RAA489204 or a VBAT connection issue on the lower RAA489204, but not both.

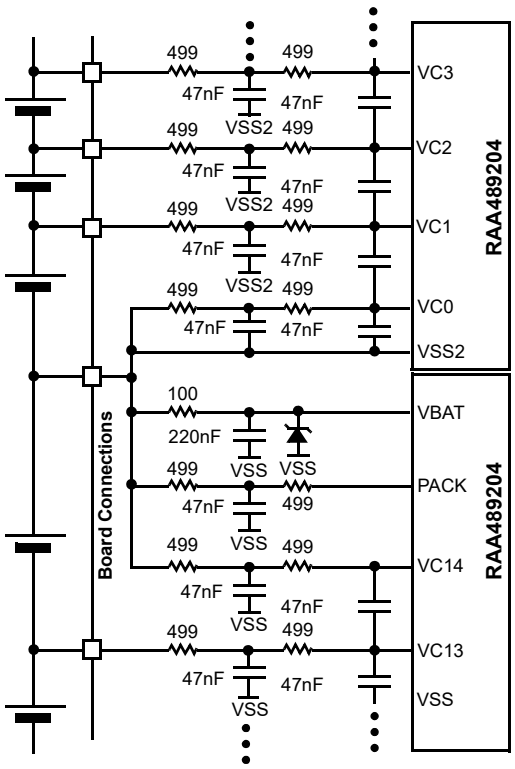


Figure 30. Battery Connection Between Stacked Devices (Option 1)

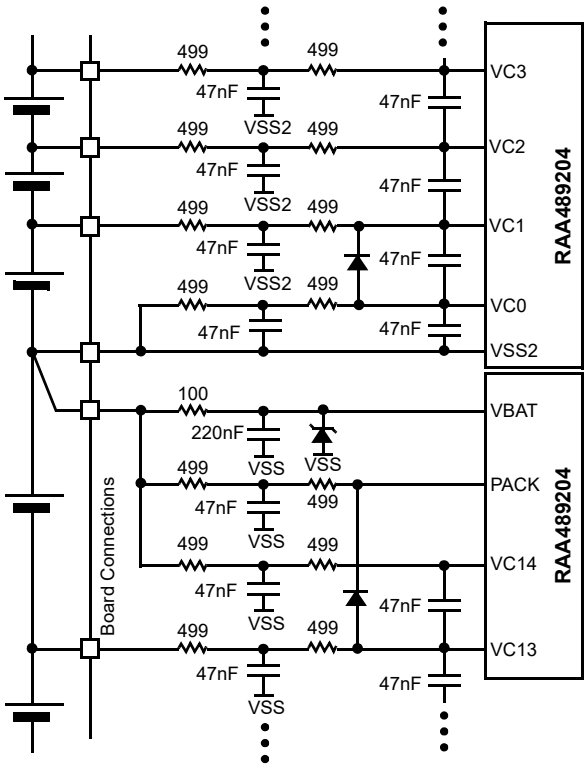


Figure 31. Battery Connection Between Stacked Devices (Option 2)

6.2 Cell Balance Connection

Cell balancing is an important function in a battery pack that consists of a stack of multiple Li-ion cells. As the cells charge and discharge, differences in each cell's ability to collect and release charge typically leads to cells with different states of charge. The problem with a stack of cells having different states of charge is that Li-ion cells have a maximum voltage above which it should not be charged, and a minimum voltage below which it should not be discharged. The extreme case, where one cell in the stack is at the maximum voltage and one cell is at the minimum voltage, results in a nonfunctional battery stack, because the battery stack cannot be charged or discharged.

The RAA489204 offers both internal and external balancing. The CB1 to CB14 outputs are controlled either directly, or indirectly by an external microcontroller through bits in various control registers.

6.2.1 External Balancing FETs

To select external balancing, set the IBAL bit (Bit 8) in the BALANCE SETUP Register to '0'. This is the default setting.

Using external balance elements (consisting of an external MOSFET, balance resistor, and related components) provides a more robust cell balance connection. The external balancing FETs are controlled by current sources or current sinks on the cell balancing (CBn) pins derived from nominal 25µA on-chip current sources. The current sources are turned on and off as needed to control the external MOSFET devices. Voltage clamps are included at each CB output to limit the maximum gate drive voltage. Series gate resistors protect both the external FET and internal IC circuits from external voltage transient effects. An internal gate-to-source connected resistor provides a redundant gate discharge path.

A mix of N-channel and P-channel devices is used for the external FETs to remove the need for a charge pump. Cell 14, Cell 13, and Cell 12 balance positions use P-channel devices. The remaining positions use N-channel devices. The basic balance FET drive arrangement is shown in Figure 32.

The external circuit for driving the FET includes a series 10k current limit resistor, a gate-source resistor that sets the gate voltage with the 25µA drive current, and a 10nF capacitor from gate to source that protects against the incursion of EMI signals. The cell balance circuits of the RAA489204 are designed to drive FET gate voltages up to 9V. This allows the use of 60V V_{DS} rated FETs that can handle the maximum voltages applied during hot plug without any additional protection. If using lower voltage FETs, Renesas recommends adding a 1nF capacitor be added across the FET gate to drain terminals. This capacitor, as shown in Figure 32, provides a self protecting mechanism for the lower voltage FET whereby a fast transient causes the FET to turn on momentarily, therefore limiting the maximum V_{DS} voltage.

Choose the external component values to prevent the 9V clamp at the output of the RAA489204 from activating.

6.2.1.1 External Balance Circuit (Preferred)

The VCn pin in Figure 32 monitors the voltage after the cell balance resistor. This configuration allows the system to diagnostically evaluate the cell balance external circuits. When the cell balance is turned on for a specific cell, the input voltage should drop to near 0V. If it does not, there is a problem with the external balance circuits. This connection is also shown in Figure 33.

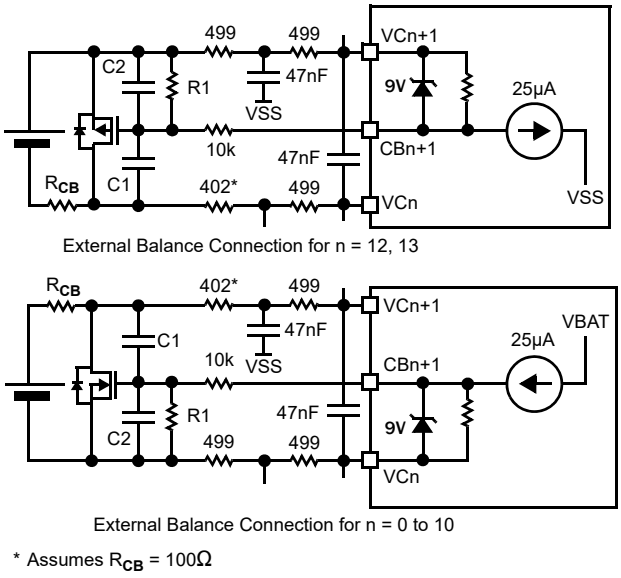


Figure 32. External Cell Balance Driving Circuits (Option 1)

Table 2. RAA489204 Input Filter Component Options for Figure 32 and Figure 33

Q_1 (P-Channel) with Examples[1]		Q_2 (N-Channel) with Examples		C_1	C_2	R_1
30V	A&O Semi AO3401	30V	A&O Semi AO3402	1nF	10nF	150k
30V	A&O Semi AO3401	30V	A&O Semi AO3402	1nF	10nF	150k
60V	Fairchild FDN5618	60V	Diodes DMN6140L-7	Not needed	10nF	250k
60V	Fairchild FDN5618	60V	Diodes DMN6140L-7	Not needed	10nF	250k

1. Q_1 and Q_2 should have low $r_{DS(ON)}$ specifications (<100mΩ) to function properly in this fault diagnostic configuration.

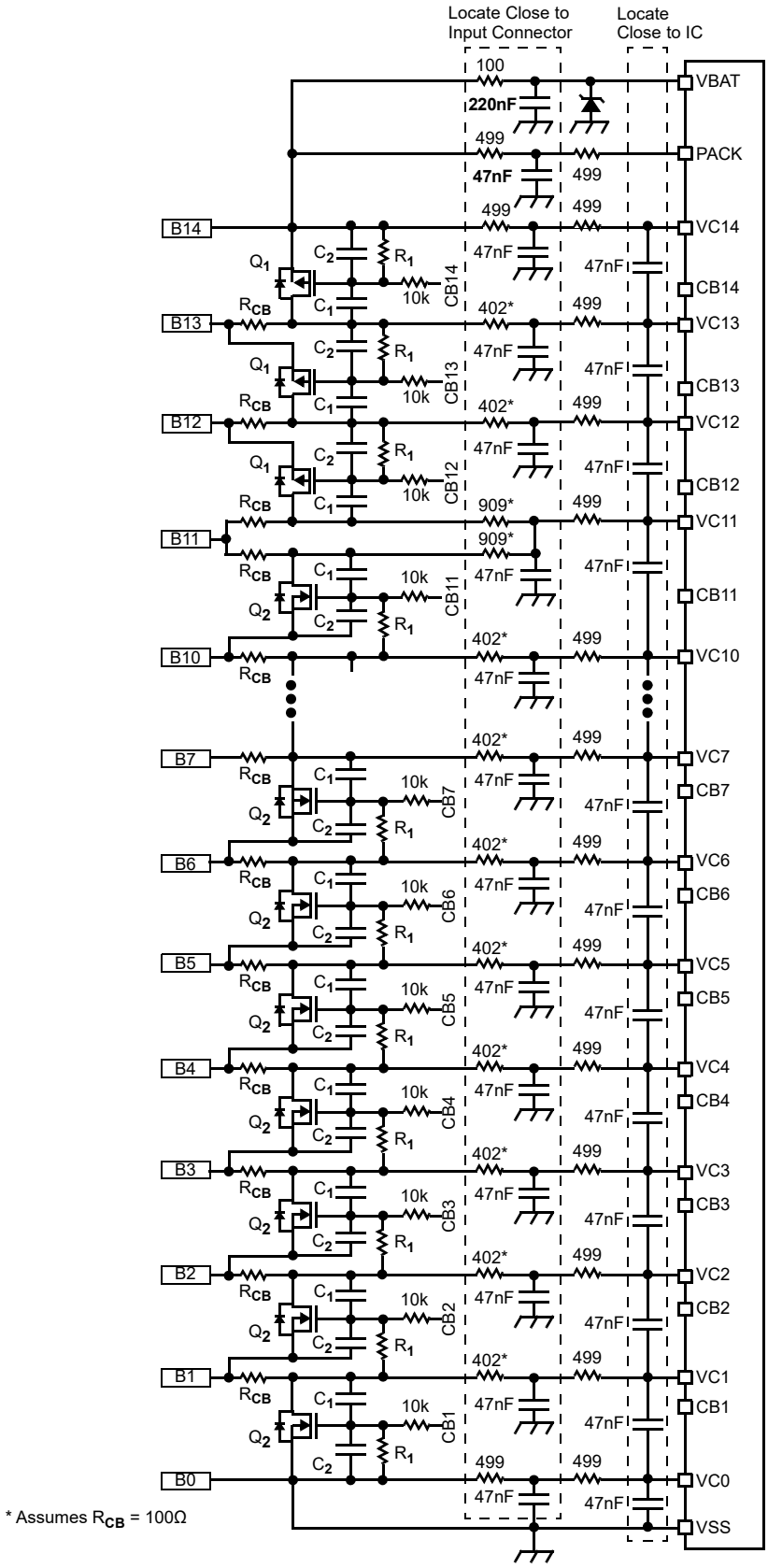


Figure 33. Typical Battery Connection Circuits with External Balancing

6.2.1.2 External Balance Circuit (Optional)

The circuits of Figure 34 and Figure 35 show an alternative method of connecting the external cell balance components. This option has the advantage of allowing accurate cell voltage readings while a cell is being balanced. However, this connection does not allow diagnostics to be performed on the external components.

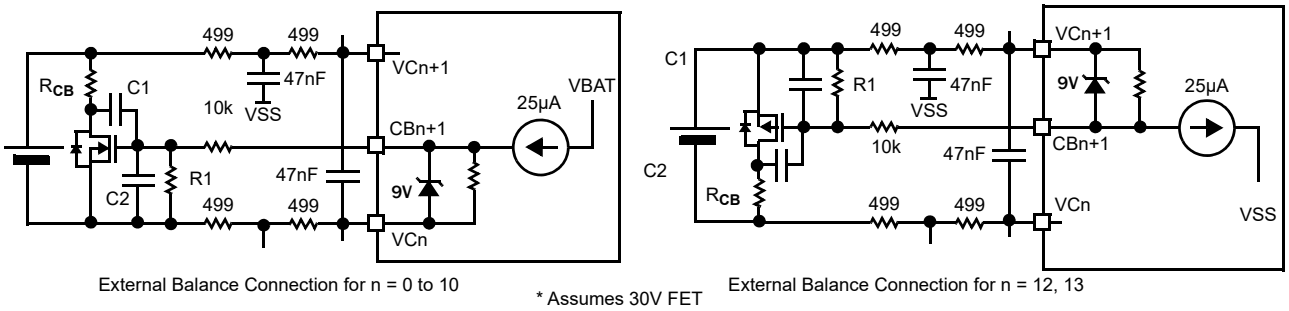


Figure 34. Alternate External Cell Balance Driving Circuits

Table 3. RAA489204 Input Filter Component Options for Figure 34 and Figure 35

Q_1 (P-Channel) with Examples[1]		Q_2 (N-Channel) with Examples		C_1	C_2	R_1
30V	A&O Semi AO3401	30V	A&O Semi AO3402	1nF	10nF	150k
30V	A&O Semi AO3401	30V	A&O Semi AO3402	1nF	10nF	150k
60V	Fairchild FDN5618	60V	Diodes DMN6140L-7	Not needed	10nF	250k
60V	Fairchild FDN5618	60V	Diodes DMN6140L-7	Not needed	10nF	250k

1. Q_1 and Q_2 $r_{DS(ON)}$ specification is not critical, because fault diagnostics are not performed in this configuration.

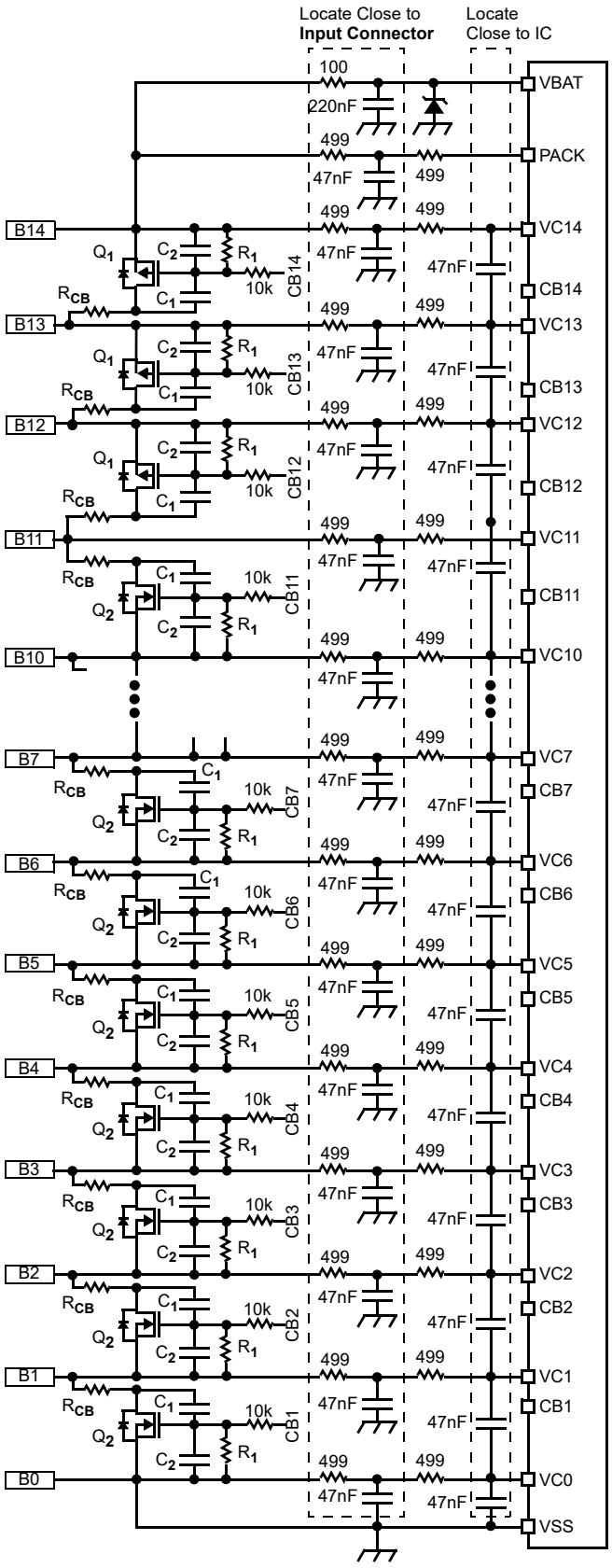
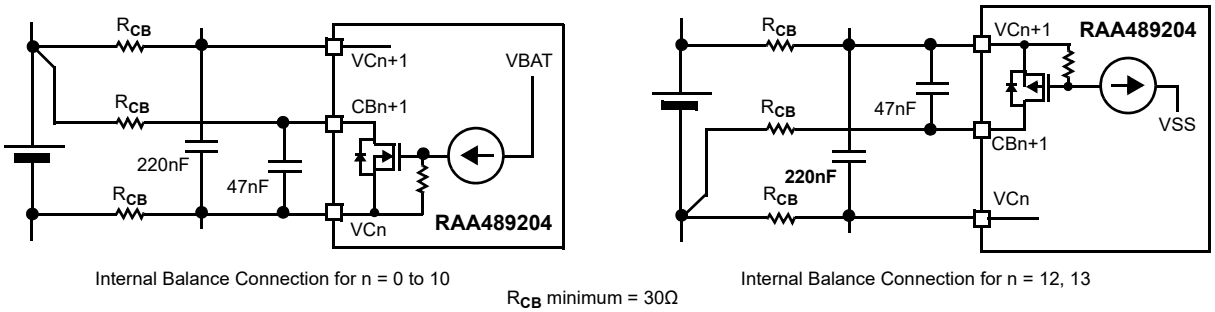


Figure 35. Alternate Battery Connection Circuits with External Balancing

6.3 Internal Balancing FETs

To select internal balancing, set the IBAL bit (Bit 8) in the BALANCE SETUP Register to ‘1’.

The CBn input connections for internal balance are shown in Figure 36, along with the typical input filter. Balance current is limited by the input filter when using the internal balance option. More balance current requires reducing the input series resistor values. This both limits the filter time constant and reduces the hot plug protection. Using a cell balance resistor (R_{CB}) of 100Ω limits the cell balance current to about 5mA to 10mA (cell voltage of 2V to 4V). The connection of batteries to the RAA489204 showing the input filter and internal balancing components is shown in Figure 37.



Internal Balance Connection for n = 0 to 10

Internal Balance Connection for n = 12, 13

R_{CB} minimum = 30Ω

Figure 36. Internal Cell Balance Driving Circuits

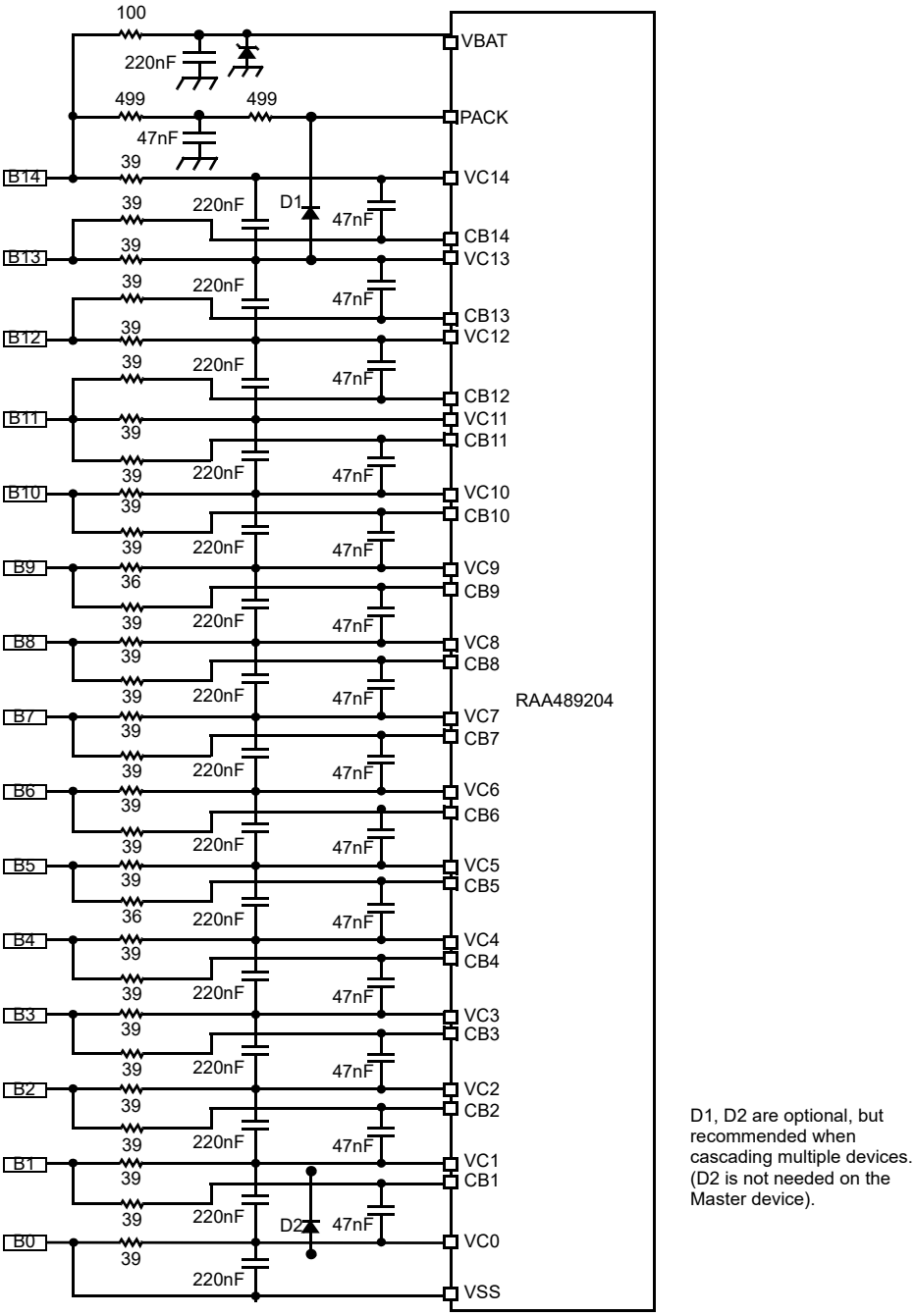


Figure 37. Typical Battery Connection Circuits with 50mA (@4.2V cell voltage) Internal Balancing

6.3.1 Cell Voltage Measurements During Balancing

The standard cell balancing circuit, using external FETs (Figure 33), is configured so that the cell measurement is taken from the drain connection of the balancing MOSFET. When balancing is enabled for a cell, the resulting cell measurement is then the voltage across the balancing MOSFET (V_{DS} voltage). This system provides a diagnostic benefit for the cell balancing function. However, the input voltage of the cell adjacent to the MOSFET drain connection is also affected by this mechanism. The input voltage for this cell increases by the same amount that the voltage of the balance cell decreases.

For example, if Cell 2 and Cell 3 are both at 3.6V and balancing is enabled for Cell 2, the voltage across the balancing MOSFET may be only 50mV. In this case, Cell 2 would read 50mV and Cell 3 would read 7.15V. The Cell 3 value in this case is outside the measurement range of the cell input. Cell 3 would then read full-scale voltage, which is 4.9994V. This full-scale voltage reading occurs if the sum of the voltages on the two adjacent cells is greater than the total of 5V plus the balancing on voltage of the balanced cell. Table 4 shows the cell affected when each cell is balanced.

Table 4. Cell Readings During Balancing

Cell Balanced	Cell With Low Reading	Cell With High Reading
1	1	2
2	2	3
3	3	4
4	4	5
5	5	6
6	6	7
7	7	8
8	8	9
9	9	10
10	10	9
11	11[1]	12[1]
12	12[1]	11[1]
13	13	13
14	14	14

1. Cells 11 and 12 produce a different result from the other cells. Cell 11 uses an N-channel MOSFET while Cell 12 uses a P-channel MOSFET. The circuit arrangement used with these devices produces approximately half the normal cell voltage when balancing is enabled. The adjacent cell then sees an increase of half the voltage of the balanced cell.

The voltage measurement behavior previously outlined is modified by impedances in the cell connector and any associated wiring. The balance current passes through the connections at the top and bottom of the balanced cell. This effect further reduces the measured voltage on the balanced cell and also increases the voltage measured on cells above and below the balanced cell. For example, if Cell 4 is balanced with 100mA and the total impedance of the connector and wiring for each cell connection is 0.1Ω, Cell 4 would read low by an additional 20mV (10mV because of each connection) while Cells 3 and 5 would both read high by 10mV.

To avoid measurement issues related to the effects above, stop any balancing activity before performing a normal cell voltage measurement. This can be done by sending a Balance Inhibit command. Balancing can be resumed following the measurement with a Balance Enable command.

When the BDDS bit is set, cell balancing automatically turns off 10ms before conducting cell voltage measurements when using any Cell Balance mode in conjunction with the Scan Continuous mode (see Scan Continuous (Address: C6H)). Balancing is automatically re-enabled at the end of the voltage scan. Cell balancing

is automatically turned off 10ms before conducting cell voltage measurements when using the RAA489204 Scan Continuous mode or using the Auto Balance Mode with the BDDS bit set. Balancing is automatically re-enabled at the end of the voltage scan.

6.4 Cell Balance Operation

The RAA489204 provides three methods of cell balance control.

- Manual mode – The host microcontroller directly controls the state of each MOSFET output using a bit in the Balance Setup register.
- Timed mode – The host microcontroller programs a balance duration timer and selects which cells are to be balanced, then starts the balance operation. The RAA489204 turns all the FETs off when the balance timer expires.
- Auto Balance mode – The host microcontroller programs the RAA489204 to control the balance MOSFETs in sequence to remove a programmed charge delta value from each cell. The RAA489204 does this by controlling the amount of charge removed from each cell over a number of balance cycles, rather than trying to balance all cells to a specific voltage or for a specific time.

See System Faults.

6.5 Operating with Reduced Cell Counts

When using the RAA489204 with fewer than 14 cells, ensure that each used cell has a normal input circuit connection to the Top and bottom monitoring inputs for that cell. The simplest way to use the RAA489204 with any number of cells is to always use the full input circuit arrangement for all inputs and short together the unused inputs at the battery terminal. In this way, each cell input has a normal source impedance whether or not it is monitoring a cell.

The cell balancing components associated with unconnected cell inputs are not required and can be removed. Tie unused cell balance outputs to the adjacent cell voltage monitoring pin (CBn connects to VC(n-1) for cells CB3 to CB11 and CBn connects to VCn for CB12 to CB14).

The input circuit component count can be reduced in cases where fewer than 14 cells are being monitored. Examples of 12-cell, 10-cell, 9-cell, and 6-cell systems are shown in Figure 38 through Figure 41. Table 5 shows the recommended cells to be left unconnected for various reduced cell count options and these settings are reflected in the circuit diagrams. It is not necessary to follow these recommendations exactly (except that VC0, VC1, VC13, and VC14 should remain connected to cells). Configure the Cell Setup register properly so the RAA489204 ignores the unused cells for its diagnostic functions.

Table 5. Cell Connection Options for Reduced Cell Count Packs

Pack Size	Skipped Inputs	Short VCn/CBn inputs	Cell Setup Register Value	See Diagram
13-Cell	VC6	VC5 - VC6 and CB6	0000 0000 0010 0000 [0x0020]	
12-Cell	VC6 - VC7	VC5 - VC7 and CB6 - CB7	0000 0000 0110 0000 [0x0060]	Figure 38
11-Cell	VC6 - VC8	VC5 - VC8 and CB5 - CB8	0000 0000 1110 0000 [0x00E0]	
10-Cell	VC6 - VC9	VC5 - VC9 and CB5 - CB9	0000 0001 1110 0000 [0x01E0]	Figure 39
9-Cell	VC6 - VC10	VC5 - VC10 and CB5 - CB10	0000 0011 1110 0000 [0x03E0]	Figure 40
8-Cell	VC4 - VC9	VC3 - VC9 and CB3 - CB9	0000 0001 1111 1000 [0x01F8]	
7-Cell	VC4 - VC10	VC3 - VC10 and CB3 - CB10	0000 0011 1111 1000 [0x03F8]	
6-Cell	VC4 - VC11	VC3 - VC11 and CB3 - CB11	0000 0111 1111 1000 [0x07F8]	Figure 41

When selecting fewer than 14 cells, configure the RAA489204 CELL SETUP (9'h040) register to ignore the missing cells. A '1' disables the overvoltage, undervoltage, and open wire detection and disables cell balance on that input. The CELL SETUP register (Data Registers) is a 16-bit volatile register that can disable inputs VC2 - VC14.

In addition to disabling the fault diagnostic functions for missing cells, the CELL SETUP register settings also limit the cell voltage data read from the device so that data from the missing cells is skipped. So, for example, a device operating with only 12 cells returns data for those 12 cells, skipping the data for the two unused cells. See Packet Data and Table 16.

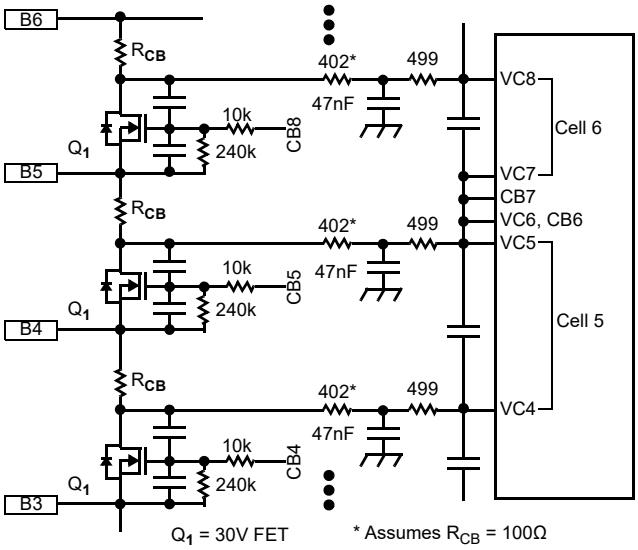


Figure 38. Typical Battery Connection for 12 Cells with External Balancing

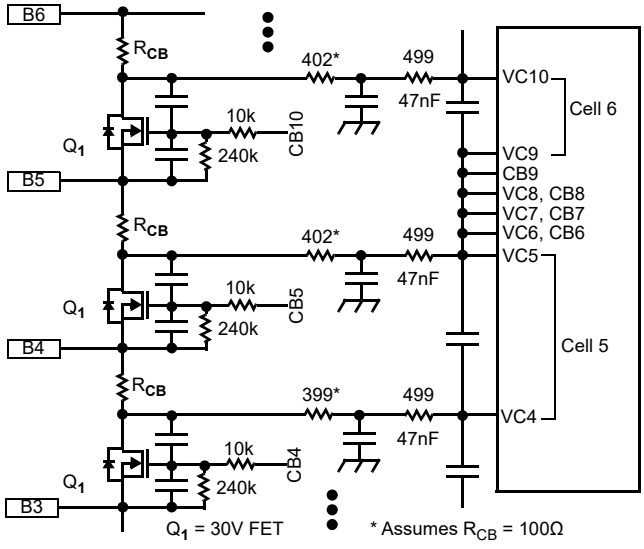


Figure 39. Typical Battery Connection for 10 Cells with External Balancing

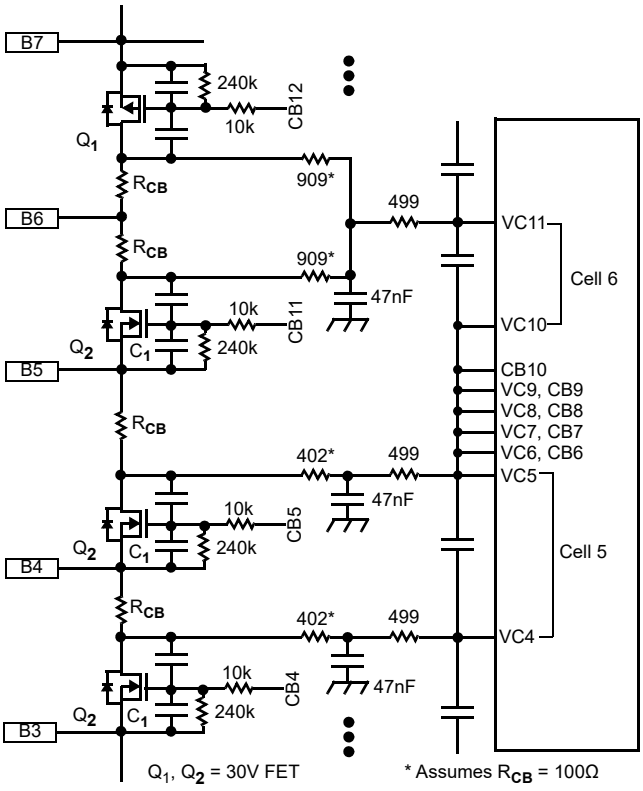


Figure 40. Typical Battery Connection for 9 Cells with External Balancing

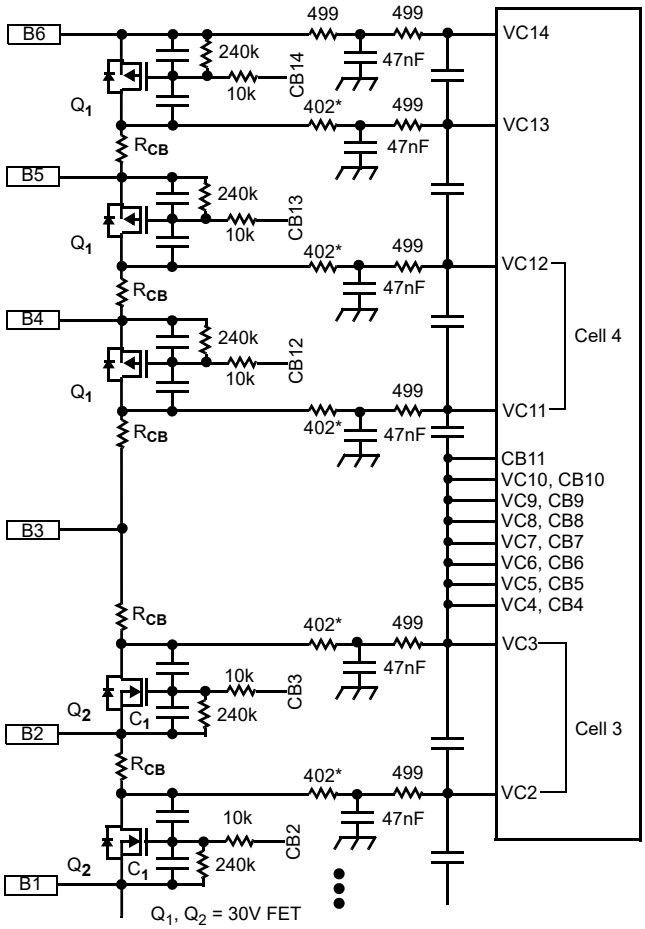


Figure 41. Typical Battery Connection for 6 Cells with External Balancing

6.6 Bus Bars/Negative Cell Voltages

Some systems use battery packs that are 4 to 6 cells, but are arranged in stacks with many more cells. Rather than using one IC per 4-cell pack, the RAA489204 can handle multiple stacks of smaller cell count packs with a single device, using a cell input as a bus bar between the packs. This allows a system monitor of the link between packs as well as monitoring the cells.

When connecting small cell count packs together using a bus bar, the voltage across the bus bar can be very small or even negative. The RAA489204 can monitor these low or negative voltages, but under normal conditions, these inputs indicate a fault condition (typically open wire or undervoltage). To deal with this, the system needs to set a bit in the Cell Fault Mask register corresponding to that input. This overrides the fault condition, while allowing the system to monitor the voltage of the bus bar. For example, the circuit in Figure 42 shows three packs of four cells stacked in a 12 cell configuration. The bus bar link between the packs is monitored by the VC10 and VC5 inputs. To avoid fault conditions, the Cell Fault Mask register for the connections shown in Figure 42, is programmed with the value in Table 6. To protect against a bus bar open condition, Figure 42 shows a 10k resistor with series diode.

Table 6. Cell Fault Mask Register Setup for Figure 42

13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFM 14	CFM 13	CFM 12	CFM 11	CFM 10	CFM 9	CFM 8	CFM 7	CFM 6	CFM 5	CFM 4	CFM 3	CFM 2	CFM 1
0	0	0	0	1	0	0	0	0	1	0	0	0	0

Because the RAA489204 can monitor negative voltages, it is suitable for use in Fuel Cell packs. When fuel cells become depleted, they start to act like resistors, so the voltage across these cells can go negative. It is necessary, however, to adhere to the following guidelines when monitoring fuel cells:

- None of the cell voltages go below VSS.
- The VBAT minimum voltage does not drop below 12V when using a capacitor coupled Daisy Chain, or 10V when using a transformer coupled Daisy Chain or no Daisy Chain.

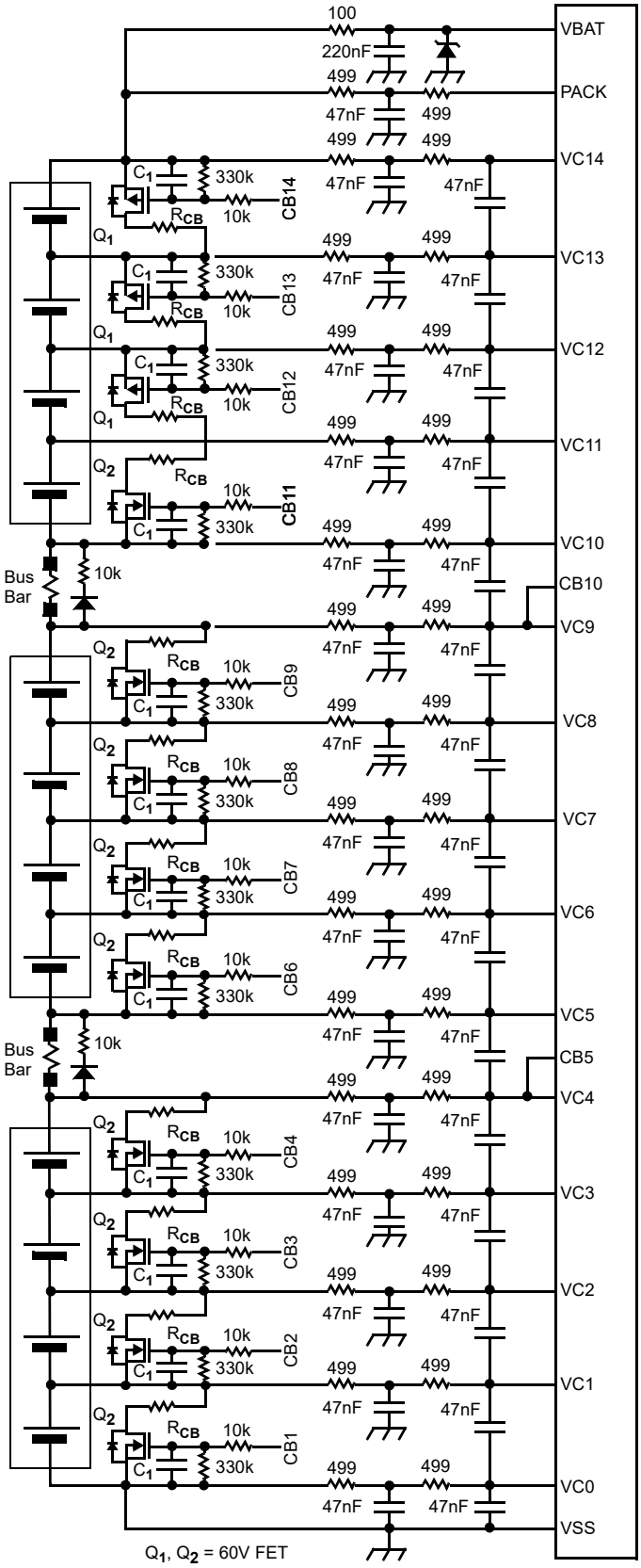


Figure 42. Battery Connection Circuits with Bus Bars

6.7 Power Supplies

The VBAT pin provides power for the high voltage circuits, the low voltage regulator, the voltage references, and internal Sleep mode regulators. The PACK pin, besides being a monitored input, also provides a small bias current to the analog front end.

The V3P3 supply powers the internal logic, through an internal 2.5V regulator, and logic I/O circuits. V_{CC} supplies the low voltage analog circuits. The V3P3 supply is powered directly from the battery voltage through an external pass transistor and is enabled whenever the RAA489204 is in Normal mode, while the Base pin provides a minimum current of 1mA over-temperature. The external V3P3 circuit is shown in Figure 43. The pass transistor is an NPN type with a preferred gain of 100 or more. The V3P3 regulator also provides the VCC supply using an external RC filter.

The V3P3 voltage should not be provided from an external supply. Also, the V3P3 and VCC pins must not be connected to external circuits other than those associated with the RAA489204 main voltage regulator. The V3P3 voltage cannot be used to power external devices, because when the RAA489204 goes into Sleep mode, the BASE output turns off and the voltage on V3P3 is supplied by a low power internal Sleep mode regulator that does not provide much current. If powering additional external circuits from the V3P3 supply, use a separate transistor, with the base connected to the BASE pin as shown in Figure 43.

A bypass capacitor is required between the REF pin and the analog ground VSS. The total value of this capacitor should be in the range of 2.0µF to 2.5µF. Use X7R type dielectric capacitors for this pin. The RAA489204 continuously performs a power-good check on the REF pin voltage starting 20ms after the device powers-up, after the rising edge of the Enable pin, or after the end of a wake-up operation. If the REF capacitor is too large, then the reference voltage may not reach its target voltage range before the power-good check starts, and results in a REF Fault. If the capacitor is too small, then it can lead to inaccurate voltage readings.

In addition to the V3P3 circuit, Figure 43 shows the connection for the VCC supply and the bypass capacitors for the V2P5 and the REF (voltage reference) supplies. In this figure, two grounds are identified. These are nominally referred to as noisy and quiet grounds. The noisy ground, denoted by an earth symbol, carries the EMI loop currents and digital ground currents while the quiet ground, denoted by the inverted triangle, defines the decoupling voltage for voltage reference and the analog power supply rail. The quiet and noisy grounds should be joined at the VSS pin. Keep the quiet ground area as small as possible. This helps with EMI immunity by making the quiet ground an island with no connections allowing current to flow across the quiet ground plane.

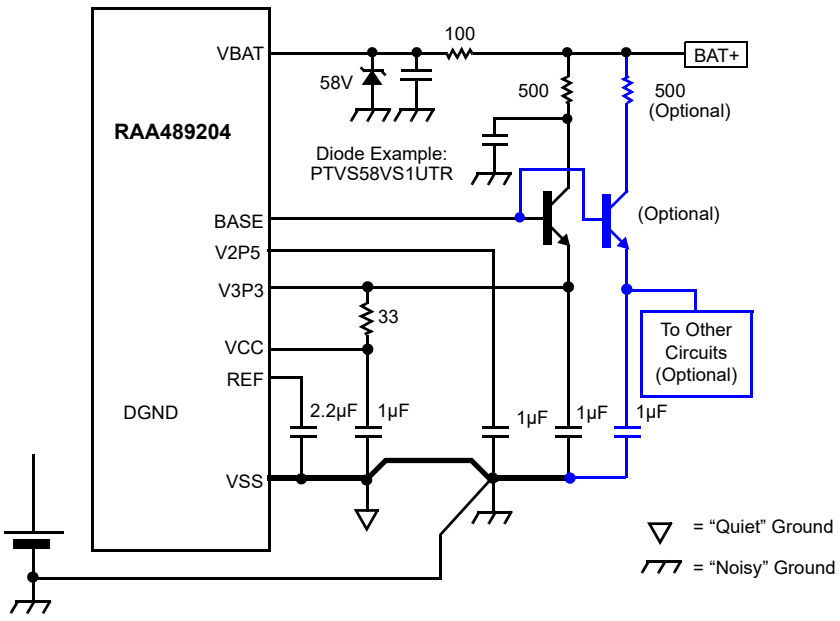


Figure 43. External Power Supply Connections

6.8 Hardware Reset

The EN pin can perform hardware resets. The EN pin is internally pulled up to V3P3. To perform a reset, pull the EN pin to DGND. It is recommended to add a low value (10k) pull-up resistor to the EN pin when this is driven from external sources to maintain EMI robustness. The RAA489204 also offers a hard reset (HReset) capability that pulls the EN pin logic Low internally in response to a special Daisy Chain command.

The HReset function of the RAA489204 provides a means of resetting the parts without adding cost to the system. The HReset function resets all internal blocks, except the V2P5 and V3P3 Sleep mode regulators.

Both the HReset and SReset commands reset the internal registers to default values.

6.9 Temperature Pins

The RAA489204 provides six pins (ExT1 to ExT4, GPIO1 and GPIO2) for use either as general purpose analog inputs or for NTC type thermistors. Each of these inputs has an internal pull-up resistor, that is connected by a switch to the VCC pin whenever the TEMPREG output is active. This arrangement results in an open input being pulled up to the V_{CC} voltage.

Inputs above 31/32 of full-scale are registered as open inputs and cause the relevant bit in the Over-Temperature Fault register, along with the OT bit in the Fault Status register to be set, on condition of the respective temperature test enable bit in the Fault Setup register. The user must then read the register value associated with the faulty input to determine if the fault was because of an open input (value above 31/32 full-scale) or an over-temperature condition (value below the external temperature limit setting).

The arrangement of the external ExTn inputs is shown in Figure 44. Connect components in the sequence shown in Figure 44. For example, connect C_2 between the junctions of R_1 and R_2. Connect R_2 between the junctions of C_2 and C_1. This ensures the correct operation of the various fault detection functions.

The function of each of the components in Figure 44 is listed in Table 7 together with the diagnostic result of an open or short fault in each component.

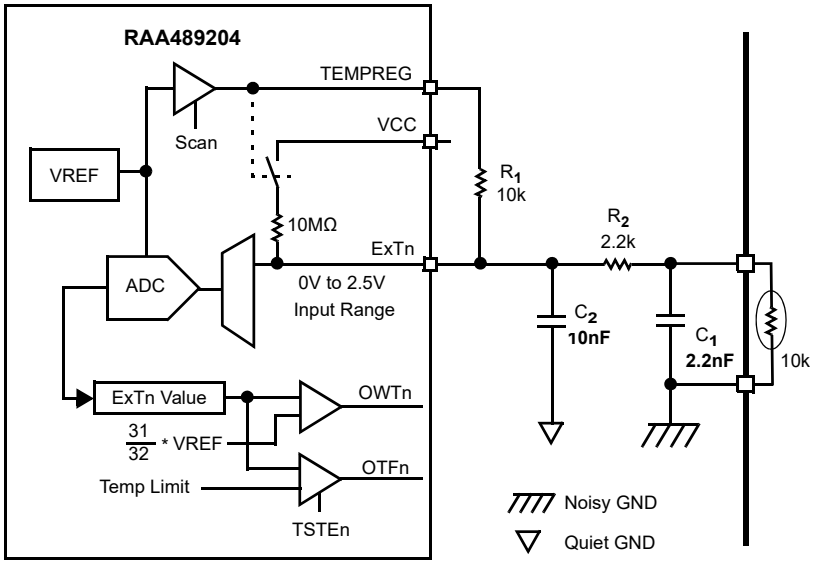


Figure 44. EXTn Block Diagram and External Temperature Circuit

Table 7. Component Functions and Diagnostic Results for Circuit of Figure 44

Component	Function	Diagnostic Result
R_1	Measurement high-side resistor	Open: Low input level (over-temperature indication) Short: High input level (open-wire indication).
R_2	Protection from wiring shorts to external high voltage connections and provides filtering.	Open: Open-wire detection Short: No diagnostic result
Thermistor	Temperature sensitive element	Open: High input level (open-wire indication). Short: Low input level (over-temperature indication)
C_1	EMI protection. Connects to PCB noisy ground.	Open: No diagnostic result Short: Low input level (over-temperature indication)
C_2	Noise filter. Connects to measurement (quiet) ground. Connect C_2 further from the ExTn pin than R_1.	Open: No diagnostic result Short: Low input level (over-temperature indication)

6.10 General Purpose I/O

The RAA489204 has two general purpose I/O pins (GPIO1 and GPIO2). These pins can be set as either inputs or outputs. As inputs, these ports are automatically scanned along with the temperature inputs.

As outputs, the GPIO pins are open drain and are pulled High externally. The state of each GPIO pin is controlled through register bits, either directly by the host controller, or using a set of selectable special functions. The GPIO1 pin has a special function that serves as a secondary fault output. Any of the fault bits can, when active, force GPIO1 active. The GPIO2 pin has two special functions. These involve an output of signals that allow external synchronization of the internal cell voltage scan. In one mode, the RAA489204 outputs a short pulse at the start of each ADC conversion. In the other mode, the GPIO2 pin is set High at the start of a voltage scan and set Low at the end of the scan.

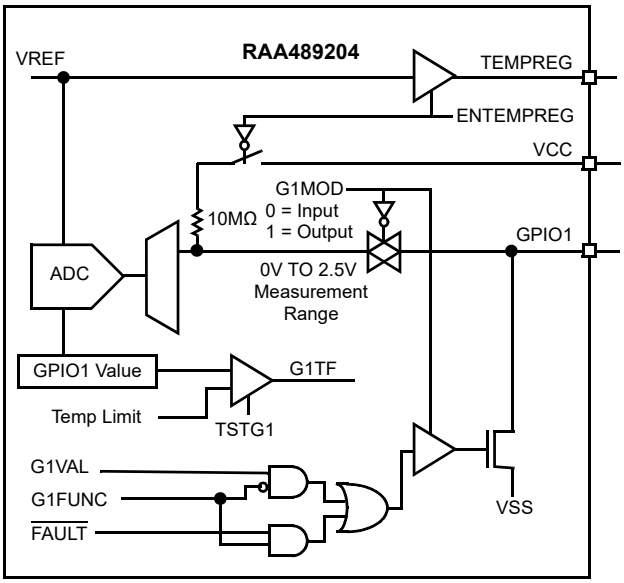


Figure 45. GPIO1 Block Diagram

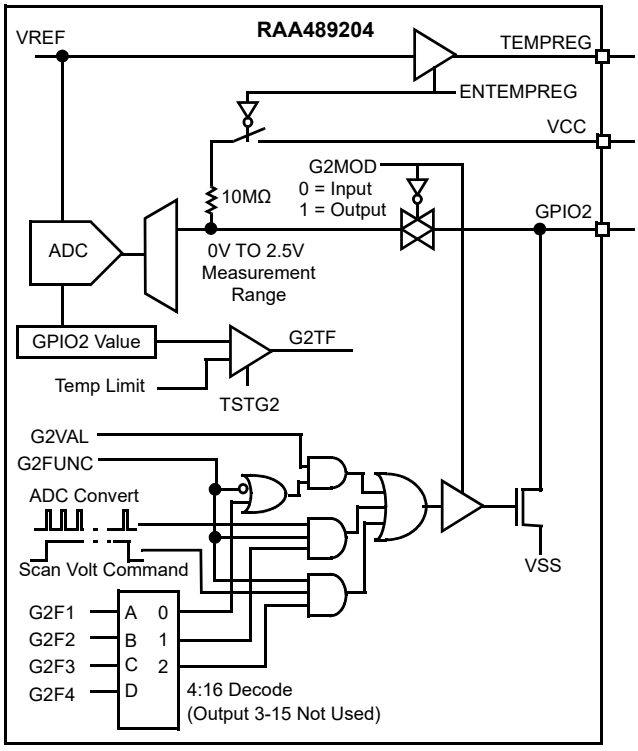


Figure 46. GPIO2 Block Diagram

6.10.1 GPIO Input/Output Select

Select the input or output modes of the General Purpose I/O pins using the G1MOD and G2MOD bits. As an input, the pin has an internal pull-up to VCC, that is active whenever a Scan Temperatures operation is in progress. As an output there is no internal pull-up. See Table 8.

Table 8. GPIO Input/Output Select

G2MOD	G1MOD	GPIO2 Pin		GPIO1 Pin	
		Mode	Internal Pull-Up to VCC	Mode	Internal Pull-Up to VCC
0	0	Input	Yes	Input	Yes
0	1	Input	Yes	Output	No
1	0	Output	No	Input	Yes
1	1	Output	No	Output	No

When a GPIO pin is selected as an output, the GPIO data register contents are not updated during any ADC measurement activity. The GPIO data register value can still be read using a single register Read operation, but the value is not defined and should be ignored. A multiple register Read operation skips the GPIO register when the GPIO is selected as an output.

6.10.2 GPIO Output Functions

When selected as an output, the system host can set or reset the GPIO1 and GPIO2 pins independently to control external circuits. However, each pin has some special functionality selected by control bits.

In addition to the standard output, GPIO1 can serve as a secondary fault pin. The GPIO1 pin has a mask register identical to the one for the $\overline{\text{FAULT}}$ pin.

For example, the $\overline{\text{FAULT}}$ pin can be set to indicate a voltage fault, while the GPIO1 pin can indicate a temperature fault.

Table 9. GPIO1 Output Function

G1FUNC	Pin Function
0	GPIO1 as general purpose output
1	GPIO1 as secondary fault output Select fault indication using GPIO1 Fault Mask Register

The GPIO2 pin has additional special functions. The GPIO2 pin can indicate the status of internal digital conversions or the internal scan, and can be used by external circuits to synchronize with the internal scan.

Table 10. GPIO2 Pin Output Function (G2MOD = 1)

G2F4	G2F3	G2F2	G2F1	G2 FUNC	Pin Function
x	x	x	x	0	GPIO2 as general purpose output
0	0	0	0	1	GPIO2 as general purpose output
0	0	0	1	1	GPIO2 pulses at the start of a cell voltage measurement. (5µs pulse)
0	0	1	0	1	GPIO2 toggles High at the start of a Scan Voltages operation and toggles Low at the end of the operation.
All Other Combinations					GPIO2 as general purpose output

6.11 GPIO/EXT Pins as General Purpose Inputs

When the ExT1 to ExT4 and GPIO1 and GPIO2 pins are used as general purpose ADC inputs, the pins are scanned and converted as part of a normal temperature scan, with the converted values saved to individual registers. The RAA489204 provides the option to disable over-temperature detection if this is not required on a particular input. Over-temperature detection is applied by comparing the measured voltage of each input to a programmable threshold. Voltage values below the threshold indicate a fault condition: the over-temperature detection feature is designed to use NTC thermistors. The function of the over-temperature detection is determined for each input by the TSTE1 to 4 and TSTG1 and 2 bits in the Fault Setup register. Setting a bit activates the over-temperature detection. Clearing a bit disables the detection. To set the ExTn and GPIOn pins to be checked against temperature limits, set the test bits as shown in Table 11.

Table 11. Select GPIO Inputs as Temperature Type

	Bit = 0	Bit = 1
TSTE1	ExT1 as General Purpose Input	ExT1 as Temperature Input
TSTE2	ExT2 as General Purpose Input	ExT2 as Temperature Input
TSTE3	ExT3 as General Purpose Input	ExT3 as Temperature Input
TSTE4	ExT4 as General Purpose Input	ExT4 as Temperature Input
TSTG1	GPIO1 as General Purpose Input	GPIO1 as Temperature Input
TSTG2	GPIO2 as General Purpose Input	GPIO2 as Temperature Input

6.12 Communication Ports

The RAA489204 provides two communications systems. An SPI synchronous port is provided for communication between a microcontroller and the RAA489204. For stand-alone (non-Daisy Chain) systems, the SPI port is the only port needed. In systems with more than one RAA489204, Daisy Chain (asynchronous) ports provide communication between RAA489204 devices.

6.12.1 SPI Port

To use the SPI port, connect the CMODE pin Low. With the CMODE pin High, the RAA489204 is in either a Mid or Top Daisy Chain location (see Figure 47).

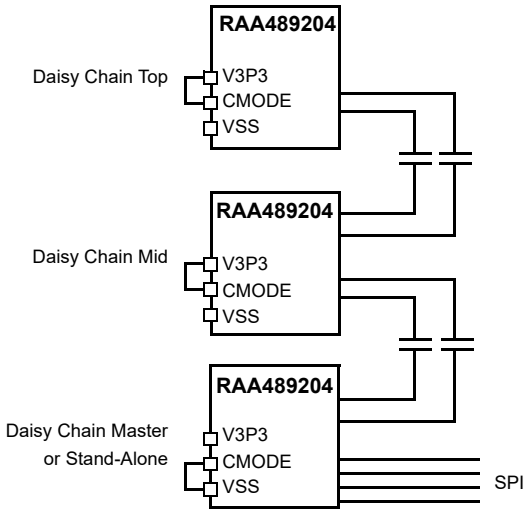


Figure 47. Communications Configuration

All communications are conducted through the SPI and/or Daisy Chain ports. Data flow is controlled by a handshake between the RAA489204 Master device $\overline{\text{DATAREADY}}$ output and the Microcontroller Chip Select output. There are two modes of communication. Data is passed either byte-by-byte (Byte Mode), or in multiple byte blocks (Block Mode). The SPI mode is selected by the DTRDYMODE pin. For all communications the MSB is transmitted first and the LSB is transmitted last.

Commands in non-Daisy Chain systems are identical to those of a Daisy Chain system. The only difference is that in a stand-alone configuration, communications on the SPI port are not passed to the Daisy Chain port.

6.12.2 Daisy Chain Ports

A Daisy Chain consists of a bottom device, a Top device, and up to 28 Mid devices. The RAA489204 device located at the bottom of the stack is called the Master and communicates to the host microcontroller using SPI communications and to other RAA489204 devices using the Daisy Chain port. Each Mid device provides two Daisy Chain ports: one is connected to the RAA489204 in the stack above and the other to the RAA489204 below. Communications between the SPI and Daisy Chain interfaces are buffered by the Master device to accommodate timing differences between the two systems.

The Daisy Chain ports are fully differential, DC balanced, bidirectional, and AC coupled to provide maximum immunity to EMI and other system transients while only requiring two wires for each port. Three operating data rates are available and are configurable by pin selection using the COMMRATE0 and COMMRATE1 pins (see Table 12).

The maximum operating data rate for the SPI interface is 2.5Mbps. When using the Daisy Chain communications system Renesas recommends that the synchronous communications data rate is at least twice that of the Daisy Chain system.

Table 12. Daisy Chain Communications Data Rate Selection[1]

COMMRATE0 Pin	COMMRATE1 Pin	Data Rate (kHz)
0	0	333
0	1	500
1	0	Do Not Use (No Function)
1	1	1000

1. ‘0’ indicates pin pulled to VSS. ‘1’ indicates pin pulled to V3P3.

The communications pins are monitored when the device is in Sleep mode, allowing the part to wake up in response to communications.

The RAA489204 provides the option of capacitive coupling or transformer coupling on the Daisy Chain. The external circuit arrangement is symmetrical to provide a bidirectional communications function. In a stand-alone (non-Daisy Chain) system, the Daisy Chain components connected to DHI2 and DLO2 are omitted.

6.12.2.1 Capacitive Coupling

The capacitive coupling option is a lower cost, short range system with a maximum cable length of 50cm (at 1MHz Daisy Clock). A capacitive coupled Daisy Chain can be used on-board or off-board (cable connected) and provides full EMI and transient immunity. The capacitively coupled Daisy Chain is not recommended for use across the low voltage to high voltage barrier. Use a transformer for this link instead. The circuit arrangement for an on-board Daisy Chain is shown in Figure 48. When the capacitive coupled system includes a cable off-board, additional components are required to provide enhanced safety protections (see Figure 49).

The basic circuit elements of the capacitively coupled Daisy Chain are the series resistor and capacitor elements R_1 and C_1, that provide the transient current limit and AC coupling functions, and the line termination components C_2, that provide the capacitive load. Capacitors C_1 and C_2 should be located as close as possible to the board connector when using an external (cable) connection.

The AC-coupling capacitors C_1 must be rated for the maximum voltage, including transients, that can be applied to the interface. Specific component values are needed for correct operation with each Daisy Chain data rate and are given in Table 13.

The Daisy Chain operates with standard unshielded twisted pair wiring. The component values given in Table 13 accommodate cable capacitance values from 0pF to 50pF when operating at the 1000kHz data rate. Higher cable capacitance values (longer cables) can be accommodated by operating at lower data rates.

In the off-board Daisy Chain diagram (Figure 49), the components are shown split into two sections. The components specified to be close to the board connector should have the capacitor terminals connected directly to a solid ground plane. This is the same ground plane that serves the first stage (single ended) filter on the cell inputs. When connecting the Daisy Chain cable off-board, the battery connector and Daisy Chain connectors should be placed close to each other on the same edge of the board to minimize any loop current area.

The value for C_2 in Table 13 is ideally 220pF. This creates a 3:1 ratio in the transmit vs received signal. Additional capacitance on the board because of device pin, board layout, and connector capacitance adds to the effective load capacitance and reduces the signal level at the receiver. A lower value of capacitance is chosen for C_2 to compensate for these effects. Renesas recommends choosing the board layout to minimize the length of Daisy Chain traces and to isolate them from ground planes. Expect at least 50pF to 90pF of additional board capacitance, depending on layout and connectors.

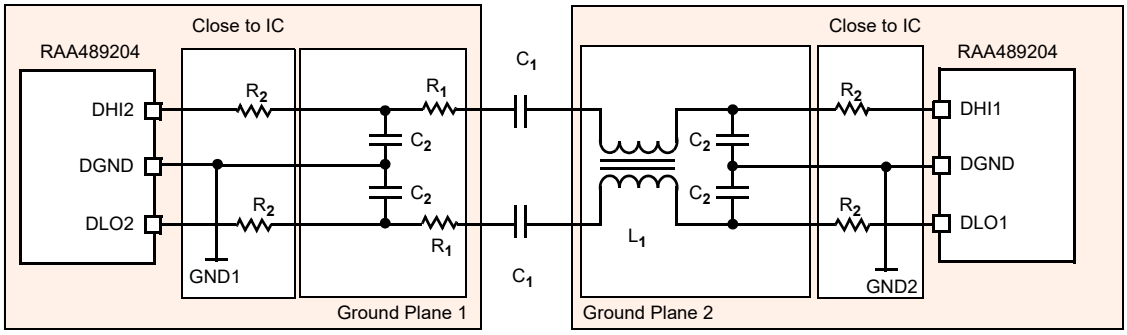


Figure 48. On-Board Capacitive Daisy Connection

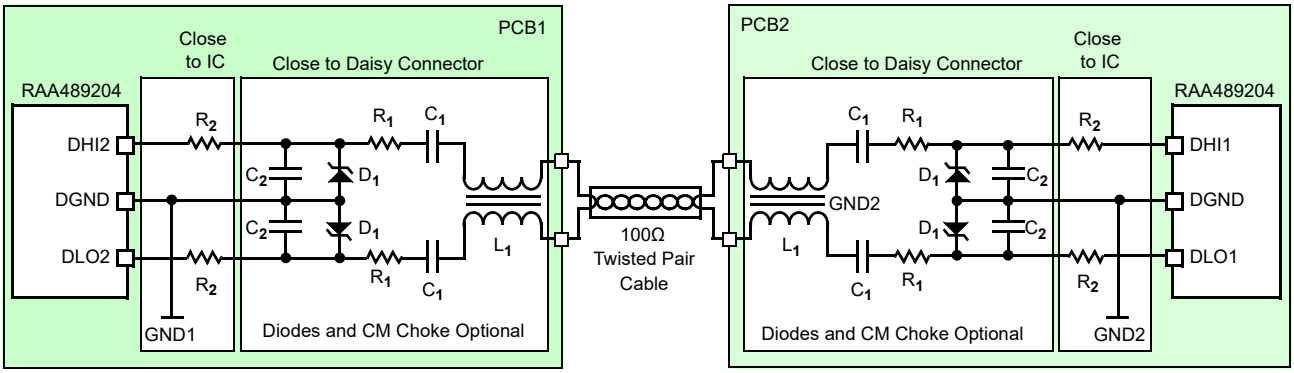


Figure 49. Off-Board Capacitive Daisy Connection

Table 13. Component Values in Figure 48 and Figure 49 for Various Daisy Chain Data Rates

Component	Component Tolerance (%)	Daisy Chain Clock Rates			Comments
		1000kHz	500kHz	333kHz	
C_1, Off-board (4 ea.) C_1, On-board (2 ea.)	5	220pF 110pF	440pF 220pF	660pF 330pF	NPO dielectric type capacitors are required.[1]
C_2 (4 ea.)	5	220pF	440pF	660pF	Use the same dielectric type as C_1. [1][2]
R_1, Off-board (4 ea.) R_1, On-board (2 ea.)		220Ω 470Ω	220Ω 470Ω	220Ω 470Ω	
D_1, Off-board Only (4 ea.)		47V	47V	47V	Example: BZX84C47-7-F. This diode is only suggested for ESD ratings above 4kV (up to 15kV tested). Diodes add capacitance, so if diodes are used, adjust C2 to a lower value.[2]
R_2 (4 ea.)		22Ω	22Ω	22Ω	
Cable Capacitance Range (Off-board Only)		0 to 50pF	0 to 200pF	0 to 400pF	Longer cables add effective capacitance of C2. If cable length is long, reduce daisy speed, reduce the value of C2, or change daisy connection to transformer coupled.
L1, Common-Mode Choke		100µH	100µH	100µH	Optional. May be required for low frequency EMC.

1. Capacitor values shown are ideal values. When selecting capacitors, select closest match, or use two series caps.
2. Ideally, this value should be 2x the C1 value. However, board, layout, and connectors increase the actual capacitance, so choose a standard C2 value lower than the ideal value. The C2 value may need to be lower still if there is significant board capacitance.

6.12.2.2 Transformer Coupling

Although the capacitive connected Daisy Chain provides an effective, low cost option for isolated communications, there is a limit to the length of the daisy cable, because of the cable capacitance. For this reason, the RAA489204 also operates with a transformer-coupled Daisy Chain. In the transformer-coupled option, the cable capacitance is not a limiting factor. Therefore, the cable can be many meters in length. The external circuits required for the transformer connection are shown in Figure 50. The 200Ω differential resistor at the transmitter end appears in parallel with the internal 200Ω source resistor, therefore providing a 100Ω termination for the cable. The Daisy Chain in a system can use a mix of capacitive and transformer coupled segments. The circuit in Figure 50 is recommended for a 1MHz Daisy Chain data rate. There is no reason to operate the Daisy Chain at rates lower than 1MHz when using a transformer coupling.

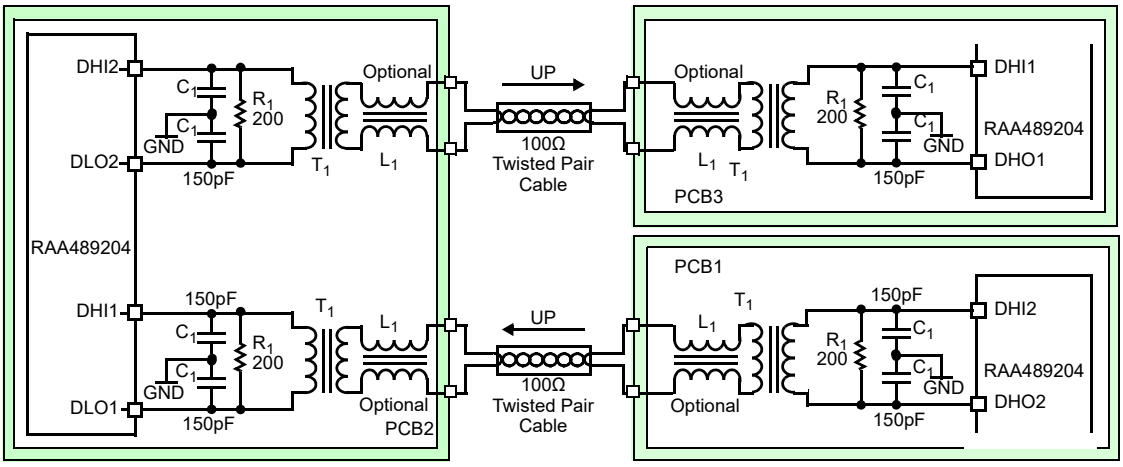


Figure 50. Transformer Connected Daisy Chain Circuit Implementation

Table 14. Component Values in Figure 50 for 1000kHz Daisy Chain Data Rate

Component	Component	Comments
C_1 (4 ea.)	150pF/5%	
R_1 (2 ea.)	200Ω/5%	
T_1/L_1 (1 ea.)	TG110-AEX50N5LF S558-5999-T7-F	Halo Electronics (-40°C to +125°C) Bel Fuse, Inc. (-40°C to +85°C)
T_1 (2 ea.)	78601/2jC 760301106	Murata Electronics (0°C to +70°C) Wurth Elektronik. (-40°C to +125°C)
L_1 (2 ea.)	DLW32MH201XK2	Murata Electronics (-40°C to +125°C)

6.12.2.3 Daisy Chain Upper Port Control

The upper Daisy Chain port on each device has a control bit (DP2) in the Device Setup 2 register. Setting this bit disables the upper port. This is useful to reduce power consumption in Top stack devices and in stand-alone devices (no Daisy Chain). The default value of this bit is '0': upper port is enabled.

When DP2 is set, turning off the upper port, a small amount of current draw is added to V_{BAT} when in Sleep mode to replace the current removed when the upper Daisy Chain port is switched off. The intent is to maintain the same amount of quiescent current in all devices while in Sleep mode independent of stack location (Top, Mid or bottom). This functionality applies only to Daisy Chained devices. A stand-alone device (stack size = 1) does not add current to V_{BAT} when the DP2 bit is set.

Note: This current burning in Sleep mode function also applies to the Daisy Chain Master device, although in this case, the current is compensating the fact that the lower Daisy Chain port is disabled.

The condition of the DP2 bit is overridden during a Roll Call function, so that all devices transmit on their upper port irrespective of the value of DP2.

6.13 Component Selection

Certain failures associated with external components can lead to unsafe conditions in electronic modules. A good example of this is a component that is connected between high energy signal sources failing short. Such a condition can easily lead to the component overheating and damaging the board and other components in its proximity.

One area to consider with the external circuits on the RAA489204 is the capacitors connected to the cell monitoring inputs. These capacitors are normally protected by the series protection resistors but could present a safety hazard in the event of a dual point fault where both the capacitor and associated series resistor fail short. Also, a short in one of these capacitors would dissipate the charge in the battery cell if left uncorrected for an extended period of time. Renesas recommends selecting that capacitors in the input filter as fail safe or open mode types. An alternative strategy is to replace each of these capacitors with two devices in series, each with double the value of the single capacitor.

A dual point failure in the balancing resistor and associated balancing MOSFET could also cause a shorted cell condition. Renesas recommends replacing the balancing resistor by two resistors in series.

A further consideration is the with the package sizes of capacitors used in the cell measurement circuits. Board leakage either to ground or cell to cell, that can be associated with small package sizes, can produce measurement errors when reading cell voltages. Renesas recommends not using packages smaller than 0603 for the capacitors in the cell measurement circuits.

7. Communication

7.1 SPI Interface

The RAA489204 operates as an SPI slave capable of bus speeds up to 2.5Mbps. Five lines make up the SPI interface: SCLK, DIN (MOSI), DOUT (MISO), $\overline{CS}$, and $\overline{DATAREADY}$. The DOUT line is normally tri-stated (high impedance) to allow use in a multi-drop bus. DOUT is active only when $\overline{CS}$ is Low.

The RAA489204 SPI port operates in half duplex mode and has two modes of operation: a Byte Transfer mode and a Block Transfer mode. The operating mode is selected by the condition of the DTRDYMODE pin. However, changing modes after power up is not supported.

All register values are sent MSB first and registers are sent in ascending order (least address first). All communications contain an integer number of bytes.

7.1.0.1 Byte Transfers

Connect DTRDYMODE to DGND to select the Byte Transfer mode SPI operation.

Data flow is controlled by a handshake system using the $\overline{DATAREADY}$ and $\overline{CS}$ signals. $\overline{DATAREADY}$ is controlled by the RAA489204. $\overline{CS}$ is controlled by the host microcontroller. In this mode, the RAA489204 requires that the $\overline{CS}$ line is pulled High between each byte. This handshake accommodates the delay between command receipt and device response because of the latency of the Daisy Chain communications system. See Figure 51.

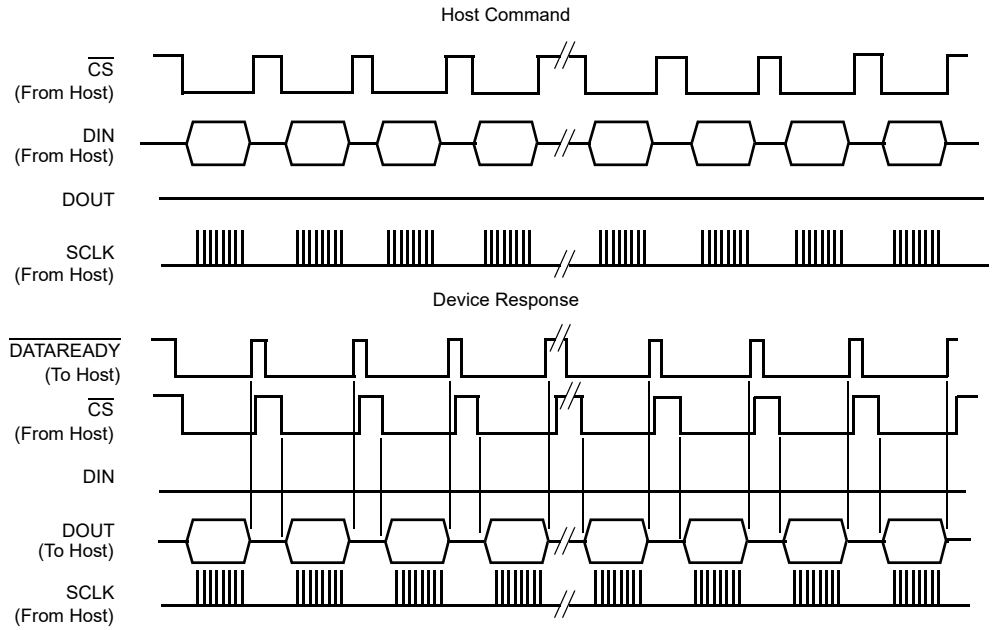


Figure 51. SPI Byte Mode Operation

The $\overline{DATAREADY}$/$\overline{CS}$ handshake operates as follows:

1. The host microcontroller sends a command to the RAA489204 using the $\overline{CS}$ line to select the RAA489204 and clocking data into the RAA489204 DIN pin.
2. A Stand-Alone or Master device responds by setting the $\overline{DATAREADY}$ output Low as soon as it is ready to send the response to the host.
3. The RAA489204 is now in transmit mode and ignores any data on DIN, so the host microcontroller must service the RAA489204 before sending further commands. Any data sent to DIN while $\overline{DATAREADY}$ is Low is ignored by the RAA489204.
4. The host microcontroller asserts $\overline{CS}$ Low and clocks eight bits of data out of DOUT using SCLK.

5. After the byte has been clocked out, the RAA489204 responds by raising $\overline{\text{DATAREADY}}$ and tri-stating DOUT. The host microcontroller then raises $\overline{\text{CS}}$.
6. The RAA489204 reasserts $\overline{\text{DATAREADY}}$ for the next byte, and so on.

It is possible for the microcontroller to interrupt a sequential data transfer by asserting $\overline{\text{CS}}$ before the RAA489204 de-asserts $\overline{\text{DATAREADY}}$. This causes a conflict with the communications and is not recommended. A conflict created in this manner would be recognized by the microcontroller either not receiving the expected response or receiving a communications failure notification.

Interface timing for SPI transfers is shown in Figure 3 (SPI Interface Timing (Byte Mode)) and Figure 4 (SPI Interface Timing (Block Mode)).

7.1.0.2 Block Transfers

Connect DTRDYMODE to V3P3 to select Block Transfer mode SPI operation.

In this mode, the $\overline{\text{DATAREADY}}$ line stays High until the RAA489204 has a complete message ready to be transmitted to the host (see Figure 52). The $\overline{\text{DATAREADY}}$ pin is then pulled Low and remains Low until the last byte has been clocked out by the host.

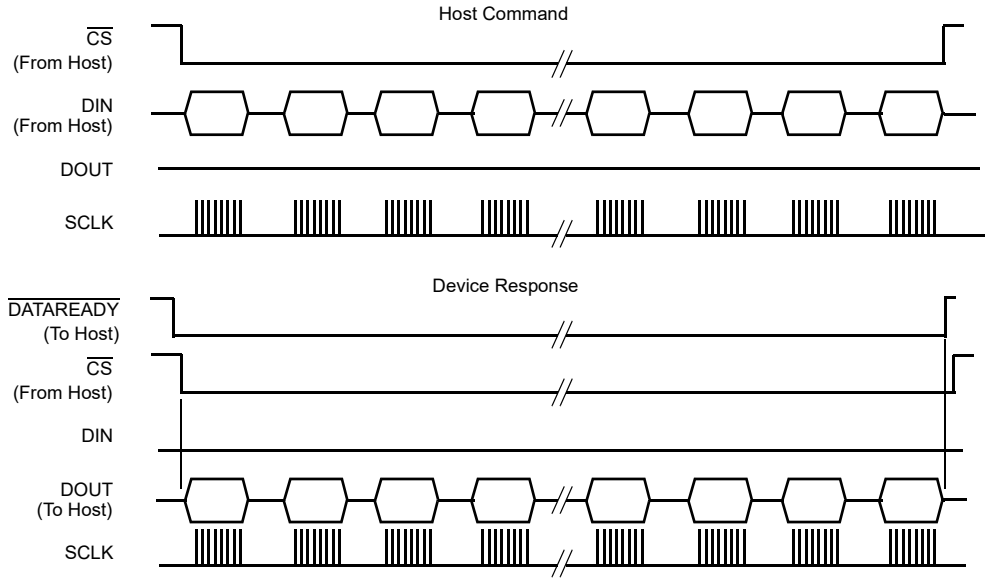


Figure 52. SPI Block Mode Operation

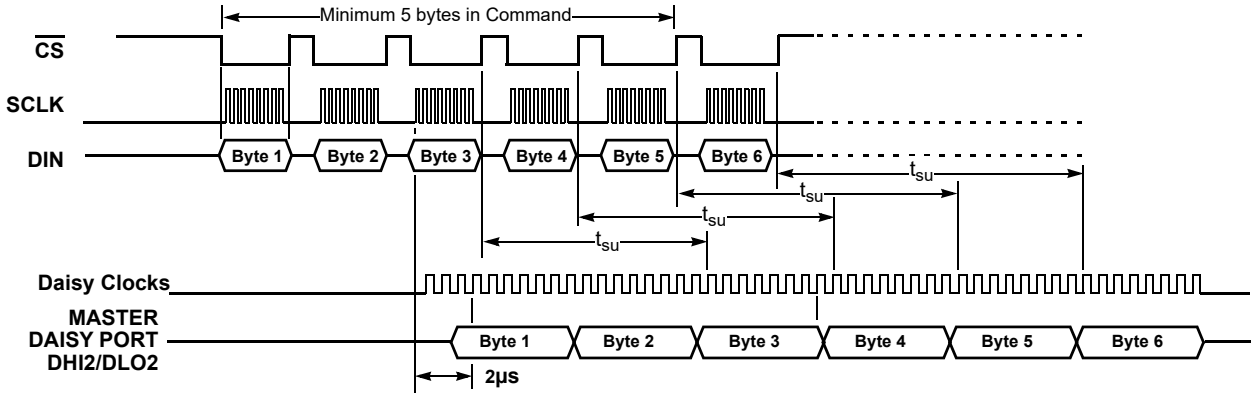
When the $\overline{\text{DATAREADY}}$ pin goes Low, the host asserts $\overline{\text{CS}}$ and clocks out data from the RAA489204 DOUT pin. The host keeps the $\overline{\text{CS}}$ Low until all data has been clocked into the host and the $\overline{\text{DATAREADY}}$ pin goes High. The host then takes $\overline{\text{CS}}$ High to end the transaction. In this manner the host does not need to provide a communications handshake function. This is more compatible with the built-in SPI functions of many microcontrollers. The host must correctly count the number of bytes in each response to avoid an attempt to read more data from the RAA489204 than is available. Each communication header contains the total number of bytes within the data portion of the communication and the host uses this information to clock in the correct number of bytes.

7.1.0.3 Memory Buffer

A Memory Buffer is provided in the RAA489204 to buffer communications between the SPI port and the upper Daisy Chain port of the Master device. The primary function of this buffer is to manage the asynchronous SPI transfer of the data between the host and Daisy Chain devices. The RAA489204 Memory Buffer size is 73 bytes. That is long enough to hold the longest response message: 5 byte header + 58 bytes of data + 4 bytes data CRC.

The RAA489204 begins moving command bits from the buffer to the Daisy Chain following the first clock pulse of the third byte received on the SPI port. Data then clocks out of the buffer at the Daisy Chain clock speed. When data starts being clocked onto the Daisy Chain, the host must continue to fill the buffer with the command bytes

(including CRC) before that byte of the command starts clocking onto the Daisy Chain. If the host does not keep the buffer full, then an invalid command (or CRC) is sent to the target device, resulting in a NAK response. If the command is a register write operation, then the host further must continue to fill the buffer with data before the RAA489204 starts clocking that data to the Daisy Chain (See Figure 53)



Note: Command bytes (starting with the third byte) need to be clocked into the SPI port before that byte is clocked out on the DHI2/DLO2 port. (t_{su} > 0µs)

Figure 53. Command Timing for Correct Transfer of Data from SPI Port to Daisy Chain

Commands must be a minimum of 5 bytes in length. If the command contains fewer than five bytes, then the Master is not able to properly decode subsequent commands and needs to be reset by toggling the EN pin.

In a response, data is clocked into the Master device buffer from the daisy chain port and is clocked out the SPI port starting after the Response Header is received (Byte transfer mode) or after the complete Response is received (Block transfer mode).

The Fault Status register BUFO bit is set in response to a Daisy Chain overrun in the Memory Buffer. An overrun occurs if the Memory Buffer is full and new data arrives on the Daisy Chain port, forcing the oldest data out from the buffer. This data is then lost. This can occur if the host microcontroller does not respond to a 62 byte Read response before the Master device receives a Fault Response from a Daisy Chain device.

7.2 Daisy Chain Interface

All Daisy Chain communications from the host pass to the Master device through the SPI port. The Master device begins transmitting on the Daisy Chain following the first full byte received on the SPI port. Each device in the chain retransmits the message with a single clock cycle delay from input port to output port; passing information from device-to-device to the Top device such that all devices in the stack receive the same information. Each device decodes the message and responds as needed. The originating device (Master in the case of commands, addressed device or Top stack device in the case of responses) generates the Daisy Chain clock and data stream.

The Top device responds to Read and Write messages with an acknowledge (ACK), or with the requested data if the command was a read addressed to the Top device. The addressed device waits to receive the full ACK response from the Top device, but does not pass this response further down the chain. Instead, the addressed device transmits data, in the case of a Read, or an ACK in the case of a Write on the lower Daisy Chain port to the Master. Action commands such as the Scan commands do not require a response. See Figure 54 and Table 26.

The first operation, following power up, is a Roll Call command. After that, each device knows its stack location and the total number of devices in the stack (see Roll Call Operation). This is important because each device that originates communications adds a number of Daisy Chain clock pulses to the data stream to allow transmissions to propagate through the stack. Each receiving device delays the data stream by one clock cycle and “swallows” one Daisy Chain clock cycle to provide filtering and retransmission of the information (see Figure 55).

All communications arriving at the Master’s upper Daisy Chain port is a whole number of bytes plus a single clock cycle, except in the case where a stack has not completed Roll Call. This last clock cycle is not counted as part of

the main message and is discarded. If Roll Call has not been completed, the Master receives a number of additional clock cycles at the end of each message. Additional Daisy Chain clock cycles that extend the communication beyond the number of bits indicated by the length portion of the communication are ignored.

A Read or Write communications transmission is only considered to be complete following receipt of a response from the target device or the identification of a communications fault condition. The host microcontroller should not transmit further data until either a response has been received from the target stack device or a communications fault condition has been identified.

The response time for commands is dependent on the operation. See Operational Timing for timing diagrams and equations for determining typical response times. Maximum response times occur if there is a Communications Failure response (see Communication Failure). If there is no response within the Communication Failure time, then the host should conclude that the Master did not properly receive a command from the host and should re-transmit. Repeated failure of the host to receive an expected response should be interpreted as a failure of the Master device or the SPI interface to the Master device.

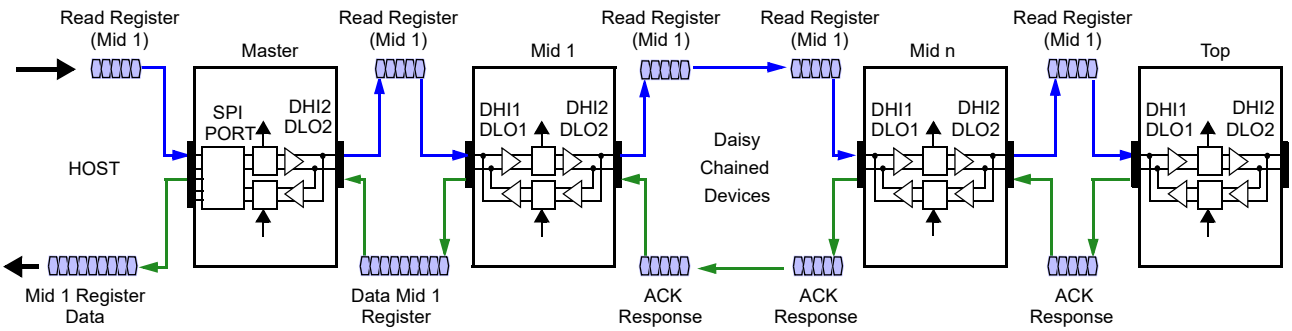
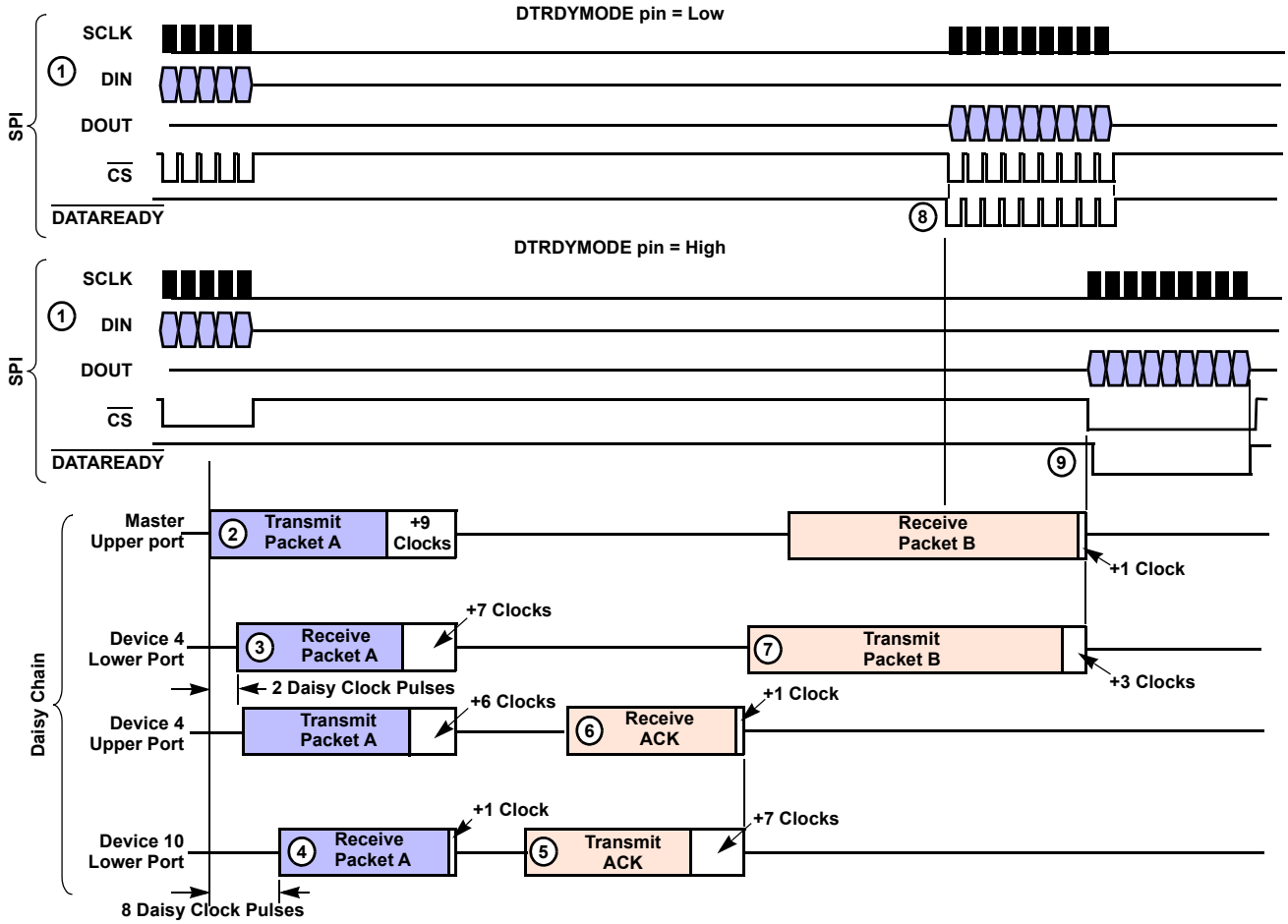


Figure 54. Daisy Chain Communication



Notes:

1. Host microcontroller sends Read device 4, cell 7 = Packet A. If DTRDYMODE pin is Low, data transmitted is byte by byte. If DTRDYMODE pin is High, data is transmitted as a block.
2. Master begins relaying Packet A on the Daisy Chain 19.5 SPI clock cycles after the first falling edge of $\overline{CS}$. The Master adds 8 extra clock cycles (Top - 2) to allow all stack devices to relay the message.
3. Device 4 receives and decodes “Read device 4, cell 7”, but waits for a response from Top stack device before sending the data.
4. Top stack device (Device 10) receives and decodes Packet A.
5. Device 10 responds ACK. Device 10 adds 6 clock cycles to allow the ACK to reach the target device.
6. Device 4 receives and decodes ACK.
7. Device 4 transmits the cell 7 data = Packet B, followed by two additional clock cycles to reach the Master.
8. For responses from Mid and Top devices in Byte Mode, the Master asserts $\overline{DATAREADY}$ after it receives 5 bytes on the Daisy Chain. For responses from the Master, $\overline{DATAREADY}$ goes low at the end of the Daisy Chain ACK response.
9. For responses in Block Mode, the Master asserts $\overline{DATAREADY}$ after receiving the last byte of Packet B from the Daisy Chain.

Figure 55. Daisy Chain Read Example Read Device 4, Cell 7. Stack of 10 Devices

7.3 Communication Protocols

All communications begin with a packet header that contains information about the length (in bytes) of the data portion of the communication (called the payload or packet data). The length segment of Read commands indicates the amount of data to be returned, rather than the length of the command itself.

7.3.1 Packet Header

Each communication carries a 5-byte packet header. Each packet header contains the device stack address, page, register address, payload length (in bytes), frame and a 16-bit CRC, as shown in Figure 56.

Read commands, action commands, and communications administration responses consist of a packet header only, with no associated data information. The only exceptions to this are the Roll Call response and Comms

Failure response, which include a data packet containing the stack size and device stack address information, respectively.

7.3.2 Packet Data

Data Write commands comprise of a packet header plus packet data, each with its own CRC.

Packet data sections carry a single CRC at the end of the data packet. Single register data packets (single register Read responses and single register Write commands) carry a 16 bit CRC. Multiple register data packets carry a 32 bit CRC.

All communications auto increment the register address. Operations begin at the register address provided in the message header and continue (increment) for the number of bytes indicated in the length portion of the header. For Read and Write operations on Page 1, the auto increment skips unused addresses. For Page 2 operations, the auto increment does not skip unused addresses, therefore multiple byte reads across a memory gap need to specify a byte count that includes the missing registers and ignore the contents. Multiple byte writes across a memory gap must specify a byte count that includes the missing registers and send ‘0’s to the unused addresses.

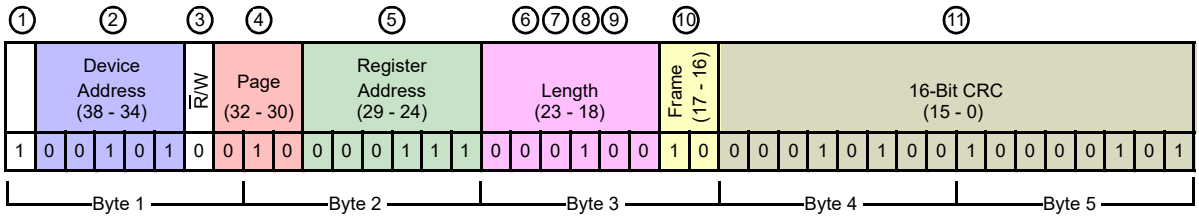
All responses to multiple register Read commands, which access Page 1 data (register address 9’h07F and below) carry the Fault Status register as the first two bytes in the response. This does not apply to single register reads (4-byte length) for which the requested register is returned without the Fault Status register being included. Read commands with register address 9’h080 and higher do not have the Fault Status register added.

Note: The number of registers read is not the same as the payload length. The payload length includes the 16 bit or 32 bit CRC. It also includes the Fault Status register if multiple registers are read starting at an address less than 0x80. (The payload length does not include the 5 byte header.) As such the number of registers read is equal to the payload length minus 2 (for single register reads), minus 6 (for multiple register reads on Page 1), or minus 4 (for multiple reads from any other page); divided by 2.

The RAA489204 responds by sending the contents of the register at the start address location followed by the contents of each subsequent register until the total number of bytes, including CRC, is met.

Packet data sections contain up to 62 bytes, that equates to up to 28 (16-bit) register values plus a 32-bit CRC and the Status Register contents. Single register data packets carry a 16b CRC. Data packets with two or more registers carry a 32b CRC. Legal Packet Data lengths for Write operations, in bytes, are 4, 8, 10, 12, and all even numbers up to 62. Legal Packet Data lengths for Read operations, in bytes, are 4, 10, 12, and all even numbers up to 62. Devices respond to an illegal length value with NAK.

A summary of Communication commands and responses, their respective lengths, and CRC types are shown in Table 15. Single register and multiple register examples are shown in Figure 57 and Table 16.



Example Packet Header: Read Overvoltage Limit Register (Address 9'h087) from device 5, with Frame = 2

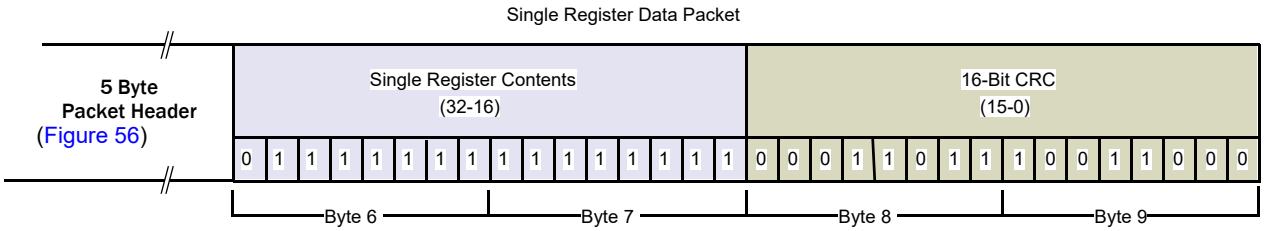
Notes:

1. The protocol requires that the first bit is always '1'.
2. The device address is assigned during the Roll Call process. This address is stored in a local register and is used to address the specific device. All communications sent to and transmitted from the device contain this stack address. A Device address of 0x1F addresses all devices at the same time.
3. The read/write bit indicates the type of operation. Read = 0, Write = 1
4. Page selects a page of the register memory map (See Register Map.
5. Register addresses access registers or commands in the memory map. See Register Map.
6. Communication data packet (payload) length is specified in bytes. Length is the total number of bytes, including CRC and Fault Status register if reading multiple bytes from Page 1.
7. Read command packet length specifies the number of bytes required in the response. For example: 4, 8, 10, 12,...62.
8. Single register Write command packet length = 4 bytes. Multiple register Write command packet length = 8, 10,...62.
9. Action command packet = 0 bytes
10. The frame value sent with a command is incremented and returned with the response.
11. The 16-bit CRC operates on the first 24 bits in the Header.

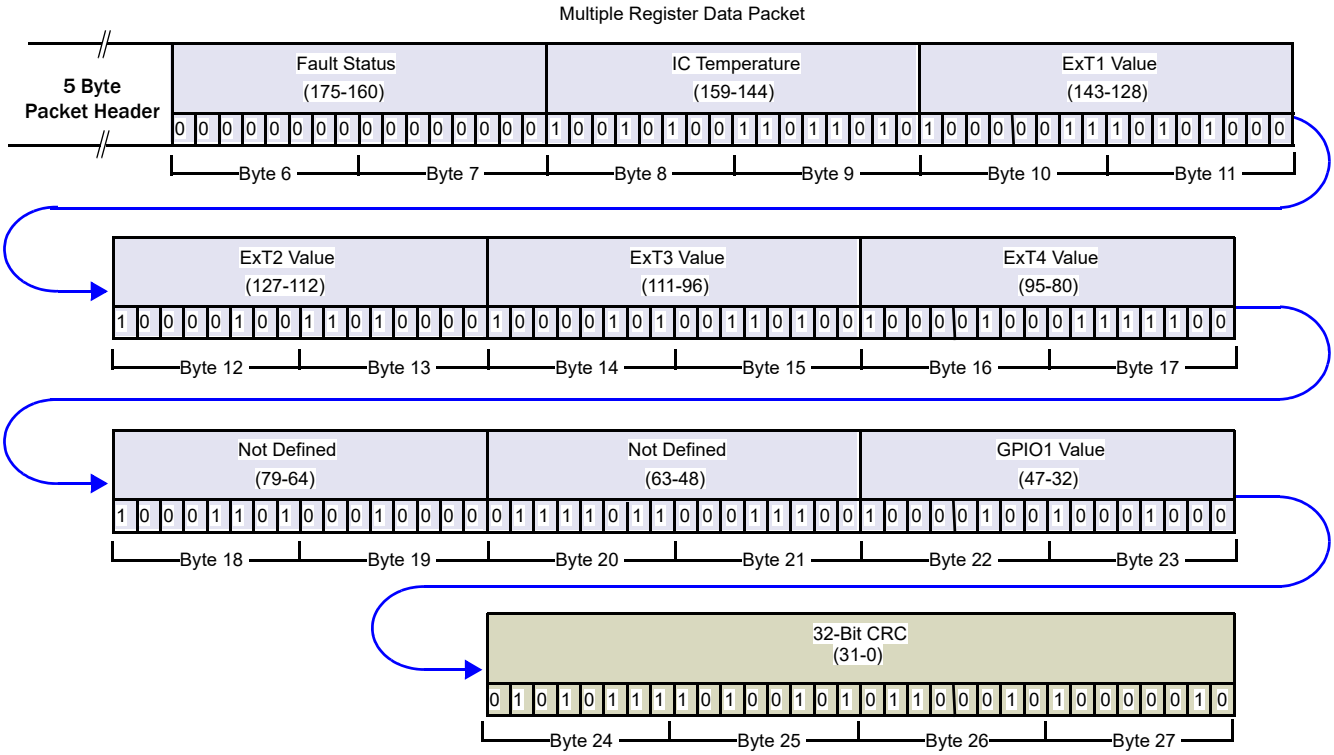
Figure 56. Communication Packet Header

Table 15. Summary of Communication Types

Communication Type	Total Command Length (Bytes)	Length Value	Registers Read/Written	CRC (Bits)	Comment
Read Command	5	0	0	16	Length = 0 because these are "action" commands, with no associated data.
Action Command	5	0	0	16	
Communication Response (ACK/NAK)	5	0	0	16	
Single Register Write	9	4	1	16 (Header); 16 (Data)	
Single Register Read Response	9	4	1	16 (Header); 16 (Data)	
Multiple Register Write	13+	8+	2+	16 (Header); 32 (Data)	
Multiple Register Read Response	13+	8+	2+	16 (Header); 32 (Data)	Registers read/written includes the Fault Status register contents if read from Page 1



a) Example Single Register Data Packet:
Read Overvoltage Limit Register contents (Address 9'h087) - This response (7FFF 1B98) for the OV limit set to the maximum value follows the Packet Header and CRC (84 87 11 AB 19 - not shown)



b) Example Multiple Register Read Data Packet:

Read eight registers starting with the Internal Temperature Register contents (Address 9'h060) - This response (0000 94DA 83A8 84D0 8534 847C 8D10 7B1C 8484 A4F4 7FF7 57A5 6282) follows the Packet Header and CRC (84 60 69 DD A3 - not shown). The values for the NOT DEFINED registers can be anything (and should be ignored), but the CRC is calculated with whatever value is returned from the register. This shows example returned data. *Note:* The Fault Status register contents are added to the response, since the starting data address is less than 9'h080.

Figure 57. Communication Data Packet (Single and Multiregister)

Table 16. Examples of Single and Multiple Register Reads [1]

Read Response																							
Packet Header	Device Address + R/W + Page MSB (See Figure 56)								1	d	d	d	d	d	r/W	p							
	Page + Register Address								p	p	r	r	r	r	r	r	Register address = Data Start Address						
	Length + Frame								L	L	L	L	L	L	f	f	Length = Number of data bytes + CRC Frame = Frame + 1 from Read CMD						
	16-bit CRC								c	c	c	c	c	c	c	c	c	c	c	c	c	c	c

Packet Data Word	Single Register Read Read from 0x41		Packet Data Word	10 Cell Pack Read Voltages (28 Bytes) Read from 0x41		Packet Data Word	Read Temp. (26 Bytes) Read from 0x60		Packet Data Word	Read All Page 1 (60 Bytes) Read from 0x40		Packet Data Word	Read All Fault Status (16 Bytes) Read from 0x80		Packet Data Word	Read Balance Status Read (32 Bytes) Read from 0xB0	
	Addr	Data (2 bytes/row)		Addr	Data (2 bytes/row)		Addr	Data (2 bytes/row)		Addr	Data (2 bytes/row)		Addr	Data (2 bytes/row)		Addr	Data (2 bytes/row)
1	41	VC1 Voltage	1	80	Fault Status	1	80	Fault Status	1	80	Fault Status	1	80	Fault Status	1	B0	Bal Status 1
2		Data CRC	2	41	Cell 1 Voltage	2	60	Int Temp	2	40	Cell Setup	2	81	OV Fault	2	B1	Bal Status 2
			3	42	Cell 2 Voltage	3	61	ExtT1 value	3	41	Cell 1 Voltage	3	82	UV Fault	3	B2	Bal Status 3
			4	43	Cell 3 Voltage	4	62	ExtT2 value	4	42	Cell 2 Voltage	4	83	OW Fault	4	B3	Bal Status 4
			5	44	Cell 4 Voltage	5	63	ExtT3 value	5	43	Cell 3 Voltage	5	84	OT Fault	5	B4	Bal Status 5
			6	45	Cell 5 Voltage	6	64	ExtT4 value	6	44	Cell 4 Voltage	6	85	Gen. Fault	6	B5	Bal Status 6
			7	4A	Cell 10 Voltage	7	65	Not Defined	7	45	Cell 5 Voltage	7		Data CRC	7	B6	Bal Status 7
			8	4B	Cell 11 Voltage	8	66	Not Defined	8	46	Cell 6 Voltage	8		Data CRC	8	B7	Bal Status 8
			9	4C	Cell 12 Voltage	9	67	GPIO1 value	9	47	Cell 7 Voltage				9	B8	Bal Status 9
			10	4D	Cell 13 Voltage	10	68	GPIO2 value	10	48	Cell 8 Voltage				10	B9	Bal Status 10
			11	4E	Cell 14 Voltage	11	70	V_{REF2} voltage	11	49	Cell 9 Voltage				11	BA	Bal Status 11
			12	50	PACK Voltage	12		Data CRC	12	4A	Cell 10 Voltage				12	BB	Bal Status 12
			13		Data CRC	13		Data CRC	13	4B	Cell 11 Voltage				13	BC	Bal Status 13
			14		Data CRC				14	4C	Cell 12 Voltage				14	BD	Bal Status 14
									15	4D	Cell 13 Voltage				15		Data CRC
									16	4E	Cell 14 Voltage				16		Data CRC

Table 16. Examples of Single and Multiple Register Reads [1]

Read Response

Packet Header			
Packet Header	Device Address + R/W + Page MSB (See Figure 56)	1 d d d d d R/W p	
	Page + Register Address	p p r r r r r r	Register address = Data Start Address
	Length + Frame	L L L L L L f f	Length = Number of data bytes + CRC Frame = Frame + 1 from Read CMD
	16-bit CRC	c c c c c c c c c c c c c c c c	

Packet Data Word	Single Register Read Read from 0x41		Packet Data Word	10 Cell Pack Read Voltages (28 Bytes) Read from 0x41		Packet Data Word	Read Temp. (26 Bytes) Read from 0x60		Packet Data Word	Read All Page 1 (60 Bytes) Read from 0x40		Packet Data Word	Read All Fault Status (16 Bytes) Read from 0x80		Packet Data Word	Read Balance Status Read (32 Bytes) Read from 0xB0	
	Addr	**Data (2 bytes/row)**		**Addr**	**Data (2 bytes/row)**		**Addr**	**Data (2 bytes/row)**		**Addr**	**Data (2 bytes/row)**		**Addr**	**Data (2 bytes/row)**		**Addr**	**Data (2 bytes/row)**
									17	50	Pack Voltage						
									18	60	Int Temp						
									19	61	ExtT1 Value						
									20	62	ExtT2 Value						
									21	63	ExtT3 Value						
									22	64	ExtT4 Value						
									23	65	Not Defined						
									24	66	Not Defined						
									25	67	GPIO1 Value						
									26	68	GPIO2 Value						
									27	70	VREF2 Voltage						
									28	71	Scan Count						
									29		Data CRC						
									30		Data CRC						

1. For the 10 Cell Pack option (second column) Cells 6 through 9 are missing. Program the CELL SETUP register = 16’h01E0 to specify skipping these cells.

7.3.3 CRC Calculation

Daisy Chain communications employ either a 16-bit CRC or a 32-bit CRC.

The communications protocol uses the 16-bit and 32-bit CRC to verify data integrity and provide a minimum Hamming Distance of 4 for the header packet and for the data packet. The 16-bit CRC is used with the packet header and with single register data packets. The 32-bit CRC is used with multiple register data packets.

All CRC calculations are performed using an initial value of all 1s and all CRC calculations use the same method, in which a CRC Register is XOR'ed with the CRC polynomial on condition of the next bit in the input data code (and its relation to the MSB of the CRC register.)

The CRC register starts with the initial value and finishes the process with the required CRC value (See Table 17). Each process loop starts with a comparison of the next bit of input data with the MSB of the CRC register. This comparison is a Bit XOR, so that if the two bits are equal, the result is '0' and if they are unequal the result is '1'.

If the result is '0', then the CRC register is rotated left one bit and the process is repeated with the next bit in sequence. If the result is '1' a register XOR is performed between the CRC polynomial and the (left shifted by one) CRC register.

The 32-bit (data) CRC is calculated in the same manner as the 16-bit CRC. The initial and polynomial values for the CRC calculations are shown in Table 17. A logical flow chart of the operation is shown in Figure 58.

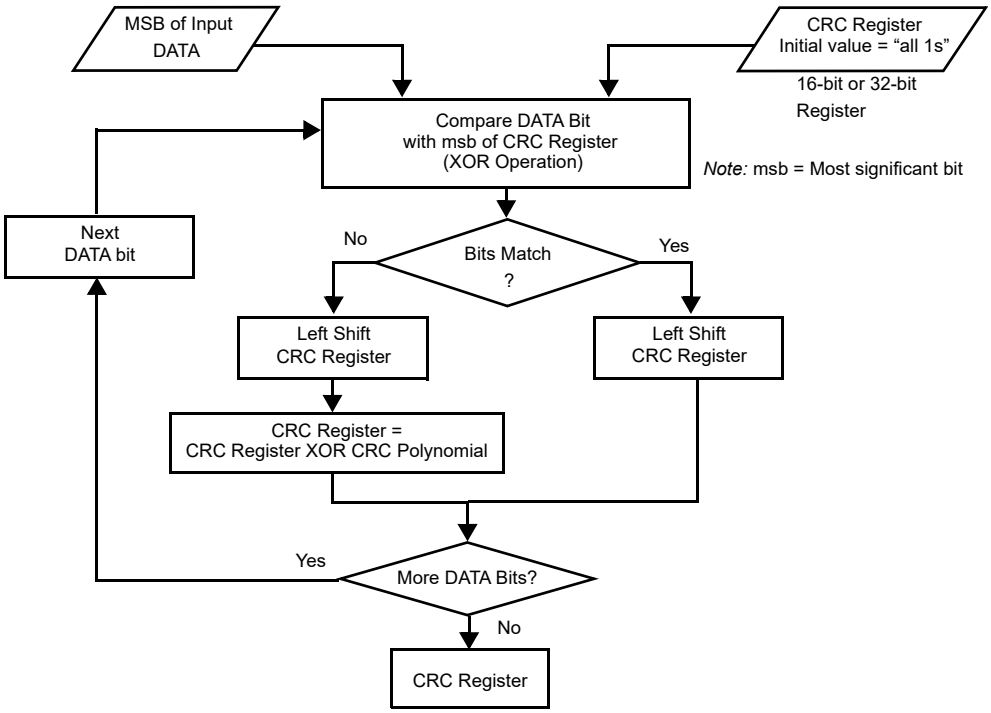


Figure 58. CRC Calculation

Table 17. CRC Polynomial and Initial Values

CRC	Initial Value	Polynomial		
		Equation	Binary	Hex
16-bit	0xFFFF	$X^{16}+X^{12}+X^5+1$	1 0001 0000 0010 0001	17'h1 1021
32-bit	0xFFFF FFFF	$X^{32}+ X^{26}+ X^{23}+ X^{22}+ X^{16}+ X^{12}+ X^{11}+ X^{10}+ X^8+ X^7+ X^5+ X^4+ X^2+ X^1+ 1$	1 0000 0100 1100 0001 0001 1101 1011 0111	33'h1 04C1 1DB7

```
package crctest;

public class Crc32mpeg2
{
     private static final int crcInit = 0xFFFFFFFF;
     private static final int XorOut = 0x0;
     private static final boolean RefOut = false;
     private static final int Poly = 0x4C11DB7;
     private static final boolean RefIn = false;
     private static final int Check = 0x376E6E7;

    private static final int array[] = {0x00000000, 0x04C11DB7, 0x09823B6E, 0x0D4326D9, 0x130476DC, 0x17C56B6B,
    0x1A864DB2, 0x1E475005, 0x2608EDB8, 0x22C9F00F, 0x2F8AD6D6, 0x2B4BCB61, 0x350C9B64, 0x31CD86D3, 0x3C8EA00A,
    0x384FBDBD, 0x4C11DB70, 0x48D0C6C7, 0x4593E01E, 0x4152FDA9, 0x5F15ADAC, 0x5BD4B01B, 0x569796C2, 0x52568B75,
    0x6A1936C8, 0x6ED82B7F, 0x639B0DA6, 0x675A1011, 0x791D4014, 0x7DDC5DA3, 0x709F7B7A, 0x745E66CD, 0x9823B6E0,
    0x9CE2AB57, 0x91A18D8E, 0x95609039, 0x8B27C03C, 0x8FE6DD8B, 0x82A5FB52, 0x8664E6E5, 0xBE2B5B58, 0xBAEA46EF,
    0xB7A96036, 0xB3687D81, 0xAD2F2D84, 0xA9EE3033, 0xA4AD16EA, 0xA06C0B5D, 0xD4326D90, 0xD0F37027, 0xDDB056FE,
    0xD9714B49, 0xC7361B4C, 0xC3F706FB, 0xCEB42022, 0xCA753D95, 0xF23A8028, 0xF6FB9D9F, 0xFBB8BB46, 0xFF79A6F1,
    0xE13EF6F4, 0xE5FFEB43, 0xE8BCCD9A, 0xEC7DD02D, 0x34867077, 0x30476DC0, 0x3D044B19, 0x39C556AE, 0x278206AB,
    0x23431B1C, 0x2E003DC5, 0x2AC12072, 0x128E9DCF, 0x164F8078, 0x1B0CA6A1, 0x1FCDBB16, 0x018AEB13, 0x054BF6A4,
    0x0808D07D, 0x0CC9CDCA, 0x7897AB07, 0x7C56B6B0, 0x71159069, 0x75D48DDE, 0x6B93DDDB, 0x6F52C06C, 0x6211E6B5,
    0x66D0FB02, 0x5E9F46BF, 0x5A5E5B08, 0x571D7DD1, 0x53DC6066, 0x4D9B3063, 0x495A2DD4, 0x44190B0D, 0x40D816BA,
    0xACA5C697, 0xA864DB20, 0xA527FDF9, 0xA1E6E04E, 0xBFA1B04B, 0xBB60ADFC, 0xB6238B25, 0xB2E29692, 0x8AAD2B2F,
    0x8E6C3698, 0x832F1041, 0x87EE0DF6, 0x99A95DF3, 0x9D684044, 0x902B669D, 0x94EA7B2A, 0xE0B41DE7, 0xE4750050,
    0xE9362689, 0xEDF73B3E, 0xF3B06B3B, 0xF771768C, 0xFA325055, 0xFEF34DE2, 0xC6BCF05F, 0xC27DEDE8, 0xCF3ECB31,
    0xCBFFD686, 0xD5B88683, 0xD1799B34, 0xDC3ABDED, 0xD8FBA05A, 0x690CE0EE, 0x6DCDFD59, 0x608EDB80, 0x644FC637,
    0x7A089632, 0x7EC98B85, 0x738AAD5C, 0x774BB0EB, 0x4F040D56, 0x4BC510E1, 0x46863638, 0x42472B8F, 0x5C007B8A,
    0x58C1663D, 0x558240E4, 0x51435D53, 0x251D3B9E, 0x21DC2629, 0x2C9F00F0, 0x285E1D47, 0x36194D42, 0x32D850F5,
    0x3F9B762C, 0x3B5A6B9B, 0x0315D626, 0x07D4CB91, 0x0A97ED48, 0x0E56F0FF, 0x1011A0FA, 0x14D0BD4D, 0x19939B94,
    0x1D528623, 0xF12F560E, 0xF5EE4BB9, 0xF8AD6D60, 0xFC6C70D7, 0xE22B20D2, 0xE6EA3D65, 0xEBA91BBC, 0xEF68060B,
    0xD727BBB6, 0xD3E6A601, 0xDEA580D8, 0xDA649D6F, 0xC423CD6A, 0xC0E2D0DD, 0xCDA1F604, 0xC960EBB3, 0xBD3E8D7E,
    0xB9FF90C9, 0xB4BCB610, 0xB07DABA7, 0xAE3AFBA2, 0xAAFBE615, 0xA7B8C0CC, 0xA379DD7B, 0x9B3660C6, 0x9FF77D71,
    0x92B45BA8, 0x9675461F, 0x8832161A, 0x8CF30BAD, 0x81B02D74, 0x857130C3, 0x5D8A9099, 0x594B8D2E, 0x5408ABF7,
    0x50C9B640, 0x4E8EE645, 0x4A4FFBF2, 0x470CDD2B, 0x43CDC09C, 0x7B827D21, 0x7F436096, 0x7200464F, 0x76C15BF8,
    0x68860BFD, 0x6C47164A, 0x61043093, 0x65C52D24, 0x119B4BE9, 0x155A565E, 0x18197087, 0x1CD86D30, 0x029F3D35,
    0x065E2082, 0x0B1D065B, 0x0FDC1BEC, 0x3793A651, 0x3352BBE6, 0x3E119D3F, 0x3AD08088, 0x2497D08D, 0x2056CD3A,
    0x2D15EBE3, 0x29D4F654, 0xC5A92679, 0xC1683BCE, 0xCC2B1D17, 0xC8EA00A0, 0xD6AD50A5, 0xD26C4D12, 0xDF2F6BCB,
    0xDBEE767C, 0xE3A1CBC1, 0xE760D676, 0xEA23F0AF, 0xEEE2ED18, 0xF0A5BD1D, 0xF464A0AA, 0xF9278673, 0xFDE69BC4,
    0x89B8FD09, 0x8D79E0BE, 0x803AC667, 0x84FBDBD0, 0x9ABC8BD5, 0x9E7D9662, 0x933EB0BB, 0x97FFAD0C, 0xAFB010B1,
    0xAB710D06, 0xA6322BDF, 0xA2F33668, 0xBCB4666D, 0xB8757BDA, 0xB5365D03, 0xB1F740B4};

    Crc32mpeg2() {};

    public int computeCrc(byte[] dataArray)
    {

        int crc = this.crcInit;

        if (this.RefOut)
        {
            for (byte d: dataArray)
            {
                crc = this.array[(d ^ crc) & 0xFF] ^ (crc >> 8 & 0xFFFFFF);
            }

        } else
        {
            for (byte d : dataArray)
            {
                crc = this.array[((crc >> 24) ^ d) & 0xFF] ^ (crc << 8);
            }
        }

        crc = crc ^ this.XorOut;
        return crc;
    }

}
```

Figure 59. Sample 32-Bit CRC Code

7.3.4 Communication Protocol Examples

Table 18 shows some example Read and Write commands, and Table 16 shows examples for single register and multiregister Read responses.

Table 18. Read and Write Command Packet Header and Packet Data Examples

Operation/ Example			Packet Header (Hex values)							Packet Data		Total Regs	Total Header + Data Bytes + CRC
			1			2	3		4, 5				
			Leading '1'	Device Address (5 bits)	R/W + Page MSB	Page + Addr (8 bits)	Length (6 bits)	Frame (2 bits)	CRC (16 bits)	Register Data	CRC (16 or 32 bits)		
Roll Call Command, Five Devices	Transmit	X	1	xx	00	D0	0	0	xxxx	No Command Data		0	5
	Receive	R	1	Top	00	D0	0	1	xxxx	None		0	5
	Example	X	80			D0	00		E2E1			0	5
		R	94			D0	01		6D63			0	5
Read All Cell and Pack Voltages Device 2, Starting at VCELL1. (32 bytes + 4 CRC)	Transmit	X	1	2	00	41	24	0	xxxx	No Command Data		0	5
	Receive	R	1	2	00	41	24	1	xxxx	Fault Status + Cell1 to Cell 14 + Pack Voltage	xxxx xxxx	16	41
	Example	X	88			41	90		E323			0	5
		R	88			41	91		F302	0000 372E 3734 371E 371C 3729 3724 3721 3734 3726 372E 372C 3726 372D 3726 623F (example)	2362 BDE 4	16	41
Read Cell Setup Register Device 5 (2 bytes + 2 CRC)	Transmit	X	1	5	00	40	04	0	xxxx	No Command Data		0	5
	Receive	R	1		00	40	04	1	xxxx	Cell Setup Register	xxxx xxxx	1	9
	Example	X	94			40	10		7798			0	5
		R	94			40	11		67B9	0000	1D0F	1	9
Read All Temperatures Device 1 (IC Temperature to Reference Voltage). (22 bytes + 4 CRC)	Transmit	X	1	1	00	60	1A	0	xxxx	No Command Data		0	5
	Receive	R	1	1	00	60	1A	1	xxxx	Fault Status + IC Temperature, all ExTn and GPIO inputs, and Reference Voltage	xxxx xxxx	11	31
	Example	X	84			60	68		CD82			0	5
		R	84			60	69		DDA3	0000 944B 7F58 80F4 8028 7FFC 8930 7BFC FFFC FFFC 8007 (example)	EBB 2 E79B	11	31
Read 9 Registers from Page = 010, Addr = 00 0001 in Device 4 (18 bytes + 4 CRC)	Transmit	X	1	4	00	81	16	0	xxxx	No Command Data		0	5
	Receive	R	1	4	00	81	16	1	xxxx		xxxx xxxx	9	27
	Example	X	90			81	58		47F1			0	5
		R	90			81	59		57D0	0000 0000 0000 0000 0000 00B8 7FFF 0000 0000 (example)	9A4E 88DE	9	27

Table 18. Read and Write Command Packet Header and Packet Data Examples (Cont.)

Operation/ Example			Packet Header (Hex values)							Packet Data		Total Regs	Total Header + Data Bytes + CRC
			1			2	3		4, 5				
			Leading '1'	Device Address (5 bits)	R/W + Page MSB	Page + Addr (8 bits)	Length (6 bits)	Frame (2 bits)	CRC (16 bits)	Register Data	CRC (16 or 32 bits)		
Write Cell Setup Register Device 1. (2 bytes + 2 CRC)	Transmit	X	1	1	10	40	04	0	xxxx	Cell Setup	xxxx	1	9
	Receive	R	1	1	00	D2	0	1	xxxx	(Response is ACK)		0	5
	Example	X	86			40	10		5A9B	000A	BC45	1	9
		R	84			D2	01		4862	(Response is ACK)		0	5
Write Four Cell Balance Value Registers in Device 1 (8 bytes + 4 CRC)	Transmit	X	1	1	10	A7	0C	0	xxxx	Cell 8 Balance Value - Cell 11 Balance Value	xxxx xxxx	4	17
	Receive	R	1	1	00	D2	0	1	xxxx	(Response is ACK)		0	5
	Example	X	86			A7	30		F7DC	8AA7 10A6 DF01 020E	8C29 66FF	4	17
		R	84			D2	01		4862			0	5
Write 14 Cell Balance Status registers from Location 010 11_0000 in Device 2 (28 bytes + 4 CRC)	Transmit	X	1	2	10	B0	20	0	xxxx	Balance Status 1 - Balance Status 14	xxxx xxxx	16	33
	Receive	R	1	2	00	D2	0	1	xxxx	(Response is ACK)		0	5
	Example	X	8A			B0	80		BF82	0040 003E 0000 0029 003E 0000 0029 0137 0000 001E 0085 000A 0005 009F	AFB6 1FB6	14	37
		R	84			D2	01		4862			0	5
Scan Cells Command (Address All)	Transmit	X	1	3F	00	C1	0	0	xxxx	No Command Data		0	5
	Receive	R	No Response - Check the Scan Count. It increments when the command is received.										
	Example	X	FC			C1	00		7FCA			0	5
		R	No Response - Check the Scan Count. It increments when the command is received.										

8. Device Commands

Commands are sent to devices in the Daisy Chain using the address of the device in the stack, as determined by the Roll Call operation. The address resides in bits 6:2 in the first byte (Byte 1) of the command header (after the leading '1'), see Figure 56.

Table 19. First Two Bytes of Packet Header

	1	Device Address					$\overline{R}$/ W	Page			Register Address					
Bit Sent	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**
Roll Call Only	1	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0
Address All	1	1	1	1	1	1	0	0	Target Register or Command Byte							
Read	1	x	x	x	x	x	0	x								
Write	1	x	x	x	x	x	1	x								

Many of the instructions can use an Address All device stack address. This address (all ones) is used with device commands to cause all stack devices to perform functions simultaneously. The commands with required Address All addressing are shown in Table 26. A device address of all zeros is only valid for a Roll Call command. Roll Call can use any address (including Address All).

Commands are sent from an external microcontroller to the RAA489204 using a memory Read operation using a specific address. The address of the command consists of the two LSBs of the page plus the register address. This address value populates the second byte of the command header. See Page 3 of the Register Map.

8.1 Read/Write

The read/write bit follows the Device address in the first byte of the Packet Header and identifies the operation as a Read or a Write. A read/write bit of '0' indicates a Read. A read/write bit of '1' indicates a Write. A Read or Write operation contains the page and address of the target register in the second byte of the Packet Header.

8.2 Scan Voltages (Address: C1H)

The Scan Voltages command causes the addressed device (or all devices if the Address All address is used) to sample all cell voltage inputs and perform an analog-to-digital conversion on all cell, PACK, and internal temperature voltages. The RAA489204 calibrates the cell and PACK results using the internal temperature and stores all results in their respective registers. For timing of internal operations relative to the command, see Figure 66 and Figure 67. For internal timing details, see Table 43.

The voltage readings of the cells connected to each device are performed sequentially in response to a Scan command. The start of the scan in the Master device begins [14.5 + N] Daisy clocks (N = number of Devices) before the start of a scan in Device 2. All Mid and Top Devices start their scans at the same time. For example, for a stack of 10 devices with a Daisy Chain operating at 1000kHz, the Master starts its scan 24.5µs before the Mid and Top devices, which subsequently start scanning within a 1µs window of each other. See Figure 67.

The RAA489204 ignores a Scan command when the device is already in a Scan mode. However, the command passes through to other devices in the Daisy Chain. All other communications functions respond normally while the device is scanning or measuring.

At the end of each scan, overvoltage and undervoltage compares are performed on each cell voltage reading, and the VBAT and VSS pins are checked for an open connection. These fault conditions are subject to filtering. If the fault condition exceeds the filter value, a fault condition exists, and the device sets the corresponding bits in the Overvoltage, Undervoltage, and Fault Status registers. At the end of each scan, the device also performs an EEPROM MISR check and flags if errors occur. If there are any faults, the device sets the $\overline{FAULT}$ pin low. Devices revert to the standby state on completion of the scan activity.

8.2.1 PACK Voltage Adjustment

The voltage read from the PACK voltage register is accurate with respect to the input pin of the RAA489204 PACK pin. However, it does not compensate for external components. There is an input bias current I_{PACK} of approximately 40µA (see Electrical Specifications on IPACK) and, when the PACK voltage measurement is taken, an internal voltage divider is switched in, drawing current from PACK through approximately 320kΩ of resistance (see Electrical Specifications on IPACK) These input currents produce a voltage drop across the PACK pin off-chip resistor, resulting in potential PACK voltage measurement errors. The RAA489204 device factory test system includes a 1kΩ series resistor and the accuracy of the PACK measurement includes this 1kΩ resistor. So, if a series resistor other than 1kΩ is used, the resulting error should be compensated in the microcontroller using the expressions shown in Figure 60.

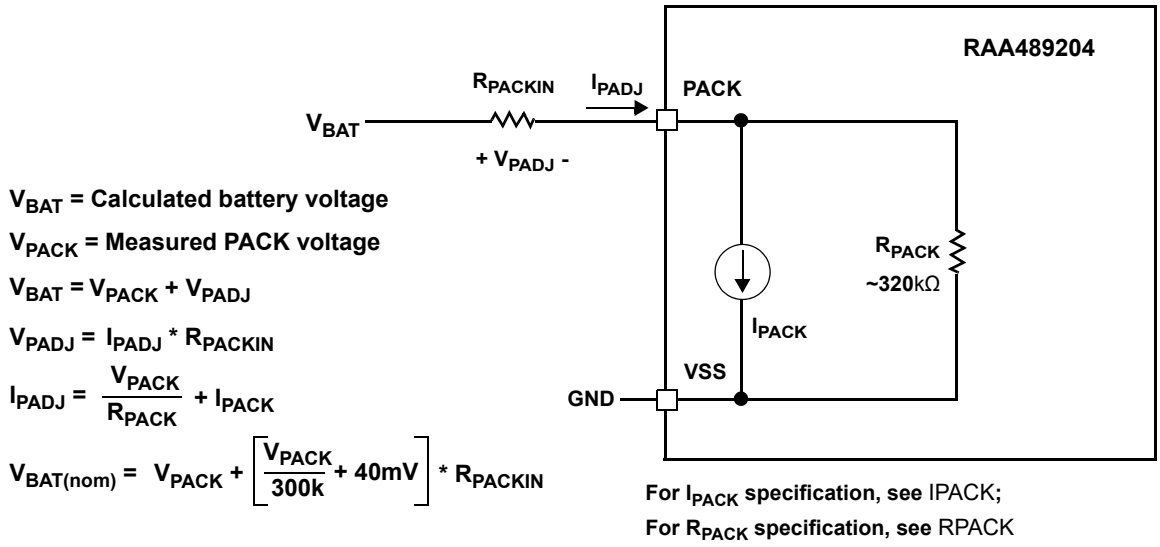


Figure 60. Pack Voltage Adjustment

8.2.2 Fault Signal Filtering

Filtering is provided for the cell overvoltage and cell undervoltage tests. These fault signals use a totalizing method in which an unbroken sequence of positive results is required to validate a fault condition. The sequence length (number of sequential positive samples) is set by the TOT[2:0] bits in the Fault Setup register. See Table 20.

Separate filter functions are provided for each cell input. The filter is reset whenever a test results in a negative result (no fault). Any write to the Fault Status register TOT[2:0] bits resets all filters. When a fault is detected, rewrite the TOT[2:0] bits to clear the Totalizers.

Table 20. Totalizer Sample Count

TOT[2:0]	Totalizer Count
000	1
001	2
010	4
011	8 (Default)
100	16
101	32
110	64
111	128

8.2.3 Cell Voltage Averaging

The RAA489204 has a cell voltage averaging function applied to the cell and PACK voltage measurements, allowing the system designer to request an averaged value from a number of samples. The averaging function is controlled by the CAV[2:0] bits in the Device Setup 2 register with the number of samples averaged determined by the setting of these bits. See Table 21 for more information.

Table 21. Cell Voltage Averaging

[CAV2:CAV0]	Number of Samples Averaged
000	1 (Default)
001	2
010	4
011	8
100	16
101	32

8.3 Scan Temperatures (Address: C2H)

The Scan Temperatures command causes the addressed device (or all devices if the Address All address is used) to scan through the PACK, Second Voltage Reference, Internal Temperature, four external temperature inputs, and two GPIO input signals. See Figure 61. For timing of internal operations relative to the command, see Figure 66 and Figure 67. For internal timing details, see Table 46.

For temperature measurements a switched bias voltage output (TEMPREG, pin 39) provides a reference to perform ratiometric measurements on the external temperature and GPIO inputs. TEMPREG is turned on in response to a Scan Temperatures command. The voltage at the TEMPREG output is a buffered version of the ADC reference voltage (see Figure 45). A dwell time of 2.5ms is provided to allow external circuits to settle after TEMPREG turns on, after which the ADC measures each external input in turn. TEMPREG turns off after temperature measurements are completed.

The ExTn and GPIO inputs, when used to monitor temperature, are designed for use with NTC type thermistor sense elements. These inputs can also be used as general purpose analog inputs. The NO_TREG bit in the Device Setup register controls the operation of the TEMPREG output and the associated 2.5ms delay when using the Measure command to measure a temperature value. NO_TREG has no effect when using the Scan Temperatures command. Setting the NO_TREG bit to ‘1’ disables the TEMPREG output and removes the 2.5ms delay from the Measure Temperature operation (see Measure (Address: C8H)).

A Temperature MUX test is performed as part of the Scan Temperatures operation. The results of this are compared against internally programmed limit values to verify correct operation of the multiplexers and ADC. The TMX bit in the Fault Status register is set if this test fails. The device then cycles through each measurement and saves the values to their respective registers. At the end of each scan, the device performs an EEPROM MISR check, compares the measured value of the internal temperature against Internal Temperature Warning and Internal Temperature Limit register values, and compares external input values against the External Temperature

Limit register value. Bits corresponding to these tests are set in the Fault Status and Over-Temperature Fault registers if any of these tests detects a fault.

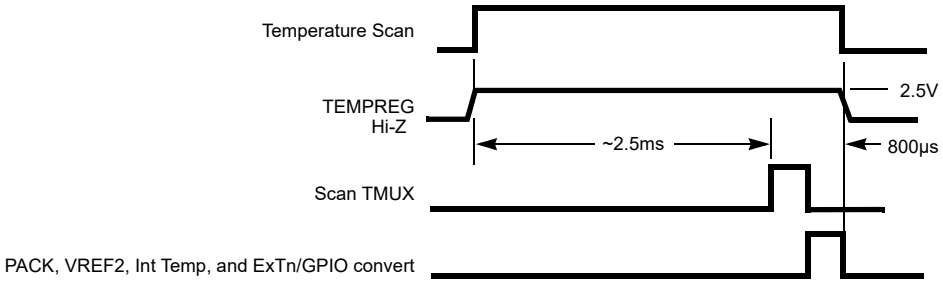


Figure 61. Timing for Scan Temperature Command

Application of the external over-temperature test is controlled by the setting of the over-temperature test bits [TSTE4:TSTE1 and TSTG2:TSTG1] in the Fault Setup register. If any of these bits are set to ‘0’, the over-temperature test is bypassed for that input.

If a fault condition exists, the device sets the $\overline{\text{FAULT}}$ pin low.

The external temperature inputs are designed so that an open connection results in the input being pulled up to the full-scale input level. This function is provided by a switched 10MΩ pull-up resistor from each input to VCC. This feature is part of the fault detection system and detects open pins. The GPIO1 and GPIO2 pins are also pulled up to VCC using a 10MΩ resistor when selected as inputs.

The TMUX bit in the RAA489204 Device Setup 2 register controls whether the temperature registers contain the measured values of the temperature inputs or the results of the TMUX test at the end of the temperature scan.

When TMUX is 0, the measured values of the temperature inputs are placed in the Temperature registers at the end of the scan function. Setting TMUX to 1 effectively cancels the measurement part of the scan and stops the scan after the Temperature MUX Scan portion. In this way, the registers are left with the results of the Temperature MUX Scan.

When TMUX is set to 1, the expected test values in the registers at the end of a temperature scan are as listed in Table 22.

Table 22. Reported Values Following External Temperature Scan with TMUX Bit = 1

Register	Page	Address	Value (mV) (Typical)	Code (Typical)
Pack Voltage	1	6h’10	1924	C504
IC Temp	1	6h’20	2116	D8AD
xT1	1	6h’21	771	4EF3
xT2	1	6h’22	963	629C
xT3	1	6h’23	1155	7645
xT4	1	6h’24	1347	89EE
GPIO1	1	6h’27	386	2786
GPIO2	1	6h’28	571	3A78
Reference Voltage	1	6h’30	193	13C3

Note: The various temperature limits are applied against the output register values, independent of the setting of the TMUX bit. This functionality may be used to verify operation of the various limits. It is up to you to disable the over-temperature fault detection before conducting a Scan with TMUX set to 1, if these limit tests are not Required.

8.3.1 Temperature Voltage Averaging

The RAA489204 has a temperature voltage averaging function applied to the ExT4:ExT1 inputs, allowing the system designer to request an averaged value from a number of samples. The averaging function is controlled by the TAV(2:0) bits in the Device Setup 2 register with the number of samples averaged determined by the setting of these bits (see Table 23).

Table 23. Temperature Voltage Averaging

TAV2:TAV0	Number of Samples Averaged
000	1 (Default)
001	2
010	4
011	8
100	16
101	32

8.4 Voltage and Temperature Data Format

The RAA489204 saves each cell and temperature voltage measurement as a 16-bit value. This means that the two LSBs are always zero for a single 14-bit ADC conversion. This provides the nominal 14-bit of ADC data plus an additional two bits for averaging.

8.5 Scan Mixed (Address: C3H)

The Scan Mixed command causes the addressed part (or all devices if the Address All address is used) to measure the external input (ExT1) in addition to measuring the cell voltages. The internal operation scans cells 1-7, then ExT1, and then cells 8-14 and the PACK voltage. For timing of internal operations relative to the command, see Figure 66 and Figure 67. For internal timing details, see Table 44.

There is no delay on the measurement of ExT1 in this mode. The Scan Mixed measurement mode is used for pack current measurement and provides minimum latency between the cell voltage and pack current measurements. The normal cell overvoltage and undervoltage compares, along with the VBAT and VSS open conditions are checked as part of the Scan Mixed operation. If any of these show a fault condition, the device sets bits in the Open-Wire Fault and Fault Status registers. In addition, the ExT1 voltage is compared with the Temperature limits, unless the TSTE1 bit is set to 0. The device performs an EEPROM MISR check at the end of the scan activity and flags if faults occur.

Cell voltage, pack voltage, and ExT1 data, along with any fault conditions, are stored in local memory ready for reading by the system host microcontroller. If a fault condition exists, the device sets the $\overline{\text{FAULT}}$ pin low.

Totalizer settings and operation, along with Voltage and temperature Averaging operations, apply to Scan Mixed command.

8.6 Scan Wires (Address: C4H)

The Scan Wires command causes the addressed part (or all devices if the Address All address is used) to execute an open wire check on all the cell input (VCn) pins. This is part of the fault detection system. For timing of internal operations relative to the command, see Figure 66 and Figure 67. For internal timing details, see Table 47.

The Scan Wires command is conducted in two phases with timing controlled by the WSCN bit in the Fault Setup 1 register. The first phase tests the VC1 to VC14 inputs and completes in approximately 1.9ms (WSCN = 0) or 5.4ms (WSCN = 1). the second phase tests the VC0 connection and completes in approximately 1ms. Also, at the end of each scan, the device performs an EEPROM MISR check and flags if faults occur.

If a fault condition occurs, the device sets the $\overline{\text{FAULT}}$ pin low. No cell voltage data is sent in response to a Scan Wires command.

The wire scan function in the RAA489204 deliberately disturbs the cell voltages to analyze the input condition. There is a settling time associated with this action, during that time an error exists on the cell inputs. This settling time is a function of the time constant of filters attached to the cell input pins. Allow a duration of at least ten time constants before conducting cell voltage measurements.

Always perform a Scan Voltage, Scan Mixed, or Scan All command following a Scan Wires command before reading cell voltages.

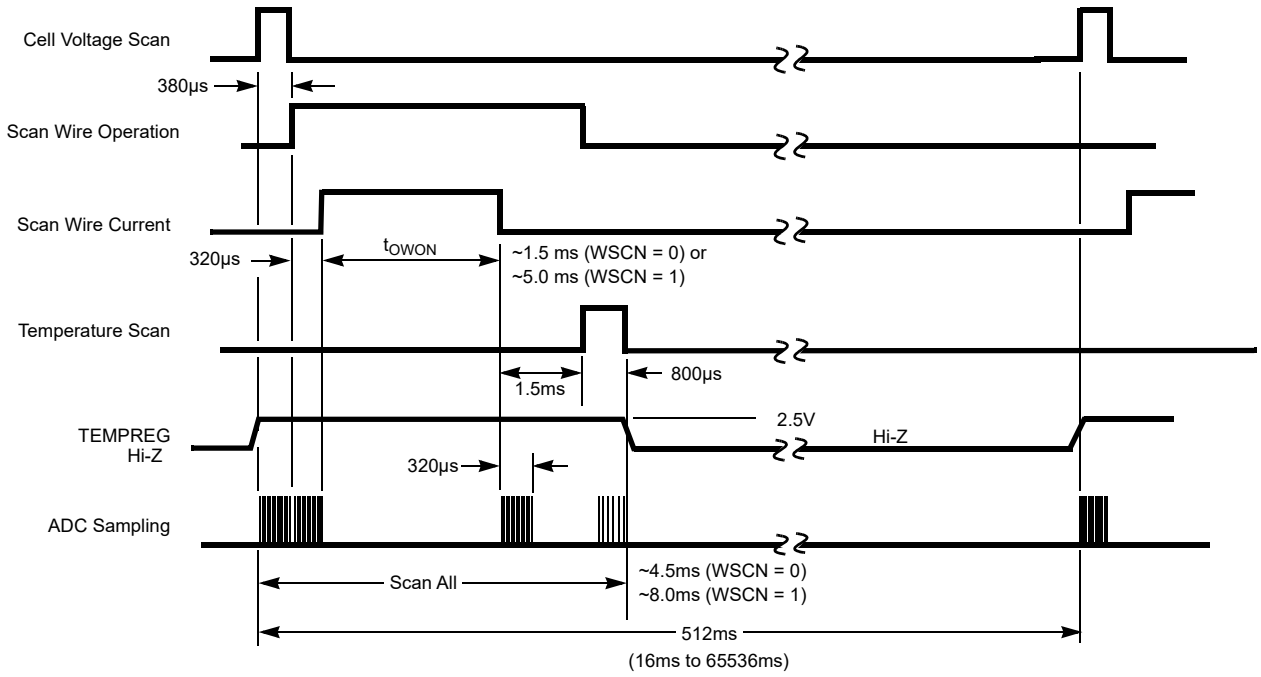
Neither the Totalizer operation nor Averaging options apply to the Scan Wires operation.

8.7 Scan All (Address: C5H)

The Scan All command performs the Scan Voltages, Scan Wires, and Scan Temperatures commands and causes the addressed part (or all parts if the common address is used) to execute each of these three scan functions once, in sequence. For timing of internal operations relative to the command, see Figure 66 and Figure 67. For internal timing details, see Table 45.

The Scan All function starts with a normal Scan Voltages operation, that measures the cell inputs, PACK voltage, IC temperature, and V_{BAT} and VSS open connections. At the conclusion of the Scan Voltages operation, the Scan Wires function begins and, at the same time, the TEMPREG output is switched on. The Scan Wires command completes in approximately 2.79ms or 6.29ms depending on the setting of the WSCN bit, during which time the temperature inputs have settled. The Scan All function then completes with measuring the temperature signals and Second Voltage Reference per the normal Scan Temperatures command (see Figure 62 for example timing). Also, at the end of each scan, the device performs an EEPROM MISR check and flags if faults occur. If a fault condition occurs, the device sets the $\overline{\text{FAULT}}$ pin low.

Totalizer settings and operation, along with Voltage and temperature Averaging operations, apply to Scan All command.



The Scan All command repeats in Scan Continuous Mode (See Table 24)

For t_{OWON} timing, see t_{OWON})

Figure 62. Timing for Scan All Command

8.8 Scan Continuous (Address: C6H)

Scan Continuous mode is used primarily for fault monitoring and incorporates the Scan All command operations.

The Scan Continuous command sets the SCAN bit in the Device Setup 1 register in the addressed device and performs repeated scans at a predetermined scan rate. Each device operates asynchronously on its own clock, and automatically executes Scan All operations at intervals determined by the SCN0-3 bits in the Fault Setup register, rather than in response to a Scan command from the microcontroller.

Due to the asynchronous nature of the Scan Continuous function, the cell and temperature (data) registers should not be read while the RAA489204 is operating in Scan Continuous mode. Stop scanning on all devices in the chain before reading data from a device. This can be done by sending the Scan Inhibit command using Address All. Restart Scan Continuous after reading data by sending the Scan Continuous command.

Table 24 shows the scan rate timing available. Figure 62 shows an example temperature scan with the RAA489204 operating in Scan Continuous mode with a scan interval of 512ms.

Changing the Scan Continuous timing interval can be done at any time, but the new value does not take effect immediately if the Scan Continuous operation is already in progress. Send a Scan Inhibit command to stop the scan, then send the Scan Continuous command to start the scan again. Or, change the timing interval value only when the continuous scan is inactive.

Table 24. Scan Continuous Timing Interval

Scan Interval [SCN3:0]	Scan Interval (ms)
0000	16
0001	32
0010	64
0011	128
0100	256
0101	512
0110	1024
0111	2048
1000	4096 (Default)
1001	8192
1010	16384
1011	32768
1100	65536

Devices can be operated in Scan Continuous mode while in Normal mode or in Sleep mode. To operate the Scan Continuous function in Sleep mode, the host microcontroller simply configures the RAA489204, starts the Scan Continuous mode, and then sends the Sleep command. The RAA489204 wakes itself up each time a scan is required. At the conclusion of the scan, devices revert to the Sleep mode or remain in Normal mode, as applicable on completion of each scan.

The voltage and temperature readings of a Scan All command in Scan Continuous operation are not immediately returned to the Master. Instead, they are stored in local volatile memory and can be accessed at any time by the system host microcontroller. However, devices detecting a fault condition take immediate action.

If the device detects a fault condition in the Scan Continuous mode, a device operating in Normal mode immediately sets the $\overline{\text{FAULT}}$ pin low and sends a Fault Response to the Master device through the Daisy Chain. A device operating Scan Continuous in Sleep mode that detects a fault, first sends the wakeup command on both its upper and lower Daisy Chain ports in order to wake up other stack devices. The device then sets its $\overline{\text{FAULT}}$ pin active and sends the Fault Response.

The RAA489204 provides an option that pauses any cell balancing activity while measuring cell voltages. This is controlled by the BDDS bit in the Balance Setup register. If BDDS is set, then cell balancing is inhibited during cell voltage measurement and for 10ms before the cell voltages are scanned. Balancing is re-enabled at the end of the scan to allow balancing to continue. This function only applies when using the Scan Continuous function (with cell balancing enabled) or when using the Auto Balance function. This allows automatic operations when using the circuit arrangement shown in Figure 32. Using this circuit connection when measuring cell voltages with host initiated scans requires the host microcontroller to manually stop balancing functions before sending a Scan or Measure command.

8.9 Scan Inhibit (Address: C7H)

The Scan Inhibit command resets the SCAN bit and stops the Scan Continuous function. Sending this command to a device that is not in a Scan Continuous mode has no effect.

8.10 Measure (Address: C8H)

This command allows the measurement of a single cell voltage, PACK voltage, internal temperature, external temperature input, GPIO input, or the Second Reference Voltage. For timing of internal operations relative to the

command, see Figure 66 and Figure 67. The Measure command uses the Length portion of the communications header to define which signal is measured. See Table 25. The device matching the target address responds by conducting the single measurement and loading the result to local memory. The host microcontroller then reads from the target device to obtain the measurement result.

Table 25. Measure Command Target Element Addresses

Measure Command	Measure Element Address (Length Portion of Communication Header)	Description
0C8	6'h00	PACK Voltage
	6'h01	Cell 1 Voltage
	6'h02	Cell 2 Voltage
	6'h03	Cell 3 Voltage
	6'h04	Cell 4 Voltage
	6'h05	Cell 5 Voltage
	6'h06	Cell 6 Voltage
	6'h07	Cell 7 Voltage
	6'h08	Cell 8 Voltage
	6'h09	Cell 9 Voltage
	6'h0A	Cell 10 Voltage
	6'h0B	Cell 11 Voltage
	6'h0C	Cell 12 Voltage
	6'h0D	Cell 13 Voltage
	6'h0E	Cell 14 Voltage
	6'h0F	Reserved
	6'h10	Internal temperature reading
	6'h11	ExT1 reading
	6'h12	ExT2 reading
	6'h13	ExT3 reading
	6'h14	ExT4 reading
	6'h15	Reserved
	6'h16	Reserved
	6'h17	GPIO1 reading
	6'h18	GPIO2 reading
	6'h19	Reference voltage

8.11 Scan Cell MUX (Address: C9H)

The Scan Cell MUX test is part of the fault diagnostics system. It tests the cell measurement input MUX and ensures that the cell inputs are correctly routed to the appropriate register. It does this by momentarily loading odd VCn inputs with a 200µA current and performing an A/D conversion before and after the load. The difference between the readings indicates a pass or fail operation. *Note:* To exclude cells from this test, set the corresponding bit in the Cell Setup register.

For this command to operate properly, there are limitations:

- The time constant of external components relative to internal timing of the operation requires a minimum series resistance between the battery connection and the RAA489204 cell input of 120Ω. Because of this limitation, the use of Scan MUX may not be useful for internal balance configurations. The same function can be achieved in software by the MCU performing the ADC operations and using Manual Balance commands.
- The maximum differential capacitance across adjacent cell inputs is also limited to be less than 220nF (±20%).

When operating with reduced cell counts, the lowest VCn input that is shorted with higher VCn inputs should be an even number (for example, VC4, VC6) See Table 5.

For timing of internal operations relative to the command, see Figure 66 and Figure 67. For internal timing details, see Table 48.

8.12 Balance Enable (Address: CAH)

When all of the other balance control bits are properly set, sending the Balance Enable command starts the balance operation by setting the BEN bit in the Balance Setup register. This command does not affect other balance settings; however, it can be a quick way to start a balance operation suspended before a voltage scan.

8.13 Balance Inhibit (Address: CBH)

The Balance Inhibit command stops the balance operation by clearing the BEN bit in the Balance Setup register. It affects no other balance setting, so it is a quick way to stop balancing before a cell voltage scan.

8.14 Roll Call (Address: D0H)

This command initializes the Daisy Chain stack devices. The Roll Call command may be sent at any time and is a required operation following initial power-up, after an SReset or HReset command, or after toggling the EN pin.

8.14.1 Roll Call Operation

Roll Call begins with the host sending a 5-byte Roll Call command using any device address. Devices in the stack self-identify with the top device sending a 5-byte Roll Call response. The response replaces the device address in the command with the address of the top device (indicating the total number of devices in the stack) and increments the Frame count. A new CRC value reflects the changes in the first 3 bytes.

For example, the command/response for a stack of ten devices is:

Send: 80 D0 00 E2 E1
Receive: A8 D0 01 DD A7

Devices exit Roll Call mode immediately if any communications are received on the lower port (or SPI port in the case of the Master device).

The Roll Call command is valid when sent with any device address (including the Address All address). An invalid CRC negates the Roll Call command. Devices do nothing if an incorrect CRC is received.

Following the Roll Call process, the Top device is identified by the matching values of the Address and Stack Size fields in the COMMS Setup register.

8.14.2 Roll Call Error Handling

During the Roll Call process, the Roll Call command is sent from the MCU and relayed to the Top device. If any devices get a CRC error, they do not complete the Roll Call process and effectively ignore the command. This means that a device that gets the correct information, and does not get a response from the device above, identifies itself as the Top device. The Master device responds with a NAK if there is a CRC error. This allows the host to know there was a problem.

During the Roll Call process, after relaying the Roll Call command from the MCU, all devices except the Master device send back eight clocks to the device below (Roll Call acknowledge). If a Mid stack or Master device receives fewer than eight clocks, this is an incorrect response and is ignored by the receiving device. In this case the receiving device would not get a correct response from above and would respond as if it were the Top device.

While relaying the response message from the Top device to the MCU, if there is a frame or CRC error condition, the message is passed to the host MCU as normal. It is then up to the host to resend the command or to take other action as appropriate.

If the wrong number of stack devices are reported at the end of the Roll Call command it is expected that the host microcontroller knows how many devices should be present. It is up to the host microcontroller to identify a problem in this event.

Another way to determine that Roll Call has completed successfully is to read a register or send an ACK to each device in the stack. A missing address would respond with an ACK response from the Top device, not the target device.

8.15 NAK (Address: D1H)

Devices send a NAK response when receiving a command that cannot be properly executed. Examples of commands that can be executed are commands that access non-existent register locations or commands that have an incorrect CRC value.

8.16 ACK (Address: D2H)

ACK is sent by the Top Daisy Chain device during normal communications or by any device in response to a register Write. ACK is normally used by the host as a No Operation command to check the integrity of the Daisy Chain communications. A stack device returns an ACK response when sent an ACK command. If there is a problem with Daisy Chain communications, the response is a NAK with information about where the problem occurred (device position within the stack).

8.17 COMMS Failure (Address: D3H)

COMMS Failure is part of the communications integrity checking. For all communications that require a response (see Table 26), each device in the stack waits for the response from the device above. If this response is not received within a timeout period, the device transmits the COMMS Failure response on its lower Daisy Chain port, or on the SPI port if the reporting device is the Master device. The COMMS Failure response typically indicates a break in the Daisy Chain or the failure of a component. See Communication Failure.

8.18 Sleep (Address: D4H)

The Sleep command puts the devices that receive the command into Sleep mode. For detailed operation about this command, see Sleep Mode.

8.19 Wakeup (Address: D5H)

The Wakeup command is sent by the host to wake up devices in the stack that are in the Sleep mode. Precede this command by the HReset_Wakeup Precursor command. When it receives the Wakeup command, the Master sends the Wakeup signal on the Daisy Chain to all devices. Wakeup is a 4kHz signal.

For more information about the operation of the Wakeup command, see Wakeup.

8.20 SReset (Address: D6H)

The SReset command is a soft reset that is completely controlled through the Daisy Chain. SReset is a command issued by the host using Address All addressing. Each device, on receiving the command, resets all registers to the factory programmed configuration, stops all scan and balancing operations and waits for the packet timeout to expire, then resets itself. The SReset command does not power down circuits in the device as does the HReset command. See HReset (Address: DFH).

A Roll Call command is required following this command.

8.21 Calculate Register Checksum (Address: D7H)

This command calculates the checksum of the Page 2 registers and stores this internally. This covers all the control registers for the device. This command should be issued whenever a register is changed by the Host microcontroller.

8.22 Check Register Checksum (Address: D8H)

This command calculates the checksum of the Page 2 registers and compares it to the previously calculated and stored value. This command can be issued periodically to determine if a register has been changed without direct control by the host microcontroller.

8.23 Override Clear on Write (Address: DAH)

When a fault occurs in a register, a write of all 1s clears the bits. If, however, it is required to set a particular bit (except OV, UV, OT, OW, PAR, BUFF_ERR), or to clear only some of the bits, the Override Clear on Write command tells the RAA489204 that the next Write operation should replace the register contents with the new data, instead of setting all the bits to zero.

8.24 HReset_Wakeup Precursor (Address: DEH)

The HReset_Wakeup Precursor command is required to be sent before either a Wakeup or HReset command. HReset_Wakeup Precursor is sent to the Master device (Device Address 6'b00001) and causes the Master device to trap the next command and not pass this onto the Daisy Chain. Both Wakeup and HReset use special signaling which is generated by the Master device. The Master responds to the host with an ACK after receiving the HReset_Wakeup Precursor command. If this command is sent to any device address other than the Master, the Master returns a NAK to the Host.

If the command following the HReset_Wakeup Precursor is anything other than Wakeup or HReset, the Master responds NAK to the host and does not send anything on the Daisy Chain.

8.25 HReset (Address: DFH)

The HReset command is a hard reset. The command toggles the EN logic internally in each device in the Daisy Chain stack. The command itself propagates through the Daisy Chain, but the effect is the same as toggling the EN pin. The command is issued by the host using Address All and is preceded by the HReset_Wakeup Precursor command. Using any address other than the Master returns a NAK.

When the Master receives the HReset command from the host, it sends the HReset signal on the Daisy Chain to all devices (HReset is a 32kHz signal.) Each device performs a hardware reset after receiving the signal.

A Roll Call command is required following this command.

8.26 Command Feature Summary

Table 26. Command Feature Summary

Command	Device Response		Address All Compatible	Increments Measurement Scan Counter?	Increments Diagnostic Scan Counter?
	Top	Target			
Read	ACK	Data	No	No	No
Write	ACK	ACK	No	No	No
NAK	ACK	ACK	No	No	No
ACK	ACK	ACK	No	No	No
Comms Failure (Response, not a command)	NAK	NAK	N/A	No	No
Calculate Register Checksum	ACK	ACK	Yes	No	No
Check Register Checksum	ACK	ACK	Yes	No	No
Balance Enable	ACK	ACK	Yes	No	No
Balance Inhibit	ACK	ACK	Yes	No	No
Roll Call	Roll Call	No Response	Yes	No	No
Override Clear on Write	ACK	ACK	Yes	No	No
HReset_Wakeup Precursor	[1]		Master address only	No	No
Wakeup	ACK	[2]	Address All Only	No	No
Sleep	ACK		Address All Only	No	No
HReset	No Response		Address All Only	No	No
SReset	No Response	No Response	Yes	No	No
Scan Continuous	No Response	No Response	Yes	No	No
Scan Inhibit	No Response	No Response	Yes	No	No
Scan Voltages	No Response	No Response	Yes	Yes	No
Scan Mixed	No Response	No Response	Yes	Yes	No
Scan Wires	No Response	No Response	Yes	Yes	No
Scan All	No Response	No Response	Yes	Yes	No
Scan Temperatures	No Response	No Response	Yes	Yes	Yes
Measure	No Response	No Response	Yes	Yes	No
Scan Cell MUX	No Response	No Response	Yes	No	Yes

1. The Master responds ACK if awake and has no response if asleep. The Master responds NAK and does not process a following Wakeup or HReset if the device addresses have not been assigned by Roll Call. If any device address except the Master is used, there is no response.
2. With Address All, there is no Target, so no Target Response, only a response from the TOP. If a target address is used, the response is NAK.

9. Cell Balance Control

The RAA489204 requires the following conditions set to properly balance:

- Set IBAL = 0 for External balancing. Set IBAL = 1 for Internal balancing.
- The BDDS bit setting of '1' indicates that balancing is turned off during the cell voltage scan in the Scan Continuous operation in any of the Balance modes.
- The BEN bit is set either directly, by using a register Write, or by using the Balance Enable command.
- The BMD[1:0] bits set the manual, timed, or auto balance mode of operation, see Table 27 and Table 28.

Table 27. Balance Setup Register Default Values

8	7	6	5	4	3	2	1	0
IBAL	EOB	BDDS	BEN	BWT2	BWT1	BWT0	BMD1	BMD0
0	0	0	0	0	0	0	0	0

Table 28. Balance Mode Control Bits

BMD[1:0]	Balance Mode
00	Off
01	Manual
10	Timed
11	Auto

- The balance wait time (see Table 27) sets the time between balance cycles in Auto Balance settings. Its use is primarily to provide thermal management of the balance FETs.
- Balance Wait Time = $2^{(n-1)}$; where n = $BWT[2:0]_{10}$
- The Balance Status Registers (see Table 29) set the pattern of cells to be balanced. Manual balance and timed balance use only the Balance Status 1 Register to specify the cells to be balanced. In Auto Balance mode, the designer can specify which cells are balanced in each auto balance cycle by specifying up to 14 different patterns, one pattern in each of the 14-cell Balance registers. This can prevent adjacent cells from balancing and can help in the thermal management of the balance FETs.

Table 29. Balance Status Registers

Balance Status Register	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	B1C14	B1C13	B1C12	B1C11	B1C10	B1C8	B1C8	B1C7	B1C6	B1C5	B1C4	B1C3	B1C2	B1C1
2	B2C14	B2C13	B2C12	B2C11	B2C10	B2C8	B2C8	B2C7	B2C6	B2C5	B2C4	B2C3	B2C2	B2C1
3	B3C14	B3C13	B3C12	B3C11	B3C10	B3C8	B3C8	B3C7	B3C6	B3C5	B3C4	B3C3	B3C2	B3C1
4	B4C14	B4C13	B4C12	B4C11	B4C10	B4C8	B4C8	B4C7	B4C6	B4C5	B4C4	B4C3	B4C2	B4C1
5	B5C14	B5C13	B5C12	B5C11	B5C10	B5C8	B5C8	B5C7	B5C6	B5C5	B5C4	B5C3	B5C2	B5C1
6	B6C14	B6C13	B6C12	B6C11	B6C10	B6C8	B6C8	B6C7	B6C6	B6C5	B6C4	B6C3	B6C2	B6C1
7	B7C14	B7C13	B7C12	B7C11	B7C10	B7C8	B7C8	B7C7	B7C6	B7C5	B7C4	B7C3	B7C2	B7C1
8	B8C14	B8C13	B8C12	B8C11	B8C10	B8C8	B8C8	B8C7	B8C6	B8C5	B8C4	B8C3	B8C2	B8C1
9	B9C14	B9C13	B9C12	B9C11	B9C10	B9C8	B9C8	B9C7	B9C6	B9C5	B9C4	B9C3	B9C2	B9C1
10	B10C14	B10C13	B10C12	B10C11	B10C10	B10C8	B10C8	B10C7	B10C6	B10C5	B10C4	B10C3	B10C2	B10C1

Table 29. Balance Status Registers (Cont.)

Balance Status Register	13	12	11	10	9	8	7	6	5	4	3	2	1	0
11	B11C14	B11C13	B11C12	B11C11	B11C10	B11C8	B11C8	B11C7	B11C6	B11C5	B11C4	B11C3	B11C2	B11C1
12	B12C14	B12C13	B12C12	B12C11	B12C10	B12C8	B12C8	B12C7	B12C6	B12C5	B12C4	B12C3	B12C2	B12C1
13	B13C14	B13C13	B13C12	B13C11	B13C10	B13C8	B13C8	B13C7	B13C6	B13C5	B13C4	B13C3	B13C2	B13C1
14	B14C14	B14C13	B14C12	B14C11	B14C10	B14C8	B14C8	B14C7	B14C6	B14C5	B14C4	B14C3	B14C2	B14C1
Default Values	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 30. Watchdog/Balance Time Register

14	13	12	11	10	9	8
BTM6	BTM5	BTM4	BTM3	BTM2	BTM1	BTM0
0	0	0	0	0	0	0

- Set the balance time out (See Table 30). This sets the duration of the balance operation and is used only for the timed and auto balance options. The balance on time is programmable in 20s intervals from 20s (0000001) to 42.33min (1111111) using bits BTM[6:0].

In Auto Balance mode, this time along with the balance wait time determines the length of an auto balance cycle. The following conditions only apply to the Auto Balance mode.

- Set the Balance Value Registers. The auto balance operation uses these values to determine the amount of charge to be removed from each cell. In practice, these settings determine the number of auto balance cycles that a particular cell is balanced. See Cell Balance Registers.

9.1 Manual Balance Mode

To manually control the cells to be balanced, the host sets the Balance Status 1 Register to indicate the specific cells to balance and then sets the BEN bit, typically by sending a balance enable command.

The selected cells then balance until the operation is stopped by the host (by sending a Balance Inhibit) or by a Watchdog Timer time out.

CAUTION 1: In Manual Balance mode, it is necessary to disable, then re-enable balancing when changing from one set of cells being balanced to another set. Balancing can be disabled before changing the Balance Status bits or after, but correct cell balance pin output requires this disable/enable sequence.

CAUTION 2: Manual balancing does not stop when the Sleep command is sent to the RAA489204. If the Sleep command is received while the device is manual balancing, the communications ports act as if the device is in sleep, but balancing continues. Therefore, while in Manual Balance mode, when the Sleep command has been sent, the host needs to send HReset_Wakeup Precursor and Wakeup commands before any other communication to the device. An option is to send a Scan Continuous command before sending the Sleep command. In this case, if the scan continuous detects a fault condition, such as cell undervoltage, balancing stops, a fault flag is set, and the device enters the Sleep mode.

During a Scan Continuous operation, setting the BDDS bit in the Balance Setup register forces the RAA489204 to turn off cell balancing 10ms before its cell voltage scan and resumes balancing when the cell scan completes. If BDDS is not set, then balance outputs remain on during cell scan measurements. This can result in false voltage detection errors. In the case of the standard battery connection configuration shown in Figure 33, set BDDS in

Scan Continuous mode, because cell voltage readings are always zero when the balance output turns on, always resulting in an overvoltage or undervoltage condition.

If the watchdog timer times out while the device is manually balancing (whether or not the Sleep command has been sent), then balancing stops immediately and the device goes into Sleep mode.

The watchdog timer function protects the battery from excess discharge due to balancing in the event that communications is lost after manual balance has started.

9.1.1 Manual Balance Example

9.1.1.1 Activate Balancing on Cells 1, 5, 7, and 11

In this example, the Balance Setup and Balance Status Registers are set up to select the cells that are to be balanced. Then, the manual Balance Mode is set, along with the balance enable bit. It is not necessary to send a balance enable command.

1. Write the Balance Status 1 register:
   Set bits 0, 4, 6 and 10 (for cells 1, 5, 7, and 11)
   B1C14:1 = 0000 0100 0101 0001 (No*te:* See BnC14:BnC1 bits in Registers)

Table 31. Balance Status 1 Register Write Command

	1+Device Addr+ R/W	Page + Address	Length + Frame	CRC	Data	CRC
Generic	1 ddddd 10	1011 0000	00 0100 00	16'hcc	0000 0100 0101 0001	32'hcccc
Device 1	86	B0	10	495A	0451	9B1F

ddddd = Device Daisy Chain address
c = calculated CRC byte

2. Write the Balance Setup register:
   Set Manual Balance mode and turn on balance.
   EOB = X
   BDDS = X
   BEN = 1 (Balancing enabled)
   BWT = XXX
   BMD = 01 (Manual Balance mode)

Table 32. Balance Setup Register Write Command

	1 + Device Addr + R/W	Page + Address	Length + Frame	CRC	Data	CRC
Generic	1 ddddd 10	1001 0000	00 0100 01	16'hcc	XXXX XXXX XX1X XX01	32'hcccc
Device 1	86	90	11	5F9D	0021	294C

ddddd = Device Daisy Chain address
c = Calculated CRC byte
X = Do not care (typically write 0's)

The balance FETs attached to Cells 1, 5, 7, and 11 turn on.

Turn balancing off by resetting the BEN bit or by sending the Balance Inhibit command.

9.2 Timed Balance Mode

To control a timed balance operation, the host sets the Balance Status Register 1 location to indicate the specific cells to balance, sets the Balance Timeout bits for the Required balance duration (see Table 33), and then sets the BEN bit, typically by sending a balance enable command.

The selected cells then balance until the timer expires or the operation is stopped by the host (by sending a Balance Inhibit or Sleep command) or by a watchdog time out.

The balance on time is programmable in 20s intervals from 20s to 42.5min.

Table 33. Balance Timeout Settings

BTM[6:0]	Minutes
0000000	Disabled
0000001	0.33
0000010	0.67
0000011	1.00
-	-
1111101	41.67
1111110	42.00
1111111	42.33

Sending the Balance Inhibit command stops the balancing functions and resets the timer values. Sending a new Balance Enable command resumes balancing, but with the full time initially set by the balance time bits.

When the balance timeout period is met, the End Of Balance (EOB) bit in the Device Setup register is set and BEN bit is reset.

The RAA489204 Sleep on balance termination function allows a device that is in Timed Balance mode to automatically enter Sleep mode when the balancing activity has completed. This function is activated by first enabling the Timed Balance function and then sending the Sleep command. Balancing continues in the Timed Balance mode following a Sleep command until the balance time ends. Then the device enters the Sleep mode. When the Sleep command has been sent, the host needs to send HReset_Wakeup Precursor and Wakeup commands before any other communication to the device.

CAUTION: When the RAA489204 is performing a Timed Balance operation following a Sleep command, the device does not monitor fault conditions. So, before sending the Sleep command, the host should periodically wake the device (by sending the HReset_Wakeup Precursor and Wakeup commands) and perform a Scan All operation or the host can send a Scan Continuous command before sending the Sleep command. The Scan Continuous operation then performs fault checking.

During a Scan Continuous operation, setting the BDDS bit in the Balance Setup register forces the RAA489204 to turn off cell balancing 10ms before its cell voltage scan and resumes balancing when the cell scan completes. If BDDS is not set, then balance outputs remain on during cell scan measurements. This can result in false voltage detection errors. In the case of the standard battery connection configuration shown in Figure 33, set BDDS in Scan Continuous mode, otherwise cell voltage readings are always zero when the balance output turns on, always resulting in an overvoltage or undervoltage condition.

If the watchdog timer times out when the device is timed balancing (whether or not the Sleep command has been sent), then balancing stops immediately and the device enters the Sleep mode.

The watchdog timer function protects the battery from excess discharge because of balancing if communication is lost after Timed Balance has started.

9.2.1 Timed Balance Example

9.2.1.1 Activate Balancing on Cells 2 and 8 for 1 Minute

In this example, the Balance Status 1 register is first set up to select the cells to be balanced. Then, the Balance Time is set. Finally, the Timed Balance mode is set, along with the Balance Enable bit. It is not necessary to send a Balance Enable Command when writing the registers in this sequence.

1. Write the Balance Status register:
   Set Bits 1 and 7 (for cells 2 and 8)
   B1C14:1 = 0000 0000 1000 0010 (*Note:* See BnC14:BnC1 in Registers)

Table 34. Balance Status 1 Register Write Command

	1 + Device Addr + R/W	Page + Address	Length + Frame	CRC	Data	CRC
Generic	1 ddddd 10	1011 0000	00 0100 00	16'hcc	0000 0000 1000 0010	16'hcc
Device 1	86	B0	10	495A	0082	AC C5

ddddd = Device Daisy Chain address
c = Calculated CRC byte

2. Write to the Balance Setup register and the Watchdog/Balance Register. Because these are adjacent in the memory address, data can be sent in a single Write command:

   Set Timed Balance mode, turn off balance, and load the timer.
   EOB = X
   BDDS = X
   BEN = 0 (balancing disabled)
   BWT = XXX
   BMD = 10 (Timed Balance mode)

   Load Timer value:
   BTM6:1 = 000 0011.

Table 35. Balance Setup Register Write Command

	1 + Device Addr + R/W	Page + Address	Length + Frame	CRC	Data	CRC
Generic	1 ddddd 10	1001 0000	00 1000 00	16'hcc	XXXX XXXX XX0X XX10 X000 0011 wwww wwww	32'hcccc
Device 1	86	90	20	79EF	0002 033F	5A23 0B8B

ddddd = Device Daisy Chain address
c = Calculated CRC byte
wwww wwww = Watchdog timer setting (Default = 8'h3F)
X = don't care (typically write 0's)

3. Start Balancing by sending the Balance Enable command:

Table 36. Balance Enable Command

	1 + Device Addr + R/W	Page + Address	Length + Frame	CRC
Generic	1 ddddd 00	1100 1010	00 0000 00	16'hcc
Device 1	84	CA	00	D299

ddddd = Device Daisy Chain address
c = Calculated CRC byte

The balance FETs attached to cells 2 and 8 turn on. The FETs turn off after 1 minute. Balancing can be stopped by resetting BEN or by sending the Balance Inhibit command.

9.3 Auto Balance Mode

Auto Balance mode provides the ability to perform balancing autonomously and in an intelligent manner. The Auto Balance operation is based on removal of a specified amount of charge from each cell. The system designer determines the amount of charge to be removed from each cell, based on the calculated cell State of Charge (SOC) and the target SOC.

At the end of each auto balance scan, the cell voltages are checked to calculate the amount of charge removed and to determine if there is an overvoltage or undervoltage condition. Auto balancing proceeds independently from the Host until the programmed amount of charge has been removed from each cell or the balance operation is terminated by the Host. A voltage fault condition halts the auto balance operation.

The RAA489204 Sleep on Balance Termination function allows a device that is in Auto Balance mode to automatically enter Sleep mode when the balancing activity has completed. This function is activated by first enabling the Auto Balance function and then sending the Sleep command. During the Auto Balance operation, the Sleep on Balance Termination function also reduces power consumption by turning off the regulators and entering the Sleep mode during the balance wait time. When the Sleep command has been sent, the host needs to send HReset_Wakeup Precursor and Wakeup commands before any other communication to the device. In Auto Balance mode the RAA489204 performs a scan operation at the end of each cycle. The scan operation detects fault conditions, so it is not necessary for the host to monitor faults in Auto Balance following transmission of a Sleep command.

If at any time the watchdog timer expires, the balance operation terminates, the WDTM bit is set, and the device enters Sleep mode.

Thermal issues are accommodated by the provision of the Balance Status registers and a balance wait time. Cells are balanced with periodic measurements being performed at a time interval determined by the sum of the Balance Timeout Value (this is the same register as for Timed Balance - see Table 33) and the Balance Wait time value (see Table 37).

Table 37. Balance Wait Time Control Bits

BWT[2:0]	Seconds
000	0
001	1
010	2
011	4
100	8
101	16
110	32
111	64

These periodic measurements calculate the reduction in State of Charge (Delta SOC) for each cell with each balancing cycle and terminate balancing of a particular cell when the total change removal target has been reached.

In Auto Balance mode, the RAA489204 controls the cell balance outputs based on bits set in the Balance Status registers. The operation begins with the value set in Balance Status Register 1 controlling the balance outputs. For the second Auto Balance cycle, the operation uses the contents of Balance Status Register 2. The third auto balance cycle uses the contents of Balance Status Register 3, and so on until a Balance Status Register contains a value of zero. In this case, the operation wraps back to Balance Status Register 1 and the pattern repeats.

If Scan Continuous operation is also selected during Auto Balance, set the BDDS to have the RAA489204 turn off cell balancing 10ms before the cell voltage scan and resume balancing when the cell scan completes. If BDDS is not set, then balance outputs remain on during cell scan measurements. This can result in false voltage detection errors. In the case of the standard battery connection configuration shown in Figure 33, set BDDS in Auto Balance mode and Scan Continuous mode, because cell voltage readings are always zero when the balance output turns on, always resulting in an overvoltage or undervoltage condition.

The next step in setting up an Auto Balance operation is to program the Balance value for each cell. The balance value (delta SOC) is the difference between the present charge in a cell and the Required charge for that cell.

The method for calculating the state of charge for a cell is left to the system designer. Typically, determining the state of charge is dependent on the chosen cell type and manufacturer, on the cell voltage, charge and discharge rates, temperature, age of the cell, number of cycles and other factors. Tables for determining SOC are often available from the battery cell manufacturer.

When the amount of charge to be removed is known, all that is needed is the total resistance of the balancing circuit, which is normally the sum of the balance resistor value and the balancing FET on resistance, $r_{DS(ON)}$, and the time for which balancing is enabled for each cycle, the Balance Time. These figures are then used to calculate a Balance Value, B, that is used by the RAA489204 to control the balancing process. The derivation of Balance Value is shown in the following.

Figure 63 shows a simple circuit with cell and balancing components.

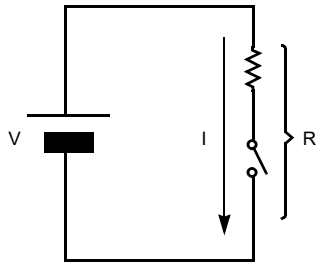


Figure 63. Simplified Cell Balance Circuit

In Figure 63 cell voltage is given by V, balance circuit resistance by R and balance current by I. The relationship of these terms is then:

(EQ. 1) $$I = \frac{V}{R}$$

The total amount of charge, Q, removed during balancing for a period of t seconds is then given by:

(EQ. 2) $$Q = I \times t = \frac{V}{R} \times t$$

When using Auto Balance mode the RAA489204 balances using fixed Balance Time periods, such that a number of these periods are required to balance for the full time, t, given in Equation 2. Using T to represent Balance Time and n to represent number of periods, Equation 2 can be rewritten as Equation 3:

(EQ. 3) $$Q = \frac{V}{R} \times T \times n$$

In Equation 3, the values of Q, R, and T are known. Only V and n are unknown. Equation 3 can be rearranged in terms of the unknown values as follows:

(EQ. 4) $$V \times n = \frac{(Q \times R)}{T}$$

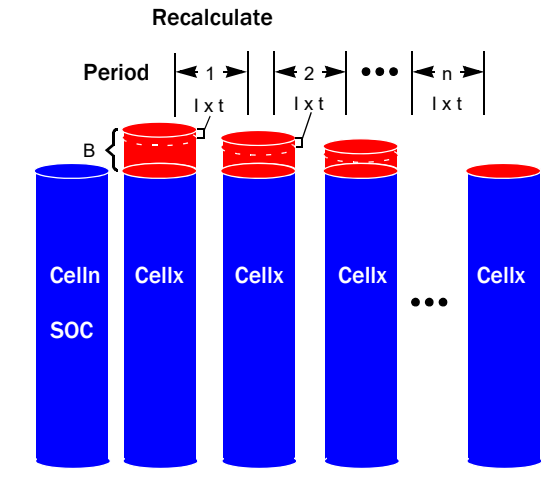
Equation 4 shows that applying balancing to a cell with voltage V for a total of n cycles completes balancing with the required amount of charge, Q, removed from the cell. The RAA489204 uses the expression V x n as the balance value and deducts the cell voltage V at the end of each balance time. In this manner, the RAA489204 applies n balancing cycles to the cell before completing the auto balance routine.

There is a slight modification required to Equation 4 when using this with the RAA489204. The RAA489204 uses the ADC conversion value of cell voltage, so we must scale the expression of Equation 4 accordingly. The scaling factor applied is 32768/5, so Equation 4 becomes Equation 5:

(EQ. 5) $$V(ADC) \times n = \frac{(Q \times R)}{T} \times \frac{32768}{5} - 1 = BalanceValue$$

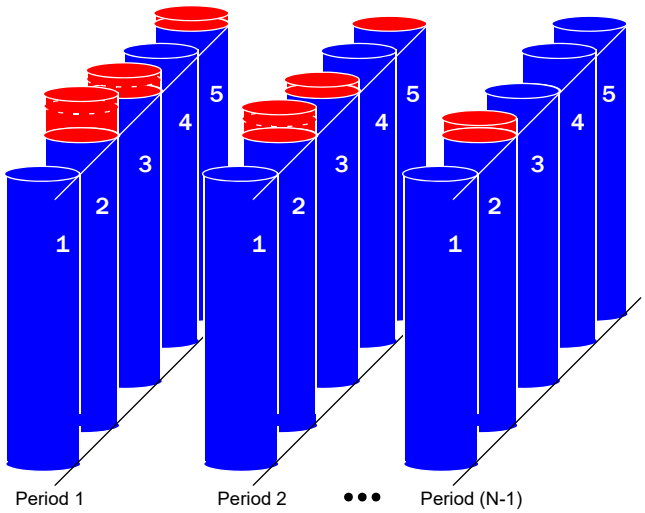
The Balance Value is calculated for each cell to be balanced. The upper 16 bits are saved to the Balance Value registers.

The RAA489204 then balances each cell, subtracting the measured cell voltage from the balance value at the end of each balance time interval, completing at the end of the cycle in which the balance value is zero, see Figure 64 and Figure 65.



- Determine amount of excess capacity in CELLx than in CELLn
- Remove part of the excess capacity in each cycle
- Continue until the excess capacity is removed

Figure 64. Illustration of Auto Balance



- Each period capacity is removed from cells
- When all capacity removed from a cell, balance for that cell ends
- Balance continues on remaining cells until excess capacity is removed from all cells.

Figure 65. Illustration of Auto Balance (Multiple Cells)

The RAA489204 has fourteen 16-bit Balance Value registers, with one register provided for each cell.

At the end of each balance cycle on-time interval, the RAA489204 performs a Scan All operation to measure the voltage on each of the cells that were balanced during that interval. The measured values are then subtracted from the balance values for those cells. This process continues until the balance value for each cell is zero, at which time the auto balancing process is complete. When Auto Balancing completes, the End Of Balance (EOB) bit in the Device Setup register is set and the BEN bit is reset.

When all of the cell balance FET controls, the balance values and the timers are set up, balance is enabled sending a Balance Enable command.

Sending the Balance Inhibit command stops the balancing functions but maintains the current Balance Value register contents. Auto balancing continues from Balance Status Register 1 when balance is restarted.

9.3.1 Auto Balance Value Calculation Example

This example is based on a cell State of Charge (SOC) of 9360 coulombs, a target SOC of 8890 coulombs, a balancing leg impedance of 31Ω (30Ω resistor plus 1Ω FET on resistance) and a sampling time interval of 5 minutes (300 seconds).

The Balance Value is calculated using Equation 6.

(EQ. 6) $$B = \frac{8191}{5 \times 256} \times (9360 - 8890) \times \frac{31}{300} = 311 = 16'h137$$

The value 8191/5 is the scaling factor of the cell voltage measurement. The division by 256 compensates for the Balance Value register being the upper 16 bits of an internal 24-bit balance register.

The value of 16’h0137 is loaded to the required Cell Balance Register and the value 7’b0001111 (5 minutes) is loaded to the Balance Time bits in the Watchdog/Balance Time register.

In this example, the total coulomb difference to be balanced is: 470 coulomb (9360 - 8890). At 3.3V/31Ω * 300s = 31.9 coulomb per cycle, it takes about 15 cycles for the balancing to terminate.

9.3.2 Auto Balance Mode Cell Balancing Example

The following describes a simple setup to demonstrate the Auto Balance mode cell balancing function of the RAA489204. *Note:* This balancing setup is not related to the balance value calculation in Equation 6.

Auto balance cells using the following criteria:

- Balance time = 1 minute (see Table 33).
- Balance wait time (dead time between balancing cycles) = 8s.
- Balancing disabled during cell measurements.
- Balance values as shown in Table 38.
- Use the Balance pattern shown in Table 39.

Program the RAA489204 using the following three steps.

1. Write Balance Values plus Balance Status registers:

Because the Cell Balance Values and Balance Status values are in sequential memory addresses, data can be sent in a single Write command, starting with the Balance Value Registers. See Table 38.

Table 38. Cell Balance Values (Hex) for Each Cell

Register	Cell Balanced	Balance Value
Balance Value Register 1	Cell 1	16'h0040
Balance Value Register 2	Cell 2	16'h003E
Balance Value Register 3	Cell 3	16'h0000
Balance Value Register 4	Cell 4	16'h0029
Balance Value Register 5	Cell 5	16'h003E
Balance Value Register 6	Cell 6	16'h0000
Balance Value Register 7	Cell 7	16'h0029
Balance Value Register 8	Cell 8	16'h0137
Balance Value Register 9	Cell 9	16'h0000
Balance Value Register 10	Cell 10	16'h001E
Balance Value Register 11	Cell 11	16'h085
Balance Value Register 12	Cell 12	16'h000A
Balance Value Register 13	Cell 13	16'h0005
Balance Value Register 14	Cell 14	16'h009F

Table 39. Cell Balance Status (Hex) for Each Cell

Register	Balance Status Value	Cells Balanced
Balance Status Register 1 BnC14:BnC1; n = 1	0001 0010 0100 1001 1249	13, 10, 7, 4, 1
Balance Status Register 2 BnC14:BnC1; n = 2	0010 0100 1001 0010 2492	14, 11, 8, 5, 2
Balance Status Register 3 BnC14:BnC1; n = 3	0000 1001 0010 0100 0924	12, 9, 6, 3
Balance Status Register 4 BnC14:BnC1; n = 4	0000 0000 0000 0000 0000	None
Balance Status Register 5 through Balance Status Register 14	N/A	N/A

Table 40. Balance Status Register Write Command

	1 + Device Addr + R/W	Page + Address	Length + Frame	CRC	Data	CRC
Generic	1 ddddd 10	1010 0000	10 1000 00	16'hcc	Data	32'hcccc
Device 1	86	A0	A0	ED F2	0040 003E 0000 0029 003E 0000 0029 0137 0000 001E 085 000A 0005 009F 1249 2492 0924 0000	4A A7 5E 97

ddddd = Device Daisy Chain address c = Calculated CRC byte

2. Write to the Balance Setup register and to the Watchdog/Balance Register. Because these are adjacent in the memory space, data can be sent to both in a single Write command:
   Set Auto Balance mode, turn off balance, load timer.
   EOB = X
   BDDS = 1 (Disable balance during voltage scan)
   BEN = 0 (Balancing disabled)
   BWT = 100 (8 seconds)
   BMD = 11 (Auto Balance mode)

   Load Timer value (1 minute):
   BTM6:1 = 000 0011.

Table 41. Balance Setup Register Write Command

	1 + Device Addr + R/W	Page + Address	Length + Frame	CRC	Data	CRC
Generic	1 ddddd 10	1001 0000	00 1000 00	16'hcc	XXXX XXXX X101 0011 0000 0011 wwww wwww	32'hcccc
Device 1	86	90	20	79EF	0053 033F	305A 4EBC

ddddd = Device Daisy Chain address c = Calculated CRC byte
w = Watchdog Timer Setting bit (Default = 8'h3F) X = Don't care (typically write 0's)

3. Start Balancing by sending the Balance Enable command:

Table 42. Balance Enable Command

	1 + Device Addr + R/W	Page + Address	Length + Frame	CRC
Generic	1 ddddd 10	1101 0000	000101 00	16'hcc
Device 1	86	D0	14	02 F4

ddddd = Device Daisy Chain address cc = Calculated CRC (each c = 8 bits)

The balance FETs attached to Cells 2 and 8 turn on. The FETs turn off after 1 minute. Balancing can be stopped by resetting BEN or by sending the Balance Inhibit command.

10. Operational Timing

Three types of operations are initiated by a command.

- Read operations that begin with a command and end with a return of data in a (relatively) immediate response.
- Write operations that begin with a command, change a register value, and end with the return of an ACK in a (relatively) immediate response.
- Command operations that begin a Scan or other internal operation where there is no response.

Typically, the most critical of the timing analyses is executing measurements within the Daisy Chained devices. Because this is a type 3 operation, the complete operation for measuring and retrieving data consists of three separate parts listed as follows:

- A command to initiate a scan.
- The scan operation internal to each device.
- A command and response to retrieve the data.

At the end of the transmitted command (for the Master) or the received command (for the slaves) each device waits for the end of its packet reset timer. When this timer expires, the Scan operation begins. Each device then

begins its scan at nearly the same time (with small differences due to synchronization with the internal clock of each device).

Scan operations occur entirely within the device and end with data being placed in a register. Internal operation times are dependent on the internal clock of each RAA489204 device.

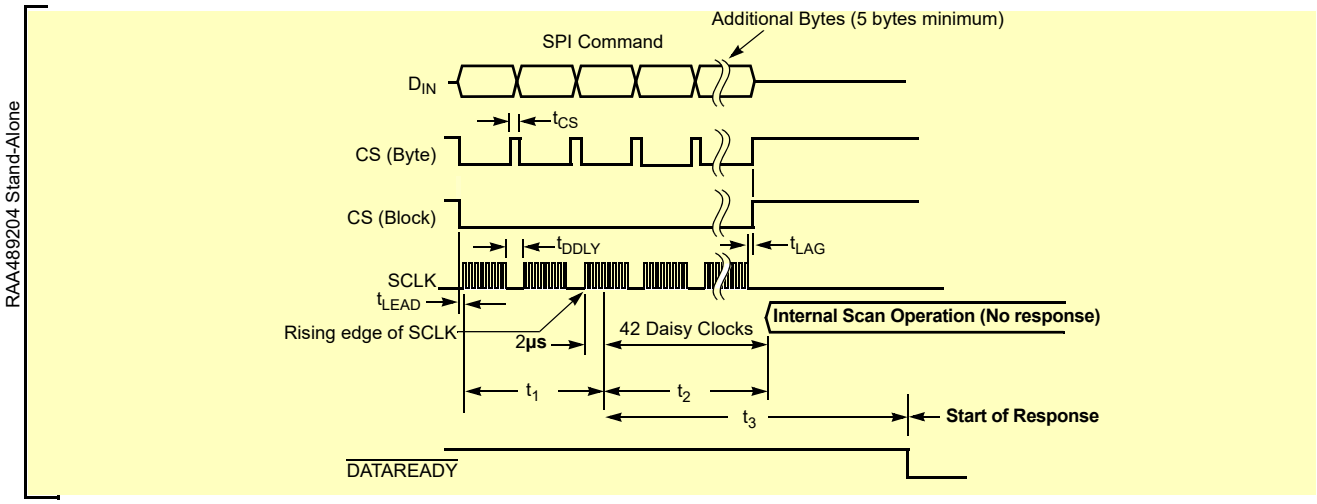
Devices that receive a command initiating a Write or Read do not immediately respond at the end of their packet reset time out. Instead, their response to the Host begins after the device receives an ACK response from the Top device.

10.1 Command Timing

The time from the start of a command to the start of an internal operation is defined by the equation for T1 in Figure 67. The internal operation begins at the same time in each device.

In the case of a command that starts a scan or measurement, the host needs to wait until the command completes, by waiting for the command to reach the last device, plus a communications wait time (see Table 54) before sending another command.

10.1.1 Command Timing Diagrams



1. Even though the Daisy Chain is not used in stand-alone operation, the Internal Scan is delayed by 42 daisy clock cycles (which includes t‘he Packet Reset). For the fastest response time, connect the COMMRATE1 and COMMRATE0 pins to V3P3 to set the daisy clock to 1MHz (1µs per clock).

$$t_1(ms) = t_{SPI} \times 16 + t_{LEAD} \times 3 + t_{LAG} \times 2 + t_{CS} \times 2 + 2\mu s$$

SPI (Byte mode)

$$t_1(ms) = t_{SPI} \times 16 + t_{LEAD} + t_{DDLY} \times 2 + 2\mu s$$

SPI (Block mode)

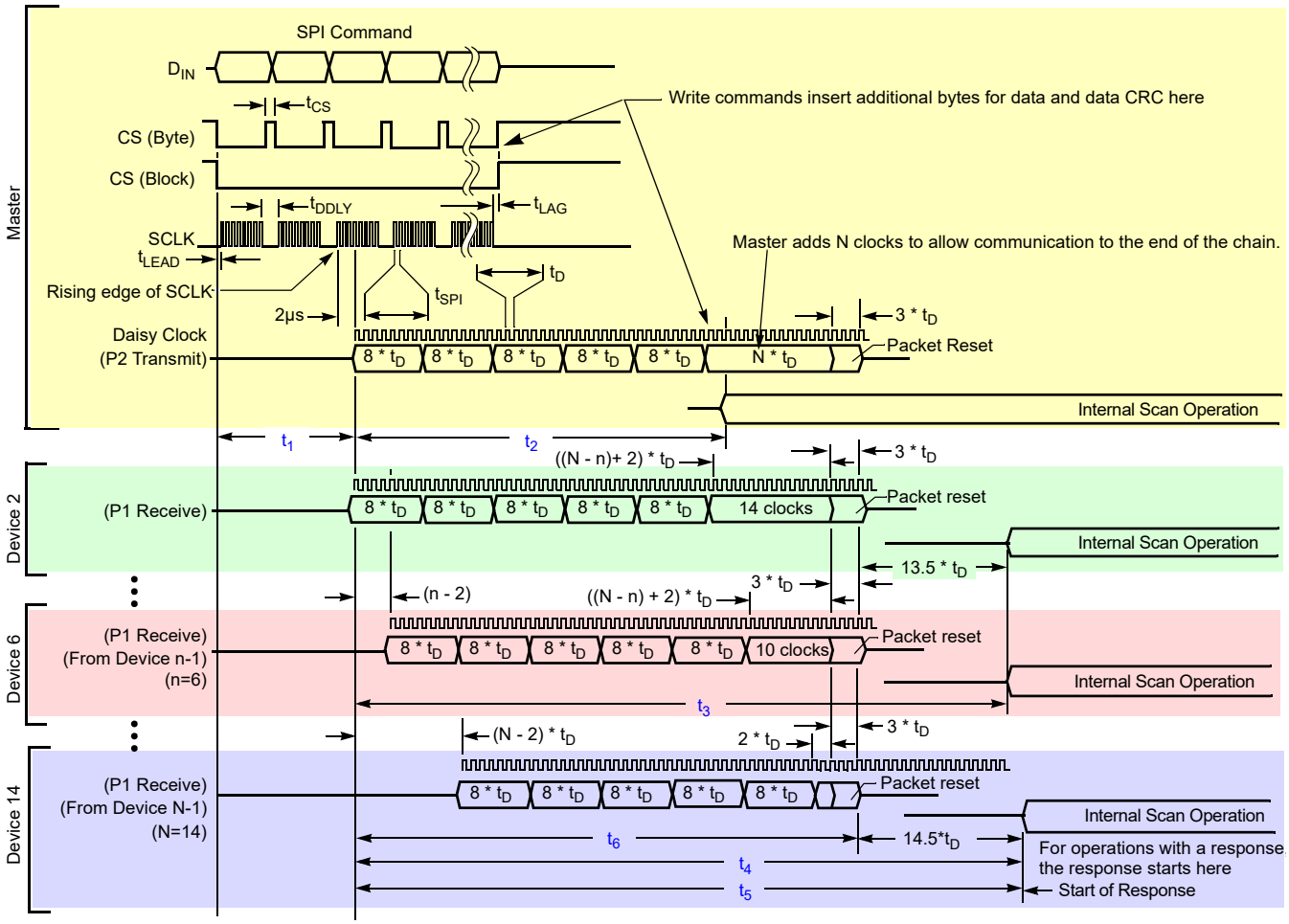
$$t_2(ms) = 42 \times t_D$$

Time to Start of Scan

Time to Start of Response

t_{SPI} = SPI clock period
t_D = Daisy Chain clock period
t_{CS} = Host CS High time (Byte mode)
t_{DDLY} = Host time between bytes (Block mode)
t_{LEAD} = $\overline{CS}$ Low to first SPI Clock
t_{LAG} = Last SPI Clock $\overline{CS}$ High
D = Number of Command Bytes
N = Stack position of Top device (N = 1 for stand alone device)

Figure 66. Command Timing (Stand-Alone Device)



$$t_1(ms) = t_{SPI} \times 16 + t_{LEAD} \times 3 + t_{LAG} \times 2 + t_{CS} \times 2 + 2\mu s$$ **SPI (Byte mode)**

$$t_1(ms) = t_{SPI} \times 16 + t_{LEAD} + t_{DDLY} \times 2 + 2\mu s$$ **SPI (Block mode)**

$$t_2(ms) = 42 \times t_D$$ **Daisy time to Start of Scan - Master**

$$t_3(ms) = (40 + N + 16.5) \times t_D$$ **Daisy time to Start of Scan - Mid**

$$t_4(ms) = (40 + N + 17.5) \times t_D$$ **Daisy time to Start of Scan - Top**

$$t_5(ms) = ((8 \times D) + N + 17.5) \times t_D$$ **Daisy time to Start of Response**

$$t_6(ms) = ((8 \times D) + N + 5) \times t_D$$ **Daisy time to end of Command**

where:

t_{SPI} = SPI clock period

t_D = Daisy Chain clock period

t_{CS} = $\overline{CS}$ High time (Byte Mode)

t_{DDLY} = Time between bytes (Block mode)

t_{LEAD} = $\overline{CS}$ Low to first SPI Clock leading edge

t_{LAG} = Last SPI Clock falling edge to $\overline{CS}$ High

t_{HIGH} = SCLK High time

n = Stack position of target device

N = Stack position of Top device

D = Number of Bytes in Command

For internal operation timing, see Table 49.

Figure 67. Command Timing (Daisy Chain)

10.2 Internal Operations

All measurement timing is derived from the RAA489204 internal oscillators. Measurements given as typical are those obtained with the oscillators operating at their nominal frequencies and with any synchronization timing also at nominal value. Maximum measurements are those obtained with the oscillators operating at their minimum frequencies and with the maximum time for any synchronization timing.

Measurement timing begins at the end of the Daisy Chain packet time out. For the Master, this is at the end of the Daisy Chain transmit. For the other devices, this is at the end of the Daisy Chain receive. See Figure 66 and Figure 67.

After receiving the Start Scan signal, the device initializes measurement circuits and performs the requested measurement(s). When the measurements are made, devices perform additional operations, such as checking for overvoltage conditions. The measurement command ends when registers are updated. At this time the registers can be read using a separate command. The processing times required to complete each measurement type are given in the Electrical Specifications table. More detailed timing breakdowns are provided in the following for each measurement type, with a summary in Table 49. The following timing information assumes no measurement averaging.

10.2.1 Scan Voltage Internal Timing

Table 43 shows the timing for each operation of the Scan Voltage command internal to the RAA489204. These times are referenced from the start of the internal operation (shown in Figure 66 and Figure 67.)

Note: If fewer cells are connected (and are masked by setting the bits in the Cell Setup Register), then the cell is skipped and the operation completes in less time. If only the bits in the Cell Fault Mask Register, are set, the ADC operation is not skipped for missing cells.

Table 43. Scan Voltage Internal Timing

Operation	Sample Time after Start of Internal Operation (µs)
Sample Cell 1	13
Sample Cell 2	40
Sample Cell 3	61
Sample Cell 4	83
Sample Cell 5	104
Sample Cell 6	125
Sample Cell 7	146
Sample Cell 8	168
Sample Cell 9	189
Sample Cell 10	210
Sample Cell 11	231
Sample Cell 12	253
Sample Cell 13	274
Sample Cell 14	295
Sample VBAT	343
Sample Internal Temperature	378
Start VBATVSS Open Check	428
End of Internal Operation	589

10.2.2 Scan Mixed Internal Timing

Table 44 shows the timing for each operation of the Scan Mixed command internal to the RAA489204. These times are referenced from the start of the internal operation (as shown in Figure 66 and Figure 67) and assume all 14 cells are enabled. If fewer cells are connected (and are masked) the cell is skipped and the operation completes in less time (see note in Scan Voltage Internal Timing.)

Table 44. Scan Mixed Internal Timing

Operation	Sample Time after Start of Internal Operation (µs)
Sample Cell 1	13
Sample Cell 2	40
Sample Cell 3	61
Sample Cell 4	83
Sample Cell 5	104
Sample Cell 6	125
Sample Cell 7	146
Sample ExT1	224
Sample Cell 8	243
Sample Cell 9	269
Sample Cell 10	291
Sample Cell 11	312
Sample Cell 12	333
Sample Cell 13	354
Sample Cell 14	376
Sample VBAT	423
Sample Internal Temperature	459
Start VBATVSS Open Check	509
End of Internal Operation	669

10.2.3 Scan All Internal Timing

Table 45 shows the timing for each operation of the Scan Voltage command internal to the RAA489204. These times are referenced from the start of the internal operation (as shown in Figure 66 and Figure 67) and assume all 14 cells are enabled. If fewer cells are connected (and are masked) the cell is skipped and the operation completes in less time (see note in Scan Voltage Internal Timing).

Table 45. Scan All Internal Timing

Operation	Sample Time after Start of Internal Operation (µs)	
	WSCN = 0	WSCN = 1
Scan Voltages		
Sample Cell 1	13	13
Sample Cell 2	40	40
Sample Cell 3	61	61
Sample Cell 4	83	83

Table 45. Scan All Internal Timing (Cont.)

Operation	Sample Time after Start of Internal Operation (µs)	
	WSCN = 0	WSCN = 1
Sample Cell 5	104	104
Sample Cell 6	125	125
Sample Cell 7	146	146
Sample Cell 8	168	168
Sample Cell 9	189	189
Sample Cell 10	210	210
Sample Cell 11	231	231
Sample Cell 12	253	253
Sample Cell 13	274	274
Sample Cell 14	295	295
Sample VBAT	343	343
Open Wires Test		
Start of Voltage Samples	423	423
Start Open Wire Disrupt	754	754
End of Open Wire Current (1.5ms or 5.0ms)	2254	5754
Start of Voltage Samples	2299	5799
Start Open Wire Logic check	2597	6097
Temperature Test		
Sample Internal Temperature MUXs	3691	7191
Sample VBAT	4094	7594
Sample Second Reference	4129	7629
Sample Internal Temperature	4234	7734
Sample ExT1	4284	7784
Sample ExT2	4320	7820
Sample ExT3	4355	7855
Sample ExT4	4390	7890
Sample GPIO1	4425	7925
Sample GPIO2	4461	7961
End of Internal Operation	4496	7996

10.2.4 Scan Temperature Internal Timing

Table 46 shows the timing for each operation of the Scan Temperature command internal to the RAA489204. These times are referenced from the start of the internal operation (as shown in Figure 66 and Figure 67) and assume all sources are enabled. If some of the sources are masked the measurement is skipped and the operation completes in less time.

Table 46. Scan Temperature Internal Timing

Operation	Sample Time after Start of Internal Operation (µs)
Sample VBAT MUX	2500
Sample BGREF MUX	2535
Sample INT TEMP MUX	2641
Sample ExT1 MUX	2691
Sample ExT2 MUX	2726
Sample ExT3 MUX	2761
Sample ExT4 MUX	2797
Sample GPIO1 MUX	2902
Sample GPIO2 MUX	2938
Sample VBAT	2973
Sample 2nd Reference	3008
Sample INT TEMP	3113
Sample ExT1	3164
Sample ExT2	3199
Sample ExT3	3234
Sample ExT4	3269
Sample GPIO1	3375
Sample GPIO2	3410
End of Internal Operation	3446

10.2.5 Scan Wires Internal Timing

Table 47 shows the timing for each operation of the Scan Voltage command internal to the RAA489204. These times are referenced from the start of the internal operation (as shown in Figure 66 and Figure 67) and assume all 14 cells are enabled. If fewer cells are connected (and are masked) the cell is skipped and the operation completes in less time. (see note in Scan Voltage Internal Timing.)

Table 47. Scan Wires Internal Timing

Operation	Sample Time after Start of Internal Operation (µs)
Sample Cell 1	13
Sample Cell 2	40
Sample Cell 3	61
Sample Cell 4	83
Sample Cell 5	104
Sample Cell 6	125
Sample Cell 7	146
Sample Cell 8	168
Sample Cell 9	189
Sample Cell 10	210
Sample Cell 11	231
Sample Cell 12	253
Sample Cell 13	274
Sample Cell 14	295
Begin Open Wire test	343
Start WSCN = 0 delay (1.5ms)	378
Sample Cell 1	1901
Sample Cell 2	1928
Sample Cell 3	1949
Sample Cell 4	1971
Sample Cell 5	1992
Sample Cell 6	2013
Sample Cell 7	2034
Sample Cell 8	2056
Sample Cell 9	2077
Sample Cell 10	2098
Sample Cell 11	2119
Sample Cell 12	2141
Sample Cell 13	2162
Sample Cell 14	2183
Start Open Wire Logic check	2218
Sample VBAT	3281

Table 47. Scan Wires Internal Timing (Cont.)

Operation	Sample Time after Start of Internal Operation (µs)
Sample IntTemp	3316
End of Internal Operation	3367

10.2.6 Scan Cell MUX Internal Timing

Table 48 shows the timing for each operation of the Scan Cell MUX command internal to the RAA489204. These times are referenced from the start of the internal operation (as shown in Figure 66 and Figure 67.)

Table 48. Scan Cell MUX Internal Timing

	Operation	Sample Time after Start of Internal Operation (µs)
1	Sample Cell 1	13
2	Sample Cell 2	40
3	Sample Cell 3	61
4	Sample Cell 4	83
5	Sample Cell 5	104
6	Sample Cell 6	125
7	Sample Cell 7	146
8	Sample Cell 8	168
9	Sample Cell 9	189
10	Sample Cell 10	210
11	Sample Cell 11	231
12	Sample Cell 12	253
13	Sample Cell 13	274
14	Sample Cell 14	295
15	MUX Test Start	343
16	CMX1P2M = 0 Time starts	378
17	Iteration completes	875
18	End of Internal Operation after repeating Items 2-17 eight (8) times	6905

10.2.7 Internal Timing Summary

Table 49 shows a summary of the internal timing for the various scan modes. This is the total time to complete each operation.

Table 49. Internal Operation Timing (Summary)

Number of Cells Connected	Scan Volts Typ (µs)	Scan Temps Typ (µs)	Scan Wires Typ (µs)	Scan All Typ (µs)[1]	Scan Mixed Typ (µs)	Scan Cell MUX Typ (µs)
14	589	3446	3367	4496	669	6905
13	567	3446	3324	4406	648	6735
12	546	3446	3282	4342	627	6565
11	525	3446	3239	4278	605	6395
10	504	3446	3197	4214	584	6225
9	482	3446	3154	4151	563	6055
8	461	3446	3112	4087	542	5885
7	440	3446	3069	4023	520	5715
6	419	3446	3027	3959	499	5545
5	397	3446	2984	3896	478	5375
4	376	3446	2942	3832	457	5205

1. Scan All operation includes Scan Volts, Scan Temps, and Scan Wires. Alll scan operations include VBAT, Vint_temp, VBAT/VSS Open, and EEPROM MISR checks.

10.2.8 Cell Voltage Measurement Averaging Time

By setting the CAV[2:0] bits, the RAA489204 can be set up to automatically average from 1 to 32 successive samples. After a scan of the cell voltages, there is a delay of 50µs before another scan. The readings for each cell are averaged over the number of cycles selected. The times shown in Table 50 are the typical times required to complete the entire Scan Voltage operation, including all average cycles. The GPIO2 output (bit G2MOD = 1; bit G2FUNC = 1; and bit G2F2 = 1) shows the action of the internal ADC. The time GPIO2 output is High is typically 330µs for 14 cells. This is shorter than shown in Table 50 for each scan, because the GPIO2 output is not reflective of the complete scan operation, which includes other operations besides the ADC conversion. The time between ADC operations (GPIO2 High) is 300µs (typical), for overhead, setup and hold times, and delay times that is not part of the specific ADC conversion of cell voltages.

Table 50. Scan Volts Timing - Averaging[1][2]

Number of Cells	Each Scan Voltage Measurement Time Typ (µs)	Number of Average Cycles					
		1 CAV[2:0] = 0 Typ (µs)	2 CAV[2:0] = 1 Typ (µs)	4 CAV[2:0] = 2 Typ (µs)	8 CAV[2:0] = 3 Typ (µs)	16 CAV[2:0] = 4 Typ (µs)	32 CAV[2:0] = 5 Typ (µs)
14	589	588.5	1216.5	2472.5	4984.5	10008.5	20056.5
13	567	567.3	1174.0	2387.5	4814.5	9668.5	19376.5
12	546	546.0	1131.5	2302.5	4644.5	9328.5	18696.5
11	525	524.8	1089.0	2217.5	4474.5	8988.5	18016.5
10	504	503.5	1046.5	2132.5	4304.5	8648.5	17336.5
9	482	482.3	1004.0	2047.5	4134.5	8308.5	16656.5
8	461	461.0	961.5	1962.5	3964.5	7968.5	15976.5

Table 50. Scan Volts Timing - Averaging[1][2] (Cont.)

Number of Cells	Each Scan Voltage Measurement Time Typ (µs)	Number of Average Cycles					
		1 CAV[2:0] = 0 Typ (µs)	2 CAV[2:0] = 1 Typ (µs)	4 CAV[2:0] = 2 Typ (µs)	8 CAV[2:0] = 3 Typ (µs)	16 CAV[2:0] = 4 Typ (µs)	32 CAV[2:0] = 5 Typ (µs)
7	440	439.8	919.0	1877.5	3794.5	7628.5	15296.5
6	419	418.5	876.5	1792.5	3624.5	7288.5	14616.5
5	397	397.3	834.0	1707.5	3454.5	6948.5	13936.5
4	376	376.0	791.5	1622.5	3284.5	6608.5	13256.5

1. Scan Voltage Measurement time includes the ADC measurement operation, it does not include additional setup and termination tasks.
2. The time between averaging cycles is 50µs.

10.2.9 External Temperature Measurement Averaging Time

By setting the TAV[2:0] bits, the RAA489204 can be set up to automatically average from 1, 2, 4, 8, 16, or 32 successive samples of the ExTn and GPIOn inputs. After a scan of the Temperature MUX, VBAT and Internal temperature, the RAA489204. The readings for each temperature are averaged over the number of cycles selected. The times shown in Table 51 are the typical times required to complete the entire Scan Temperature operation, including all average cycles.

Table 51. Temperature Measurement Timing - Averaging

Time to:	Number of Average Cycles					
	1 TAV[2:0] = 0 Typ (µs)	2 TAV[2:0] = 1 Typ (µs)	4 TAV[2:0] = 2 Typ (µs)	8 TAV[2:0] = 3 Typ (µs)	16 TAV[2:0] = 4 Typ (µs)	32 TAV[2:0] = 5 Typ (µs)
Complete Scan MUX, VBAT, Internal Temp[1]	3164	3164	3164	3164	3164	3164
Complete Scans of ExTn, GPIOn	282	564	1128	2256	4512	9024
Total Time	3446	3728	4292	5420	7676	12188

1. Scan MUX, VBAT and Internal Temperature timing includes the 2.5ms wait time.

10.3 Response Timing

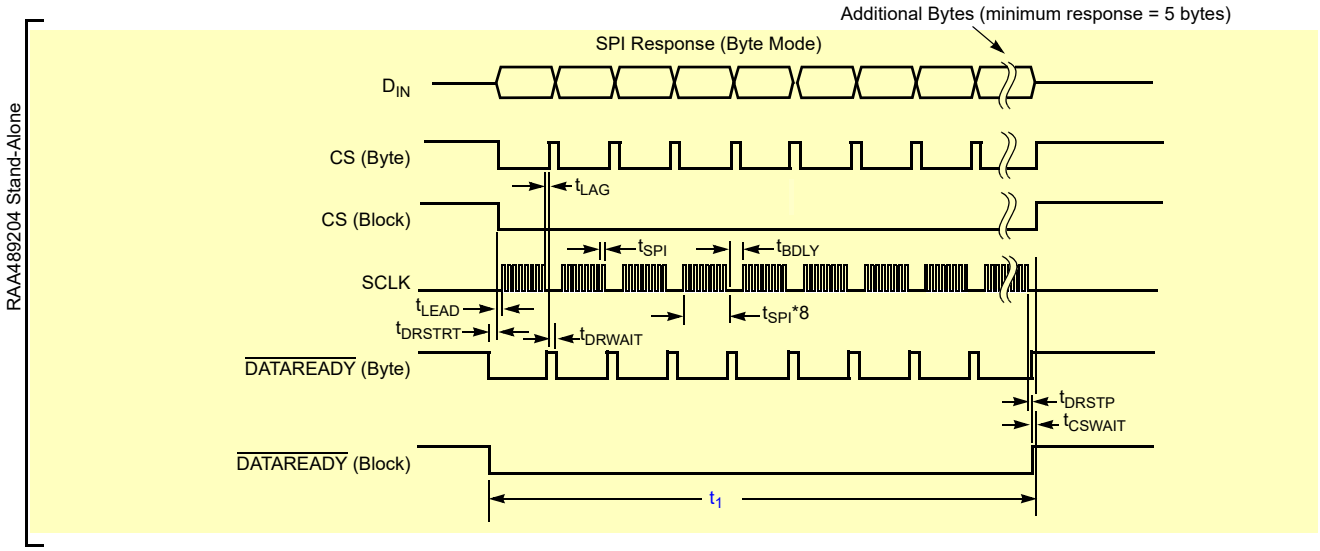
For commands that have a response, the response begins in the Top device following the packet reset time out plus a time delay equal to 16 daisy clocks, plus 1.5µs.

If the target device is the Top device, it responds with ACK or Data, as defined by the command. If the target device is not the Top device, the Top device responds with an ACK. The response from the target device begins after it receives the ACK response from the Top device.

The response timing diagrams show the time from the end of an internal operation on the Top device to the host receiving the complete response message on the SPI port.

Responses are different for Master, Mid, and Top devices. The response timings are shown in Figure 68 through Figure 73.

10.3.1 Response Timing Diagrams



Byte Mode

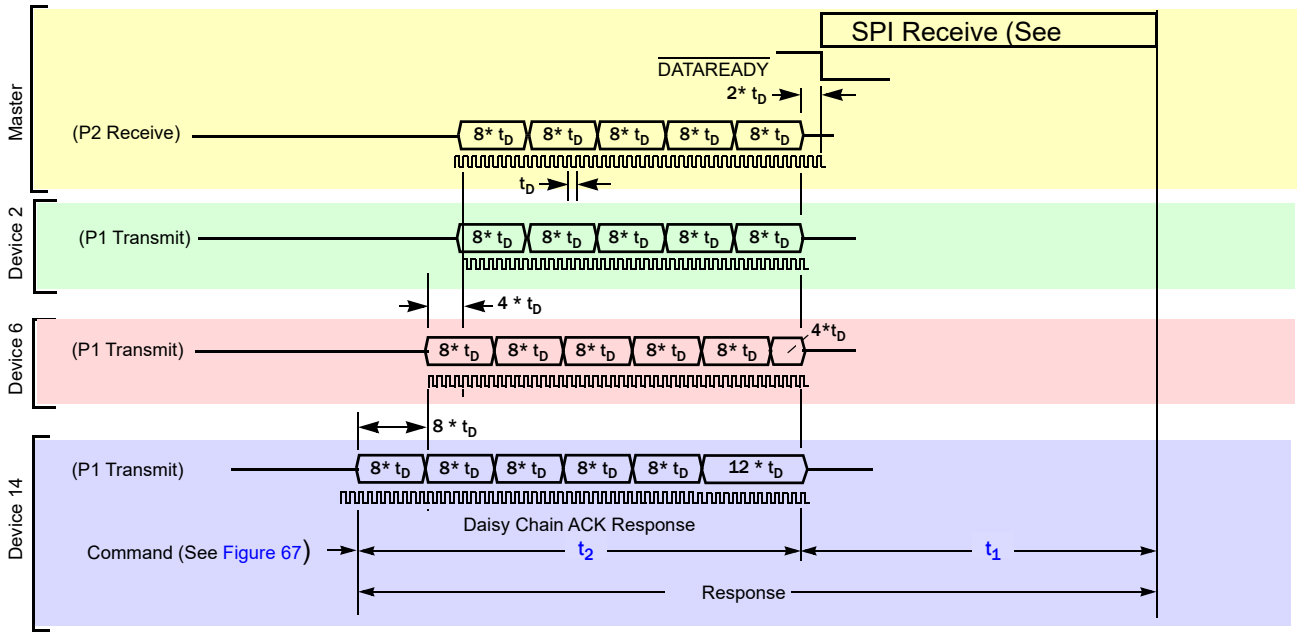
$$t_1 = (t_{DRSTRT} + t_{LEAD} + (t_{SPI} \times 8) + t_{LAG} + t_{DRWAIT}) \times D$$

Block Mode

$$t_1 = t_{DRSTRT} + t_{LEAD} + (t_{SPI} \times 8) \times D + (t_{BDLY} \times (D - 1)) - (t_{SPI}/2) - t_{DRSTP} + t_{CSWAIT}$$

t_{DRSTRT} = $\overline{\text{DATAREADY}}$ Low to $\overline{\text{CS}}$ Low
t_{LEAD} = $\overline{\text{CS}}$ Low to first SPI Clock
t_{SPI} = SPI clock period
t_{LAG} = Last SPI Clock to $\overline{\text{CS}}$ High
t_{DRWAIT} = $\overline{\text{CS}}$ High to $\overline{\text{DATAREADY}}$ Low
t_{BDLY} = Time between data bytes (block mode)
t_{DRSTP} = $\overline{\text{DATAREADY}}$ High to $\overline{\text{CS}}$ High
t_{CSWAIT} = $\overline{\text{DATAREADY}}$ High to $\overline{\text{CS}}$ High

Figure 68. SPI Receive Timing

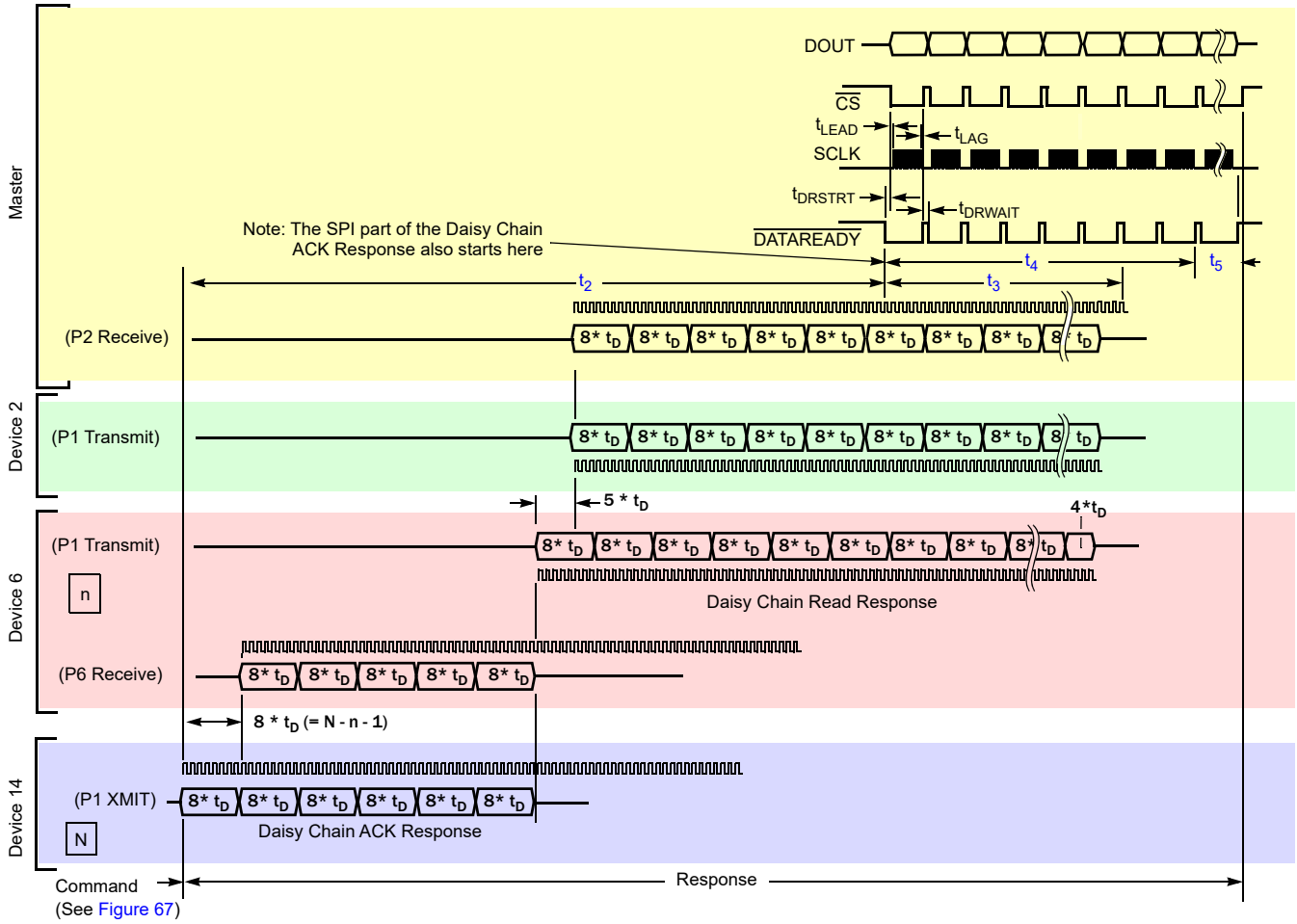


t_1 = (See "t1" in SPI Block or Byte Mode timing in Figure 68)

$t_2 = t_D \times (40 + N + 2)$

t_D = Daisy Chain clock period
N = Stack position of TopTop device
D = Number of transmitted bytes
D = 5 for ACK/NAK response
D = 9 for Read one Register

Figure 69. Response Timing (Master Device - Byte or Block Mode)



$$\text{Response Time} = t_2 + t_3 + (t_4 - t_3) + t_5$$

Note: t_4 is never less than t_3. $\overline{\text{DATAREADY}}$ stays High waiting for the last byte.

$$t_2 = t_D \times (80 + N - 1 + 3)$$

$$t_3 = t_D \times ((D - 5) \times 8)$$

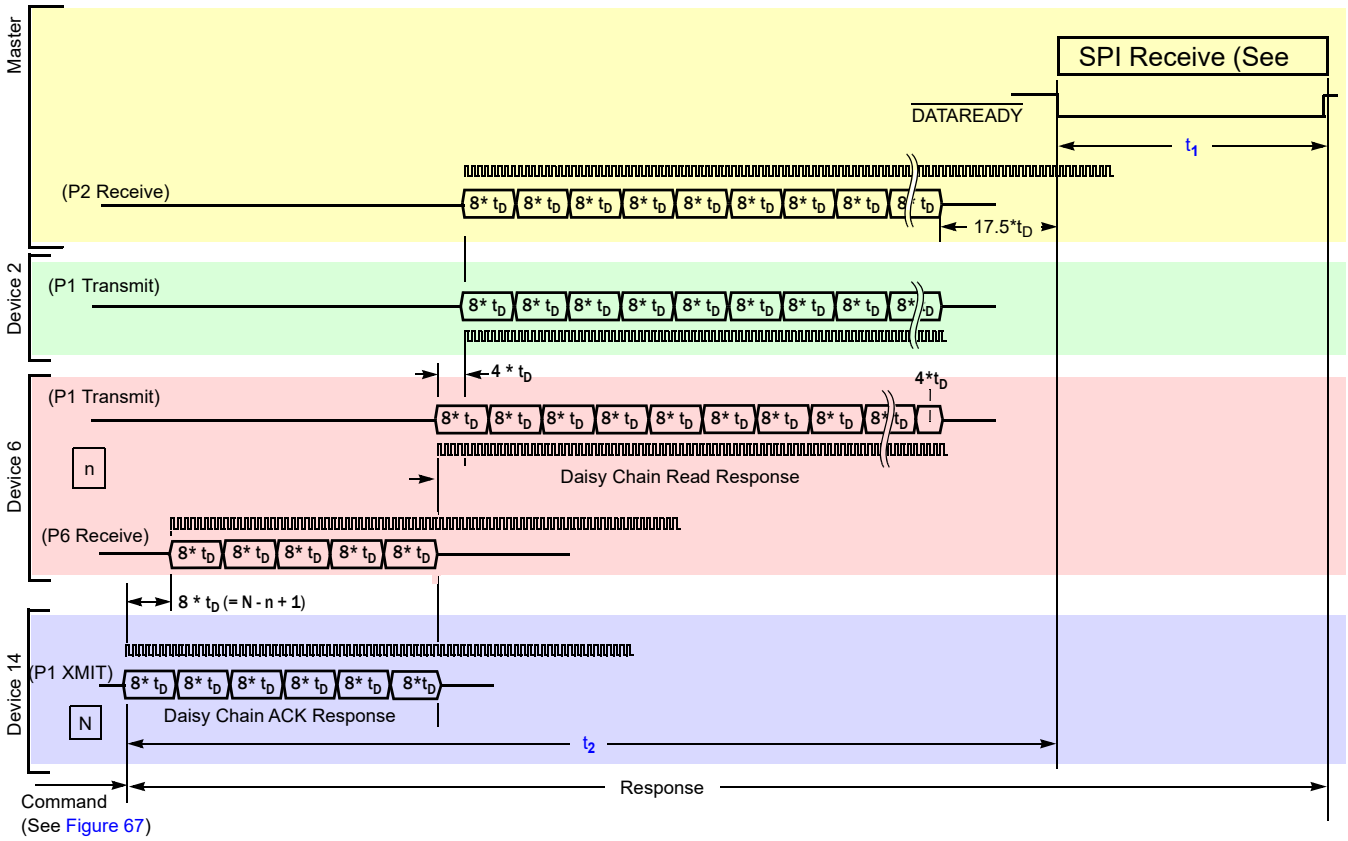
$$t_4 = (t_{SPI} \times 8 + t_{DRSTRT} + t_{LEAD} + t_{LAG} + t_{DRWAIT}) \times (D - 1)$$

$$t_5 = t_{SPI} \times 8 + t_{DRSTRT} + t_{LEAD} + t_{LAG}$$

t_D = Daisy Chain clock period
t_{DRSTRT} = $\overline{\text{DATAREADY}}$ Low to $\overline{\text{CS}}$ Low
t_{SPI} = SPI Clock Period
t_{LAG} = Last SPI Clock to $\overline{\text{CS}}$ High
t_{DRWAIT} = $\overline{\text{CS}}$ High to $\overline{\text{DATAREADY}}$ Low
N = Stack position of Top device
n = Stack position of Mid stack device
D = Number of bytes in the Mid stack device response

1. Top device adds (N -- 1) Daisy clocks to allow communications to the targeted Mid stack device.
2. Mid stack device adds (n -- 2) Daisy clocks to allow communications to the Master device.

Figure 70. Response Timing (Mid Stack Device - Byte Mode)



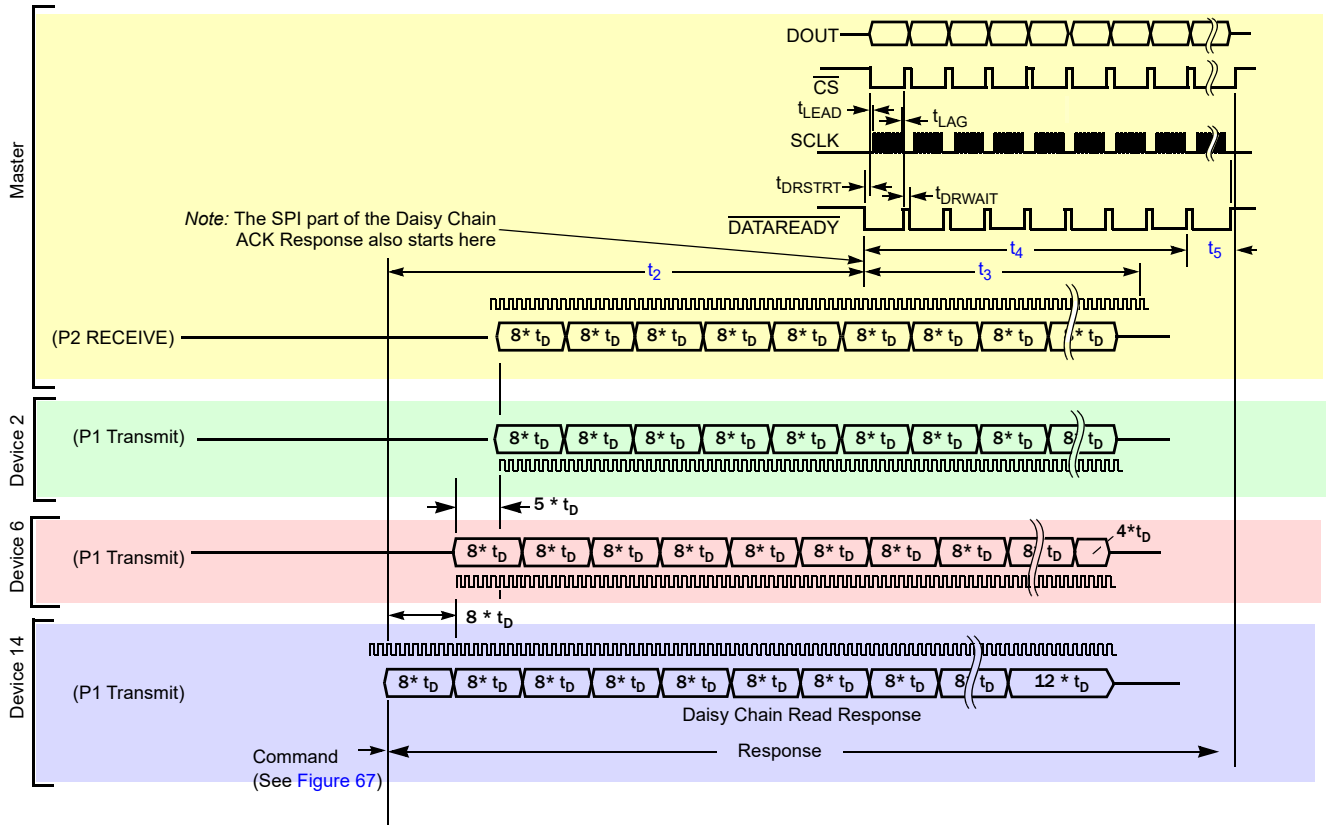
t_1 = (See “t1” in SPI Block Mode timing in Figure 68)

$$t_2 = t_D \times ((D + 5) \times 8 + N - 2 + 17.5)$$

t_D = Daisy Chain clock period
N = Stack position of Top device
n = Stack position of Mid stack device
D = Number of bytes in the Mid stack device response

1. Top device adds (N - n - 1) daisy clocks to allow communications to the targeted Mid stack device.
2. Mid stack device adds (n - 2) daisy clocks to allow communications to the Master device.

Figure 71. Response Timing (Mid Stack Device - Block Mode)



$$ResponseTime = t_2 + t_3 + (t_4 - t_3) + t_5$$

Note: t_4 is never less than t_3. DATAREADY stays High waiting for the last byte.

$$t_2 = t_D \times (40 + N - 1 + 3)$$

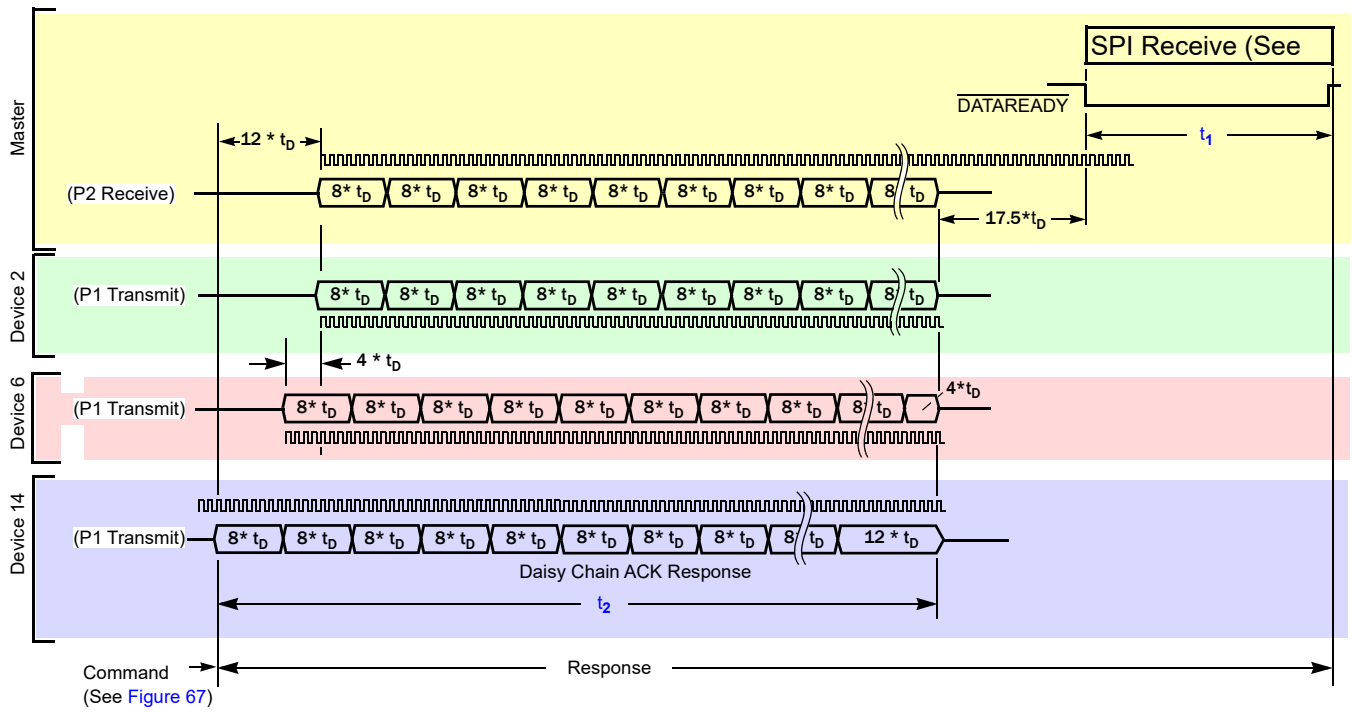
$$t_3 = t_D \times ((D - 5) \times 8)$$

$$t_4 = (t_{SPI} \times 8 + t_{DRSTRT} + t_{LEAD} + t_{LAG} + t_{DRWAIT}) \times (D - 1)$$

$$t_5 = t_{SPI} \times 8 + t_{DRSTRT} + t_{LEAD} + t_{LAG}$$

t_D = Daisy Chain clock period
t_{DRSTRT} = $\overline{\text{DATAREADY}}$ Low to $\overline{\text{CS}}$ Low
t_{SPI} = SPI Clock Period
t_{LAG} = Last SPI Clock to $\overline{\text{CS}}$ High
t_{DRWAIT} = $\overline{\text{CS}}$ High to $\overline{\text{DATAREADY}}$ Low
N = Stack position of Top device
n = Stack position of Mid stack device
D = Number of bytes in the Mid stack device response

Figure 72. Response Timing (Top Device - Byte Mode)



t_1 = (See “t1” in SPI Block Mode timing in Figure 68)

$$t_2 = t_D \times (D \times 8 + N - 2)$$

where:

t_D = Daisy Chain clock period
N = Stack position of Top device
D = Number of bytes in response

Figure 73. Response Timing (Top Device - Block Mode)

10.3.2 Response Timing Tables

Response timing depends on the number of devices in the stack, the position of the device in the stack, how many bytes are read back, and whether the transfer mode is Byte or Block mode. Table 52 and Table 53 show the command plus response times for the Master, Mid and Top devices for a specified number of Daisy Chain devices and read bytes. The values show the total time required to complete the entire Read operation. This is calculated using Equation 7:

(EQ. 7) $$(N \times T_{COMMAND}) + ((N-2) \times T_{MID}) + T_{TOP} + T_{MASTER}$$

where N = Number of devices in the stack.

In Table 52 and Table 53, daisy and SPI timing are assumed to be:

SPI clock = t_{SCK} = 2MHz
$\overline{CS}$ Low to first SCLK rising edge = t_{LEAD} = 100ns
$\overline{CS}$ High to $\overline{DATAREADY}$ Low = t_{DRWAIT} = 500ns
Last SPI SCLK to $\overline{DATAREADY}$ High = t_{DRSTP} = 140ns
Block mode, SPI time between bytes = t_{BDLY} = 0
$\overline{DATAREADY}$ High to $\overline{CS}$ High = t_{CSWAIT} = 39ns
Last SCLK to $\overline{CS}$ rising edge = t_{LAG} = 32ns
Daisy clock = t_D = 1MHz

For most settings and returned bytes, the Byte mode communication takes less time, but Block mode timing can offer a smaller overhead to software operations, especially if the microcontroller can use DMA type transfers from the SPI port directly to memory.

The values in the table are computed using a Microsoft Excel spreadsheet with the timing equations shown in Figure 73. The values in the table are nominal values. Variations in daisy and SPI clocks and in microcontroller/RAA489204 response times change the results.

Table 52. Read Register Command/Response Timing (SPI Byte Mode Transfer) in Microseconds

Number of Bytes in Response	Number of Devices in Daisy Chain						
	1 (Stand-Alone)	2	3	5	8	15	30
5	93	275	459	843	1436	2972	6924
9	112	313	516	938	1589	3259	7498
13	131	358	587	1060	1788	3639	8264
15	140	384	628	1134	1910	3872	8737
17	150	409	670	1207	2031	4106	9211
19	160	435	711	1281	2153	4339	9685
21	169	460	753	1355	2275	4573	10158
23	179	486	794	1428	2396	4807	10632
25	188	512	836	1502	2518	5040	1185
27	198	537	878	1575	2639	5274	11579
29	207	563	919	1649	2761	5507	12052
31	217	588	961	1722	2882	5741	12526
33	227	614	1002	1796	3004	5974	13000
35	236	639	1044	1869	3126	6208	13473
37	246	665	1085	1943	3247	6441	13947
39	255	691	1127	2017	3369	6675	14420
41	265	716	1168	2090	3490	6909	14894
43	274	742	1210	2164	3612	7142	15367
45	284	767	1252	2237	3733	7376	15841
47	293	793	1293	2311	3855	7609	16315
49	303	818	1335	2384	3976	7843	16788
51	313	844	1376	2458	4098	8076	17262
53	322	870	1418	2532	4220	8310	17735
55	332	895	1459	2605	4341	8544	18209
57	341	921	1501	2679	4463	8777	18682
59	351	946	1543	2752	4584	9011	19156
61	360	972	1584	2826	4706	9244	19629
63	370	997	1626	2899	4827	9478	20103

Table 53. Read Register Command/Response Timing (SPI Block Mode Transfer) in Microseconds

Number of Bytes in Response	Number of Devices in Daisy Chain						
	1 (Stand-Alone)	2	3	5	8	15	30
5	89	281	475	878	1502	3107	7208
9	85	345	587	1086	1854	3795	8616
13	121	409	699	1294	2206	4483	10024
15	129	441	755	1398	2382	4827	10728
17	137	473	811	1502	2558	5171	11432
19	145	505	867	1606	2734	5515	12136
21	153	537	923	1710	2910	5859	12840
23	161	569	979	1814	3086	6203	13544
25	169	601	1035	1918	3262	6547	14248
27	177	633	1091	2022	3438	6891	14952
29	185	665	1147	2126	3614	7235	15656
31	193	697	1203	2230	3790	7579	16360
33	201	729	1259	2334	3966	7923	17064
35	209	761	1315	2438	4142	8267	17768
37	217	793	1371	2542	4318	8611	18472
39	225	825	1427	2646	4494	8955	19176
41	233	857	1483	2750	4670	9299	19880
43	241	889	1539	2854	4846	9643	20584
45	249	921	1595	2958	5022	9987	21288
47	257	953	1651	3062	5198	10331	21992
49	265	985	1707	3166	5374	10675	22696
51	273	1017	1763	3270	5550	11019	23400
53	281	1049	1819	3374	5726	11363	24104
55	289	1081	1875	3478	5902	11707	24808
57	297	1113	1931	3582	6078	12051	25512
59	305	1145	1987	3686	6254	12395	26216
61	313	1177	2043	3790	6430	12739	26920
63	321	1209	2099	3894	6606	13083	27624

10.4 Sequential Daisy Chain Communications

When sending a sequence of commands to the Master device, the host must allow time after each response and before sending the next command for the Daisy Chain ports of all stack devices (other than the Master) to switch to Receive mode. This wait time is equal to eight Daisy Chain clock cycles and is imposed from the time of the last edge on the Master's input Daisy Chain port to the last edge of the first byte of the subsequent command on the SPI (see Figure 74).

The minimum recommended wait time, between the host receiving a response and sending the next command, is given in Equation 8. For definition of terms, see Figure 74. Also, see Table 54 and Figure 74.

(EQ. 8) $$t_{WAIT} = t_{CLR} - 2 \times ((8 \times t_{SPI}) + t_{LEAD} + t_{LAG}) + t_{DRSP} + t_{CS}$$

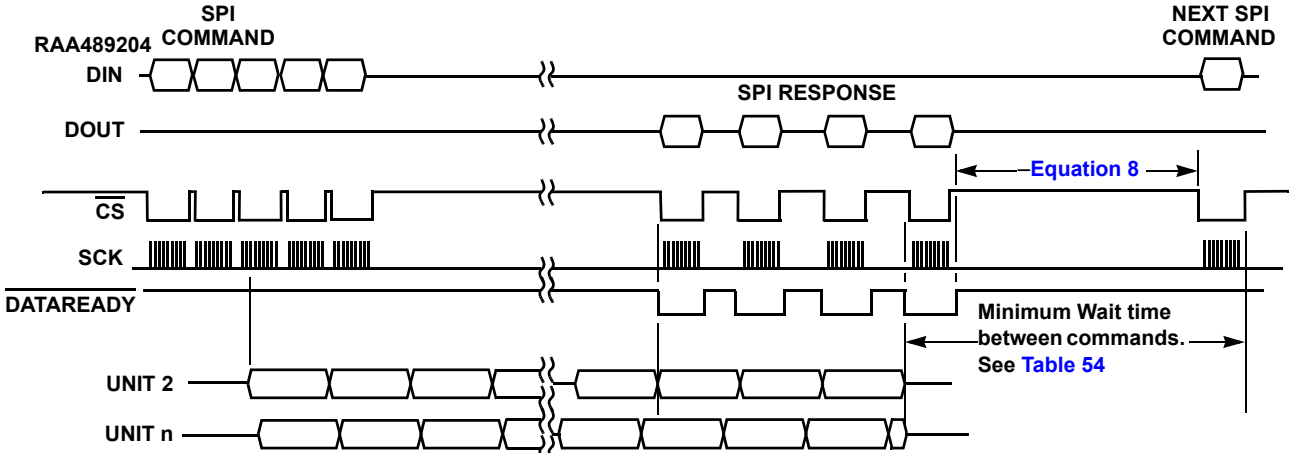


Figure 74. Minimum Wait Time Between Commands (Daisy Chain Response - Top Device)

Table 54. Minimum Recommended Communications Wait Time

Daisy Chain Data Rate	Maximum Time For Daisy Chain Ports to Clear			Unit
	1000	500	333	kHz
Communications Wait Time	18	72	144	µs

10.5 Summary Timing Tables

The total time to initiate a scan, wait for the internal operation to complete, and to read back the responses is a sum of the times shown above in Command Timing, Internal Operations, and Response Timing. Tables that show example timing for Scan Voltage, Scan Mixed, and Scan All operations plus read back of data are shown in the following tables.

Table 55. Sample Transmit, Execute, Read Data for SCAN VOLTAGE Command[1]

Number of Devices	Max number of cells	First Cell Sample (Device 1) (µs)	Last Cell Sample (Device N) (µs)	All Registers Loaded (µs)	Time to read all Cell Data (µs)	Total Time (ms)
1	14	10	305	664	281	0.945
2	28	91	401	730	798	1.529
3	42	92	402	731	1317	2.049
5	70	94	404	735	2368	3.103
7	98	96	406	736	3070	3.806
8	112	98	407	737	3978	4.714

Table 55. Sample Transmit, Execute, Read Data for SCAN VOLTAGE Command[1] (Cont.)

Number of Devices	Max number of cells	First Cell Sample (Device 1) (µs)	Last Cell Sample (Device N) (µs)	All Registers Loaded (µs)	Time to read all Cell Data (µs)	Total Time (ms)
9	126	99	409	738	4523	5.261
15	210	105	415	745	7889	8.633
30	420	122	432	761	17003	17.764

1. Data Read Back includes VBAT, Internal IC Temp, and device status. 17 registers (34 data bytes) + 4 CRC + 5 header = 43 bytes

Table 56. Sample Transmit, Execute, Read Data for SCAN MIXED Command[1]

Number of Devices	Max number of cells	First Cell Sample (Device 1) (µs)	Last Cell Sample (Device N) (µs)	All Registers Loaded (µs)	Time to Read All Cell Data (µs)	Total Time (ms)
1	14	25	423	718	290	1.008
2	28	91	489	784	826	1.610
3	42	92	490	785	1362	2.147
5	70	94	493	787	2449	3.236
7	98	96	495	790	3163	3.953
8	112	98	496	791	4112	4.902
9	126	99	497	792	4675	5.466
15	210	105	504	798	8147	8.946
30	420	122	520	815	17528	18.343

1. Data Read Back includes VBAT, Internal IC Temp, ExtTemp1, and device status.
18 registers (36 data bytes) + 4 CRC + 5 header = 45 bytes

Table 57. Sample Transmit, Execute, Read Data for SCAN ALL Command[1]

Number of Devices	Max number of cells	First Cell Sample (Device 1) (µs)	Last Cell Sample (Device N) (µs)	All Registers Loaded (µs)	Time to Read All Cell Data (µs)	Total Time (ms)
1	14	25	335	4982	376	5.358
2	28	91	401	5048	1072	6.120
3	42	92	402	5049	1768	6.817
5	70	94	404	5051	3175	8.226
7	98	96	406	5054	4000	9.053
8	112	98	407	5055	5318	10.372
9	126	99	409	5056	6041	11.097
15	210	105	415	5062	10473	15.536
30	420	122	432	5079	22254	27.333

1. Data Read Back includes Cells, VBAT, Internal IC Temp, all ExtTemp, all GPIO, 2nd Vref, Scan Count, and device status = 27 registers (54 data bytes) + 4 CRC + 5 header = 63 bytes

11. Power Modes

The RAA489204 has three main power modes: Normal mode, Shutdown mode, and Sleep mode.

11.1 Normal Mode

Normal mode consists of an Active state and a Standby state. In the Standby state, all systems are powered and the device is ready to perform an operation in response to commands from the host microcontroller. In the Active state, the device performs an operation, such as ADC conversion, open-wire detection, etc.

11.2 Shutdown Mode

Drive the Enable pin LOW to place the part in Shutdown mode. When entering Shutdown mode, the internal bias for most of the IC is powered down except digital core and Sleep mode regulators.

Release the EN pin to resume operation. When exiting the Shutdown mode, the device powers up and reloads the factory programmed configuration data from EEPROM. A Roll Call is needed following an EN cycle.

The Hard Reset (HReset) function is related to the Shutdown mode. The HReset command sends a Daisy Chain signal to toggle the EN control logic internal to each RAA489204 device. This forces a reset in the same way as controlling the EN pin. The HReset command can be sent to the stack whether or not the stack is initialized.

The time required to reset a complete stack of devices is dependent on the number of devices in the stack. The maximum wake up time is shown in Equation 9:

(EQ. 9) $$t_{HRESET} = (t_{PUD} + 14ms) \times (N - 1)$$

where:

- t_{PUD} = 13ms (see Electrical Specifications)
- N = Number of devices

Table 58 provides an example of the maximum times from the HRESET command transmission to reset of all devices for stacks of 8 devices and 14 devices (Daisy Chain data rates do not substantially affect the Reset time).

Table 58. Maximum Reset Times for Stacks of 8 Devices and 14 Devices

Number of Devices	Maximum Wakeup Time (ms)
Stack of 8 Devices	190
Stack of 14 Devices	352

11.3 Sleep Mode

The RAA489204 enters the Sleep mode in response to the following:

- Sleep command
- Watchdog timeout
- Completion of an Auto Balance operation when followed by a Sleep command
- Oscillator fault
- Internal Over-Temperature

Only the communications input circuits, low speed oscillator, and internal registers are active in Sleep mode, allowing the part to perform timed scan and balancing activity and to wake up in response to communications.

The Sleep command is sent to all devices at the same time, using the Address All stack address, so it can be sent to the stack whether or not the stack is initialized. The devices do not need to know their position in the stack to respond to the Sleep command.

After receiving a valid Sleep command, devices wait before entering the Sleep mode. This is to allow time for the Top stack device to respond with an ACK, or for all devices that do not recognize the command to respond NAK and for the host microcontroller to respond with another command. Receipt of any valid communications on Port 1 of the RAA489204 before the wait period expires cancels the Sleep command. Receipt of another Sleep command restarts the wait timers. Table 59 provides the maximum wait time for various Daisy Chain data rates.

Table 59. Maximum Wait Time for Devices Entering Sleep Mode Following the Sleep Command

Daisy Chain Data Rate	Maximum Wait Time To Sleep			Unit
	1000	500	333	kHz
Time to Enter Sleep mode	500	2000	4000	µs

11.4 Wakeup

Device wake up responses:

- The device wakes up momentarily during a Scan Continuous scan cycle, if the device was set to Sleep mode with Scan Continuous mode active. The device wakes up, performs the scan, then goes back to sleep after the scan.
- The Master device wakes up in response to a Wakeup command from the host via the SPI port. This command forces the device to exit the Sleep Mode, send a Wakeup signal to the other devices in the chain, and resume normal operations.
- The device wakes up if it detects a fault condition while in Sleep mode with Scan Continuous mode active. This forces the device to exit the Sleep Mode, send a Wakeup signal on the Daisy Chain to devices above and below, and then resume normal operations. When all devices are awake, the device detecting the fault sends a Fault response to the Master. The Master then sets the $\overline{\text{DATAREADY}}$ pin low, notifying the host of a pending Fault Response. Fault Response is the same as the response to a Read Fault Status Register from the device detecting the fault.
  A Master device wakes up if it detects a fault condition while in Sleep mode with Scan Continuous mode active. It then sends the Wakeup signal up the Daisy Chain. When all devices are awake, the Master sets the $\overline{\text{DATAREADY}}$ pin low indicating a pending Fault Response to the host.
- The device wakes up if it receives a Wakeup signal on the Daisy Chain, (This communication is normally a result of a fault condition on another device in the chain.) This condition forces the device to exit the Sleep Mode and resume normal operations.

Write the Wakeup command using the Address All stack address. The command is not recognized if sent with an individual device address and causes the Master device to respond with a NAK. The devices do not need to know their position in the stack to respond to the Sleep and Wakeup commands.

The Wakeup command from the host should be preceded by a HReset_Wakeup Precursor command. This command puts the Master device into a special mode that traps the next command. If the next command is a Wakeup, the Wakeup signal is sent out on the Daisy Chain. Any other command, except an HReset command, forces a NAK back to the host.

The HReset_Wakeup Precursor command can be sent to both a sleeping and an awake Master with the same effect. If the Wakeup is sent without the HReset_Wakeup Precursor and the Master is already awake, then the Master does not send the wake up signal on the Daisy Chain. This may lead to communication errors resulting from some devices that remain in Sleep mode.

A sleeping Master receiving the Wakeup command (without first receiving the HReset_Wakeup Precursor) can wake up and proceed to send the wakeup signal on the Daisy Chain when the full Wakeup command is received (and CRC verified). However, Renesas recommends to always precede the Wakeup command with the HReset_Wakeup Precursor command.

Each device in the chain wakes up on receipt of the Wakeup signal and sends the signal onto the next device. Devices transmitting the Wakeup signal on Port 2 ignore any communications received on Port 1.

Daisy Chain devices registering a fault in Sleep mode (as might happen if a device is operating in Scan Continuous mode while also in Sleep mode) proceed to wakeup the other devices in the stack (for example, Mid devices send the Wakeup signal on both ports).

After receiving the Wakeup signal, the Top stack device waits before sending an ACK response on Port 1. This delay is to allow other stack devices to wakeup. The total wait time is dependent on the number of devices in the stack.

The ACK response following the wakeup propagates to the Master device, that passes it on to the host microcontroller to complete the wake up sequence.

The total time required to wake up a complete stack of devices is dependent on the number of devices in the stack. The maximum wake up time is shown in Equation 10:

(EQ. 10) $$t_{WAKE} = 14.5ms \times (N - 1) + ACK$$

where:

N = Number of devices
ACK = ACK response time for the Top device in the Daisy Chain (see Figure 72 or Figure 73.)

Table 60 provides an example of the maximum times from the Wakeup command transmission to receipt of the ACK response ($\overline{DATAREADY}$ asserted Low) for stacks of 8 devices and 14 devices at various Daisy Chain data rates.

Table 60. Maximum Wakeup Times for Stacks of 8 Devices and 14 Devices (Wakeup Command to ACK Response)

Number of Devices	Maximum Wakeup Time (ms)
Stack of 8 Devices	102
Stack of 14 Devices	189

There is no additional checking for communications faults while devices are waking up. A communications fault is indicated by the host microcontroller not receiving an ACK response within the expected time.

The normal host microcontroller response to receiving an ACK while the stack is in Sleep mode is to read the Fault Status register contents of each device in the stack to determine which device (or devices) has a fault.

11.5 Power Sequencing

The RAA489204 follows an initialization procedure following initial power on, following the toggling the EN pin, and after receiving an HReset or SReset command, see Figure 75. These operations reinitialize the device regulators, the Daisy Chain stack, and the device registers. Following these power sequencing operations, it is necessary to re-initialize the RAA489204 Daisy Chain using the Roll Call procedure. The diagram in Figure 75 also includes timing for a Sleep/Wake cycle. This does not require a new Roll Call sequence.

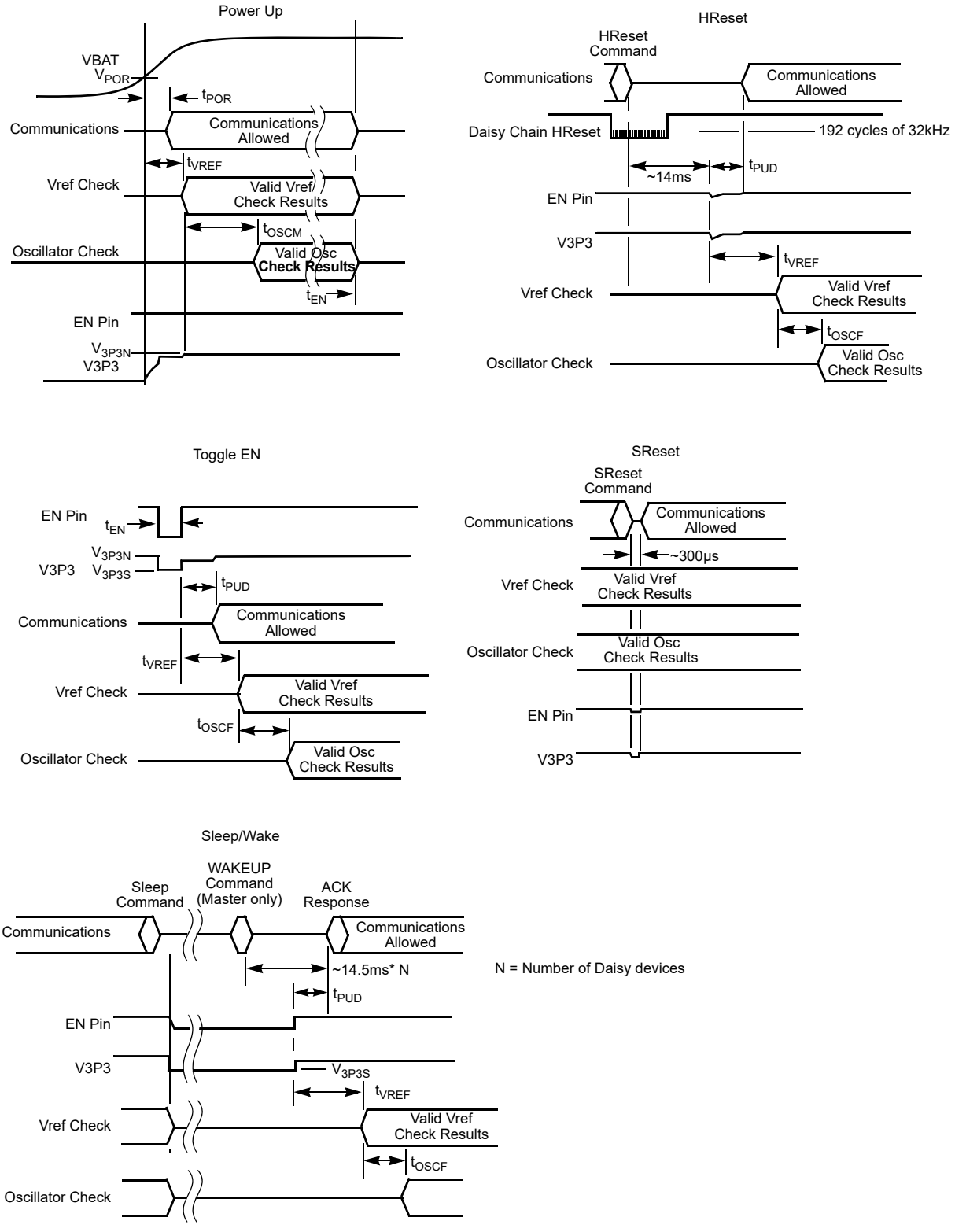


Figure 75. Power Sequencing

11.5.1 Fault Limit Settings

Various fault limit values are saved to the RAA489204 volatile registers by the host microcontroller following power up or a power cycling and following a software reset. The default values are shown in Table 61. The host microcontroller should reset the Checksum value (Send Calc Register Checksum command) after changing any of these limit values.

Table 61. Default Limit Settings

Limit Value	Default Setting
Cell Overvoltage	5V
Cell Undervoltage	0V
External Over-Temperature	0
Internal Over-Temperature Warning	239°C
Internal Over-Temperature Limit	139°C (fixed at factory and not changeable by user)

11.5.2 Configuration Settings

In addition to the limit settings for temperatures and cell voltages (see Table 61) the host may need to set up additional configuration registers on power-up. These registers, and their default values, are shown in Table 62. The host microcontroller should reset the Checksum value (Send Calc Register Checksum command) after changing any of these configuration values.

Table 62. Default Device Configuration Settings

Configuration Value	Default Setting	Default Conditions
Fault Setup Register	TSTIT = 1 TOT2:0 = 3 SCN3:0 = 8	Internal Temp Limit Enabled Totalizer set to 8 Scan Continuous Interval = 4.096 seconds
$\overline{\text{FAULT}}$ Pin Mask	0	All faults enabled
GPIO1 Fault Mask	0	All faults included in a GPIO1 Fault output
Cell Balance Setup	BMD1:0 = 0 BWT2:0 = 0 BEN = 0 BDDS = 0 EOB = 0 IBAL = 0	Balance Mode = Off Balance Wait time = 0 Balance Enable = Not enabled Balancing is not turned off during Scan Continuous or Auto Balance This is an indicator for end of balance (not set by user) External balance is enabled.
Watchdog/Balance Time	0x003F	Balance time = 0 (not enabled) Watchdog timeout = 64 seconds
Device Setup 1	0	GPIO selected as Input GPIO1, GPIO2 selected as normal operation Scan Continuous mode off Wire Scan current on time = 1.5ms Watchdog disable password entry = 0 (must be changed to disable WDT) TEMPREG output enabled Open Wire current on time during Scan Cell MUX command = 0.5ms

Table 62. Default Device Configuration Settings

Configuration Value	Default Setting	Default Conditions
Device Setup 2	0	Cell Measurement Averaging is off Temperature Measurement Averaging is off GPIO1, GPIO2 output values set to 0 (when GPIO set to output) GPIO2 output mode controlled by G2VAL (no special function) Daisy Chain upper port turned on TMUX control disabled ADC input NOT forced to limits
Cell Fault Mask	0	None of the cells have had fault conditions over-ridden. (Value might be changed for when fewer than 14 cells are connected.)

12. Communication Faults

12.1 Communication Failure

All commands except the Scan commands, Measure, Sleep, Wakeup, and HReset require a response (see Table 26) from the stack Top device, that propagates back down the Daisy Chain. If any device in the stack fails to receive a response from the device above within a timeout period, then it indicates a communications fault to the device below (and ultimately to the Master) by sending a Fault Status Register Read response.

A communications fault can be caused by one of two circumstances: that the communications system has been compromised (for example a broken wire, faulty component, bad connection, or stuck condition) or that a device is in Sleep mode.

The Comms Failure timeout must reliably recognize that an expected response has not been received but must also allow sufficient time for higher devices in the stack to themselves detect the failure condition and send the Comms Failure response. The Comms Failure timing applied by each device depends on the stack location of that device. So each device calculates the required timeout based on its location in the stack.

The Comms Failure timeout value is counted from the end of the Packet Reset timeout. Table 63 gives calculated Comms Failure timeout values for a stack of up to 30 devices. The table shows the maximum time required to return the Communications Failure response to the host microcontroller (from the end of the packet reset delay on the target device). In the table, the stack location of each device is in relation to the Top device, so device [-1] is the device immediately below top, device [-2] is the device below device [-1], etc. In the case where the Stack has not completed Roll Call, devices all have stack address 0 (zero) and the maximum delay should be expected.

If the target device receives a Communications Failure response from the device above, then the target device relays the Communications Failure followed by the requested data (in the case of a Read) or simply relays the Communications Failure only (in the case of a command that either has no response or normally responds with an ACK).

If one or more stack devices are asleep, there is a Communication Failure response from the top awake device.

If there is a Communications Failure, the host microcontroller sends a Wakeup/HReset Precursor command followed by a Wakeup command. This should wake all devices in the stack. Any devices that went to sleep due to a Watchdog timeout would show a WDGF bit set in the Fault Status register when awake and responding to a command.

If the Wakeup command does not generate a response, this is a likely indication that the communications have been compromised. In this case, send an SReset followed by a Roll Call command to try to clear communications.

If commands repeatedly result in a Communications Failure response, the next steps are for the host microcontroller to send a Wakeup/HReset Precursor command followed by an HReset command, followed by a Roll Call command.

If clock cycles are missing from the end of a communication such that the communication does not have sufficient length to be transmitted to the Top stack device, then some devices record a CRC error and respond NAK. This situation can happen if devices have incorrect address or stack size information. If there are insufficient clock cycles to allow complete transmission to the Master stack device, the host receives a short message, with CRC errors, and the Master device indicates a buffer under-run condition. Additional clock cycles, which extend the transmission beyond the length indicated in the length part of the communication header, are ignored.

Table 63. Communication Failure Timeouts

Stack Location	Maximum Time to Assertion of $\overline{\text{DATAREADY}}$ (Number Of Daisy Cycles)
Top	60
-1	70
-2	138
-3	167
-4	234
-5	284
-6	353
-7	430
-8	524
-9	639
-10	779
-11	950
-12	1160
-13	1415
-14	1729
-15	2110
-16	2577
-17	3148
-18	3846
-19	4699
-20	5742
-21	7015
-22	8572
-23	10475
-24	12801
-25	15644
-26	19119
-27	23366
-28	28557
-29	34901

12.2 Measurement Scan Counter

Because there is no expected response from a Scan command, a Measurement Scan Counter is provided to allow confirmation of execution of the Scan command. The Measurement Scan Counter is a 6-bit counter, that increments each time a Scan command is completed. This allows the host microcontroller to compare the counter value before and after the Scan command was sent to verify that the operation executed. The counter wraps to zero when overflowed.

The RAA489204 does not perform a requested Scan function if a Scan function is already in progress. In this case, the Scan Counter does not increment.

Commands that increment the Measurement Scan Counter are Scan Voltage, Scan Temperature, Scan Mixed, Scan All, and Scan Wires.

12.3 Diagnostic Scan Counter

The Diagnostic Scan Counter allows confirmation of execution of diagnostic commands. The Diagnostic Scan Counter is a 6-bit counter, that increments each time a Diagnostic Scan command is completed. This allows the host microcontroller to compare the counter value before and after the command was sent to verify that the operation executed. The counter wraps to zero when overflowed.

Commands that increment the Diagnostic Scan Counter are the Measure command with addresses of 0x00 or 0x10 through 0x19, Scan Temperatures, and Scan Cell MUX.

The RAA489204 does not perform a requested Diagnostic Scan function if there is already a function in progress. In this case, the Scan Counter does not increment.

12.4 Daisy Chain Communications Conflicts

Conflicts in the Daisy Chain system can occur if both a stack device and the host microcontroller are transmitting at the same time, or if more than one stack device transmits at the same time. Conflicts caused by a stack device transmitting at the same time as the host microcontroller are recognized by the absence of the required response (for example, an ACK response to a Write command), or by the scan counter not being incremented in the case of Scan or Measure commands.

Conflicts that arise from more than one device transmitting simultaneously can occur if two or more devices detect faults at the same time. This can occur (for example) when the stack is operating in Scan Continuous mode and more than one device registers an undervoltage fault at the same time. Renesas recommends that the host microcontroller checks the Fault Status register contents of all devices whenever a Fault Response is received from one device.

12.5 Watchdog Function

A watchdog timer is part of the communications fault detection system. Each device must receive a valid communications sequence before its watchdog timeout period is exceeded.

A valid communications sequence requires an action or response from the device. This functionality guards against situations where a runaway host microcontroller continually sends unrecognized data. Address All commands, such as the Scan and Balance commands, provide a simple way to reset the watchdog timers on all devices with a single communication. Individually send single device communications (for example, an ACK) to each device to reset the watchdog timer in that device. A read of the Fault Status register of each device is also a good way to reset the watchdog timer on each device.

The watchdog timeout is settable in three ranges (see Table 64). The low range (7’b0000001 to 7’b011 1111) provides timeout settings in 1 second increments from 1 second to 63 seconds. The high range (7’b100 0010 to 7’b1111111) provides timeout settings in 8 minute intervals from 8 minutes to 1520 minutes. The Mid range has settings of 2 minutes and 4 minutes.

A zero setting (6'b000000) disables the watchdog function. A watchdog password function is provided to guard against accidental disabling of the watchdog function. Set Bits [11:6] of the Device Setup 1 register to 6'h3A (111010) to allow the watchdog to be set to zero.

When a device fails to receive valid communications within the required time, it sets the WDGF bit, asserts the $\overline{\text{FAULT}}$ output, ceases all scanning and balancing activity (including scan continuous operations), and enters Sleep mode (if not already in Sleep mode). *Note:* There is no automatic watchdog Fault Response sent on the Daisy Chain interface.

Table 64. Watchdog Timeout Settings

WDG[7:0]	Timeout	Units
0000 0000	Disabled	
0000 0001	1	seconds
0000 0010	2	seconds
-	-	
0011 1110	62	seconds
0011 1111	63 (Default)	seconds
0100 0000	2	minutes
0100 0001	4	minutes
0100 0010	8	minutes
0100 0011	16	minutes
0100 0100	24	minutes
-	-	
1111 1110	1512	minutes
1111 1111	1520	minutes

13. System Faults

13.1 Alarm Signals

Bits are set in the fault data registers for overvoltage, undervoltage, open-wire, and over-temperature conditions in response to a fault detection. Additionally, the bits from each of the fault data registers are ORed and reflected to bits in the Fault Status register (one bit per data register).

A fault is registered when any of the bits in the Fault Status register are asserted. Two fault response methods indicate the existence of a fault. First, immediately on detection of the fault, the device sets the $\overline{\text{FAULT}}$ output pin Low. The $\overline{\text{FAULT}}$ output remains Low until the host resets the bits of all fault data and status registers to zero. Next, if the device is in Scan Continuous mode, the device provides a Fault Response on the Daisy Chain link.

The Daisy Chain Fault Response, a normal 9-byte Fault Status register read response, is immediate if the device is in Scan Continuous mode and there is no other communication activity on the device ports. If the device is not in Scan Continuous mode, the host must specifically read the Fault Response. But, the Fault Response consists of the Fault Status Register value returned as part of a normal page 1 multiple register read, so the operation requires no extra overhead. (*Note:* The Fault Response is not returned with a single register read operation or multiple register read from another page.)

In Scan Continuous mode, the Fault Response is only sent for the first fault occurrence. Subsequent faults do not activate the Fault Response until after the Fault Status register has been cleared.

A device running the Scan Continuous mode detects an overvoltage or undervoltage condition following an unbroken sequence of fault conditions equal to the Totalizer value or an immediate detection of an open VBAT or open VSS. The time required to determine this alarm condition is dependent on the chosen Scan Continuous Scan interval and the Totalizer count. The time required to detect the alarm condition is shown in Table 65.

Table 65. Alarm Detection Time

Scan Interval Code	Scan Interval (ms)	Overvoltage, Undervoltage, Open V_{DD}, Open V_{SS} Detection Time (ms)							
		Totalizer Count – [TOT2:TOT0] Value							
		1 000	2 001	4 010	8 011	16 100	32 101	64 110	128 111
0000	16	16	32	64	128	256	512	1024	2048
0001	32	32	64	128	256	512	1024	2048	4096
0010	64	64	128	256	512	1024	2048	4096	8192
0011	128	128	256	512	1024	2048	4096	8192	16384
0100	256	256	512	1024	2048	4096	8192	16384	32768
0101	512	512	1024	2048	4096	8192	16384	32768	65536
0110	1024	1024	2048	4096	8192	16384	32768	65536	131072
0111	2048	2048	4096	8192	16384	32768	65536	131072	262144
1000	4096	4096	8192	16384	32768	65536	131072	262144	524288
1001	8192	8192	16384	32768	65536	131072	262144	524288	1048576
1010	16384	16384	32768	65536	131072	262144	524288	1048576	2097152
1011	32768	32768	65536	131072	262144	524288	1048576	2097152	4194304
1100	65536	65536	131072	262144	524288	1048576	2097152	4194304	8388608

If a device is in Sleep mode running a Scan Continuous operation and detects an alarm condition, the device sends a Wakeup command both up and down the Daisy Chain, then sends the Fault Response following the Wakeup ACK response. When waken by communications on its upper port, the Master device sets its $\overline{\text{DATAREADY}}$ signal Low and, as commanded by the MCU, sends a normal Fault Response using the SPI bus.

If a fault occurs while the device ports are active, then the device waits until communications activity ceases before sending the Fault Response. The host microcontroller has the option to wait for this response before sending the next message. Alternately, the host microcontroller can send the next message immediately (after allowing the Daisy Chain ports to clear – see Sequential Daisy Chain Communications). If the host does not wait a sufficient time for all error responses, then any conflicts resulting from additional transmissions from the stack are recognized by the lack of response from the stack.

Table 66 provides the maximum time from $\overline{\text{DATAREADY}}$ going Low for the last byte of the normal response to $\overline{\text{DATAREADY}}$ going Low for the first byte of the Fault Response in the case where a Fault Response is held up by active communications.

Table 66. Maximum Time Between $\overline{\text{DATAREADY}}$ Signals - Delayed Fault Response

	Maximum Time Between $\overline{\text{DATAREADY}}$ Assertions				Unit
Daisy Chain Data Rate	500	250	125	62.5	kHz
Fault Response	68	136	272	544	µs

13.2 Memory Checksum

Two checksum operations are available, one for the EEPROM and one for the Page 2 registers.

Two values are provided to verify the contents of EEPROM memory. One 24-bit value contains the correct checksum value, which is calculated during factory testing at Renesas (Page 4, 6'h1C and the upper byte of 6'h1E.) The other 24-bit value contains the checksum (Page 4 6'h1D and the lower byte of 6'h1E) calculated each time the nonvolatile memory is loaded to shadow registers, either after a power cycle, following a Soft Reset (SReset command), or after a Hard Reset (HReset command or toggle EN). An inequality between these two numbers indicates corruption of the shadow register contents (and possible corruption of EEPROM data). The two registers are automatically compared during each Scan operation, with a difference flagged as a PAR fault, or the external microcontroller can compare the two registers. Resetting the device (using the SReset or HReset commands) reloads the shadow registers. A persistent difference between these two register values indicates EEPROM corruption.

All Page 2 registers (device configuration registers) are subject to a checksum calculation. A Calculate Register Checksum command calculates the Page 2 checksum and saves the value internally (it is not accessible). The Calculate Register Checksum command can be run any time, but should be sent whenever a Page 2 register is changed.

A Check Register Checksum command recalculates the Page 2 checksum and compares it to the internal value. The occurrence of a Page 2 checksum error sets the PAR bit in the Fault Status register, sets the $\overline{\text{FAULT}}$ pin low and causes the device to cease any scanning or cell balancing activity. If the device is in Scan Continuous mode, the device also sends a Fault Response. The normal host response to a PAR error is for the host microcontroller to rewrite the Page 2 register contents.

13.3 Fault Diagnostics

The RAA489204 incorporates extensive fault diagnostics functions, summarized in the following tables. The tables show various fault detection mechanisms. Some of these mechanisms are automatically run with no host intervention. Some require only a command from the host to perform the fault check. Others require the host to perform multiple operations and process data to determine a fault. These different fault mechanisms are indicated by columns marked Auto, CMD, and MCU.

The Auto column indicates whether the device automatically scans a particular fault condition. No action is required by the host microcontroller to detect these fault conditions.

The CMD column requires the host microcontroller to send a command to the RAA489204 devices. The command initiates an internal fault check and responds as defined in the table if there is an error.

The MCU column indicates that the fault condition is determined by the host microcontroller performing multiple operations, likely including commands and analysis of the response or register contents.

The Auto, CMD, and MCU columns show either an 'X' or 'O'. An 'X' indicates that this is the primary mechanism for detecting a fault. An 'O' indicates that this is a secondary mechanism.

For most faults, a flag is set and the device takes additional actions. When in Scan Continuous mode, the device automatically sends an unprompted Fault Response when an internal fault is detected. In other fault cases, the RAA489204 sends other types of responses back to the host. These fault responses are summarized in Table 67 and included in Table 68, Table 69, and Table 70.

Table 67. Failure Response Summary

Fault	Flag Set	$\overline{\text{FAULT}}$ Pin	RAA489204 Stops		RAA489204 Enters Sleep Mode	Comms Response
			Balance Operations	Scan Operations		
Open Wire	X	X				[1]
Cell MUX fault	X	X				[1]
TMUX fault	X	X				[1]
External Over-Temperature	X	X				[1]
REG/REF fault	X	X				[1]
EEPROM MISR	X	X				[1]
P1PAR error	X	X				[1]
OV/UV fault detected (after reaching totalizer limit)	X	X	[2]			[1]
Internal Over-Temperature	X	X	[1]	X		[1]
Watchdog Time out	X	X	X	X	X	None
Oscillator fault	X	X	X	X	X	[1]
Communication FIFO fault	X	X				None
Communication CRC fault						NAK
Communication Timeout						Comms Failure

1. If the Scan Continuous operation is active, the device sends to the host an unprompted Fault Response (Fault Status Register read response). If the Scan Continuous operation is inactive, the Fault Response is the first register read in a Page 1 multiple register Read operation.
2. Balance operations do not automatically stop in response to a fault condition unless the device is performing an Autobalance operation or performing any balance operation in conjunction with a Scan Continuous condition.

Table 68. Analog/Mixed Signal Circuits Fault Monitoring

Block	Description	Auto	CMD	MCU	Fault Flags	Test Mechanism	Device Response to a Fault
Open-Wire Circuits	Check Open connections to Cell pins		X	O	OW, OW14-OW0	Checked by sending the Open wire or Scan All commands.	Set $\overline{\text{FAULT}}$ pin low. Fault Response sent during Scan continuous. Otherwise, Fault Response prepended to next Read.
				X		MCU Sends Scan Voltage or Scan All commands and records results. MCU compares these to results of Scan Wires to validate diagnostic.	
	Cell1 Negative Reading			X		MCU Reads the Cell1 voltage. A negative reading is an error and indicates that both VSS and VC0 may be open.	
	Check Open connections to temperature pins		X		OWT1, OWT2, OWT3, OWT4	Automatically checked during Temp Scan.	Set $\overline{\text{FAULT}}$ pin low. Fault Response sent during Scan continuous. Otherwise, Fault Response prepended to next Read.
	Check Open connections to VBAT, VSS pins		X		OVBAT OVSS	Scan Voltages command checks violation and sets fault indication.	Set $\overline{\text{FAULT}}$ pin low. Fault Response sent during Scan continuous. Otherwise, Fault Response prepended to next Read.
ADC	ADC data path			X		MCU sets FFSP or FFSN flags to check that the ADC returns Max or Min values for cell voltages.	Host detects error by checking results
	Maximum Allowable Range Limits			X		MCU checks relevant measurement data against applicable limits to prevent overlap with any diagnostic ranges (for example, FFSP, FFSN, or non overlapping ExTn input ranges).	
Cell/Pack Voltage Readings	Cell under/overvoltage threshold		X	O	OV, UV, OF14-OF1, UF14-UF1	Scan Voltage commands detect fault condition. Device sets fault condition after “Totalizer” number of successive fault conditions.	Set $\overline{\text{FAULT}}$ pin low. Fault Response sent during Scan continuous. Otherwise, Fault Response prepended to next Read. Stop balance during Auto Balance or during Balance plus Scan Continuous operation.
	Cell under/overvoltage threshold MCU test			X		Scan Voltage commands provide MCU with cell voltage values. MCU can compare voltage each scan to defined limits.	
	Pack Compare			X		MCU compares the sum of individual cell readings with the PACK reading. Differences outside a specific range are flagged by MCU as faults.	

Table 68. Analog/Mixed Signal Circuits Fault Monitoring (Cont.)

Block	Description	Auto	CMD	MCU	Fault Flags	Test Mechanism	Device Response to a Fault
Temperature	External temperature limit threshold		X	O	OT, OTF1, OTF2, OTF3, OTF4, G1TF, G2TF	Temperature Scan checks violation of limit and sets fault indication. This is a digital test, so host can check ADC values can confirm operation.	Set $\overline{\text{FAULT}}$ pin low. Fault Response sent during Scan continuous. Otherwise, Fault Response prepended to next Read.
	External Temperature Diagnostic			X		The over-temperature detection system is tested by programming a threshold value that is above the current Ext input voltage values.	Set $\overline{\text{FAULT}}$ pin low. Fault Response sent during Scan continuous. Otherwise, Fault Response prepended to next Read.
	TEMPREG Diagnostic			X		Requires External circuit to apply a voltage divider from TEMPREG to an ExTn or GPIO input. MCU compares voltage input is within range.	
	Non-Overlapping ExTn/GPIO input ranges			X		Requires special external component arrangement designed to provide non-overlapping input ranges e.g. each input is provided with a signal range that does not overlap other ranges.	
	Internal temperature limit threshold		X		OTIT	Temperature or Voltage Scan checks violation of limit and sets fault indication.	Set $\overline{\text{FAULT}}$ pin low. Fault Response sent during Scan continuous. Otherwise, Fault Response perpended to next Read. Stop balance during Auto Balance or during Balance plus Scan Continuous operation. Scan Continuous stops.
	Internal temperature limit threshold diagnostic			X	ITWFG	MCU monitors the ITWG flag to indicate that the internal temperature is nearing an over-temperature limit.	ITWFG flag set
	External Temperature sensor			X		An additional external temperature sensor is required to be added to the circuit. The MCU compares the board mounted sensor temperature with the RAA489204 internal temperature reading.	
AFE-ADC MUX Circuits	Cell input MUX Internal Check		X		CMUX	Cell MUX is checked as part of a normal scan or a Scan Cell MUX command performs check. Device sets fault condition if test fails.	Set $\overline{\text{FAULT}}$ pin low. Fault Response sent during Scan continuous. Otherwise, Fault Response perpended to next Read.

Table 68. Analog/Mixed Signal Circuits Fault Monitoring (Cont.)

Block	Description	Auto	CMD	MCU	Fault Flags	Test Mechanism	Device Response to a Fault
Balance Check	Host MCU performs operations to check balance circuits			X		MCU scans 3 cell balance configurations: Config 1: Cell 1, 4, 7, 10, 13 Config 2: Cell 2, 5, 8, 11, 14 Config 3: Cell 3, 6, 9, 12 Each configuration comprises setting up cell balance registers, waiting 10ms for settling, then scanning cells/reading back cell data.Cell balance registers are reset at the end.	

Auto = Automatic fault detection by RAA489204

CMD = Fault detection following a command from the host. Host reads the response

MCU = Fault detection following multiple host operations and post processing of responses

X = Primary detection method

O = Secondary (optional) method

Table 69. Internal Circuits Fault Monitoring

Block	Description	Auto	CMD	MCU	Fault Flags	Test Mechanism	Device Response to a Fault
Regulators, Reference, Biasing	Second reference		X			Scan voltage returns a value that the host compares to 2.5V.	
	V3P3, V2P5, VCC, VREF power-good range	X		O	REF, REG	Window comparators are always active. A fault shows a failure of regulator or diagnostic circuit.	Set $\overline{\text{FAULT}}$ pin low. Fault Response sent during Scan continuous. Otherwise, Fault Response prepended to next Read.
Oscillators	Internal Oscillators	X		O	OSCF	Device checks two independent oscillators with each other and with an independent timer (continuous check). If diagnostic circuit fails to send a fault when the oscillators are not working, a communication fault is the likely a response to a command.	
Digital Core	TMUX logic (Temperature input MUX) Internal Operation		X	O	TMX	Temperature scans do automatic test of Temp and GPIO (as temp) MUX and checks against limits. Applies known voltages to Ext 1 - 4 and GPIO, during temperature scan and internally checks ADC results for proper operation.	
	Temperature input MUX (TMUX) Diagnostic - MCU Operation			X	TMX	MCU sets TMUX bit and performs Scan Temperature or Scan All, then reads the Temperature registers, comparing the results with expected values.	
	Register Checksum Page 2 registers Setup registers. Subject to CRC content check			X	P1PAR	Check Register Checksum. Checksum is calculated following a CHECK REGISTER CHECKSUM Command. After register change, host needs to send a CALC REGISTER CHECKSUM command to reflect the new register contents.	
	Register Checksum Diagnostic			X	P1PAR	Operation of the register checksum function is checked by the MCU first sending the calculate register checksum command, then changing a register and sending the check register checksum command and reading the fault status register.	

Table 69. Internal Circuits Fault Monitoring (Cont.)

Block	Description	Auto	CMD	MCU	Fault Flags	Test Mechanism	Device Response to a Fault
EEPROM	EEPROM MISR		X		EEPAR	MISR of EEPROM shadow registers is compared with factory programmed EEPROM MISR each Scan Command.	Set $\overline{\text{FAULT}}$ pin low. Fault Response sent during Scan continuous. Otherwise, Fault Response prepended to next Read. Also, numerous potential faults could occur, including ADC and communications
	EEPROM MISR Diagnostic			X		MCU compares EEPROM MISR and EEPROM CALC MISR to confirm automatic comparison is correct.	

Auto = Automatic fault detection by RAA489204

CMD = Fault detection following a command from the host. Host reads the response

MCU = Fault detection following multiple host operations and post processing of responses

X = Primary detection method

O = Secondary (optional) method

Table 70. Communications Circuits Fault Monitoring

Block	Description	Auto	CMD	MCU	Fault Flags	Test Mechanism	Device Response to a Fault
Communications	Communication CRC		X			Commands and responses must have the correct CRC	NAK response or CRC error in Response message
	Communication CRC Diagnostic			X		MCU sends erroneous CRC, expecting a NAK back	NAK response
	Communication Time Out		X			MCU sends a command and a device does not receive an expected response from another device within an expected time limit	Comms Failure response
	Communication Failure, Lack of SPI Response		X	X		An MCU command does not return an expected response within a time window is a communication failure.	
	Measurement Counter		X	X		The MCU checks the Scan Count value following a Voltage Scan command that does not have a response. The Measurement Counter value in the Scan count register increases each time it receives a correct command.	
	Diagnostic Scan Counter		X	X		The MCU checks the Scan Count value following a Scan Temperature, Measure, or Scan Cell MUX command. These do not have a response. The Diagnostic Scan Counter value in the Scan count register increases each time it receives a correct command.	
	Communications FIFO		X	X	BUFFER R, BUFU, BUFO	RAA489204 detects the integrity of the data in the FIFO. A buffer over-run (BUFO) occurs if a FIFO which is already full receives new data which would overwrite existing data, leading to a loss of data. A buffer under-run (BUFU) occurs when the Daisy Chain clocks out data faster than the data is arriving on the SPI.	
	Comms watchdog logic		X	O	WDGF	Valid commands reset watchdog timer. WDGF set if timeout. Host can check the WDG function, by setting the minimum watchdog time, waiting until the timer times out and trying to communicate.	Device goes to sleep on watchdog timeout. Scan and Balance operations stop. WDGF read by host after wake-up.

Auto = Automatic fault detection by RAA489204

CMD = Fault detection following a command from the host. Host reads the response

MCU = Fault detection following multiple host operations and post processing of responses

X = Primary detection method

O = Secondary (optional) method

14. System Registers

System registers contain 16 bits each. All register locations are memory mapped using a 9-bit address. The 3-bit page value makes up the MSBs of the address. Page 1 (3'b001) registers are the measurement result registers for cell voltages and temperatures. Page 3 (3'b011) is used for commands. Pages 1 and 3 are not subject to the checksum calculations. Pages 4 through 7 (3'b100 to 3b'111), are reserved for internal functions.

All Page 2 registers (device configuration registers and EEPROM checksum registers) are subject to a checksum calculation. The checksum is calculated in response to the Calculate Register Checksum command using a Multiple Input Shift Register (MISR) error detection technique. The checksum is tested in response to a Check Register Checksum command (see Memory Checksum).

A description of each register is included in Data Registers. The registers include bit names and initialization alues. Reserved bits (indicated by gray areas) should be ignored when reading and should be set to '0' when writing.

14.1 Data Registers

Cell Setup Register												Access		Read/Write		
Address	9'hxx Addr:			Page (binary)			Register Address (binary)									
	040			001			00 0000									
Description This register selects the cells to be monitored. Set a bit to 1 to disable cell overvoltage, undervoltage, and open wire detection on cells 2 to 14. It should be noted that C1, Bit 0, is NOT writable and is always logic level 0 (that is, it is always enabled). Default value is zero (16'h0000).																
ADDR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
040	Reserved		C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Cell/Pack Voltage Registers				Access	Read Only
	9'hxx Addr		Page (binary)	Register Address (binary)	
Address Range	041 to 071		001	00 0001 to 11 0001	

Description

These registers provide a digital representation of the cell and pack voltages.
The Cell Voltage values are 13 bits plus a sign bit. The PACK value, showing the voltage on the PACK pin, is 14 bits. The voltage values reside in the upper 14 bits of these 16-bit registers. The two LSBs are zero for single sample conversions, but contain residual value for conversions averaged over many cycles, as defined by the CAV[2:0] bits.

Default value after power up and before a scan is zero: (16'h0000)

ADDR		
041	**Cell 1 Voltage**	$if...HEXvalue_{10} \geq 32768 \rightarrow VCx = \frac{(HEXvalue_{10} - 65536) \times 2 \times 2.5}{8192 \times 4}$ $else \rightarrow VCx = \frac{HEXvalue_{10} \times 2 \times 2.5}{8192 \times 4}$ $PACK(V) = \frac{HEXvalue_{10} \times 31.45728 \times 2.5}{16384 \times 4} = HEXvalue_{10} \times 0.0012$ **$HEXvalue_{10}$ = Hex to Decimal conversion of the 16-bit register contents.**
042	**Cell 2 Voltage**	
043	**Cell 3 Voltage**	
044	**Cell 4 Voltage**	
045	**Cell 5 Voltage**	
046	**Cell 6 Voltage**	
047	**Cell 7 Voltage**	
048	**Cell 8 Voltage**	
049	**Cell 9 Voltage**	
04A	**Cell 10 Voltage**	
04B	**Cell 11 Voltage**	
04C	**Cell 12 Voltage**	
04D	**Cell 13 Voltage**	
04E	**Cell 14 Voltage**	
050	**PACK Voltage**	

Internal Temperature Reading				Access	Read Only
Address Range	9'hxx Addr		Page (binary)	Register Address (binary)	
	060		001	10 0000	

Description
The Internal temperature reading is in degrees Kelvin.

ADDR			
060	**IT**	$Internaltemp\ (°C) = \frac{HEXvalue_{10}}{128} - 273$	**$HEXvalue_{10}$ = Hex to Decimal conversion of the register contents.**

External Temperature Voltages				Access	Read Only
Address Range	9'hxx Addr	Page (binary)	Register Address (binary)		
	060 to 064	001	10 0000 to 10 0100		

Description
The External temperature values reside in these 16-bit registers. The two LSBs are zero for single sample conversions, but contain residual value for conversions averaged over many cycles, as defined by the [TAV2:0] bits. The returned value is the voltage read on the external temperature ExTn pin. The temperature measurement depends on the external components.

ADDR			
061	ExT1 Voltage	$Vtemp = \frac{HEXvalue_{10} \times 2.5}{16384 \times 4}$	$HEXvalue_{10}$ = Hex to Decimal conversion of the register contents.
062	ExT2 Voltage		
063	ExT3 Voltage		
064	ExT4 Voltage		

GPIO Voltages				Access:	Read Only
Address Range:	9'hxx Addr:	Page (binary)	Register Address (binary)		
	067 to 068	001	10 0111 to 10 1000		

Description
The External GPIO values reside in these 16-bit registers. The two LSBs are zero for single sample conversions but contain residual value for conversions averaged over many cycles, as defined by the [TAV2:0] bits. The returned value is the voltage read on the general purpose GPIO1 and GPIO2 pins. When configured as temperature inputs, the temperature measurement depends on the external components.

ADDR			
067	GPIO1 Voltage	$Vgpio = \frac{HEXvalue_{10} \times 2.5}{16384 \times 4}$	$HEXvalue_{10}$ = Hex to Decimal conversion of the register contents.
068	GPIO2 Voltage		

Reference Voltage				Access:	Read Only
Address Range:	9'hxx Addr:	Page (binary)	Register Address (binary)		
	070	001	11 0000		

Description
The voltage reference value resides in the upper 14 bits. The lower 2 LSBs are zero.

ADDR			
070	Reference Voltage	$Vref = \frac{HEXvalue_{10} \times 5}{16384 \times 4}$	$HEXvalue_{10}$ = Hex to Decimal conversion of the register contents.

Scan Count Register				Access:	Read Only
Address Range:	9'hxx Addr:	Page (binary)	Register Address (binary)		
	071	001	11 0001		

Description
This register contain counters for Scan and Diagnostic operations.

ADDR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
071	Reserved		DSN5	DSN4	DSN3	DSN2	DSN1	DSN0	Reserved		MSN5	MSN4	MSN3	MSN2	MSN1	MSN0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MSN0 to MSN5	The Measurement Scan Counter (MSN5:MSN0) increments each time a measurement scan command completes and the registers load. The value wraps to zero when overflowed.
DSN0 to DSN5	The Diagnostic Scan Counter (DSN5:DSN0) counts completed diagnostic activity. The Scan Count Register can be compared to previous value to confirm diagnostic scan operations are complete.

14.2 Fault Status and Setup Registers

Fault Status Register																Access:	Read/Write
Address Range:	9'hxx Addr:						Page (binary)									Register Address (binary)	
	080						010									00 0000	

Description

A fault condition exists, and the $\overline{\text{FAULT}}$ pin is asserted Low if any bits in the Fault Status register are set to '1'. (The $\overline{\text{FAULT}}$ pin logic output is a NOR function of the bits in this register.)

Bits in the Fault Status register (other than OW, OV, UV, OT, PAR, and BUFERR) are reset by writing a '1' to each bit position that is set, or write 16'hFFFF regardless of the bits that are set. Alternatively, these register bits can be cleared by a direct write operation. A direct write starts with an Override Clear on Write command followed by a Write command with data in the command replacing the register contents. Clear all bits in a direct write with a data value of 16'h0000. *Note:* The OW, OV, UV, OT, PAR, and BUFERR bits are only reset by clearing bits in the other associated fault registers.

ADDR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
080	ITWFG	CMX	TMX	REG	REF	PAR	OVSS	OVBAT	OW	UV	OV	OT	WDGF	OSCF		BUFERR
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BUFERR	**Buffer Error flag.** The BUFERR bit is set to '1' if a Memory Buffer under-run or overrun condition is detected and is a logical OR of the BUFU and BUFO bits in the General Fault register. Reset the BUFO and BUFU bits to '0' to reset BUFERR bit to '0'. This bit cannot be set or cleared by a write to this register if the BUFU or BUFO are set.
OSCF	**Oscillator fault bit.** The OSCF bit is set to '1' in response to a fault on any on-chip oscillator. Reset the OSCF bit to '0' with a write of 16'h0004 or 16'hFFFF to this register. This bit can be set to '1' by a direct write to this register and this results in a fault condition.
WDGF	**Watchdog timeout fault.** The WDFG bit is set in response to a watchdog timeout. Reset the WDGF bit to '0' with a write of 16'h0008 or 16'hFFFF to this register. This bit can be set to '1' by a direct write to this register and this results in a fault condition.
OT	**Over-temperature fault.** The OT bit is a logical 'OR' of over-temperature fault bits: OTF1 to OTF4, G1TF/G2TF and OTIT. Clearing the over-temperature bits in the Over-temperature Fault register clears the OT bit. Setting any over-temperature bits in the Over-Temperature Fault register sets the OT bit and this results in a fault condition. OT cannot be set or cleared by a write to this register.
OV	**Overvoltage fault.** The OV bit is a logical 'OR' of Overvoltage fault bits: OF1 to OF14. Clearing the bits in the Overvoltage Fault register clears the OV bit. Setting any bit in the Overvoltage Fault register sets the OV bit and this results in a fault condition. OV cannot be set or cleared by a write to this register.
UV	**Undervoltage fault.** The UV bit is a logical 'OR' of Undervoltage fault bits: UF1 to UF14. Clearing the bits in the Undervoltage Fault register clears the UV bit. Setting any bit in the Undervoltage Fault register sets the UV bit and this results in a fault condition. UV cannot be set or cleared by a write to this register.
OW	**Open-Wire fault.** The OW bit is a logical 'OR' of open-wire fault bits: OW0 to OW14. Clearing the bits in the Open-Wire Fault register clears the OW bit. Setting any bit in the Open-Wire Fault register sets the OW bit. OW cannot be set or cleared by a write to this register.
OVBAT	**Open-Wire fault on VBAT connection.** The OVBAT bit is set to '1' when a fault is detected. Reset the OVBAT bit to '0' with a write of 16'h0100 or 16'hFFFF to this register. This bit can be set to '1' by a direct write to this register and this results in a fault condition.

Fault Status Register			Access:	Read/Write
080 (Cont.)	OVSS	**Open-Wire fault on VSS connection.** The OVSS bit set to ‘1’ when a fault is detected. Reset the OVSS bit to ‘0’ with a write of 16’h200 or 16’hFFFF to this register. This bit can only be set to ‘1’ by a direct write to this register and this results in a fault condition.		
	PAR	**Register checksum (Parity) error.** The PAR bit is a logical ‘OR’ of the P1PAR and the EEPAR bits. Clearing the P1PAR and EEPAR bits in the General Fault register clears the PAR bit. Setting either P1PAR or EEPAR in the General Fault register sets the PAR bit and this results in a fault condition. PAR cannot be set or cleared by a write to this register.		
	REF	**Voltage reference fault.** The REF bit is set to ‘1’ if the voltage reference value is outside its power-good range. Reset the REF bit to ‘0’ with a write of 16’h0800 or 16’hFFFF to this register. This bit can be set to ‘1’ by a direct write to this register and this results in a fault condition.		
	REG	**Voltage regulator fault.** The REG bit is set if a voltage regulator value (V3P3, VCC or V2P5) is outside its power-good range. Reset the REG bit to ‘0’ with a write of 16’h1000 or 16’hFFFF to this register. This bit can be set to ‘1’ by a direct write to this register and this results in a fault condition.		
	TMX	**Temperature multiplexer error.** The TMX bit is set if the temperature MUX test detects a fault. Reset the TMX bit to ‘0’ with a write of 16’2000 or 16’hFFFF to this register. This bit can be set to ‘1’ by a direct write to this register and this results in a fault condition.		
	CMX	**Cell multiplexer error.** The CMX bit is set if the cell MUX test detects a fault. Reset the CMX bit to ‘0’ with a write of 16’h4000 or 16’hFFFF to this register. This bit can be set to ‘1’ by a direct write to this register and this results in a fault condition.		
	ITWFG	**IC Temperature Flag.** The ITWFG bit is set if the IC temperature exceeds the value contained in the Internal Temp Warning register. Reset the ITWFG bit to ‘0’ with a write of 16’h8000 or 16’hFFFF to this register. This bit can be set to ‘1’ by a direct write to this register and this results in an Internal Temperature Warning condition. The ITWFG bit provides the system a possible warning signal before the device reaches its normal over-temperature condition and allows the user to adjust to the system to prevent further temperature rise rather than just waiting for a temperature shutdown condition.		

Overvoltage Fault Register				Access:	Read/Write
Address Range:	9’hxx Addr:		Page (binary)	Register Address (binary)	
	081		010	00 0001	

Description

Overvoltage fault on cells 14 to 1 correspond with bits OF14 to OF1, respectively. Default values are all zero. Bits are set to ‘1’ when faults are detected.

The contents of this register can be reset using register Write (16’hFFFF). Alternatively, these register bits can be cleared by a direct write operation. A direct write starts with an Override Clear on Write command followed by a Write command with data in the command replacing the register contents. Clear all bits in a direct write with a data value of 16’h0000.

Clearing this register does not reset the associated totalizer value, so the totalizer count is 1 and there is no filtering once a fault is detected. For example, once cleared, the OFn bit is set again if the next sample also shows an overvoltage condition. Remember to reset the TOT bits after clearing this register.

ADDR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
081	Reserved		OF14	OF13	OF12	OF11	OF10	OF9	OF8	OF7	OF6	OF5	OF4	OF3	OF2	OF1
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Undervoltage Fault Register				Access:	Read/Write
Address Range:	9'hxx Addr:		Page (binary)	Register Address (binary)	
	082		010	00 0010	

Description

Undervoltage fault on cells 12 to 1 correspond with bits UF12 to UF1, respectively. Default values are all zero. Bits are set to 1 when faults are detected.

The contents of this register can be reset using register Write (16'hFFFF). Alternatively, these register bits can be cleared by a direct write operation. A direct write starts with an Override Clear on Write command followed by a Write command with data in the command replacing the register contents. Clear all bits in a direct write with a data value of 16'h0000.

Clearing this register does not reset the associated totalizer value, so the totalizer count is 1; and, there is no filtering. For example, once cleared, the UFn bit is set again if the next sample also shows an undervoltage condition. Remember to reset the TOT bits after clearing this register.

ADDR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
082	Reserved		UF14	UF13	UF12	UF11	UF10	UF9	UF8	UF7	UF6	UF5	UF4	UF3	UF2	UF1
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Open-Wire Fault Register				Access:	Read/Write
Address Range:	9'hxx Addr:		Page (binary)	Register Address (binary)	
	083		010	00 0011	

Description

Open-Wire fault on Pins VC14 to VC0 correspond with bits OW14 to OW0, respectively. Default values are all zero. Bits are set to 1 when faults are detected.

The contents of this register can be reset using register Write (16'hFFFF). Alternatively, these register bits can be cleared by a direct write operation. A direct write starts with an Override Clear on Write command followed by a Write command with data in the command replacing the register contents. Clear all bits in a direct write with a data value of 16'h0000.

ADDR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
083		OW14	OW13	OW12	OW11	OW10	OW9	OW8	OW7	OW6	OW5	OW4	OW3	OW2	OW1	OW0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Over-Temperature Fault Register				Access:	Read/Write
Address Range:	9'hxx Addr:		Page (binary)	Register Address (binary)	
	084		010	00 0100	

Description

Over-temperature fault on ExT4 to ExT1 correspond with bits OTF4 to OTF1, respectively. Over Internal Temperature fault corresponds to the OTIT bits. Default values are all zero. Bits are set to 1 when fault are detected.

The contents of this register can be reset using register Write (16'hFFFF). Alternatively, these register bits can be cleared by a direct write operation. A direct write replaces the register contents by the Write command data. A direct write to clear the register starts with the Override Clear on Write command followed by a Write command with a data value of 16'h0000.

ADDR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
084	Reserved			OWT4	OWT3	OWT2	OWT1	G2TF	G1TF	Reserved		OTF4	OTF3	OTF2	OTF1	OTIT
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

OTIT	**Internal over-temperature fault.** Bit set to 1 when a fault is detected.
OTF4, OTF3, OTF2, OTF1	**External over-temperature fault bits** for ExT1 to ExT4 pins (respectively). Set TSTE1 to TSTE4 bits to enable the test of the ExTn voltage against the temperature limit. Bit set to 1 when a fault is detected.
G2TF, G1TF	**External over-temperature fault bits** for GPIO1 and GPIO2. Set the G1MOD, G2MOD bits in the Device Setup 1 register to 0 to set these ports as inputs and set the TSTG1 and TSTG2 bits in the Fault Setup register to 1 to automatically test the GPIO input voltage against a temperature limit. Bit set to 1 when a fault is detected.
OWT4, OWT3, OWT2, OWT1	**Open input Fault on ExT1 to ExT4** (respectively.) Bit set to 1 when a fault is detected.

General Fault Register													Access:		Read/Write	
Address Range:	9'hxx Addr:			Page (binary)		Register Address (binary)										
	085			010		00 0101										

Description
Default values are all zero. Bits are set to 1 when a fault is detected.
The contents of this register can be reset using register Write (16'h000F). Alternatively, these register bits can be cleared by a direct write operation. A direct write replaces the register contents by the Write command data. A direct write to clear the register starts with the Override Clear on Write command followed by a Write command with a data value of 16'h0000.

ADDR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
085	Reserved												P1PAR	EEPAR	BUFO	BUFU
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BUFU	**Buffer under run flag.** Set if a Memory Buffer underrun condition is detected.
BUFO	**Buffer over run flag.** Set if a Memory Buffer overrun condition is detected.
EEPAR	**EEPROM Checksum Parity Error.** The EEPAR bit is set in response to a register checksum error or to an EEPROM MISR checksum error. The EEPROM MISR checksum error is calculated automatically following the execution of a scan command and the result is compared with the value stored in the EEPROM. The PAR bit is then set if the two results are not equal.
P1PAR	**Register Checksum Parity Error.** The P1PAR bit is set in response to the Check Register Checksum command if the calculated and stored register checksums do not match. The register checksum is calculated after a register change by the Calculate Register Checksum command and acts on the contents of all page 2 registers. The Check Register Checksum command is used to repeat the calculation and compare the results to the stored value.

Fault Setup Register												Access:		Read/Write	
Address Range:	9'hxx Addr:			Page (binary)		Register Address (binary)									
	086			010		00 0110									

Description
These bits control various fault configurations.
Default values are shown below, as are descriptions of each bit.

ADDR	15	14	11	10	11	10	9	8	7	6	5	4	3	2	1	0
086	TSTG2	TSTG1	Reserved		TSTE4	TSTE3	TSTE2	TSTE1	TSTIT	TOT2	TOT1	TOT0	SCN3	SCN2	SCN1	SCN0
	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0

SCN0 SCN1 SCN2 SCN3	**Scan interval code.** Decoded to provide the scan interval setup for the Scan Continuous function. Initialized to 1000 (4096ms scan interval). SCN3-0 is decoded into a binary timing sequence with value: 16ms * 2^BIN2DEC(SCN3-0), for example, 0000 = 16ms and 1100 = 65536ms. See Table 24.
TOT0 TOT1 TOT2	**Fault totalize code bits.** Decoded to provide the required fault totalization. An unbroken sequence of positive fault results equal to the totalizer amount is needed to verify a fault condition. Initialized to 011 (8 sample totalizing.) TOT2-0 is decoded into a binary sequence with 000 = 1, 001 = 2, 010 = 4, etc. The maximum totalizer count is then 111 = 128. See Table 20. Rewrite this register following an error detection resulting from totalizer overflow.
TSTIT	**Internal Temperature limits.** Set bit to 1 to stop internal orations in response to an Internal Temperature violation. Set to 0 to NOT stop internal operations in response to an Internal Temperature Limit violation (not recommended). Initialized to 1 (on).
TSTE1 TSTE2 TSTE3 TSTE4	**External temperature limits on inputs ExT1 to ExT4,** respectively. Set bit to 1 to enable the corresponding temperature test. If set, values below the External temp limit register value is flagged as a temperature fault. Set to 0 to disable the over-temperature detection and allows external inputs to be used for general voltage monitoring without imposing a limit value. TST1 to TST6 are initialized to 0 (off).
TSTG1 TSTG2	**External temperature limits for GPIO inputs 1 and 2.** Set bit to 1 to enable the corresponding temperature test. GPIO voltages below the External Temperature Limit register value are flagged as a temperature fault if the corresponding TSTGn bit is set. Set TSTGn to 0 to disable temperature testing. These bits are initialized to 0 (off). The value of TSTGn is ignored if the corresponding GPIO is set to output mode.

Overvoltage Limit Value				Access:	Read/Write
Address Range:	9'hxx Addr:		Page (binary)	Register Address (binary)	
	087		010	00 0111	

Description
This Overvoltage limit is compared to the measured values for cells 1 to 14 to test for an overvoltage condition.
Bit 0 is the LSB, Bit 15 is the MSB (sign). For normal operation (positive input voltage) set Bit 15 to 0.

ADDR			
087	**Overvoltage Limit Value**	$OV_{VAL} = \left[\frac{OV_{TH} \times 8192 \times 4}{2 \times 2.5}\right]_{HEX}$	OV_{TH} = Desired Overvoltage Threshold (Volts) OV_{VAL}= Stored Overvoltage Value (HEX) Default = 16'h7FFF

Undervoltage Limit Value				Access:	Read/Write
Address Range:	9'hxx Addr:		Page (binary)	Register Address (binary)	
	088		010	00 1000	

Description
This Undervoltage limit is compared to the measured values for cells 1 to 14 to test for an undervoltage condition.
Bit 0 is the LSB, Bit 15 is the MSB (sign). For normal operation (positive input voltage) set Bit 15 to 0.

ADDR			
088	**Undervoltage Limit Value**	$UV_{VAL} = \left[\frac{UV_{TH} \times 8192 \times 4}{2 \times 2.5}\right]_{HEX}$	UV_{TH} = Desired Undervoltage Threshold (Volts) UV_{VAL}= Stored Undervoltage Value (HEX) Default = 16'h0000

External Temperature Limit Value				Access:	Read/Write
Address Range:	9'hxx Addr:		Page (binary)	Register Address (binary)	
	089		010	00 1001	

Description
The over-temperature limit is compared to the measured values for ExT1 to ExT4 to test for an over-temperature condition at any input. The temperature limit assumes NTC temperature measurement devices (that is, an over-temperature condition is indicated by a temperature reading below the limit value). Temperature register values below this limit cause the respective bits (OTF1 to 4) to be set in the Over-temperature Fault register.
Bit 0 is the LSB, Bit 15 is the MSB.

ADDR			
089	**External Temperature Limit Value**	$ExOT_{VAL} = \left[\frac{XOT_{TH} \times 16384 \times 4}{2.5}\right]_{HEX}$	XOT_{TH} = Desired External Temperature Threshold (Volts) $ExOT_{VAL}$= Stored External Temperature Voltage Value (HEX) Default = 16'h0000

$\overline{\text{FAULT}}$ Pin Mask Register				Access:	Read/Write
Address Range:	9'hxx Addr:		Page (binary)	Register Address (binary)	
	08A		010	00 1010	

Description
Determines which bits in the Fault Status Register are NORed to cause the $\overline{\text{FAULT}}$ pin to assert.
Bits correspond to the bits in the Fault Status register. Set bit to 1 to prevent this bit being included in the NOR function.
Default value is zero (16'h0000).

ADDR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
08A	ITWFG	CMX	TMX	REG	REF	PAR	OVSS	OVBAT	OW	UV	OV	OT	WDGF	OSCF	Reserved	BUFF
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIO1 Pin Mask Register												Access:		Read/Write	
Address Range:	9'hxx Addr:		Page (binary)		Register Address (binary)										
	08B		010		00 1011										

Description
Determines which bits in the Fault Status register are ORed to cause GPIO1 pin to assert. (GPIO1 needs to be selected as an output). Bits correspond to the bits in the Fault Status register. Set bit to 1 to prevent this bit being included in the OR function.
Default value is zero (16'h0000).

ADDR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
08B	ITWFG	CMX	TMX	REG	REF	PAR	OVSS	OVBAT	OW	UV	OV	OT	WDGF	OSCF	Reserved	BUFF
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Internal Temperature Warning Value						Access:	Read/Write
Address Range:	9'hxx Addr:		Page (binary)		Register Address (binary)		
	08C		010		00 1100		

Description
The Over-temperature warning threshold is compared to the Internal Temperature reading to test for a warning condition. Temperature values above the warning level cause the ITWFG bit to be set in the Fault Status register and the device sends a Fault Response message to the host. If the $\overline{FAULT}$ pin Mask bit (ITWFG) is '0', the device also sets the $\overline{FAULT}$ pin Low.
Bit 0 is the LSB, Bit 15 is the MSB.

ADDR			
08C	**Internal Temperature Warning Value**	$IOTWVAL = [(IOTWTH + 273) \times 128]_{HEX}$	IOTWTH = Desired Internal Temperature Threshold (°C) IOTWVAL= Stored Internal Temperature Voltage Value (HEX) Default = 16'hFFFF

Internal Temperature Limit Value						Access:	Read Only
Address Range:	9'hxx Addr:		Page (binary)		Register Address (binary)		
	08D		010		00 1101		

Description
Over-temperature limit is compared to the output register value for internal temperature. to test for an over-temperature condition. Temperature values above the limit level cause the OTIT bit to be set in the Over-temperature Fault register and the OT fault bit in the Fault Status register. The device stops all activity and sends a Fault Response message to the host. If the $\overline{FAULT}$ Pin Mask bit (OT) is '0', the device also sets the $\overline{FAULT}$ pin Low.
Bit 0 is the LSB, Bit 15 is the MSB. This register is factory programmed to 16'hCE1B (~139.2degC). For a different limit value contact Renesas.

ADDR			
08D	**Internal Temperature Limit Value**	$IOTLTH(°C) = \frac{IOTLVAL_{10}}{128} - 273$	IOTLTH = Internal Temperature Threshold (°C) IOTLVAL= Stored Internal Temperature Voltage Value (HEX) Default = 16'hCE1B

Cell Balance Enabled Status Register						Access:	Read Only
Address Range:	9'hxx Addr:		Page (binary)		Register Address (binary)		
	08E		010		00 1110		

Description
This register reports the current condition of the cell balance outputs of cell 1 to cell14 (respectively). '1' indicates balancing is enabled for this cell. '0' indicates that balancing is turned off.
Default value is zero (16'h0000).

ADDR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
08E	Reserved		CBEN 14	CBEN 13	CBEN 12	CBEN 11	CBEN 10	CBEN 8	CBEN 8	CBEN 7	CBEN 6	CBEN 5	CBEN 4	CBEN 3	CBEN 2	CBEN 1
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Cell Balance Setup Register												Access:		Read/Write			
Address Range:	9'hxx Addr:							Page (binary)		Register Address (binary)							
	090							010		01 0000							
Description Default values are shown below, as are descriptions of each bit.																	
ADDR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
090	Reserved							IBAL	EOB	BDDS	BEN	BWT2	BWT1	BWT0	BMD1	BMD0	
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	BMD1, BMD0		Balance mode. These bits set balance mode.														
			BMD1	BMD0	Mode												
			0	0	OFF												
			0	1	Manual												
			1	0	Timed												
			1	1	Auto												
	BWT2, BWT1, BWT0		Balance wait time. Register contents are decoded to provide the required wait time between device balancing. This is to assist with thermal management and is used with the Auto Balance mode. Balance wait time is encoded as a binary series from 0 - 64s. For example, 000 = 0s, 001 = 1s, 010 = 2s, 011 = 4s, 100 = 8s etc.														
	BEN		Balance enable. Set to '1' to enable balancing. '0' inhibits balancing. Setting or clearing this bit does not affect any other register contents. Balance Enable and Balance Inhibit commands are provided to allow control of this function without requiring a register Write. These commands have the same effect as setting this bit directly. This bit is cleared automatically when balancing is complete and the EOB bit is set (see Balance Enable (Address: CAH)).													
	BDDS		Balance condition during measurement. Controls the balance condition in Scan Continuous mode and any Balance mode. Set to 1 to have balancing functions turned off 10ms before and during cell voltage measurement. Set to 0 for normal operation (balancing functions not affected by measurement).														
	EOB		End Of Balance. The device sets this bit when balancing is complete. This function is used in the Timed Balance mode and Auto Balance mode. The BEN bit is cleared as a result of this bit being set. Initialized to 0.														
	IBAL		Internal Balance. Set this bit to '1' to enable internal balancing. Set this bit to '0' to enable External Balance. Initialized to 0.														

Watchdog/Balance Time Register												Access:		Read/Write			
Address Range:	9'hxx Addr:							Page (binary)		Register Address (binary)							
	091							010		01 0001							
Description Default values are shown below, as are descriptions of each bit.																	
ADDR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
091	Reserved	BTM6	BTM 5	BTM 4	BTM 3	BTM 2	BTM 1	BTM 0	WDG7	WDG6	WDG5	WDG4	WDG3	WDG2	WDG1	WDG0	
	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	
	WDG0 to WDG7		Watchdog timeout setting. Decoded to provide the time out value for the watchdog function. See Watchdog Function for details. The watchdog can only be disabled (set to 8'h00) if the watchdog password is set. The watchdog setting can be changed to a nonzero value without writing to the watchdog password. Initialized to 8'h3F (63 seconds).														
	BTM0 to BTM6		Balance timeout setting. Decoded to provide the time out value for Timed Balance mode and Auto Balance mode. The Balance on time is programmable in 20 sec intervals from 20 seconds (0000001) to 42.33 minutes (1111111) using bits BTM[6:0]. A setting of 0000000 disables balancing in Auto and Timed modes. Initialized to 7'00 (Disabled).														

Device Setup 1 Register												Access:		Read/Write		
Address Range:	9'hxx Addr:			Page (binary)		Register Address (binary)										
	092			010		01 0010										
Description Default values are shown below, as are descriptions of each bit.																
ADDR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
092	Reserved		CMX 1P2M	NO_ TREG	WP5	WP4	WP3	WP2	WP1	WP0	WSCN	SCAN	G2 FUNC	G1 FUNC	G2 MOD	G1 MOD
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	G1MOD G2MOD		**GPIO Port Mode Select.** This bit sets the operation of the GPIO port. G1MOD, G2MOD = 0 Selects Input G1MOD, G2MOD = 1 Selects Output													
	G1FUNC		**GPIO1 Port Output Function.** This bit activates the Special Output Function for the GPIO1 Port. G1FUNC = 0; Normal Output Operation G1FUNC = 1; Special Output. GPIO1 Outputs result of NORing all Fault Status bits, Output selected by the GPIO Fault Mask.													
	G2FUNC		**GPIO2 Port Output Function.** This bit activates the Special Output Functions for the GPIO2 Port. G2FUNC = 0; Normal Output Operation G2FUNC = 1; GPIO2 Special Output signal selected by G2F[4:1] bits (Device Setup 2 Register).													
	SCAN		**Scan Continuous mode.** This bit is set in response to a Scan Continuous command and cleared by a Scan Inhibit command. It can also be set/cleared by writing to the bit.													
	WSCN		**Set wire scan current on time.** Set to '0' for 1.5ms on time. Set to '1' for 5ms on time.													
	WP5:0		**Watchdog disable password.** Set these bits to 6'h3A (111010) before the watchdog can be disabled. Disable watchdog by writing 8'h00 to the watchdog bits WDG0 - WDG7 in Watchdog/Balance Time Register.													
	NO_TREG		**No Temp Reg Output.** This bit, when set to '1' turns off the TEMPREG output during Measure Temperature Command Only.													
	CMX1P2M		**Scan Cell MUX timing.** Set to **'0'**, Scan Cell MUX bias current is on for 0.5ms Set to **'1'**, Scan Cell MUX bias current is on for 1.25ms.													

Device Setup 2 Register												Access:		Read/Write		
Address Range:	9'hxx Addr:			Page (binary)		Register Address (binary)										
	093			010		01 0011										

Description
Default values are shown below, as are descriptions of each bit.

ADDR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
093	FFSN	FFSP	TMUX	DP2	G2F4	G2F3	G2F2	G2F1	G2VAL	G1VAL	TAV2	TAV1	TAV0	CAV2	CAV1	CAV0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CAV2, CAV1, CAV0	**Cell averaging function setup.** See Cell Voltage Averaging Default value is 0 (no averaging).
TAV2, TAV1, TAV0	**Temperature averaging function setup.** See Temperature Voltage Averaging Default value is 0 (no averaging).
G1VAL	**GPIO1 Output Value.** When the G1MOD bit = '1' and the G1FUNC bit is set to '0', the GPIO1 pin output reflects the setting of this bit. G1VAL" = '1', GPIO1 pin = High. G1VAL" = '0', GPIO1 pin = Low.
G2VAL	**GPIO2 Output Value.** When the G2MOD bit = '1' and the G2FUNC bit is set to '0' (or in cases of the GPIO2 Special Output settings), the GPIO2 pin output reflects the setting of this bit. G2VAL" = '1', GPIO2 pin = High. G2VAL" = '0', GPIO2 pin = Low.
G2F1 G2F2 G2F3 G2F4	**GPIO2 Mode Select.** These bits select the special output function of the GPIO2 pin, when the G2MOD bit = '1' and the G2FUNC bit is set to '1'

G2F4	G2F3	G2F2	G2F1	Operation
0	0	0	0	Output controlled by G2VAL bit.
0	0	0	1	Output is a short pulse at the start of the voltage measurement part of the scan operation.
0	0	1	0	Output is a long pulse with a rising edge at the start of the voltage measurement part of the scan operation and a falling edge at the end of the measurement.
Other Combinations				Output controlled by G2VAL bit.

DP2	**Daisy Chain Upper Port function.** This bit is set to '1' to disable the Daisy Chain upper port. Default is 0 (Daisy Chain upper port enabled). See Daisy Chain Upper Port Control.
TMUX	TMUX Control bit.
FFSP	**Force ADC input to Full Scale Positive.** All cell scan readings forced to 16'h7FFC. All temperature scan readings forced to 16'hFFFC. *Note:* These values are each shifted left by two bits when loaded to the output registers.
FFSN	**Force ADC input to Full Scale Negative.** All cell scan readings forced to 16'h8000. All temperature scan readings forced to 16'h0000. *Note:* These values are each shifted left by two bits when loaded to the output registers
Note: The ADC input functions normally if both FFSN and FFSP are set to '1', but this setting is not supported.	

User Registers					Access:	Read/Write
Address Range:	9'hxx Addr:		Page (binary)	Register Address (binary)		
	094 to 095		010	01 0100		

Description
32 bits of register space available for user data. The contents have no effect on the operation of the RAA489204.
These registers are included in the register checksum function.

ADDR		
094	**User Register 1**	16 bits of register space available for user data. Default value 16'h0000.
095	**User Register 2**	16 bits of register space available for user data. Default value 16'h0000.

Comms Setup Register												Access:		Read Only	
Address Range:	9'hxx Addr:			Page (binary)		Register Address (binary)									
	096			010		01 0110									

Description
This register provides state of communications and Daisy Chain conditions.

ADDR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
096	CRAT1	CRAT0	0	CMOD	SIZE4	SIZE3	SIZE2	SIZE1	SIZE0	ADD4	ADD3	ADD2	ADD1	ADD0	1	DR MODE

DRMODE	**DataReady Mode.** Indicates the condition of the DTRDYMODE pin (pin 46 on the 64 pin parts).
ADD0 ADD1 ADD2 ADD3 ADD4	**Device stack address.** The stack address (device position in the stack) is determined automatically by the device in response to a "Roll Call" command. The resulting address is stored in ADD[4:0} and is used internally for communications paring and sequencing. The stack address can be read by the user but not written.
SIZE0 SIZE1 SIZE2 SIZE3 SIZE4	**Device stack size** (Top stack device address). Corresponds to the number of devices in the stack. The stack size is determined automatically by the stack devices in response to an "Roll Call" command. The resulting number is stored in SIZE[4:0] and is used internally for communications paring and sequencing. The stack size can be read by the user but not written.
CMOD	**Comm Mode:** A '1' indicates SPI communications. A '0' indicates a Daisy Chained device.
CRAT0 CRAT1	**Communications rate bits.** These bits reflect the state of the COMMRATE0, COMMRATE1 pins and determine the bit rate of the Daisy Chain communications system. See Table 12.

Serial Number				Access:	Read Only
Address Range:	9'hxx Addr:		Page (binary)	Register Address (binary)	
	097 to 099		010	01 0111 to 01 1001	

Description
The 48b serial number programmed in nonvolatile memory during factory test is mirrored to these 3 x 16 bit registers. The serial number can be read at any time but can not be written.

ADDR		
097	**Serial Number 1**	User Serial Number[15:0]
098	**Serial Number 2**	User Serial Number[31:16]
099	**Serial Number 3**	User Serial Number[47:32]

Trim Voltages												Access:		Read Only	
Address Range:	9'hxx Addr:			Page (binary)		Register Address (binary)									
	09A			010		01 1010									

Description
The nominal cell voltage is programmed into nonvolatile memory during factory test and loaded to the Trim Voltage register at power-up.

ADDR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
09A	Reserved								TV7	TV6	TV5	TV4	TV3	TV2	TV1	TV0
	0	0	0	0	0	0	0	0								

TV7:0	**Trim voltage.** The nominal value is a 8-bit representation of the 0V to 5V cell voltage input range with 50 (6'h32) representing 5V (for example, LSB = 0.1V). The parts are additionally marked with the trim voltage by the addition of a two digit code to the part number. For example, 3.3V is denoted by the code 33. (1 bit per 0.1V of trim voltage, so 0 to 50 decimal covers the full range.)

Cell Fault Mask Register				Access:	Read/Write
Address Range:	9'hxx Addr:		Page (binary)	Register Address (binary)	
	09B		010	01 1011	

Description

This register masks off any overvoltage or undervoltage fault conditions for Cell 2 to Cell14 (respectively). '1' indicates the faults are disabled for this cell. '0' indicates that fault testing is ON. The main use of this register is to prevent faults on cells that are designated as "bus bars", which may be low voltage or negative. Cell1 cannot be masked.

Default value is zero (16'h0000).

ADDR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
09B	Reserved		CFM 14	CFM 13	CFM 12	CFM 11	CFM 10	CFM 9	CFM 8	CFM 7	CFM 6	CFM 5	CFM 4	CFM 3	CFM 2	CFM 1
			0	0	0	0	0	0	0	0	0	0	0	0	0	0

MISR Checksum Registers				Access:	Read Only
Address Range:	9'hxx Addr:		Page (binary)	Register Address (binary)	
	09C to 09E		010	01 1100 to 01 1110	

Description

The 24-bit CALCULATED EEPROM MISR CHECKSUM value is calculated on the contents of the shadow registers each time the shadow registers are loaded from EEPROM. The resulting number must equal the factory programmed 24-bit EEPROM MISR CHECKSUM value to ensure no data corruption of the shadow register space. This check is performed automatically with each scan. Additionally, the check my be performed manually by the user comparing the contents of MISR EEPROM CHECKSUM and the CALCULATED MISR EEPROM CHECKSUM values.

ADDR																
09C	EEPROM MISR CHECKSUM [15:0] This is the lower 16 bits of the factory programmed EEPROM MISR checksum value.															
09D	CALCULATED EEPROM MISR CHECKSUM [15:0] This is the lower 16 bits of the calculated EEPROM MISR checksum value.															
09E	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EEPROM MISR CHECKSUM [23:16] This is the upper 16 bits of the factory programmed EEPROM MISR Checksum value.								CALCULATED EEPROM MISR CHECKSUM [23:16] This is the upper 16 bits of the calculated EEPROM MISR Checksum value.							

14.3 Cell Balance Registers

Cell Balance Value Registers				Access:	Read Only
Address Range:	9'hxx Addr:		Page (binary)	Register Address (binary)	
	0A0 to 0AD		010	10 0000 to 10 1101	

Description
These registers are loaded with a value related to change in SOC desired for each cell. This values are then used during Auto Balance mode. The value in the register is decremented with each successive ADC sample until a zero value is reached. The registers are cleared at device power-up or by a Reset command. See Auto Balance Mode.

ADDR		
0A0	**Cell 1 Balance Value**	Cell 1 Balance Value[15:0]. Default = 16'h0000.
0A1	**Cell 2 Balance Value**	Cell 2 Balance Value[15:0]. Default = 16'h0000.
0A2	**Cell 3 Balance Value**	Cell 3 Balance Value[15:0]. Default = 16'h0000.
0A3	**Cell 4 Balance Value**	Cell 4 Balance Value[15:0]. Default = 16'h0000.
0A4	**Cell 5 Balance Value**	Cell 5 Balance Value[15:0]. Default = 16'h0000.
0A5	**Cell 6 Balance Value**	Cell 6 Balance Value[15:0]. Default = 16'h0000.
0A6	**Cell 7 Balance Value**	Cell 7 Balance Value[15:0]. Default = 16'h0000.
0A7	**Cell 8 Balance Value**	Cell 8 Balance Value[15:0]. Default = 16'h0000.
0A8	**Cell 9 Balance Value**	Cell 9 Balance Value[15:0]. Default = 16'h0000.
0A9	**Cell 10 Balance Value**	Cell 10 Balance Value[15:0]. Default = 16'h0000.
0AA	**Cell 11 Balance Value**	Cell 11 Balance Value[15:0]. Default = 16'h0000.
0AB	**Cell 12 Balance Value**	Cell 12 Balance Value[15:0]. Default = 16'h0000.
0AC	**Cell 13 Balance Value**	Cell 13 Balance Value[15:0]. Default = 16'h0000.
0AD	**Cell 14 Balance Value**	Cell 14 Balance Value[15:0]. Default = 16'h0000.

Cell Balance Status Registers				Access:	Read Only
Address Range:	9'hxx Addr:		Page (binary)	Register Address (binary)	
	0B0 to 0BD		010	11 0000 to 10 1101	

Description

Balance Status 1 register is used for Timed and Manual Mode selection.
Balance Status 2 to Balance Status 14 are used for Auto Balance Mode.
Bit 0 is the LSB, Bit 13 is the MSB.

Cell 1 to Cell 14 balance control, respectively. A bit set to 1 enables balance control (turns FET on) of the corresponding cell. Writing this bit enables balance output for the current incidence of the Balance Status register for the cells corresponding to the particular bits, depending on the condition of BEN in the Balance Setup register. Read this bit to determine the current status of each cell's balance control.

In Auto Balance mode, the RAA489204 controls the cell balance outputs based on bits set in the Balance Status registers. The operation begins with the value set in Balance Status 1 controlling the balance outputs. For the second Auto Balance cycle, the operation uses the contents of Balance Status 2; for the third auto balance cycle, the operation uses the contents of Balance Status 3, and the operation continues until a Balance Status Register contains a value of zero. In this case, the operation wraps back to Balance Status 1 and the pattern repeats.

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR	n = Balance Status, 1 to 14	Reserved		BnC14	BnC13	BnC12	BnC11	BnC10	BnC8	BnC8	BnC7	BnC6	BnC5	BnC4	BnC3	BnC2	BnC1
0B0	**Balance Status 1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0B1	**Balance Status 2**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0B2	**Balance Status 3**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0B3	**Balance Status 4**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0B4	**Balance Status 5**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0B5	**Balance Status 6**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0B6	**Balance Status 7**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0B7	**Balance Status 8**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0B8	**Balance Status 9**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0B9	**Balance Status 10**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0BA	**Balance Status 11**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0BB	**Balance Status 12**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0BC	**Balance Status 13**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0BD	**Balance Status 14**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

14.4 Register Map

Page	Addr	Write 10'h	Read 10'h	Register Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
001	00 0000	240	040	Cell Setup	0	0	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1
	00 0001		041	Cell 1 Voltage	SIGN	CELL 1 Voltage[14:0]														
	00 0010		042	Cell 2 Voltage	SIGN	CELL 2 Voltage[14:0]														
	00 0011		043	Cell 3 Voltage	SIGN	CELL 3 Voltage[14:0]														
	00 0100		044	Cell 4 Voltage	SIGN	CELL 4 Voltage[14:0]														
	00 0101		045	Cell 5 Voltage	SIGN	CELL 5 Voltage[14:0]														
	00 0110		046	Cell 6 Voltage	SIGN	CELL 6 Voltage[14:0]														
	00 0111		047	Cell 7 Voltage	SIGN	CELL 7Voltage[14:0]														
	00 1000		048	Cell 8 Voltage	SIGN	CELL 8 Voltage[14:0]														
	00 1001		049	Cell 9 Voltage	SIGN	CELL 9 Voltage[14:0]														
	00 1010		04A	Cell 10 Voltage	SIGN	CELL 10 Voltage[14:0]														
	00 1011		04B	Cell 11 Voltage	SIGN	CELL 11 Voltage[14:0]														
	00 1100		04C	Cell 12 Voltage	SIGN	CELL 12 Voltage[14:0]														
	00 1101		04D	Cell 13 Voltage	SIGN	CELL 13 Voltage[14:0]														
	00 1110		04E	Cell 14 Voltage	SIGN	CELL 14 Voltage[14:0]														
	01 0000		050	PACK Voltage	PACK Voltage[15:0]															
	10 0000		060	IC Temperature	Internal Temperature[15:0]															
	10 0001		061	External Temperature Input 1 Voltage (ExT1 pin)	ExT1 Voltage[15:0]															
	10 0010		062	External Temperature Input 2 Voltage (ExT2 pin)	ExT2 Voltage[15:0]															
	10 0011		063	External Temperature Input 3 Voltage (ExT3 pin)	ExT3 Voltage[15:0]															
	10 0100		064	External Temperature Input 4 Voltage (ExT4 pin)	ExT4 Voltage[15:0]															
	10 0101		065	Not Defined	Not Defined (Ignore the contents of this register)															
	10 0110		066	Not Defined	Not Defined (Ignore the contents of this register)															
	10 0111		067	GPIO1 Input Voltage	GPIO1 Voltage[15:0]															
	10 1000		068	GPIO2 Input Voltage	GPIO2 Voltage[15:0]															
	11 0000		070	Reference Voltage	VREF2 (secondary reference) Voltage[15:0]															
	11 0001	271	071	Scan Count			DSN 5	DSN 4	DSN 3	DSN 2	DSN 1	DSN 0			MSN 5	MSN 4	MSN 3	MSN 2	MSN 1	MSN 0

Note: Multi-register Reads on Page 1 automatically skip unused addresses. (It does not skip Not Defined addresses.)
Cell Voltages are 16-bits 2's complement values. The maximum positive value is '3FFFH'. The maximum negative value is '8000H'. Convert from the Hex value to Voltage using the following equations. $HEXvalue_{10}$ is the decimal representation of the HEX value.

$$if...HEXvalue_{10} \geq 32768 \qquad CellV(Volts) = \frac{(HEXvalue_{10} - 65536) \times 5}{32768}$$

$$else \qquad CellV(Volts) = \frac{HEXvalue_{10} \times 5}{32768}$$

Page	Addr	Write 10'h	Read 10'h	Register Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
010	00 0000	280	080	Fault Status	IT WFG	CMX	TMX	REG	REF	PAR	O VSS	O VBA T	OW	UV	OV	OT	WDG F	OSCF	0	BUF ERR
	00 0001	281	081	Overvoltage Fault			OF 14	OF 13	OF 12	OF 11	OF 10	OF 9	OF 8	OF 7	OF 6	OF 5	OF 4	OF 3	OF 2	OF 1
	00 0010	282	082	Undervoltage Fault			UF 14	UF 13	UF 12	UF 11	UF 10	UF 9	UF 8	UF 7	UF 6	UF 5	UF 4	UF 3	UF 2	UF 1
	00 0011	283	083	Open-Wire Fault		OW 14	OW 13	OW 12	OW 11	OW 10	OW 9	OW 8	OW 7	OW 6	OW 5	OW 4	OW 3	OW 2	OW1	OW 0
	00 0100	284	084	Over-Temperature Fault				OWT 4	OWT 3	OWT 2	OWT 1	G2T F	G1T F			OTF 4	OTF 3	OTF 2	OTF 1	OT IT
	00 0101	285	085	General Fault Status													P1 PAR	EE PAR	BUF O	BUF U
	00 0110	286	086	Fault Setup	TST G2	TST G1			TST E4	TST E3	TST E2	TST E1	TST IT	TOT 2	TOT 1	TOT 0	SCN 3	SCN 2	SCN 1	SCN 0
	00 0111	287	087	Overvoltage Limit	SIGN	OV Limit Voltage[14:0]														
	00 1000	288	088	Undervoltage Limit	SIGN	UV Limit Voltage[14:0]														
	00 1001	289	089	External Temp Limit	ExTn Over Temp Limit Voltage[15:0]															
	00 1010	28A	08A	$\overline{\text{FAULT}}$ Pin Mask	IT WFG	CMX	TMX	REG	REF	PAR	O VSS	O VBA T	OW	UV	OV	OT	WDG F	OSCF		BUFF
	00 1011	28B	08B	GPIO1 Fault Mask	IT WFG	CMX	TMX	REG	REF	PAR	O VSS	O VBA T	OW	UV	OV	OT	WDG F	OSCF		BUFF
	00 1100	28C	08C	Internal Temp Warning	Internal Over-Temperature Warning Threshold[15:0]															
	00 1101	28D	08D	Internal Temp Limit	Internal Over-Temperature Limit Threshold[15:0]															
	00 1110		08E	Cell Balance Enabled			CB EN14	CB EN13	CB EN12	CB EN11	CB EN10	CB EN9	CB EN8	CB EN7	CB EN6	CB EN5	CB EN4	CB EN3	CB EN2	CB EN1
	01 0000	290	090	Cell Balance Setup	Reserved							IBAL	EOB	BDDS	BEN	BWT 2	BWT 1	BWT 0	BMD 1	BMD 0
	01 0001	291	091	Watchdog/Balance Time		BTM 6	BTM 5	BTM 4	BTM 3	BTM 2	BTM 1	BTM 0	WDG 7	WDG 6	WDG 5	WDG 4	WDG 3	WDG 2	WDG 1	WDG 0
	01 0010	292	092	Device Setup 1			CMX1 P2M	NO_ TREG	WP 5	WP 4	WP 3	WP 2	WP 1	WP 0	WSC N	SCAN	G2 FUNC	G1 FUNC	G2 MOD	G1 MOD
	01 0011	293	093	Device Setup 2	FFS N	FFSP	TMU X	DP2	G2F 4	G2F 3	G2F 2	G2F 1	G2 VAL	G1 VAL	TAV 2	TAV 1	TAV 0	CAV 2	CAV 1	CAV 0
	01 0100	294	094	User Register 1	User Register 1[15:0]															
	01 0101	295	095	User Register 2	User Register 2[15:0]															
	01 0110		096	Comms Setup	CRA T1	CRA T0	0	CMO D	SIZE 4	SIZE 3	SIZE 2	SIZE 1	SIZE 0	ADD4	ADD3	ADD2	ADD1	ADD0	TEST	DR MOD E
	01 0111		097	Serial Number 0	User Serial Number[15:0]															
	01 1000		098	Serial Number 1	User Serial Number[31:16]															
	01 1001		099	Serial Number 2	User Serial Number[47:32]															
	01 1010		09A	Trim Voltage	Reserved										TV5	TV4	TV3	TV2	TV1	TV0
	01 1011	29B	09B	Cell Fault Mask			CFM 14	CFM 13	CFM 12	CFM 11	CFM 10	CFM 9	CFM 8	CFM 7	CFM 6	CFM 5	CFM 4	CFM 3	CFM 2	CFM 1
	01 1100		09C	EEPROM MISR	EEPROM MISR[15:0]															

Page	Addr	Write 10'h	Read 10'h	Register Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
010 (Cont.)	01 1101		09D	EEPROM CALC MISR	EEPROM Calculated MISR[15:0]															
	01 1110		09E	EEPROM MISR/CALC	EEPROM MISR[23:16]								EEPROM Calculated MISR[23:16]							
	10 0000	2A0	0A0	Cell 1 Balance Value	Cell 1 Balance Value[15:0]															
	10 0001	2A1	0A1	Cell 2 Balance Value	Cell 2 Balance Value[15:0]															
	~		~	~	~															
	10 1101	2AD	0AD	Cell 14 Balance Value	Cell 14 Balance Value[15:0]															
	11 0000	2B0	0B0	Balance Status 1			B1 C14	B1 C13	B1 C12	B1 C11	B1 C10	B1 C9	B1 C8	B1 C7	B1 C6	B1 C5	B1 C4	B1 C3	B1 C2	B1 C1
	11 0001	2B1	0B1	Balance Status 2			B2 C14	B2 C13	B2 C12	B2 C11	B2 C10	B2 C9	B2 C8	B2 C7	B2 C6	B2 C5	B2 C4	B2 C3	B2 C2	B2 C1
	~		~	~	~								~							
	11 0010	2BD	0BD	Balance Status 14			B14 C14	B14 C13	B14 C12	B14 C11	B14 C10	B14 C9	B14 C8	B14 C7	B14 C6	B14 C5	B14 C4	B14 C3	B14 C2	B14 C1

Note: Green Highlighted bits are included in Calc Register Checksum and Check Register Checksum commands.

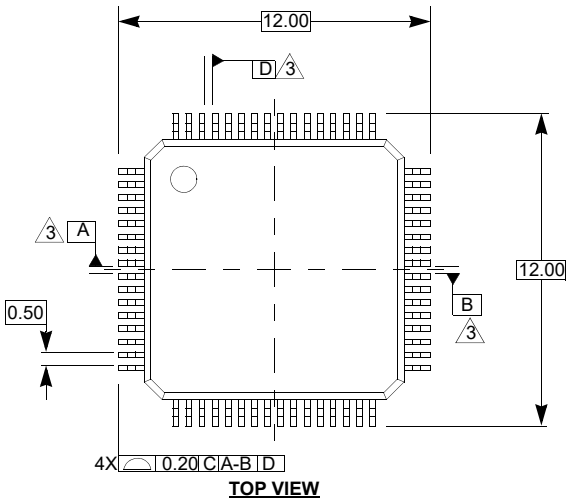
Page	Addr	Write 10'h	Read 10'h	Register Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
011	00 0001		0C1	Scan Voltages																
	00 0010		0C2	Scan Temperatures																
	00 0011		0C3	Scan Mixed																
	00 0100		0C4	Scan Wires																
	00 0101		0C5	Scan All																
	00 0110		0C6	Scan Continuous																
	00 0111		0C7	Scan Inhibit																
	00 1000		0C8	Measure																
	00 1001		0C9	Scan Cell MUX																
	00 1010		0CA	Balance Enable																
	00 1011		0CB	Balance Inhibit																
	01 0000		0D0	Roll Call																
	01 0001		0D1	NAK																
	01 0010		0D2	ACK																
	01 0011		0D3	Comms Failure																
	01 0100		0D4	Sleep																
	01 0101		0D5	Wakeup																
	01 0110		0D6	SReset																
	01 0111		0D7	Calc Register Checksum																
	01 1000		0D8	Check Register Checksum																
	01 1010		0DA	Override Clear on Write																
	01 1110		0DE	HReset_Wakeup Precursor																
	01 1111		0DF	HReset																

15. Package Outline Drawing

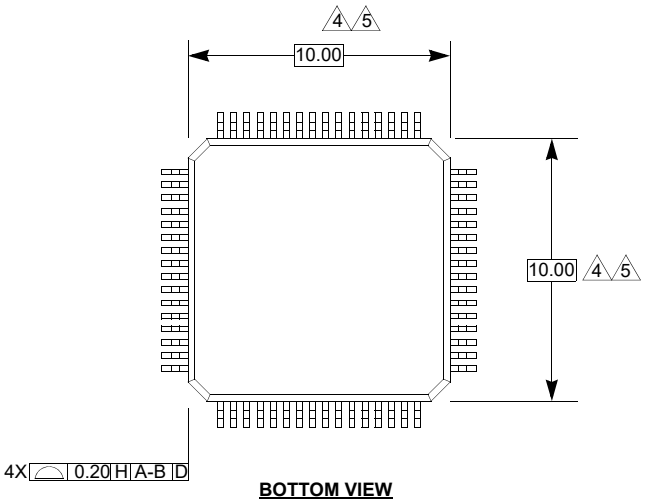
For the most recent package outline drawing, see Q64.10x10D.

Q64.10x10D

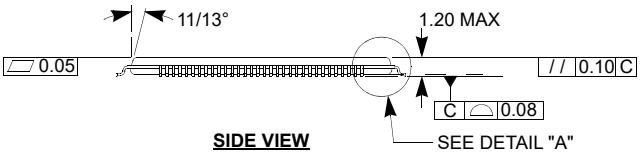
64 Lead Thin Plastic Quad Flatpack Package
Rev 3, 11/16



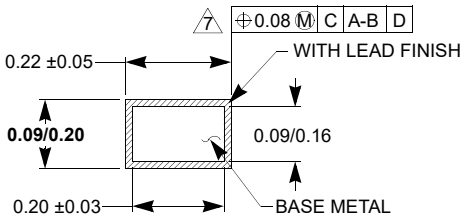
TOP VIEW

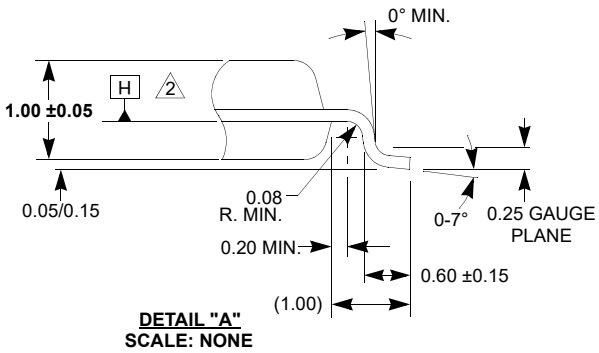


BOTTOM VIEW

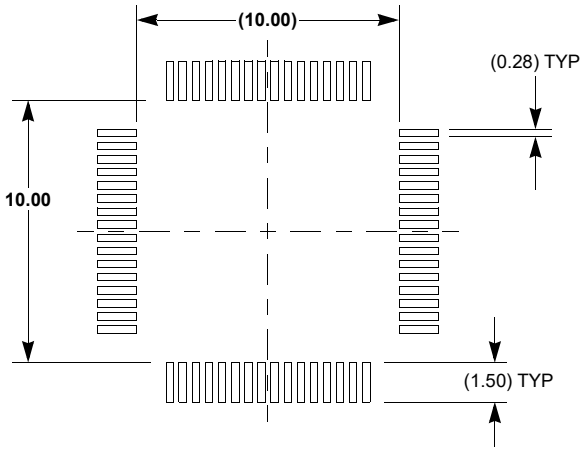


SIDE VIEW





DETAIL "A"
SCALE: NONE



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. All dimensioning and tolerancing conform to ANSI Y14.5-1982.
2. Datum plane H located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and D to be determined at centerline between leads where leads exit plastic body at datum plane H.
4. Dimensions do not include mold protrusion. Allowable mold protrusion is 0.254mm.
5. These dimensions to be determined at datum plane H.
6. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package.
7. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total at maximum material condition. Dambar cannot be located on the lower radius or the foot.
8. Controlling dimension: millimeter.
9. This outline conforms to JEDEC publication 95 registration MS-026, variation ACD.
10. Dimensions in ( ) are for reference only.

16. Ordering Information

Part Number[1][2]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Temp. Range
RAA4892042GFT#AA0	RAA 489204	64 Ld TQFP	Q64.10x10D	Tray	-40 to +85°C
RAA4892042GFT#HA0				Reel, 1k	
RTKA489204DE0000BU	Evaluation Board				
RTKA489204DK0000BU	Daisy Chain Evaluation Kit				

1. For the Moisture Sensitivity Level (MSL), see the RAA489204 device page. For more information about MSL, see TB363.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. See TB347 for details about reel specifications.

17. Revision History

Revision	Date	Description
1.01	Feb 16, 2023	Updated the Absolute Maximum Ratings section by doing the following: ▪ Changed several minimum values from -0.3 to -0.5. ▪ Changed VCn-CBn minimum value from -9.0 to -0.5 and the maximum value from 0.5 to 9.0. Updated Figures 30, 33, 37, 43, 44, 48, 49, 50, 68 Updated Tables 5, 13, 14, 18, 26, 29, 43, 44, 45, 46, 47.48, 49, 50, 55, 56, 57, 60. Updated Scan Cell MUX (Address: C9H) section. Updated Shutdown Mode section. Updated Data Registers section. Updated Fault Status and Setup Registers section. Updated Equation 10. Added External Temperature Measurement Averaging Time section.
1.00	Aug 24, 2021	Initial release.

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