

# LP5910DRV EVM User Guide

## 1 Introduction

The Texas Instruments LP5910DRV evaluation module (EVM) helps designers evaluate the operation and performance of the LP5910 LDO voltage regulator. The LP5910DRV EVM contains one LP5910 LDO voltage regulator in the WSON / DRV package (see [Table 1](#)).

**Table 1. Device Information**

EVM ORDERABLE NUMBER	OUTPUT VOLTAGE	PART NAME	PACKAGE
LP5910DRV18EVM	1.8 V	LP5910-1.8DRVR	6-pin DRV (WSON)

## 2 Setup

This section describes the jumpers and connectors on the EVM as well and how to properly connect, set up and use the LP5910DRV EVM.

The device has been designed to work with 1- $\mu$ F input and output ceramic capacitors down to 0402 component size.

### 2.1 Input/Output Connector Descriptions

**VIN** and **GNDIN** are the connection terminals for the input supply. The VIN terminal is the positive connection, and the GNDIN terminal is the negative (that is, ground) connection.

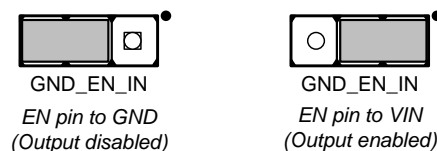
**VOUT** and **GNDOUT** are the connection terminals for the output load. The VOUT terminal is the positive connection, and the GNDOUT terminal is the negative (that is, ground) connection.

**GND\_EN\_IN** is a 3-pin terminal used to enable, or disable, the LP5910.

When the shunt is across EN\_IN terminal pins the Enable (EN) pin is directly connected to VIN. The LP5910 will be enabled when VIN is applied.

When the shunt is across GND\_EN terminal pins the EN pin is connected directly to GND. The LP5910 will be disabled.

The shunt must be in place, or the EN terminal pin must be driven by an off-board supply, otherwise LP5910 EN pin is floating, and the EN status may be undefined. The default, and recommended, shunt position is across the EN\_IN terminal pins (enabled).



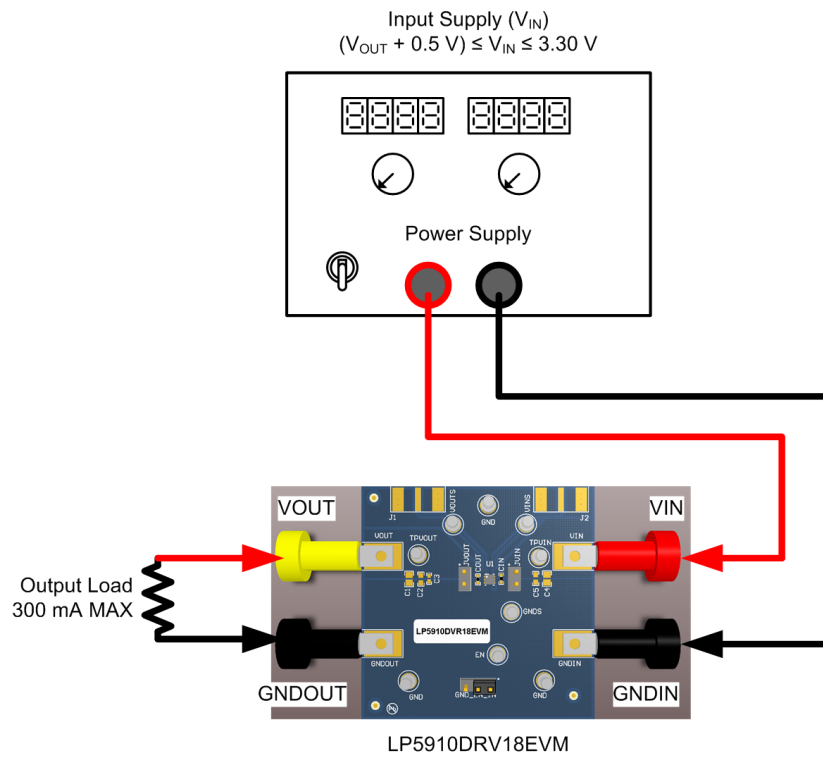
**Figure 1. EN Jumper Settings**

### 2.2 Setup

The recommended operating input voltage range for the LP5910DRV EVM is :  $V_{OUT} + 0.5$  V (minimum) to 3.3 V (maximum).

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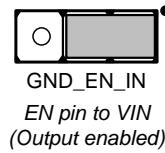
A load should be applied between the VOUT terminal and the GNDOUT terminal for proper operation. Load current should be maintained between 1 mA and 300 mA.



**Figure 2. LP5910DRV EVM Setup**

### 2.3 Operation

For proper operation of the LP5910DRV EVM, the jumper terminal should be properly configured. The default, and recommended, jumper setting is:



**Figure 3. Jumper Settings**

**GND\_EN\_IN** shunt across the EN\_IN pins.

In this configuration, the device will power up when power is applied at the VIN terminal.

### 2.4 Options

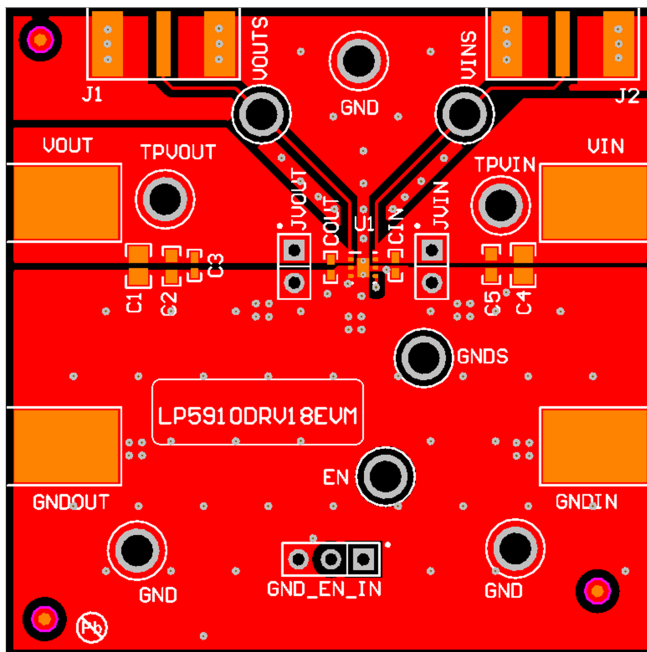
The LP5910DRV EVM has some assorted unpopulated footprints that some users may find useful:

- Footprint for optional CIN at C4 (0805) and C5 (0603).
- Footprints for optional COUT at C1 (0805), C2 (0603), and C3 (0402).
- Footprints for optional end launch SMA connectors (Emerson 142-0701-851, or equivalent) at VIN (J2) and VOUT (J1) for noise or PSRR testing.

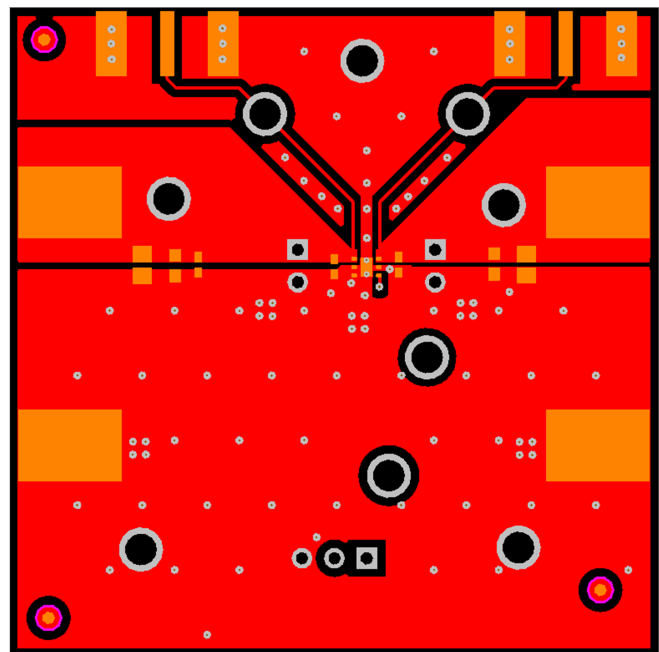
## 3 Board Layout

Figure 4 through Figure 9 show the board layout for the LP5910DRV EVM PCB. The EVM offers resistors, capacitors and jumpers to program the EN pin status.

The LP5910 will dissipate power. The 6-pin DRV (WSON) package offers an exposed thermal pad to enhance thermal performance. The exposed thermal pad must be soldered to the copper landing on the PCB for optimal thermal performance. The PCB provides 1 oz. (0.0014 inch) copper planes on all four layers to dissipate heat.



**Figure 4. Top Assembly Layer and Silk-Screen**



**Figure 5. Top-Layer Routing**

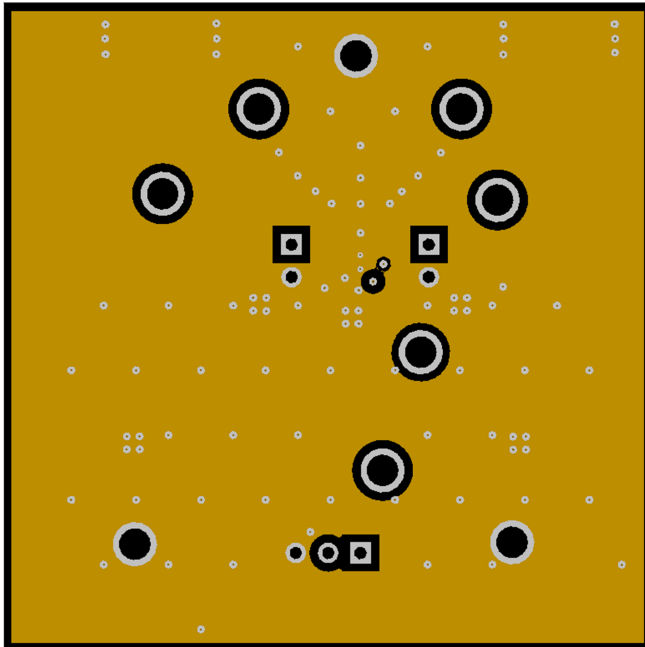


Figure 6. Layer 2: GND Plane

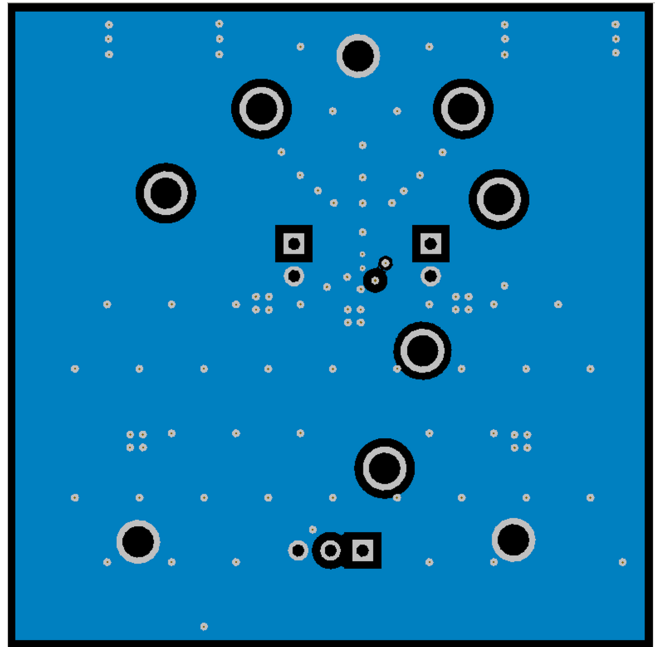


Figure 7. Layer 3: GND Plane

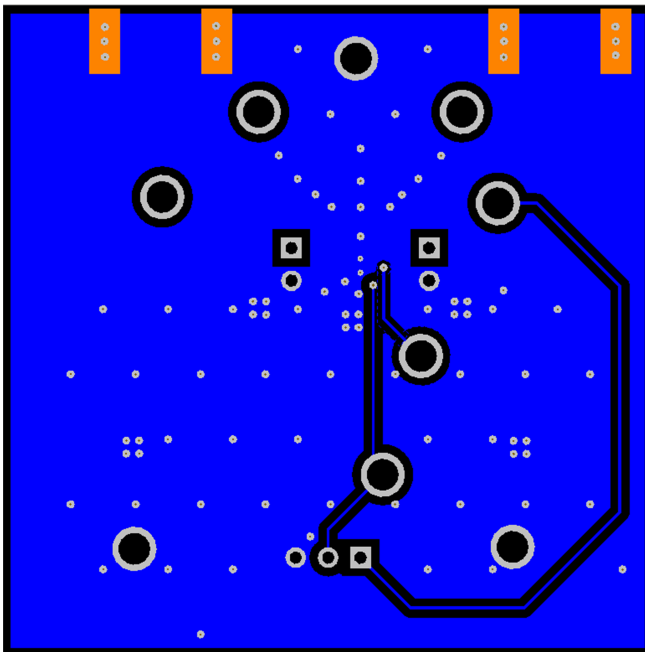


Figure 8. Bottom-Layer Routing

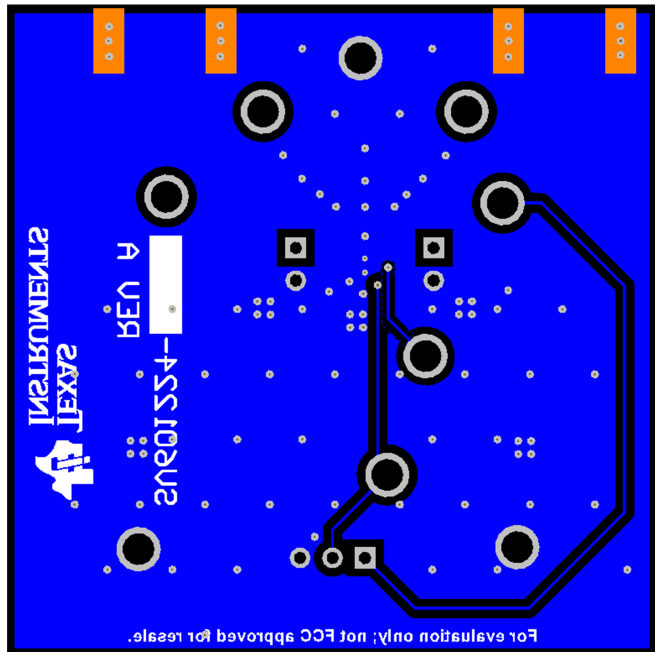
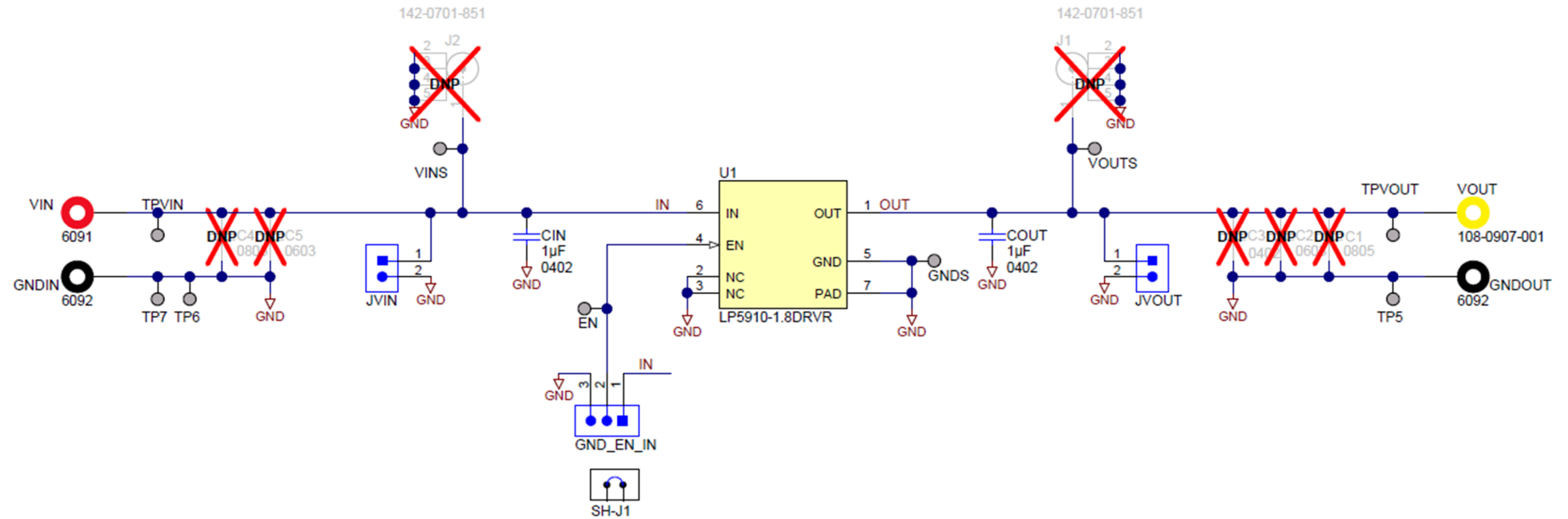


Figure 9. Bottom Assembly Layer and Silk-Screen

Figure 10. LP5910DRVEVM Schematic



## 4 Bill of Materials

DESCRIPTION	DESIGNATOR	PART NUMBER	MFR	QUANTITY
Capacitor: Ceramic, 1 $\mu$ F, 10%, 10 V, X5R, 0402	CIN, COUT	GRM155R61A105KE15D	Murata	2
Terminal, Turret, TH, Double	EN, GNDS, TP5, TP6, TP7, TPVIN, TPVOUT, VINS, VOUTS	1502-2	Keystone	9
Standard Banana Jack, Insulated, Black	GNDIN, GNDOUT	6092	Keystone	2
Standard Banana Jack, Insulated, Red	VIN	6091	Keystone	1
Standard Banana Jack, Insulated, Yellow	VOUT	108-0907-001	Cinch	1
Header, 2-pin, 100-mil spacing	JVIN, JVOUT	HTSW-102-07-G-S	Samtec	2
Header, 3-pin, 100-mil spacing	GND_EN_IN	HTSW-103-07-G-S	Samtec	1
Shunt, 100 mil, Gold plated, Black	SH-J1	SNT-100-BK-G	Samtec	1
Ultra Low-Noise, 300-mA Linear Regulator for RF and Analog Circuits - Requires No Bypass Capacitor	U1	LP5910-1.8DRVR	TI	1
PCB, 2 inch x 2 inch x 0.062	LP5910DRV EVM PCB	SV601224	TI	1

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.



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