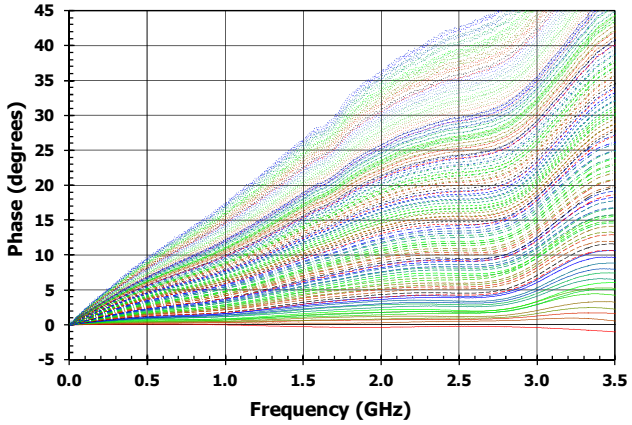
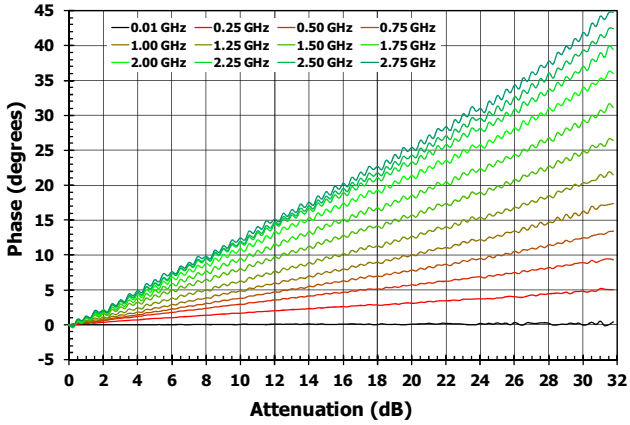
TYPICAL OPERATING CONDITIONS (- 2 -)

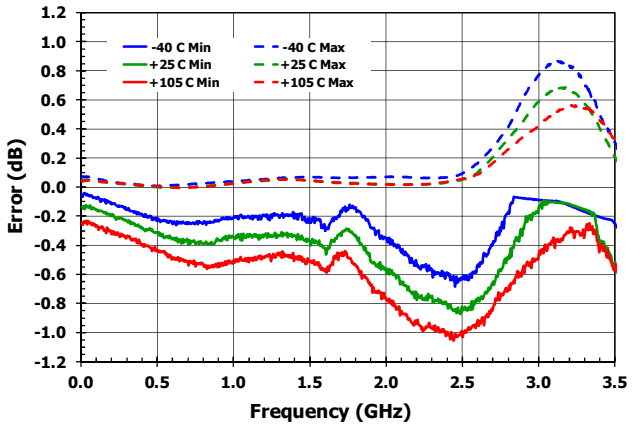
Relative Insertion Phase vs Frequency



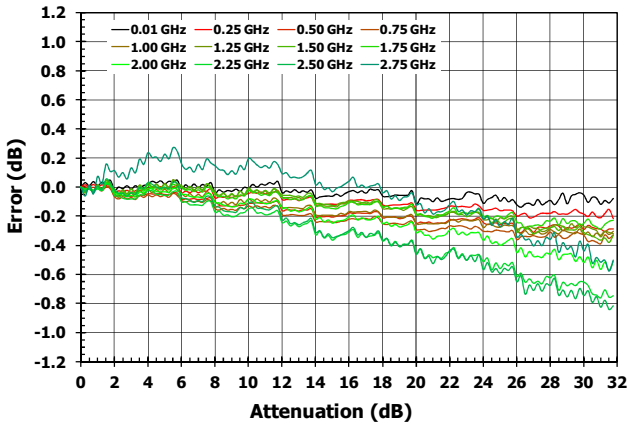
Relative Insertion Phase vs Attenuation



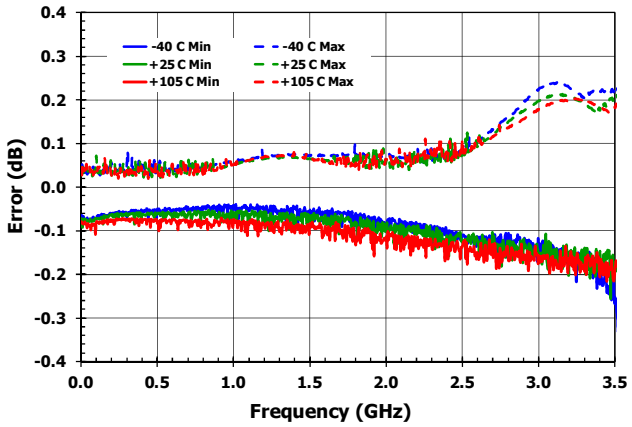
Worst Case Absolute Accuracy vs Frequency



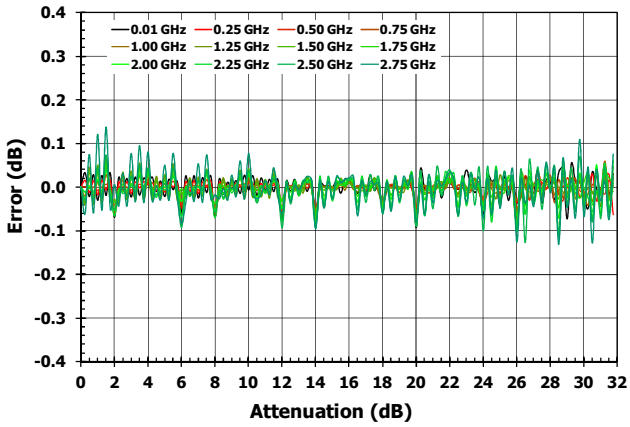
Absolute Accuracy vs Attenuation



Worst Case Step Accuracy vs Frequency

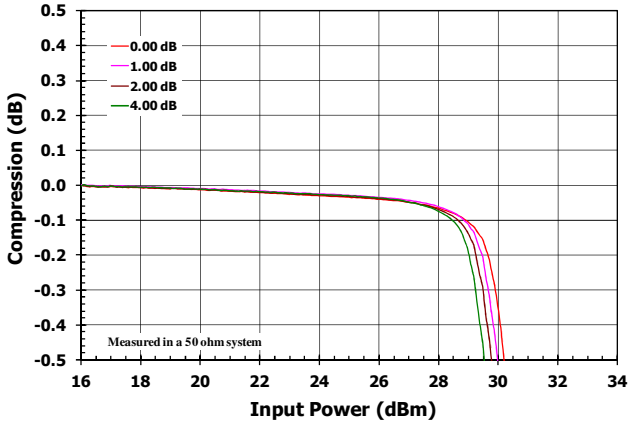


Step Accuracy vs Attenuation

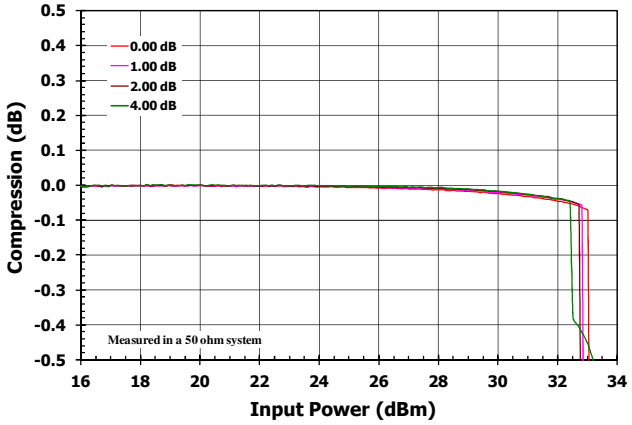


TYPICAL OPERATING CONDITIONS (- 3 -)

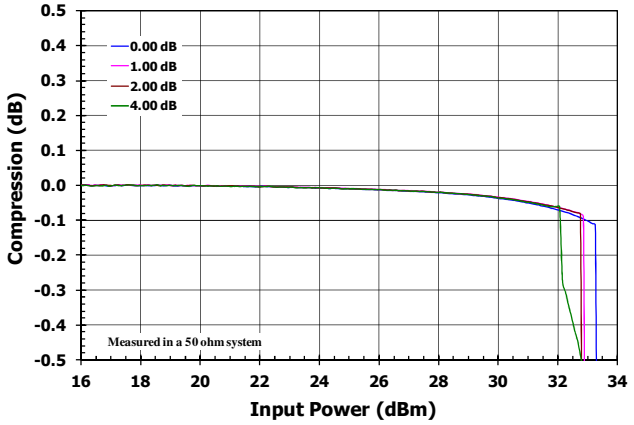
Input Compression at 50 MHz



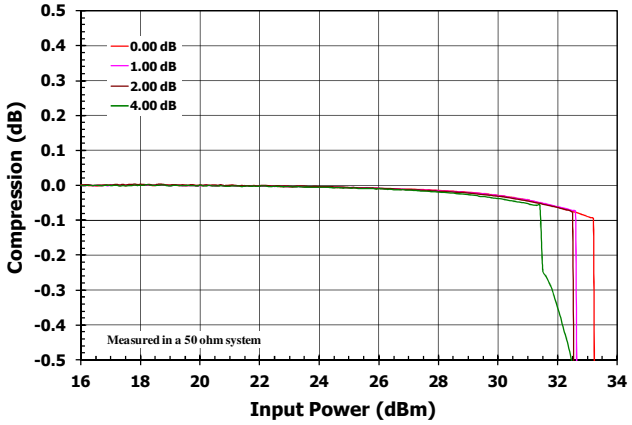
Input Compression 500 MHz



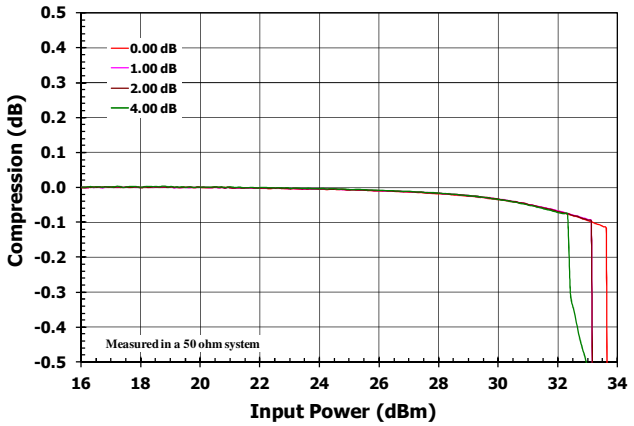
Input Compression 1.0 GHz



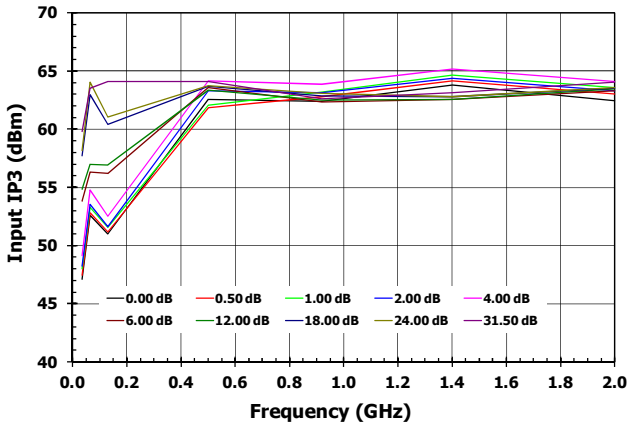
Input Compression 1.5 GHz



Input Compression 2.0 GHz

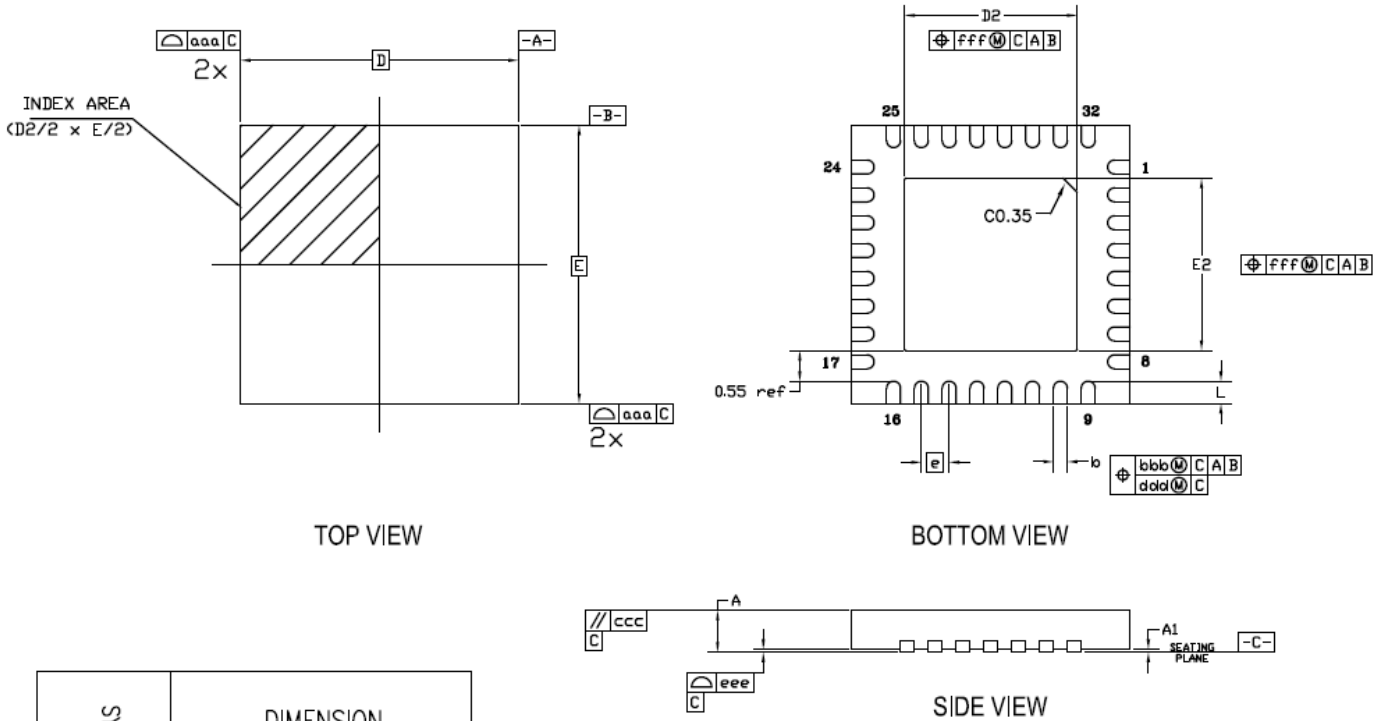


Input IP3



PACKAGE DRAWING

(5 mm x 5 mm 32-pin TQFN), Use Exposed PAD (EPAD) ***Option P1***



SYMBOL	DIMENSION		
	MIN	NOM	MAX
L	0.30	0.40	0.50
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	.20	.25	.30
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

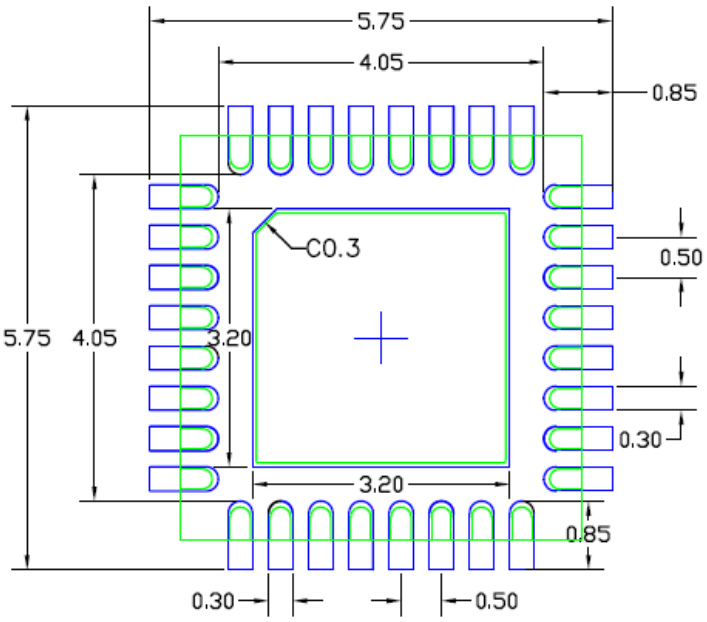
EPAD OPTION

SYMBOL	P1		
	MIN	NOM	MAX
E2	3.00	3.10	3.20
D2	3.00	3.10	3.20

NOTES:

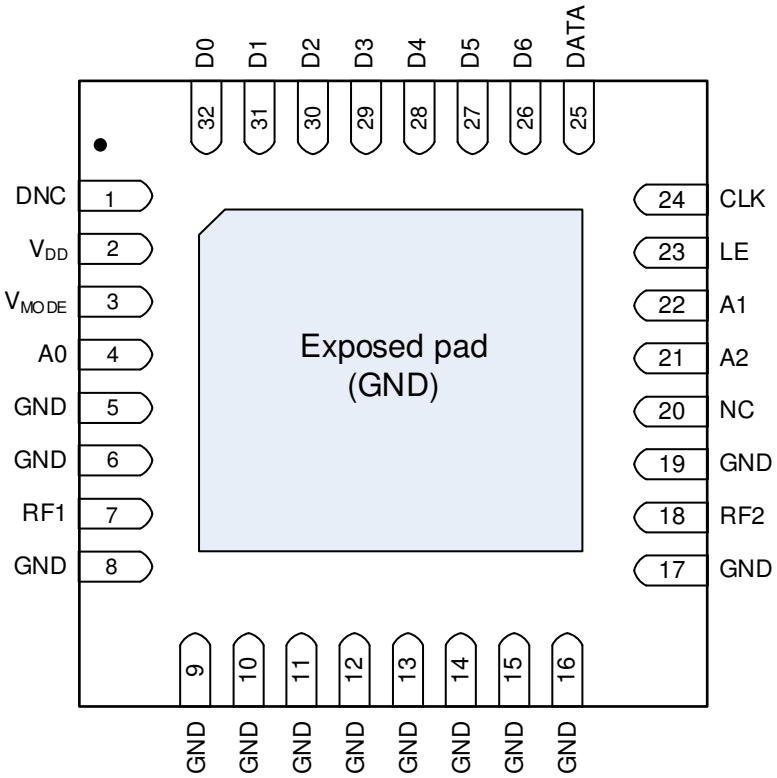
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.

LAND PATTERN DIMENSION



PIN DIAGRAM

TOP View
(looking through the top of the package)



PIN DESCRIPTION

Pin	Name	Function
1	DNC	**This pin must be left open.**
2	V_{DD}	Main Supply. Use 3.3 V or 5 V. Bypass capacitor as close to pin as possible.
3	V_{MODE}[1]	Logic low for parallel mode. Logic high or NC for serial mode.
4	A0[2]	Address bit A0 connection.
5	GND	Connect directly to paddle ground or as close as possible to pin with thru via. This pin is not internally connected.
6	GND	Connect directly to paddle ground or as close as possible to pin with thru via.
7	RF1[3]	Device RF input or output (bi-directional).
8 – 17	GND	Connect each pin directly to paddle ground or as close as possible to pin with thru vias.
18	RF2[3]	Device RF input or output (bi-directional).
19	GND	Connect directly to paddle ground or as close as possible to pin with thru via.
20	NC	No internal connection. These pins can be left unconnected, voltage applied, or connected to ground (recommended).
21	A2[2]	Address bit A2 connection
22	A1[2]	Address bit A1 connection.
23	LE[1]	Serial interface latch enable input.
24	CLK[1]	Serial interface clock input.
25	DATA[1]	Serial interface data input.
26	D6[1]	Parallel control bit, 16 dB.
27	D5[1]	Parallel control bit, 8 dB.
28	D4[1]	Parallel control bit, 4 dB.
29	D3[1]	Parallel control bit, 2 dB.
30	D2[1]	Parallel control bit, 1 dB.
31	D1[1]	Parallel control bit, 0.5 dB.
32	D0[1]	Parallel control bit, 0.25 dB.
EP	Exposed Paddle	Connect to Ground with multiple vias for good thermal and RF performance.

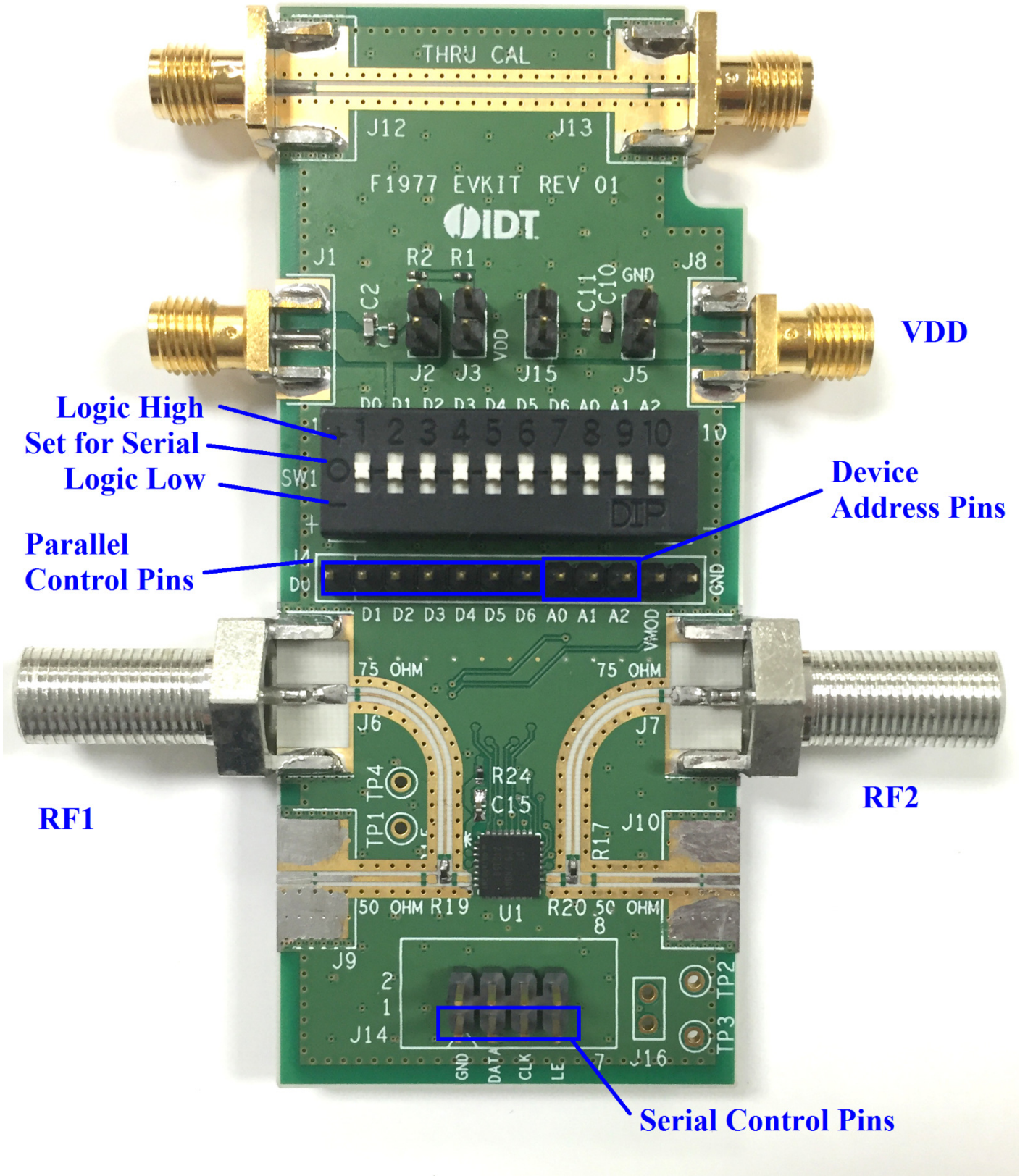
Pin Description Notes:

Note 1: Includes an internal 100 kΩ pullup resistor to an internal regulated 2.5V supply. If pin is grounded then there is an additional 25 µA per pin for the supply current.

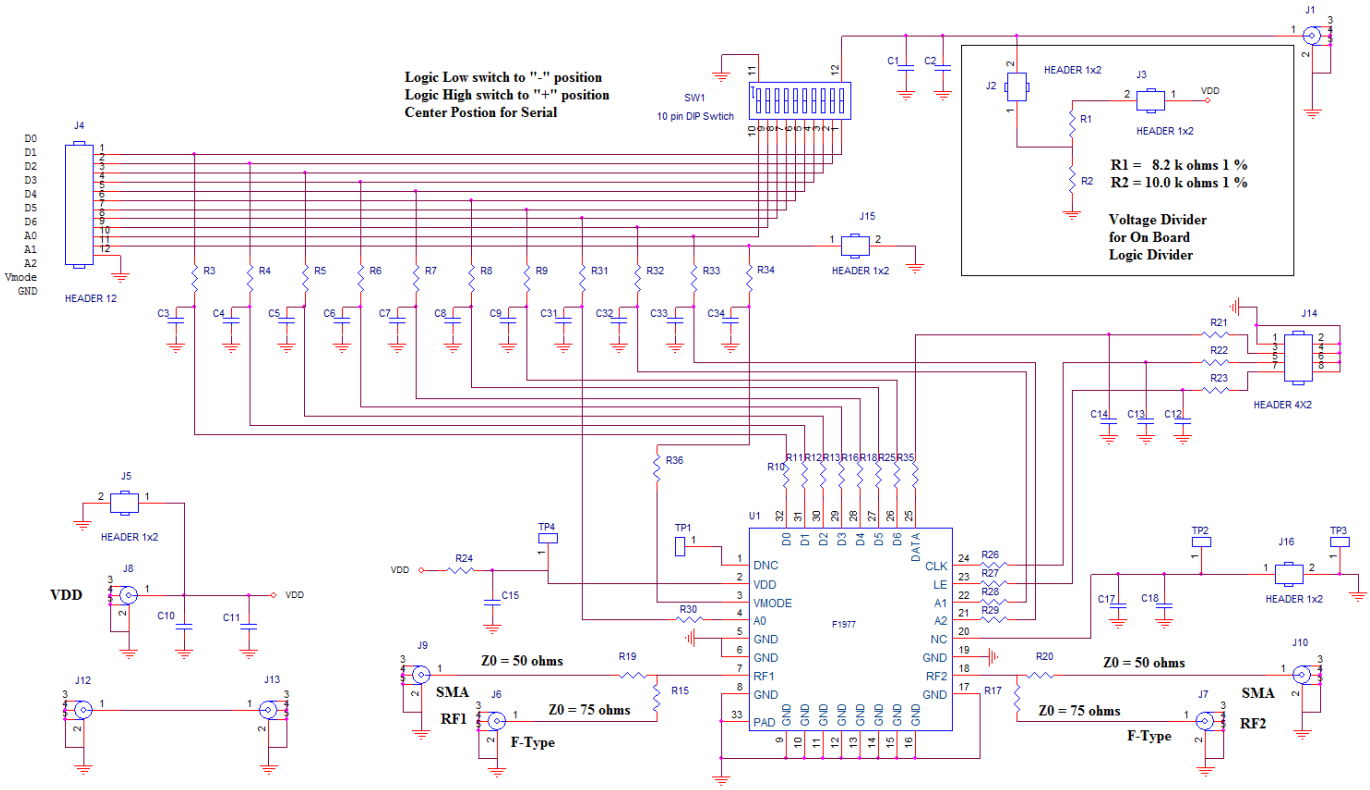
Note 2: Includes an internal 100 kΩ pull-down resistor to GND.

Note 3: RF pins 7 and 18 do not require DC blocking capacitors for operation if they are at 0 V DC. If they are not at 0V DC, then they require DC blocking capacitors.

EVKIT PICTURE



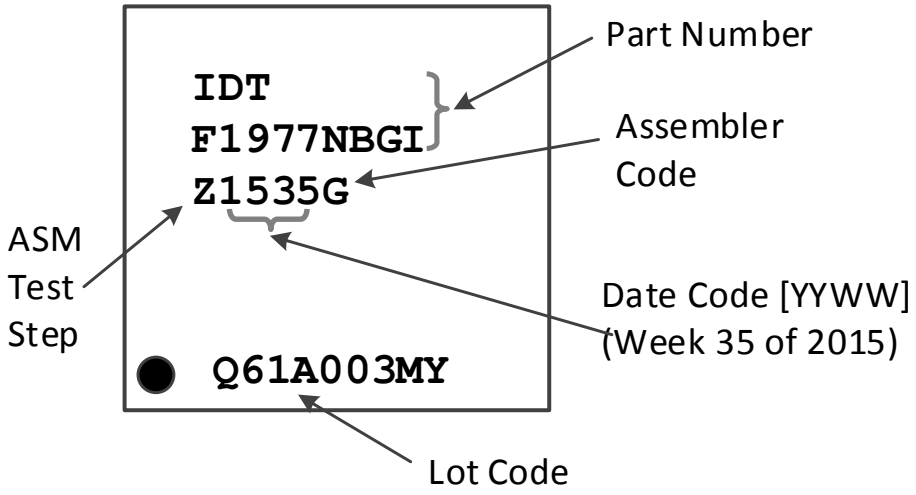
EVKIT / APPLICATIONS CIRCUIT



EVKIT BOM

Item #	Part Reference	QTY	DESCRIPTION	Mfr. Part #	Mfr.
1	C1, C11, C15	3	100 nF ±10%, 16 V, X7R Ceramic Capacitor (0402)	GRM155R71C104K	MURATA
2	C2, C10	2	10 nF ±5%, 50 V, X7R Ceramic Capacitor (0603)	GRM188R71H103J	MURATA
3	C3 - C9, C12, C13, C14, C31 - C34	14	100 pF ±5%, 50 V, C0G Ceramic Capacitor (0402)	GRM1555C1H101J	MURATA
4	R3 - R9, R31 - R34	11	100 Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1000X	PANASONIC
5	R10-R13, R15-R18, R24-R30, R35, R36	17	0 Ω Resistors (0402)	ERJ-2GE0R00X	PANASONIC
6	R21, R22, R23	3	3 kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF3001X	PANASONIC
7	R1	1	8.2 kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF8201X	PANASONIC
8	R2	1	10 kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1002X	PANASONIC
9	J2, J3, J5	3	CONN HEADER VERT SGL 2 X 1 POS GOLD	961102-6404-AR	3M
10	J14, J15	1	CONN HEADER VERT DBL 4 X 2 POS GOLD	67997-108HLF	FCI
11	J4	1	CONN HEADER VERT SGL 12 X 1 POS GOLD	961112-6404-AR	3M
12	J1, J8	2	Edge Launch SMA (0.250 inch pitch ground, round)	142-0711-821	Emerson Johnson
13	J6, J7	2	Edge Launch F TYPE 75 ohm SMA	222181	Amphenol
14	U2	1	SWITCH 10 POSITION DIP SWITCH	KAT1110E	E-Switch
15	U1	1	DSA	F1977NCGI	IDT
16		1	Printed Circuit Board	F1977 Evkit Rev 01	IDT

TOP MARKINGS



APPLICATIONS INFORMATION

Power Supplies

A common VCC power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1 V / 20 µS. In addition, all control pins should remain at 0 V (+/-0.3 V) while the supply voltage ramps or while it returns to zero.

Digital Pin Voltage & Resistance Values

The following table provides open-circuit DC voltage referenced to ground and resistance values for each of the control pins listed.

Pin	Name	Open Circuit DC Voltage	Internal Connection
3	V_{MODE}	2.5 V	100 kΩ pullup resistor to internally regulated 2.5 V
4, 21, 22	A0, A2, A1	0 V	100 kΩ resistor to GND
23, 24, 25	LE, CLK, DATA	2.5 V	100 kΩ pullup resistor to internally regulated 2.5 V
26-32	D[6:0]	2.5 V	100 kΩ pullup resistor to internally regulated 2.5 V

REVISION HISTORY SHEET

Rev	Date	Page	Description of Change
O	2016-Feb-19		Initial Release
1	2016-Apr-21	2	Typo on V_{HBM} rating. Voltage changed from 1.5kV to 1kV. No chng. to Class