# D2-6 Family Audio SOC

Intelligent Digital Amplifier and Sound Processor

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The D2-6 family (D2-71083, D2-74083, D2-71583, D2-74583, and D2-74383) digital audio processor devices are complete System-on Chip (SoC) audio processor and Class-D amplifier controllers. Integrated DSP processing and configurable audio processing algorithms provide an extremely flexible platform for feature rich and cost-effective quality audio solutions which benefit from the addition of Class-D amplifiers and DSP audio processing, meeting demands of consumer electronics applications.

The 12 integrated digital PWM controllers can be used in a variety of multi-channel audio system configurations, supporting powered as well as line outputs. Fully protected amplifier control provides efficient and clean Class-D power output support.

The D2-6 device family supports full audio decoding for formats including Dolby® Digital, Dolby® Pro Logic IIx, AAC LC™, DTS® Digital Surround, and Dolby® Digital Plus. The D2-6 family is pin-compatible and function/feature compatible with the D2-3 family devices, enabling additional decoding capability to existing designs, or providing cost optimization to lower-featured systems not requiring the additional audio processing and decode capability.

## Applications

- Audio Video Receiver (AVR)
- Multi-channel surround soundbar
- Home Theater in a Box (HTiB)
- Multi-channel Multi-Media (MM) systems
- Installed steerable audio arrays
- Bluetooth/WiFi voice-enabled speaker systems
- Automotive trunk/amplified solutions

## Related Literature

For a full list of related documents, visit our website:

- D2-71083, D2-74083, D2-71583, D2-74583, D2-74383 device pages

## Features

- Advanced D2-6 family digital audio processor IC
  - Pin compatible and function/feature compatible with the D2 Audio DSP D2-3 family device
- Total System on Chip (SoC)
  - All digital Class-D amplifier controller
  - Full 5.1/7.1/9.1-channel amplifier platform support
- Enhanced audio processing decoders
  - Dolby® Digital/AC3
  - Dolby® Pro Logic IIx
  - AAC LC™
  - DTS® Digital Surround
  - Dolby® Digital Plus
- D2 Audio DSP sound enhancement algorithm and virtualization
- Expanded on-chip memory capacity
- Integrated DSP processing
  - 12 channels of Digital Signal Processing (DSP) including equalizers, filters, mixers and other common audio processing blocks
  - Fully configurable and routable audio signal paths
- Flexible audio input and output configurations
- Embedded 8-channel sample rate converter
  - Sample rates from 32kHz up to 192kHz
- Real-time amplifier control and monitoring
  - Supports bridged, half-bridged, and Bridge-Tied Load (BTL) topologies, using discrete or integrated power stages from 10W to over 500W
  - Complete fault protection with automatic recovery

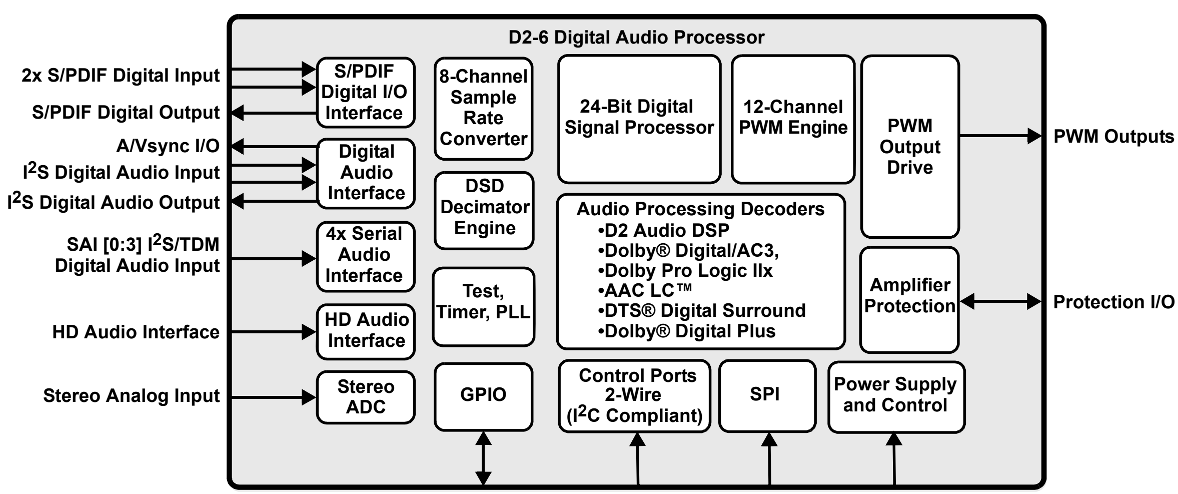



FIGURE 1. BLOCK DIAGRAM

# Ordering Information

| PART NUMBER (Notes 2, 3) | PART MARKING | AUDIO PROCESSING FEATURE SET SUPPORT (Note 1) | TEMP. RANGE (°C) | PACKAGE (RoHS COMPLIANT) | PKG. DWG. # |
|---|---|---|---|---|---|
| D2-71083-LR | D2-71083-LR | Refer to Table 1 | -10 to +85 | 128 Ld LQFP | Q128.14x14 |
| D2-74083-LR | D2-74083-LR | Refer to Table 1 | -10 to +85 | 128 Ld LQFP | Q128.14x14 |
| D2-71583-LR | D2-71583-LR | Refer to Table 1 | -10 to +85 | 128 Ld LQFP | Q128.14x14 |
| D2-74583-LR | D2-74583-LR | Refer to Table 1 | -10 to +85 | 128 Ld LQFP | Q128.14x14 |
| D2-74383-LR | D2-74383-LR | Refer to Table 1 | -10 to +85 | 128 Ld LQFP | Q128.14x14 |
| D2-71683-LR (No longer available, recommended replacement: D2-71583-LR) | D2-71683-LR | Refer to Table 1 | -10 to +85 | 128 Ld LQFP | Q128.14x14 |

NOTES:

1. The D2-6 devices support multiple audio processing algorithms and decoders, and support is device-dependent. Refer to Table 1 for the supported features for each device part number.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the D2-71083, D2-74083, D2-71583, D2-74583, D2-74383 product information pages. For more information about MSL, see TB363.

# D2-6 Family Device Feature Set Offering

The D2-6 family has specific part numbers to specify the features and algorithms supported in the device. These part numbers and their supported features are shown in Table 1.

**TABLE 1. D2-6 DEVICE PART NUMBERS AND FEATURES**

| PART NUMBER | FEATURES | ALGORITHM SUPPORT (Note 4) | DSP CLOCK AND MEMORY (Note 5) |
|---|---|---|---|
| D2-71083-LR | 8-Channels Audio of $I^2S$ Digital Inputs<br>2 S/PDIF Digital Inputs<br>8 Audio Processing Channels with PWM Outputs<br>Embedded 8-Channel Sample Rate Converter | D2 Audio DSP Sound Enhancement Algorithm Audio Processing | 147MHz DSP Clock<br>24k X and Y Memory Capacities<br>32k P Memory Capacity |
| D2-74083-LR | 8-Channels Audio of $I^2S$ Digital Inputs<br>2 S/PDIF Digital Inputs<br>8 Audio Processing Channels with PWM Outputs<br>Embedded 8-Channel Sample Rate Converter | D2 Audio DSP Sound Enhancement Algorithm Audio Processing | 160MHz DSP Clock<br>40k X and Y Memory Capacities<br>56k P Memory Capacity |
| D2-71583-LR | 8-Channels Audio of $I^2S$ Digital Inputs<br>2 S/PDIF Digital Inputs<br>8 Audio Processing Channels with PWM Outputs<br>Embedded 8-Channel Sample Rate Converter | D2 Audio DSP Sound Enhancement<br>Dolby® Digital/AC3 Decoder<br>Dolby® Pro Logic IIx<br>DTS® Digital Surround Decoder | 147MHz DSP Clock<br>24k X and Y Memory Capacities<br>32k P Memory Capacity |
| D2-74583-LR | 8-Channels Audio of $I^2S$ Digital Inputs<br>2 S/PDIF Digital Inputs<br>8 Audio Processing Channels with PWM Outputs<br>Embedded 8-Channel Sample Rate Converter | D2 Audio DSP Sound Enhancement<br>Dolby® Digital/AC3 Decoder<br>Dolby® Pro Logic IIx<br>DTS® Digital Surround Decoder | 160MHz DSP Clock<br>40k X and Y Memory Capacities<br>56k P Memory Capacity |
| D2-74383-LR | 8-Channels Audio of $I^2S$ Digital Inputs<br>2 S/PDIF Digital Inputs<br>8 Audio Processing Channels with PWM Outputs<br>Embedded 8-Channel Sample Rate Converter | D2 Audio DSP Sound Enhancement Algorithm<br>Dolby® Digital Plus<br>Dolby® Pro Logic IIx<br>DTS® Digital Surround Decoder | 160MHz DSP Clock<br>40k X and Y Memory Capacities<br>56k P Memory Capacity |
| D2-71683-LR (No longer available, recommended replacement: D2-71583-LR) | 8-Channels Audio of $I^2S$ Digital Inputs<br>2 S/PDIF Digital Inputs<br>8 Audio Processing Channels with PWM Outputs<br>Embedded 8-Channel Sample Rate Converter | D2 Audio DSP Sound Enhancement<br>Dolby® Digital/AC3 Decoder<br>Dolby® Pro Logic IIx Surround<br>DTS® Digital Surround Decoder<br>AAC LC™ Decoder | 147MHz DSP Clock<br>24k X and Y Memory Capacities<br>32k P Memory Capacity |

NOTES:

4. D2 Audio DSP Sound Enhancements are included with all D2-6 family devices with no additional licensing or royalties required. The D2-71583-LR and D2-74583-LR devices include Dolby Digital and DTS Digital Surround support and third part licenses are required. The D2-74383-LR device includes Dolby Digital Plus and DTS Digital Surround support and third party licenses are required. Dolby Pro Logic IIx support is an optional feature that can be added to the D2-71583-LR, D2-74583-LR, and D2-74383-LR products. Additional third part licensing is required for Dolby Pro Logic IIx.
5. 147MHz DSP clock speed represents an actual DSP clock of 147.456MHz, and 160MHz DSP clock speed represents an actual DSP clock of 159.744MHz, when using a crystal frequency of 24.576MHz.

# Table of Contents

## Absolute Maximum Ratings (Note 8)

Supply Voltage
- RVDD, PWMVDD, ADCVDD . . . . . . . . . . . . . . . . . . . . . . . . . . -0.3V to 4.0V
- CVDD, PLLVDD . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . -0.3V to 2.4V

Input Voltage
- Any Input but XTALI . . . . . . . . . . . . . . . . . . . . . . . . .-0.3V to RVDD +0.3V
- XTALI . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .-0.3V to PLLVDD +0.3V

Input Current, Any Pin but Supplies . . . . . . . . . . . . . . . . . . . . . . . . . ±10mA

## Thermal Information

| Thermal Resistance (Typical) | θJA (°C/W) | θJC (°C/W) |
|---|---|---|
| 128 Ld LQFP Package (Notes 6, 7) | 40 | 6.5 |

Maximum Storage Temperature. . . . . . . . . . . . . . . . . . . . -55°C to +150°C
Pb-Free Reflow Profile . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . see TB493

## Recommended Operating Conditions

Temperature Range . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .-10°C to +85°C
Digital I/O Supply Voltage, PWMVDD . . . . . . . . . . . . . . . . . . . . . . . . . .3.3V
Core Supply Voltage, CVDD . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .1.8V
Analog Supply Voltage, PLLVDD . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .1.8V

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

6. $\theta_{JA}$ is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
7. For $\theta_{JC}$, the "case temp" location is taken at the package top center.
8. Absolute Maximum parameters are not tested in production.

## Electrical Specifications

$T_A$ = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground. PLL at 294.912MHz, OSC at 24.576MHz, core running at 147.456MHz with typical audio data traffic. Minimum supply currents are measured in full power down configuration.

| PARAMETER | | SYMBOL | TEST CONDITIONS | MIN (Note 12) | TYP | MAX (Note 12) | UNIT |
|---|---|---|---|---|---|---|---|
| Digital Input High Logic Level (Note 9) | | $V_{IH}$ | RVDD = 3.3V (Scales with RVDD) | 2.0 | - | - | V |
| Digital Input Low Logic Level (Note 9) | | $V_{IL}$ | RVDD = 3.3V (Scales with RVDD) | - | - | 0.8 | V |
| High Level Output Drive Voltage ($I_{OUT}$ at - Pin Drive Strength Current, see "Pin Descriptions" on page 11) | | $V_{OH}$ | | RVDD - 0.4 | - | - | V |
| Low Level Output Drive Voltage ($I_{OUT}$ at + Pin Drive Strength Current, see "Pin Descriptions" on page 11) | | $V_{OL}$ | | - | - | 0.4 | V |
| High Level Input Drive Voltage XTALI Pin | | VIHX | | 0.7 | - | PLLVDD | V |
| Low Level Input Drive Voltage XTALI Pin | | VILX | | - | - | 0.3 | V |
| Input Leakage Current (Note 10) | | $I_{IN}$ | | - | - | ±10 | µA |
| Input Capacitance | | $C_{IN}$ | | - | 9 | - | pF |
| High Level Output Drive Voltage OSCOUT Pin | | VOHO | | PLLVDD - 0.3 | - | - | V |
| Low Level Output Drive Voltage OSCOUT Pin | | VOLO | | - | - | 0.3 | V |
| Output Capacitance | | $C_{OUT}$ | | - | 9 | - | pF |
| nRESET Pulse Width | | $t_{RST}$ | | - | 10 | - | ns |
| Typical Digital and PWM I/O Pad Ring Supply | (Voltage) | $R_{VDD}$/ $PWM_{VDD}$ | | 3.0 | 3.3 | 3.6 | V |
| | (Current, Active) | | | - | 15 | - | mA |
| | (Current, Power-down) | | | - | <1 | - | mA |
| Typical Core Supply | (Voltage) | CVDD | | 1.7 | 1.8 | 1.9 | V |
| | (Current, Active) | | | - | 450 | - | mA |
| | (Current, Power-down) | | | - | 15 | - | mA |
| Typical PLL Analog Supply | (Voltage) | PLLVDD | | 1.7 | 1.8 | 1.9 | V |
| | (Current, Active) | | | - | 25 | - | mA |
| | (Current, Power-down) | | | - | 10 | - | mA |
| Typical ADC Analog Supply | (Voltage) | ADCVDD | | 3.0 | 3.3 | 3.6 | V |
| | (Current, Active, Power-Down) | | | - | 12 | - | mA |

**Electrical Specifications** $T_A$ = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground. PLL at 294.912MHz, OSC at 24.576MHz, core running at 147.456MHz with typical audio data traffic. Minimum supply currents are measured in full power down configuration. **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 12) | TYP | MAX (Note 12) | UNIT |
|---|---|---|---|---|---|---|
| **CRYSTAL OSCILLATOR** | | | | | | |
| Crystal Frequency (Fundamental Mode Crystal) | Xo | | 20 | 24.576 | 24.822 (24.576 + 1%) | MHz |
| Duty Cycle | Dt | | 40 | - | 60 | % |
| Start-Up Time (Start-Up Time is Oscillator Enabled (with Valid Supply) to Stable Oscillation) | $t_{START}$ | | - | 5 | 20 | ms |
| **PLL** | | | | | | |
| VCO Frequency | $F_{VCO}$ | | 80.00 | 294.912 | 297.86 | MHz |
| Input Reference Frequency | $F_{IN}$ | | 20 | - | 24.822 (24.576 + 1%) | MHz |
| Feedback Dividers (Integer) | | | 4 | 12 | 15 | |
| PLL Lock Time from any Input Change | | | - | 2 | - | ms |
| **1.8V POWER-ON RESET** | | | | | | |
| Reset Enabled Voltage Level | $V_{EN}$ | | - | 1.1 | 1.4 | V |
| POR Pulse Width Rejection | $t_{REJ}$ | | - | 150 | 500 (Note 13) | µs |
| POR Minimum Output Pulse Width | $t_{DIS}$ | | - | 5 | - | µs |
| **1.8V BROWNOUT DETECTION** | | | | | | |
| Detect Level | | | 1.4 | 1.5 | 1.6 | V |
| Pulse Width Rejection | $t_{BOD1}$ | | - | 100 | - | ns |
| Minimum Output Pulse Width | $t_{O1}$ | | 20 | - | - | ns |
| **3.3V BROWNOUT DETECTION** | | | | | | |
| Detect Level | | | 2.5 | 2.7 | 2.9 | V |
| Pulse Width Rejection | $t_{BOD3}$ | | - | 100 | - | ns |
| Minimum Output Pulse Width | $t_{O3}$ | | 20 | - | - | ns |
| **ADC PERFORMANCE SPECIFICATIONS** | | | | | | |
| ADCREF DC Level | $V_{REF}$ | $I_{REF}$ = 0 | 1.3 | 1.4 | 1.5 | V |
| ADCREF Load Current | $I_{REF}$ | | - | - | ±20 | µA |
| ADCREF Source Impedance | $R_{REF}$ | | - | 14 | - | kΩ |
| Analog Input Level | $V_{AIN}$ | | $V_{REF}$ - 0.6 | - | $V_{REF}$ + 0.6 | V |
| Dynamic Range | | | - | 94 | - | dB |
| THD+N | | | - | -80 | - | dB |
| Gain Mismatch | | | - | 0.1 | - | dB |
| Crosstalk | | | - | -80 | - | dB |
| Power Supply Rejection | | | - | -70 | - | dB |

NOTES:

9. All input pins except XTALI.
10. Input leakage applies to all pins except XTALO.
11. Power-down is with device in reset and clocks stopped.
12. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
13. Limits established by characterization and are not production tested.

## Serial Audio Interface Port Timing

(Figure 2) $T_A$ = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground.

| SYMBOL | DESCRIPTION | MIN (Note 12) | TYP | MAX (Note 12) | UNIT |
|---|---|---|---|---|---|
| $tc_{SCLK}$ | SCKRx Frequency - SCKR0, SCKR1 | | | 12.5 | MHz |
| $tw_{SCLK}$ | SCKRx Pulse Width (High and Low) - SCKR0, SCKR1 | 40 | | | ns |
| $ts_{LRCLK}$ | LRCKRx Set-Up to SCLK Rising - LRCKR0, LRCKR1 | 20 | | | ns |
| $th_{LRCLK}$ | LRCKRx Hold from SCLK Rising - LRCKR0, LRCKR1 | 20 | | | ns |
| $ts_{SDI}$ | SDINx Set-Up to SCLK Rising - SDIN0, SDIN1 | 20 | | | ns |
| $th_{SDI}$ | SDINx Hold from SCLK Rising - SDIN0, SDIN1 | 20 | | | ns |
| $t_{dSDO}$ | SDOUTx Delay from SCLK Falling | | | 20 | ns |

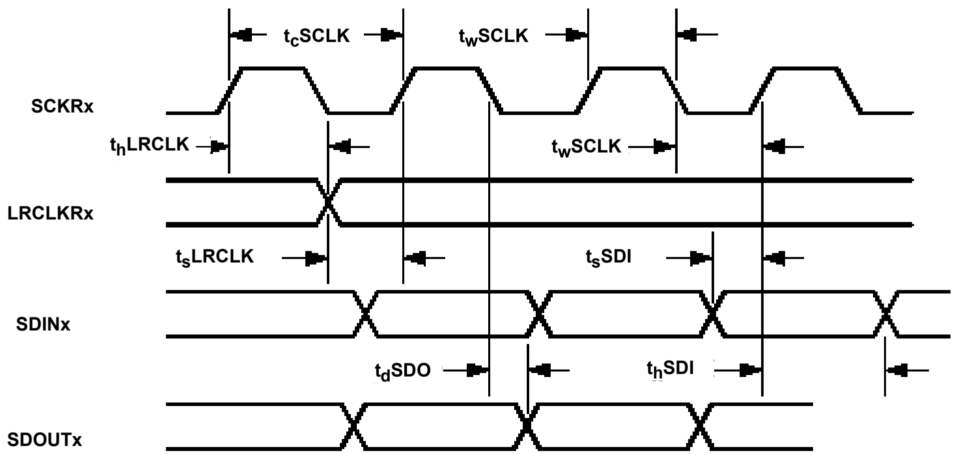



FIGURE 2. SERIAL AUDIO INTERFACE PORT TIMING

## Two-Wire ($I^2C$) Interface Port Timing

(Figure 3) $T_A$ = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground.

| SYMBOL | DESCRIPTION | MIN (Note 12) | TYPICAL | MAX (Note 12) | UNIT |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL Frequency | | | 100 | kHz |
| $t_{buf}$ | Bus Free Time Between Transmissions | 4.7 | | | µs |
| $tw_{lowSCLx}$ | SCL Clock Low | 4.7 | | | µs |
| $tw_{highSCLx}$ | SCL Clock High | 4.0 | | | µs |
| $ts_{STA}$ | Set-Up Time For a (Repeated) Start | 4.7 | | | µs |
| $th_{STA}$ | Start Condition Hold Time | 4.0 | | | µs |
| $th_{SDAx}$ | SDA Hold From SCL Falling (Note 14) | | 1 | | µs |
| $ts_{SDAx}$ | SDA Set-Up Time to SCL Rising | 250 | | | ns |
| $td_{SDAx}$ | SDA Output Delay Time From SCL Falling (Note 15) | | | 3.5 | µs |
| $t_r$ | Rise Time of Both SDA and SCL (Note 15) | | | 1 | µs |
| $t_f$ | Fall Time of Both SDA and SCL (Note 15) | | | 300 | ns |
| $ts_{STO}$ | Set-Up Time for a Stop Condition | 4.7 | | | µs |

NOTES:

14. Data is clocked in as valid on next XTALI rising edge after SCL goes low.
15. Limits established by characterization and not production tested.

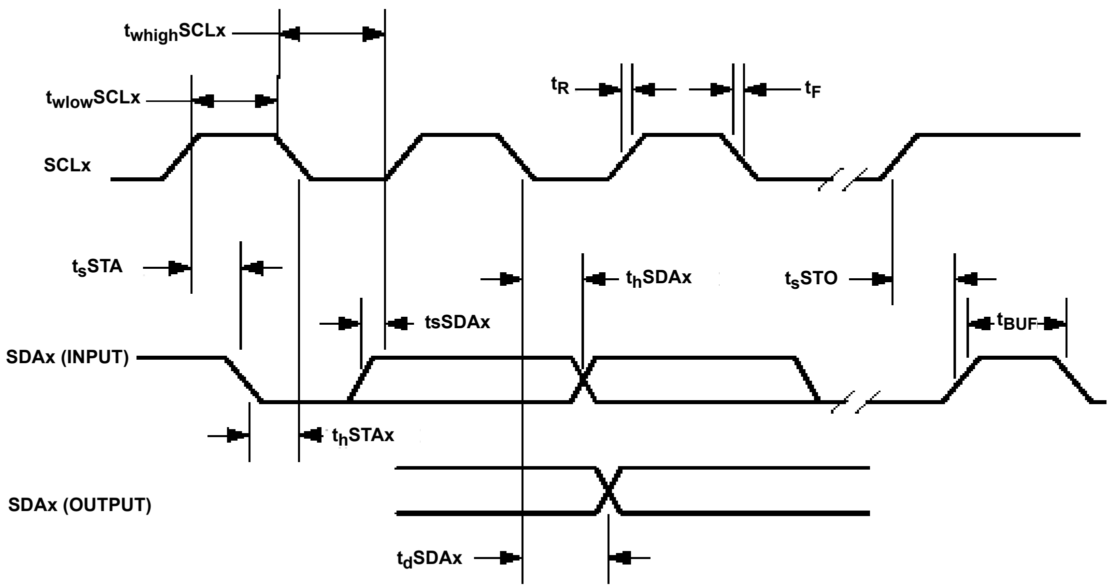



FIGURE 3. $I^2C$ INTERFACE TIMING

**SPI™ Interface Port Timing** (Figure 4) $T_A$ = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground.

| SYMBOL | DESCRIPTION | MIN (Note 12) | MAX (Note 12) | UNIT |
|---|---|---|---|---|
| **SPI MASTER MODE TIMING** | | | | |
| $t_V$ | MOSI Valid From Clock Edge | - | 8 | ns |
| $t_S$ | MISO Set-Up to Clock Edge | 10 | - | ns |
| $t_H$ | MISO Hold From Clock Edge | 1 system clock + 2ns | | |
| $t_{WI}$ | nSS Minimum Width | 3 system clocks + 2ns | | |
| **SPI SLAVE MODE TIMING** | | | | |
| $t_V$ | MISO Valid From Clock Edge | 3 system clocks + 2ns | | |
| $t_S$ | MOSI Set-Up to Clock Edge | 10 | - | ns |
| $t_H$ | MOSI Hold From Clock Edge | 1 system clock + 2ns | | |
| $t_{WI}$ | nSS Minimum Width | 3 system clocks + 2ns | | |

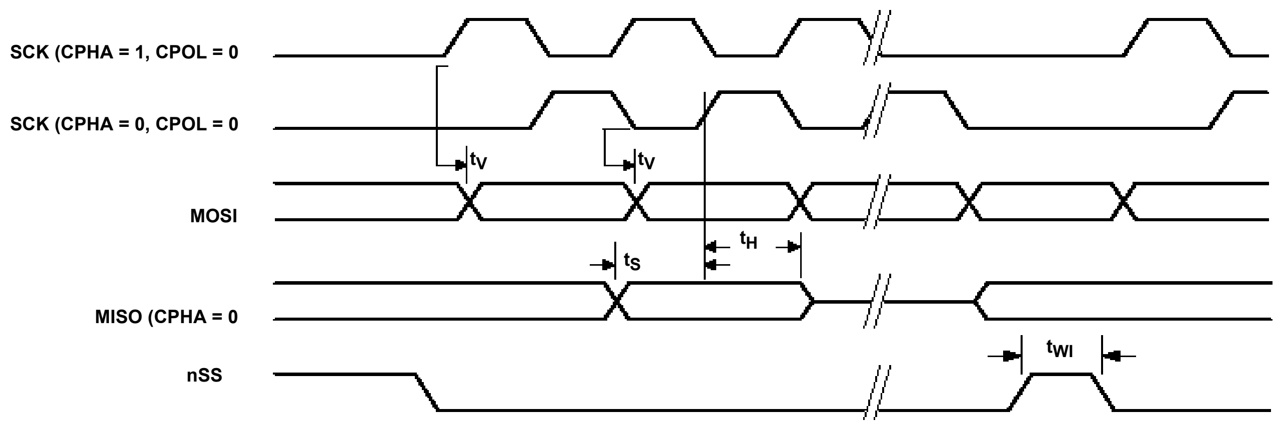
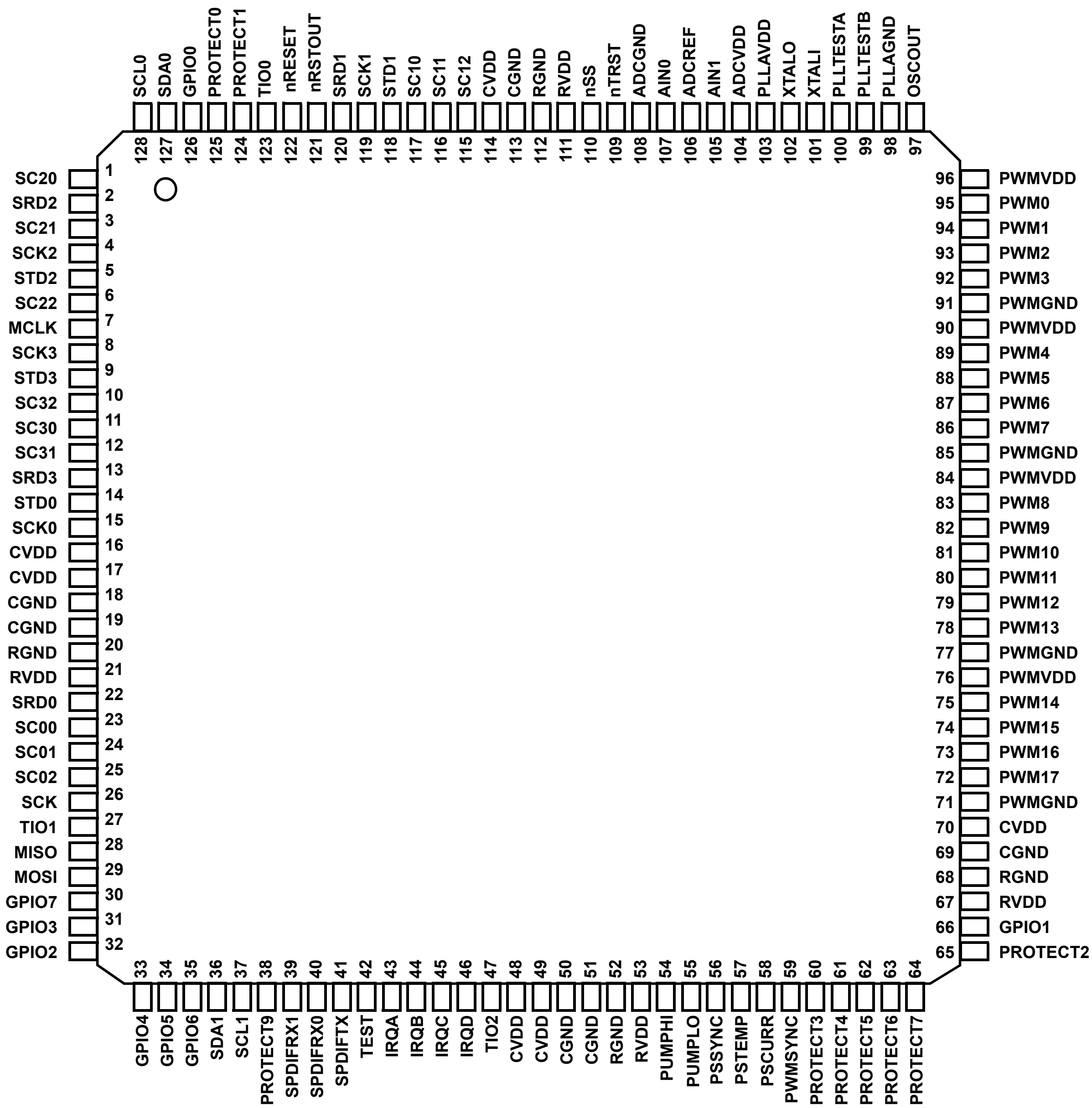



**FIGURE 4. SPI TIMING**

## Pin Configuration



# Pin Descriptions

| PIN | PIN NAME (Note 16) | TYPE | VOLTAGE LEVEL (V) | DRIVE STRENGTH (mA) | DESCRIPTION |
|---|---|---|---|---|---|
| 1 | SC20 | I/O | 3.3 | 8 | Serial Audio Interface 2, $I^2S0$ SCLK |
| 2 | SRD2 | I/O | 3.3 | 4 | Serial Audio Interface 2, $I^2S0$ SDIN |
| 3 | SC21 | I/O | 3.3 | 8 | Serial Audio Interface 2, $I^2S0$ LRCK |
| 4 | SCK2 | I/O | 3.3 | 8 | Serial Audio Interface 2, $I^2S1$ SCLK |
| 5 | STD2 | I/O | 3.3 | 8 | Serial Audio Interface 2, $I^2S1$ SDIN |
| 6 | SC22 | I/O | 3.3 | 4 | Serial Audio Interface 2, $I^2S1$ LRCK |
| 7 | MCLK | O | 3.3 | 16 | $I^2S$ Serial Audio Master Clock output for external ADC/DAC components, drives low on reset and is enabled by firmware assignment. |
| 8 | SCK3 | I/O | 3.3 | 8 | Serial Audio Interface 3, $I^2S3$ SCLK |
| 9 | STD3 | I/O | 3.3 | 8 | Serial Audio Interface 3, $I^2S3$ SDIN |
| 10 | SC32 | I/O | 3.3 | 8 | Serial Audio Interface 3, $I^2S3$ LRCK |
| 11 | SC30 | I/O | 3.3 | 8 | Serial Audio Interface 3, $I^2S2$ SCLK |
| 12 | SC31 | I/O | 3.3 | 8 | Serial Audio Interface 3, $I^2S2$ LRCK |
| 13 | SRD3 | I/O | 3.3 | 4 | Serial Audio Interface 3, $I^2S2$ SDIN |
| 14 | STD0 | I/O | 3.3 | 8 | Serial Audio Interface 0, $I^2S$ SDAT0 |
| 15 | SCK0 | I/O | 3.3 | 8 | Serial Audio Interface 0, $I^2S$ LRCK0 |
| 16, 17, 48, 49, 70, 114 | CVDD | P | 3.3 | | Core power, 1.8V |
| 18, 19, 50, 51, 69, 113 | CGND | P | 3.3 | | Core ground |
| 20 | RGND | P | 3.3 | | Digital pad ring ground. Internally connected to PWMGND. |
| 21 | RVDD | P | 3.3 | | Digital pad ring power, 3.3V. This 3.3V supply is used for all the digital I/O pad drivers and receivers, except for the analog pads. Internally connected to PWMVDD. |
| 22 | SRD0 | I/O | 3.3 | 4 | Serial Audio Interface 0, SDIO, Defaults to input, and may be configured as GPIO by firmware. |
| 23 | SC00 | I/O | 3.3 | 8 | Serial Audio Interface 0, SDIO, Defaults to input, and may be configured as GPIO by firmware. |
| 24 | SC01 | I/O | 3.3 | 8 | Serial Audio Interface 0, $I^2S$ SDAT1 |
| 25 | SC02 | I/O | 3.3 | 8 | Serial Audio Interface 0, $I^2S$ LRCK1 |
| 26 | SCK | I/O | 3.3 | 4 | SPI clock I/O with hysteresis input. |
| 27 | TIO1 | I/O | 3.3 | 16 | Timer I/O port 1. Operation and assignment is controlled by firmware. Leave unconnected when not in use. |
| 28 | MISO | I/O | 3.3 | 4 | SPI master input, slave output data signal. |
| 29 | MOSI | I/O | 3.3 | 4 | SPI master output, slave input data signal. |
| 30 | GPIO7 | I/O | 3.3 | 16 | General purpose I/O Bidirectional GPIO port. (One of 8 GPIO. Resets to input port. Operation and assignment is defined by product application's firmware.) |
| 31 | GPIO3 | I/O | 3.3 | 16 | General purpose I/O Bidirectional GPIO port. (One of 8 GPIO. Resets to input port. Operation and assignment is defined by product application's firmware.) |
| 32 | GPIO2 | I/O | 3.3 | 16 | General purpose I/O Bidirectional GPIO port. (One of 8 GPIO. Resets to input port. Operation and assignment is defined by product application's firmware.) |
| 33 | GPIO4 | I/O | 3.3 | 16 | General purpose I/O Bidirectional GPIO port. (One of 8 GPIO. Resets to input port. Operation and assignment is defined by product application's firmware.) |

# Pin Descriptions (Continued)

| PIN | PIN NAME (Note 16) | TYPE | VOLTAGE LEVEL (V) | DRIVE STRENGTH (mA) | DESCRIPTION |
|---|---|---|---|---|---|
| 34 | GPIO5 | I/O | 3.3 | 16 | General purpose I/O Bidirectional GPIO port. (One of 8 GPIO. Resets to input port. Operation and assignment is defined by product application's firmware.) |
| 35 | GPIO6 | I/O | 3.3 | 16 | General purpose I/O Bidirectional GPIO port. (One of 8 GPIO. Resets to input port. Operation and assignment is defined by product application's firmware.) |
| 36 | SDA1 | I/O | 3.3 | 8 - OD | Two-Wire Serial data port 1. Bidirectional signal used by both the master and slave controllers for data transport. |
| 37 | SCL1 | I/O | 3.3 | 8 - OD | Two-Wire Serial clock port 1. Bidirectional signal is used by both the master and slave controllers for clock signaling. |
| 38 | PROTECT9 | I/O | 3.3 | 4 | PWM protection input with hysteresis. (One of 9 protection inputs. Specific function and channel assignment is defined by firmware.) |
| 39 | SPDIFRX1 | I | 3.3 | - | S/PDIF Digital audio data input 1 |
| 40 | SPDIFRX0 | I | 3.3 | - | S/PDIF Digital audio data input 0 |
| 41 | SPDIFTX | O | 3.3 | 4 | S/PDIF Digital audio output. (Audio content and audio processing signal flow is dependent upon firmware, driving stereo output up to 192kHz.) |
| 42 | TEST | I | 3.3 | - | Factory test use only. Must be tied low. |
| 43 | IRQA | I | 3.3 | - | Interrupt request port A, Boot mode select. One of four IRQ pins. Connects to logic high (3.3V) or to ground & High/Low logic status establishes boot mode selection upon de-assertion of reset (nRESET) cycle. |
| 44 | IRQB | I | 3.3 | - | Interrupt request port B, Boot mode select. One of four IRQ pins. Connects to logic high (3.3V) or to ground & High/Low logic status establishes boot mode selection upon de-assertion of reset (nRESET) cycle. |
| 45 | IRQC | I | 3.3 | - | Interrupt request port C, Boot mode select. One of four IRQ pins. Connects to logic high (3.3V) or to ground & High/Low logic status establishes boot mode selection upon de-assertion of reset (nRESET) cycle. |
| 46 | IRQD | I | 3.3 | - | Interrupt request port D, Boot mode select. One of four IRQ pins. Connects to logic high (3.3V) or to ground & High/Low logic status establishes boot mode selection upon de-assertion of reset (nRESET) cycle. |
| 47 | TIO2 | I/O | 3.3 | 16 | Timer I/O port 2. Operation and assignment is controlled by firmware. Leave unconnected when not in use. |
| 52 | RGND | P | 3.3 | - | Digital pad ring ground. Internally connected to PWMGND. |
| 53 | RVDD | P | 3.3 | - | Digital pad ring power, 3.3V. This 3.3V supply is used for all the digital I/O pad drivers and receivers, except for the analog pads. Internally connected to PWMVDD. |
| 54 | PUMPHI | I/O | 3.3 | 16 | Assignable I/O. Function and operation defined by firmware. |
| 55 | PUMPLO | I/O | 3.3 | 16 | Assignable I/O. Function and operation defined by firmware. |
| 56 | PSSYNC | I/O | 3.3 | 16 | Synchronizing output signal to switching power supply. (Operates under specification of firmware and resets to high impedance inactive state when not used.) |
| 57 | PSTEMP | I/O | 3.3 | 4 | Assignable I/O. Function and operation defined by firmware. |
| 58 | PSCURR | I/O | 3.3 | 4 | Assignable I/O. Function and operation defined by firmware. |
| 59 | PWMSYNC | I/O | 3.3 | 16 | PWM synchronization port. (Function and operation is defined by firmware.) |
| 60 | PROTECT3 | I/O | 3.3 | 4 | PWM protection input with hysteresis. (One of 9 protection inputs. Specific function and channel assignment is defined by firmware.) |
| 61 | PROTECT4 | I/O | 3.3 | 4 | PWM protection input with hysteresis. (One of 9 protection inputs. Specific function and channel assignment is defined by firmware.) |
| 62 | PROTECT5 | I/O | 3.3 | 4 | PWM protection input with hysteresis. (One of 9 protection inputs. Specific function and channel assignment is defined by firmware.) |

## Pin Descriptions (Continued)

| PIN | PIN NAME (Note 16) | TYPE | VOLTAGE LEVEL (V) | DRIVE STRENGTH (mA) | DESCRIPTION |
|---|---|---|---|---|---|
| 63 | PROTECT6 | I/O | 3.3 | 4 | PWM protection input with hysteresis. (One of 9 protection inputs. Specific function and channel assignment is defined by firmware.) |
| 64 | PROTECT7 | I/O | 3.3 | 4 | PWM protection input with hysteresis. (One of 9 protection inputs. Specific function and channel assignment is defined by firmware.) |
| 65 | PROTECT2 | I/O | 3.3 | 4 | PWM protection input with hysteresis. (One of 9 protection inputs. Specific function and channel assignment is defined by firmware.) |
| 66 | GPIO1 | I/O | 3.3 | 16 | General purpose I/O Bidirectional GPIO port. (One of 8 GPIO. Resets to input port. Operation and assignment is defined by product application's firmware.) |
| 67 | RVDD | P | 3.3 | - | Digital pad ring power, 3.3V. This 3.3V supply is used for all the digital I/O pad drivers and receivers, except for the analog pads. Internally connected to PWMVDD. |
| 68 | RGND | P | 3.3 | - | Digital pad ring ground. Internally connected to PWMGND. |
| 71 | PWMGND | P | 3.3 | - | PWM output pin ground. Internally connected to RGND. |
| 72 | PWM17 | I/O | 3.3 | 8 or 16 | PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.) |
| 73 | PWM16 | I/O | 3.3 | 8 or 16 | PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.) |
| 74 | PWM15 | I/O | 3.3 | 8 or 16 | PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.) |
| 75 | PWM14 | I/O | 3.3 | 8 or 16 | PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.) |
| 76 | PWMVDD | P | 3.3 | - | PWM output pin power. This 3.3V supply is used for the PWM pad drivers. Internally connected to RVDD. |
| 77 | PWMGND | P | 3.3 | - | PWM output pin ground. Internally connected to RGND. |
| 78 | PWM13 | I/O | 3.3 | 8 or 16 | PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.) |
| 79 | PWM12 | I/O | 3.3 | 8 or 16 | PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.) |
| 80 | PWM11 | I/O | 3.3 | 8 or 16 | PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.) |
| 81 | PWM10 | I/O | 3.3 | 8 or 16 | PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.) |
| 82 | PWM9 | I/O | 3.3 | 8 or 16 | PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.) |
| 83 | PWM8 | I/O | 3.3 | 8 or 16 | PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.) |
| 84 | PWMVDD | P | 3.3 | - | PWM output pin power. This 3.3V supply is used for the PWM pad drivers. Internally connected to RVDD. |
| 85 | PWMGND | P | 3.3 | - | PWM output pin ground. Internally connected to RGND. |
| 86 | PWM7 | I/O | 3.3 | 8 or 16 | PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.) |
| 87 | PWM6 | I/O | 3.3 | 8 or 16 | PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.) |
| 88 | PWM5 | I/O | 3.3 | 8 or 16 | PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.) |
| 89 | PWM4 | I/O | 3.3 | 8 or 16 | PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.) |

## Pin Descriptions (Continued)

| PIN | PIN NAME (Note 16) | TYPE | VOLTAGE LEVEL (V) | DRIVE STRENGTH (mA) | DESCRIPTION |
|---|---|---|---|---|---|
| 90 | PWMVDD | P | 3.3 | - | PWM output pin power. This 3.3V supply is used for the PWM pad drivers. Internally connected to RVDD. |
| 91 | PWMGND | P | 3.3 | - | PWM output pin ground. Internally connected to RGND. |
| 92 | PWM3 | I/O | 3.3 | 8 or 16 | PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.) |
| 93 | PWM2 | I/O | 3.3 | 8 or 16 | PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.) |
| 94 | PWM1 | I/O | 3.3 | 8 or 16 | PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.) |
| 95 | PWM0 | I/O | 3.3 | 8 or 16 | PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.) |
| 96 | PWMVDD | P | 3.3 | - | PWM output pin power. This 3.3V supply is used for the PWM pad drivers. Internally connected to RVDD. |
| 97 | OSCOUT | P | 1.8 | - | Analog oscillator output to slave D2-71x83 devices. OSCOUT drives a buffered version of the crystal oscillator signal from the XTALI pin. |
| 98 | PLLAGND | P | 1.8 | - | PLL Analog ground |
| 99 | PLLTESTB | O | 1.8 | - | Factory test use only. Must be tied low. |
| 100 | PLLTESTA | O | 1.8 | - | Factory test use only. Must be tied low. |
| 101 | XTALI | P | 1.8 | - | Crystal oscillator analog input port. An external clock source would be driven into the this port. In multi-D2-71x83 systems, the OSCOUT from the master D2-71x83 would drive the XTALI pin. |
| 102 | XTALO | P | 1.8 | - | Crystal oscillator analog output port. When using an external clock source, this pin must be open. XTALO does not have a drive strength specification. |
| 103 | PLLAVDD | P | 1.8 | - | PLL Analog power, 1.8V |
| 104 | ADCVDD | P | 3.3 | - | Analog power for internal ADC, 3.3V |
| 105 | AIN1 | I | 3.3 | - | Analog input 1 to internal ADC |
| 106 | ADCREF | O | 3.3 | - | Analog voltage reference output. Must be de-coupled to analog ground with 1µF capacitor. |
| 107 | AIN0 | I | 3.3 | - | Analog input 0 to internal ADC |
| 108 | ADCGND | P | 3.3 | | Analog ground for internal ADC |
| 109 | nTRST | I | 3.3 | - | Factory test only. Must be tied high at all times. |
| 110 | nSS | I/O | 3.3 | 4 | SPI slave select I/O. |
| 111 | RVDD | P | 3.3 | - | Digital pad ring power, 3.3V. This 3.3V supply is used for all the digital I/O pad drivers and receivers, except for the analog pads. Internally connected to PWMVDD. |
| 112 | RGND | P | 3.3 | - | Digital pad ring ground. Internally connected to PWMGND. |
| 115 | SC12 | I/O | 3.3 | 8 | Serial Audio Interface 1, LRCK |
| 116 | SC11 | I/O | 3.3 | 8 | Serial Audio Interface 1, SDAT3 |
| 117 | SC10 | I/O | 3.3 | 8 | Serial Audio Interface 1, data (Assignment by firmware control.) |
| 118 | STD1 | I/O | 3.3 | 8 | Serial Audio Interface 1, SDAT2 |
| 119 | SCK1 | I/O | 3.3 | 8 | Serial Audio Interface 1, SCK |
| 120 | SRD1 | I/O | 3.3 | 4 | Serial Audio Interface 1, data (Assignment by firmware control.) |
| 121 | nRSTOUT | O | 3.3 | 16 - OD | Active low open drain reset output. Pin drives low from POR generator, 3.3V brown out detector going active, or from 1.8V brown out detector going active. This output should be used to initiate a system reset to the nRESET pin upon brownout event detection. |

# Pin Descriptions (Continued)

| PIN | PIN NAME (Note 16) | TYPE | VOLTAGE LEVEL (V) | DRIVE STRENGTH (mA) | DESCRIPTION |
|---|---|---|---|---|---|
| 122 | nRESET | I | 3.3 | - | Active low reset input with hysteresis. Activates system level reset when pulled low, initializing all internal logic and program operations. System latches boot mode selection of the IRQ input pins on the rising edge. |
| 123 | TIO0 | I/O | 3.3 | 16 | Timer I/O port 0. Operation and assignment is controlled by firmware. Leave unconnected when not in use. |
| 124 | PROTECT1 | I/O | 3.3 | 4 | PWM protection input with hysteresis. (One of 9 protection inputs. Specific function and channel assignment is defined by firmware.) |
| 125 | PROTECT0 | I/O | 3.3 | 4 | PWM protection input with hysteresis. (One of 9 protection inputs. Specific function and channel assignment is defined by firmware.) |
| 126 | GPIO0 | I/O | 3.3 | 16 | General purpose I/O Bidirectional GPIO port. (One of 8 GPIO. Resets to input port. Operation and assignment is defined by product application's firmware.) |
| 127 | SDA0 | I/O | 3.3 | 8 - OD | Two-Wire Serial data port 0. Bidirectional signal used by both the master and slave controllers for data transport. |
| 128 | SCL0 | I/O | 3.3 | 8 - OD | Two-Wire Serial clock port 0. Bidirectional signal is used by both the master and slave controllers for clock signaling. |

NOTES:

16. Unless otherwise specified all pin names are active high. Those that are active low have an “n” prefix.
17. All power and ground pins of same names are to be tied together to all other pins of their same name. (i.e., CVDD pins to be tied together, CGND pins to be tied together, RVDD pins to be tied together, and RGND pins to be tied together.) CGND and RGND are to be tied together on board. RGND and PWMGND pins are also internally connected and are to be tied together.

## Functional Block Diagram

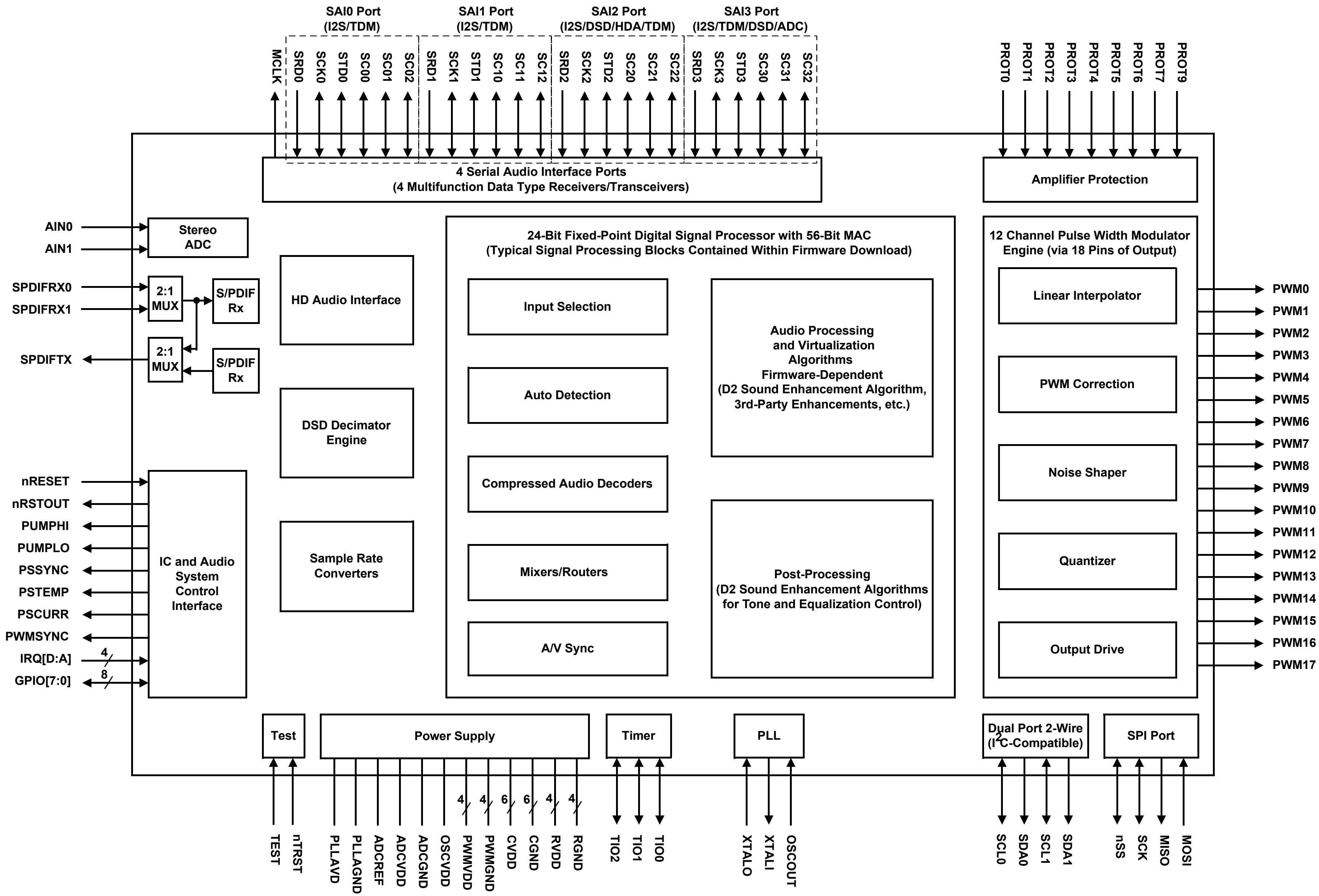



**FIGURE 5. D2-6 FAMILY IC FUNCTIONAL BLOCK DIAGRAM**

# Introduction

The D6 family of ICs provide the core functionality, amplifier control, and complete audio signal processing for D2 Audio's Class-D amplifier solutions. A variety of reference designs from Renesas D2 Audio DSP include specific signal flows designed for their applications, supporting today's design features. Support is also provided for future planned features, with little or no additional hardware or logic to enable new features. The signal flow, digital audio I/O, and amplifier hardware control support is handled completely by the D2-6 family firmware.

The products are targeted at high-volume Home Theater in a Box (HTiB), Multimedia, Soundbar, and similar solutions, where rich features and cost-effective quality audio are required to meeting demands of current consumer electronics markets.

The D2-6 family devices are completely pin-compatible with the D2-3 family family devices, allowing full flexibility for function vs cost trade-off, providing cost-effective solutions for applications of varying end-user features and capabilities.

## Target Performance

Typical systems built around the D2-6 family support performances that includes or exceeds:

- >110 dB SNR/dynamic range system support
- <0.06% THD+N at full scale at 1kHz
- 20Hz to 20kHz audio frequency response
- Scalable amplifier power control capability
- Discrete component and integrated power stages using full-bridge, half-bridge, and BTL output topologies
- Encrypted code loads and unique decryption for each IC part number
- Support for all standard audio data delivery formats and protocols employed in the target markets
- The delivery formats include: $I^2S$, left-justified, Time-Division Multiplexed (TDM), S/PDIF, DSD, HDA, 2-channel analog

## Application Markets

The powerful DSP coupled with flexible peripherals and excellent signal processing hardware results in a chip for solutions that cover many markets. All are characterized by the need for complex signal processing and high audio channel count. Typical applications include a wide variety of cost sensitive but feature-demanding performance such as in:

- Multimedia speaker solutions
- Multi-driver (Bi-Amp, Tri-Amp) speaker arrays
- Home theater systems with compressed audio decoder
- Soundbar system solutions
- Set-top box solutions
- Low-cost virtualized stereo, 5.1, 7.1, and 9.1 AVR systems
- Bluetooth/WiFi voice-enabled speaker systems
- Aftermarket/OEM automotive amplifiers

## System Features and Support

The D2-6 enables multiple solutions consisting of a class-D amplifier system built around internal audio processing functional blocks. Features include:

- Flexible audio input and output configurations
  - Four independent asynchronous $I^2S$ digital inputs
  - Support of 8 audio channels of HDMI
  - HD Audio (HDA)
  - Direct Stream Digital™ (DSD) input support
  - Integrated high-performance stereo ADC
  - Dual multiplexed S/PDIF™ digital audio inputs (Linear IEC-61958 PCM or compressed IEC-61937 audio)
  - S/PDIF Digital Audio PCM Output
  - Line-level Outputs (Left, Right, Subwoofer) using passive or active output filter stages
- Flexible DSP clock speed and DSP memory capacity options
  - 147.456MHz DSP clock speed devices, with 24k X and Y memory and 32k P memory capacity
  - 159.744MHz DSP clock speed devices, with 24k X and Y memory and 32k P memory capacity
- Real-time amplifier control and monitoring
  - Supports bridged, half-bridged, and Bridge-Tied Load (BTL) topologies, using discrete or integrated power stages from 10W to over 500W
  - Graceful protection and recovery
  - Complete fault protection with automatic recovery
- Serial control interface using $I^2C$, HDA, SPI, or SCI
- Decoding of Compressed audio formats, including
  - Dolby® Digital/AC3
  - Dolby® Pro Logic IIx
  - AAC™ LC
  - DTS® Digital Surround
  - Dolby® Digital Plus
- Audio enhancement feature support
  - D2 Audio DSP Sound Enhancement Algorithm audio processing enhancement

## Audio Processing Signal Flow Support

The D2-6 family series of ICs support a wide variety of signal flows and audio processing options that are fully programmable and are completely defined by the system firmware and system architecture.

The firmware provided for the D2-6 family is application-specific and includes its own specific signal flow and associated performance level. Much of the signal flow is also hardware dependent and that hardware integrates with the full system architecture that is defined within that system's programmed firmware. Each firmware design includes a specific set of control tool support, including the D2 Audio DSP customization GUI software and system design data.

Additional design-specific reference documentation is included within each firmware application design, that includes platform-specific signal flows, control registers, and descriptions of advanced processing features.

The various system support capabilities include:

- Flexible system configuration with 8 audio input and audio processing channels, with up to 12 audio output PWM channels, supporting differential or single-end PWM outputs with up to 18 PWM output pins.
- Audio processing for up to 4 simultaneous stereo asynchronous digital audio inputs from a variety of sources (HDA, I$^2$S, HDMI, DSD, S/PDIF Digital)
- Multiple D2-6 family devices may be cascaded to support higher channel count designs.

# Functional Description

The D2-6 family of ICs, integrated into D2 Audio DSP offerings of reference design platforms support present and future design features with little or no additional hardware or logic to enable new features.

## Audio Input

Multiple versions of the D2-6 family IC-based reference designs support a wide range of market applications and each of these market applications has a variety of potential audio sources such as:

- Mono and stereo analog inputs
- Serial audio, I$^2$S and Time Division Multiplexed (TDM) Single Line "Network" mode
- HD-audio interface (UAA-Class Driver Capable)
- Stereo and multichannel DSD
- S/PDIF digital (IEC60958-compliant and IEC61937-compliant)

### SERIAL AUDIO INPUT

Because most systems incorporate some mix of digital and analog inputs, the D2-6 family offers a very flexible digital audio peripheral interface. The D2-6 family features four independent Serial Audio Interface (SAI) ports. All SAI ports support both master or slave clocking and can support sample rates from 32kHz to 192kHz.

Each SAI port supports the digital audio industry I$^2$S standard, which supports carrying up to 24-bit Linear PCM audio words per subframe IEC60958, or compressed digital audio (Dolby® Digital, AAC, DTS®, MPEG, etc.) packing per the IEC61937 specification. The SAI port also supports left-justified formatted linear PCM or compressed digital audio. Each SAI port supports time division multiplexing (TDM) capability (also known as "Network mode") with up to 32 words per frame.

SAI Ports 2 and 3 (the 3rd and 4th ports) have multiplexed inputs to provide a standard input signal flow for the ADC, DSD, and HDA audio interfaces. All serial audio input data streams go through an SAI interface, which simplifies the data flow configuration.

SAI data formats are shown in Figure 6. For I$^2$S format, the left channel data is read when LRCK is low. For the left-justified format, the left channel data is read when LRCK is high. Either format requires data to be valid on the rising edge of SCLK and sent MSB-first on SDIN with 32 bits of data per channel. Each set of digital inputs runs asynchronously to the others and may accept different sample rates and formats.

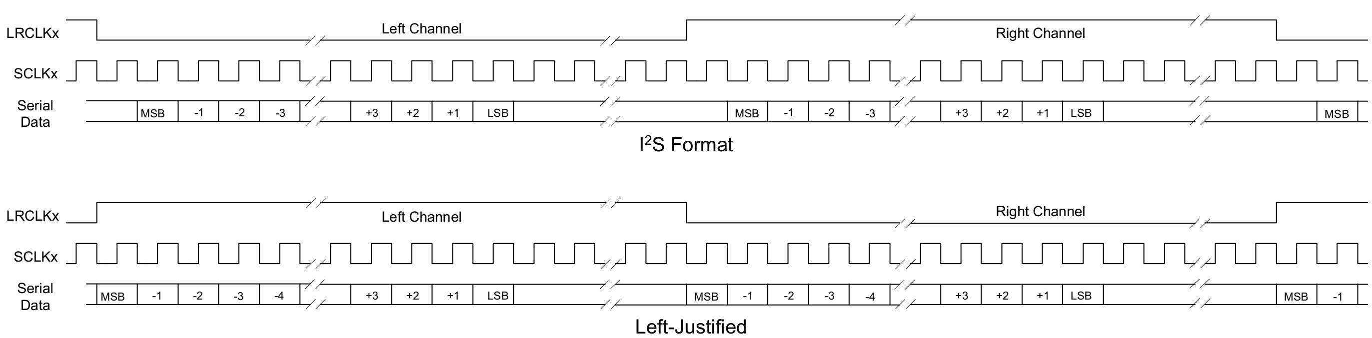



**FIGURE 6. SAI PORT SUPPORTED DATA FORMATS FOR DELIVERY OF LINEAR PCM OR COMPRESSED AUDIO DATA**

### S/PDIF RECEIVER

The D2-6 family contains two input pins internally multiplexed into one IEC60958 compliant S/PDIF Digital receiver. The receiver input pins are 3.3V CMOS input level compatible, requiring external circuitry to condition the serial input. The receiver contains an input transition detector, digital PLL clock recovery, and a decoder to separate audio, channel status, and user data. Only the first 24-channel status bits are supported. The receiver constantly monitors the incoming data stream to detect the IEC61937-1 packet headers, and if found, captures the Pc and Pd data words into registers. The receiver meets the jitter tolerance specified in IEC60958-4.

S/PDIF is a commonly used interface for receiving compressed (IEC61937-compliant) and stereo PCM (IEC60958-compliant) audio data. This interface also supports receipt of compressed audio data that is not compliant with the IEC61937 specification, but instead meets the IEC60958 specification.

### ADC INPUT

The D2-6 family contains a high-performance Analog-to-Digital Converter (ADC) that connects to input analog sources with a minimum of interface circuitry. At a bandwidth of 20kHz at nominal voltage and temperature, the ADC input of the D2-6 family provides a typical THD+N (unweighted) value of -81dB and an SNR/dynamic range of 94dB.

The ADC master clock can be supplied from either the low jitter PLL of the D2-6 family, or from the HD audio interface. When the PLL provides the ADC master clock, the ADC operates synchronous to the DSP processing, which minimizes noise pickup. When operated from the HD audio clock system, the ADC decimator output is synchronous to the HDA frame rate, eliminating the need for sample rate conversion to the HDA frame rate. Figure 7 shows the ADC decimator frequency response over full bandwidth and passband, and Figure 8 shows the ADC performance with full scale input processed through the SRC to a 48kHz sample rate.

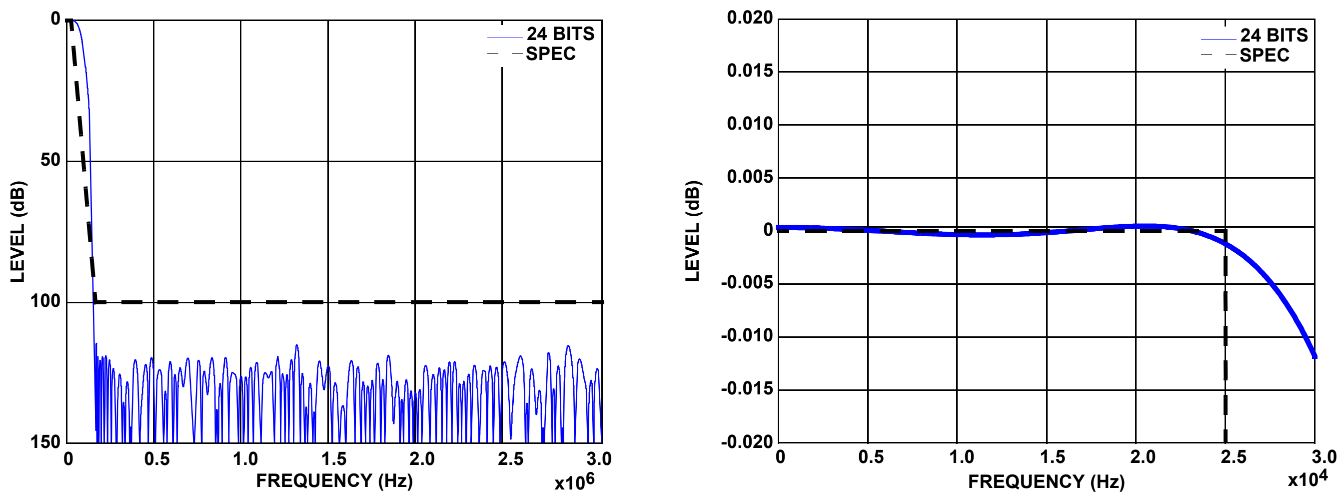



FIGURE 7. ADC DECIMATOR FREQUENCY RESPONSE (256 TAPS DECIMATE BY 32)

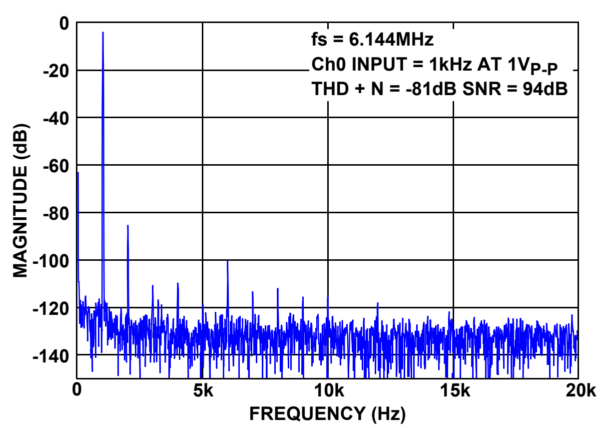



FIGURE 8. ADC PERFORMANCE AT FULL SCALE INPUT

## DSD

The HDMI specification (version 1.2 and later) used in TV systems supports streaming DSD encoded audio over HDMI. To support this, the system can receive and process up to six DSD audio streams. The DSD interface supports both standard and phase-modulated data formats. A high-quality 16x decimator engine converts all of the DSD data streams into 24-bit PCM words with an FS of 176.4kHz using a 128-tap FIR filter. The DSD decimation filter has a cutoff frequency of 50kHz and is optimized for passband flatness.

SAI Ports 2 and 3 support DSD format inputs. When the DSD interface is enabled, all the pins of SAI 2 and the SC21 pin of SAI3 become the DSD input signals. The six channels of DSD audio are merged into three $I^2S$ PCM streams at a 176.4kHz sample rate. These $I^2S$ streams are routed into both receivers on SAI 2 and the first receiver of SAI 3. The data is then passed to the Sample Rate Converter (SRC). The SRC rate-locks to the DSD input clock and attenuates any jitter in the DSD input stream.

The DSD input processing clusters the DSD data into channel pairs. This allows a flexible channel count of 2, 4, or all 6 DSD data streams to be handled. Using 4-channel DSD frees the SAI 3 port for other uses. Similarly, using only 2-channel DSD frees the second SAI 2 port and the SAI 3 port for other uses.

The D2-6 family of ICs also offers digital audio format conversion support for DSD stereo format input to S/PDIF or $I^2S$ format output, as well as DSD multichannel format input to multiple $I^2S$ format output. This high-quality digital audio format conversion path also offers the ability to reduce clock jitter in the audio system introduced by certain transmission paths such as HDMI.

This technique also enables consumer products to output a downsampled and/or downmixed (if necessary) digital audio output for audio that may not otherwise be made available to the consumer in the original higher-bandwidth format due to certain consumer electronic/content protection licensing restrictions.

The graphs in Figure 9 show the DSD decimation filter frequency response at two different frequency zoom levels.

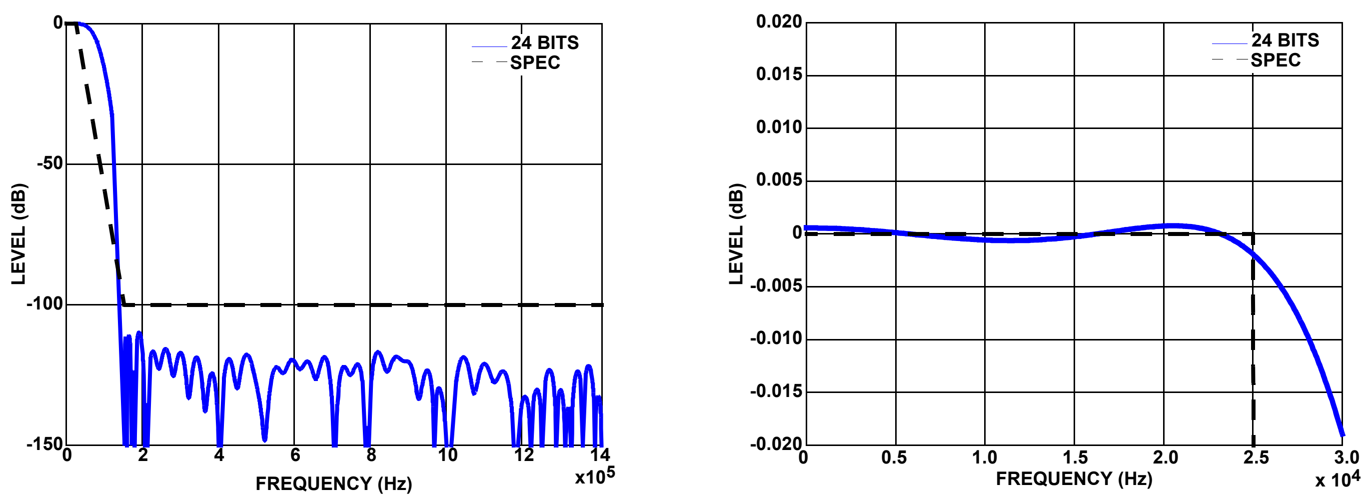



FIGURE 9. DSD DECIMATOR FREQUENCY RESPONSE (128 TAPS DECIMATE BY 16)

## Audio Output

### PWM AUDIO AMPLIFIER OUTPUT

The D2-6 family supports multiple PWM output topologies, which enables system designs to use an output stage, which meets the cost and performance requirements of the particular application. Twelve PWM channels are mapped to 18 PWM output pins by the programmed firmware. The PWM output pins are 3.3V CMOS levels with either 8mA or 16mA drive capability.

Output topologies supported include:

- Half-bridge, N+N or N+P
- Full-bridge, N+N or N+P using 2-level modulation, 2 or 4-quadrant control

### LINE LEVEL OUTPUT

In addition to amplified outputs, the D2-6 family IC also supports line-level outputs that generate a nominal $1V_{RMS}$ output using a simple passive filter.

Headphone outputs or line-level outputs that require a $2V_{RMS}$ (or higher output level) are also supported, using an active filter to accomplish the signal level needs.

### S/PDIF TRANSMITTER

The D2-6 family contains one IEC60958 compatible S/PDIF Digital transmitter. The transmitter complies with the consumer applications defined in IEC60958-3. The transmitter supports 24-bit audio data, 24-bit user data, and 30-bit channel status data.

A bit-exact pass-through mode from the selected SPDIFRX[1:0] input is also supported. This simplifies system designs that require that the IEC61937-compliant original compressed audio bitstream be made available at the back panel of the product, as well as giving the user the capability to select a decoded (and downmixed, if necessary) IEC60958-compliant stereo or mono linear PCM output for digital audio recording/playback capabilities.

The D2-6 family optional firmware offers digital audio format conversion support for $I^2S$ digital format input to S/PDIF digital format output, as well as S/PDIF digital format input to $I^2S$ digital format output, for all digital audio Linear PCM (non-compressed) audio sources. This functionality is not available for compressed audio inputs, unless the compressed audio data is first decoded by the internal DSP, and if necessary, downmixed to two channels.

This format conversion path offers the ability to reduce the clock jitter on the output due to the fact that both inputs (when in this mode) pass through the professional-grade Sample-Rate Converters (SRC). This approach also enables consumer products to output a downsampled digital audio output for audio that may not otherwise be made available to the consumer in the original higher-bandwidth format due to certain consumer electronic/content protection licensing restrictions.

### SERIAL AUDIO OUTPUT

The D2-6 family IC-based systems support outputting a bit-exact pass-through of a compressed audio bitstream, or a decoded, down-mixed (Lt/Rt or Lo/Ro) and downsampled 2-channel Linear PCM audio bitstream using a specified SAI port, or S/PDIF digital transmitter. In addition, depending on the firmware functionality, it is possible for unused SAI (Serial Audio Interfaces) to also support $I^2S$ output as well, in either slave or master mode. The output audio sample rate is determined by the firmware and can vary from 32kHz up to 192kHz.

## HD Audio

### HDA INTERFACE

The HD audio interface also provides a control interface. This control interface uses the HD audio GPI, GPO, and GPIO 8-bit ports to provide a message passing facility between the D2-6 family and the PC.

The D2-6 family fully supports Windows® Hardware Quality Labs (WHQL™)-certification as, it is a UAA-Compliant Secondary HD Audio CODEC. The devices may be used either as the primary HDA CODEC, or as the second HDA CODEC in the system.

Features supported are:

- Message passing to other devices located on the motherboard (for example, HP jack detection and reporting)
- Amplifier firmware download
- Amplifier code load during system boot
- Amplifier control protocol (D2 Audio DSP customization GUI support)

### HD AUDIO PLAY

The D2-6 family provides for direct connection of a PC’s HD Audio (HDA) Controller to the device. In this configuration, the D2-6 family functions as an HDA CODEC with powered (amplified) outputs.

Supported features include:

- 2, 4, 6, or 8 amplified or PWM DAC channels
- Audio sample rates 48kHz, 96kHz, and 192kHz
- Data widths of 16-bit, 20-bit, and 24-bit
- Independent channel gain control

The HDA interface uses five of the six pins of the SAI 3 port. The HDA interface captures the audio streams and converts them into one to four $I^2S$ data streams, depending on the number of channels used. These $I^2S$ stereo streams are routed through SAI 3 and SAI 4 and then on to the sample rate converter. The SRC will rate lock to the HDA stream and remove any jitter while converting the data to the output sample rate.

## HD AUDIO FUNCTIONS AND FUNCTION TYPES

TABLE 2.

| FUNCTION | FUNCTION TYPE | NODE ID | CONNECTIONS |
|---|---|---|---|
| Audio Function Group | Function Group | 01 | Parent of all other nodes, also holds GPIO functions |
| Front L/R DAC | Stereo DAC | 02 | To Front L/R mixer |
| Center/LFE DAC | Stereo DAC | 03 | To Center/LFE mixer |
| Surround L/R DAC | Stereo DAC | 04 | To Surround L/R mixer |
| Side Surround L/R DAC | Stereo DAC | 05 | To side surround mixer |
| Front L/R Mixer | Sum/Mixer Node | 06 | To front L/R pin |
| Center/LFE Mixer | Sum/Mixer Node | 07 | To center/LFE pin |
| Surround L/R Mixer | Sum/Mixer Node | 08 | To surround L/R pin |
| Side Surround L/R Mixer | Sum/Mixer Node | 09 | To side surround L/R pin |
| Front L/R Output Pin | Pin Complex | 0A | To system per configuration default register |
| Center/LFE Output Pin | Pin Complex | 0B | To system per configuration default register |
| Surround L/R Output Pin | Pin Complex | 0C | To system per configuration default register |
| Side Surround L/R Output Pin | Pin Complex | 0D | To system per configuration default register |

## HD AUDIO VERBS SUPPORTED

TABLE 3.

| VERB FUNCTION | GET CODE | SET CODE | WIDGET NID | | | |
|---|---|---|---|---|---|---|
| | | | 01 | 02 - 05 | 06 - 09 | 0A - 0D |
| Converter Format | A | 2 | | Y | | |
| Gain/Mute | B | 3 | | | | Y |
| Processing Coefficient | C | 4 | | | | |
| Coefficient Index | D | 5 | | | | |
| Get Parameter | F00 | | Y | Y | Y | Y |
| Connection Select | F01 | 701 | | | | |
| Get Connection List | F02 | | | | Y | Y |
| Processing | F03 | | | | | |
| SDI Select | F04 | 704 | | | | |
| Power State | F05 | 705 | Y | | | |
| Channel/Stream ID | F06 | 706 | | Y | | |
| Pin Widget | F07 | 707 | | | | Y |
| Unsolicited Response | F08 | 708 | | | | |
| Pin Sense | F09 | 709 | | | | Y |
| Beep | F0A | 70A | | | | |
| EAPD/BTL | F0C | 70C | | | | |
| Digital Converter | F0D | 70D - 70E | | | | |
| Volume Knob | F0F | 70F | | | | |
| GPI | F10 - F1A | 710 - 71A | Y | | | |
| Config Default | F1C | 71C - 71F | | | | Y |
| Subsystem ID | F20 | 720 - 723 | Y | | | |
| Stripe | F24 | 724 | | | | |
| Reset | | 7FF | Y | | | |

## HD AUDIO WIDGET REQUIRED PARAMETERS

TABLE 4. VERB ID - 0xF00; PARAMETERS 0x9 - 0xD

| NODE ID | FUNCTION | WIDGET CAP. | PCM SIZE RATE | FORMAT | PIN CAP. | INPUT AMP CAP. |
|---|---|---|---|---|---|---|
| | | PID 0x9 | PID 0xA | PID 0xB | PID 0xC | PID 0xD |
| 01 | Function | | Y | Y | | |
| 02 | DAC | Y | Y | Y | | |
| 03 | DAC | Y | Y | Y | | |
| 04 | DAC | Y | Y | Y | | |
| 05 | DAC | Y | Y | Y | | |
| 06 | Mixer | Y | | | | Y |
| 07 | Mixer | Y | | | | Y |
| 08 | Mixer | Y | | | | Y |
| 09 | Mixer | Y | | | | Y |
| 0A | Pin | Y | | | Y | |
| 0B | Pin | Y | | | Y | |
| 0C | Pin | Y | | | Y | |
| 0D | Pin | Y | | | Y | |

TABLE 5. VERB ID - 0xF00; PARAMETERS 0xE - 0x13

| NODE ID | FUNCTION | CONNECT LIST LENGTH | POWER STATES | PROCESS CAP. | OUTPUT AMP CAP. | VOLUME KNOB |
|---|---|---|---|---|---|---|
| | | PID 0xE | PID 0xF | PID 0x10 | PID 0x12 | PID 0x13 |
| 01 | Function | | Y | | | |
| 02 | DAC | | | | | |
| 03 | DAC | | | | | |
| 04 | DAC | | | | | |
| 05 | DAC | | | | | |
| 06 | Mixer | Y | | | Y | |
| 07 | Mixer | Y | | | Y | |
| 08 | Mixer | Y | | | Y | |
| 09 | Mixer | Y | | | Y | |
| 0A | Pin | Y | | | Y | |
| 0B | Pin | Y | | | Y | |
| 0C | Pin | Y | | | Y | |
| 0D | Pin | Y | | | Y | |

## HD AUDIO SYSTEM TOPOLOGY

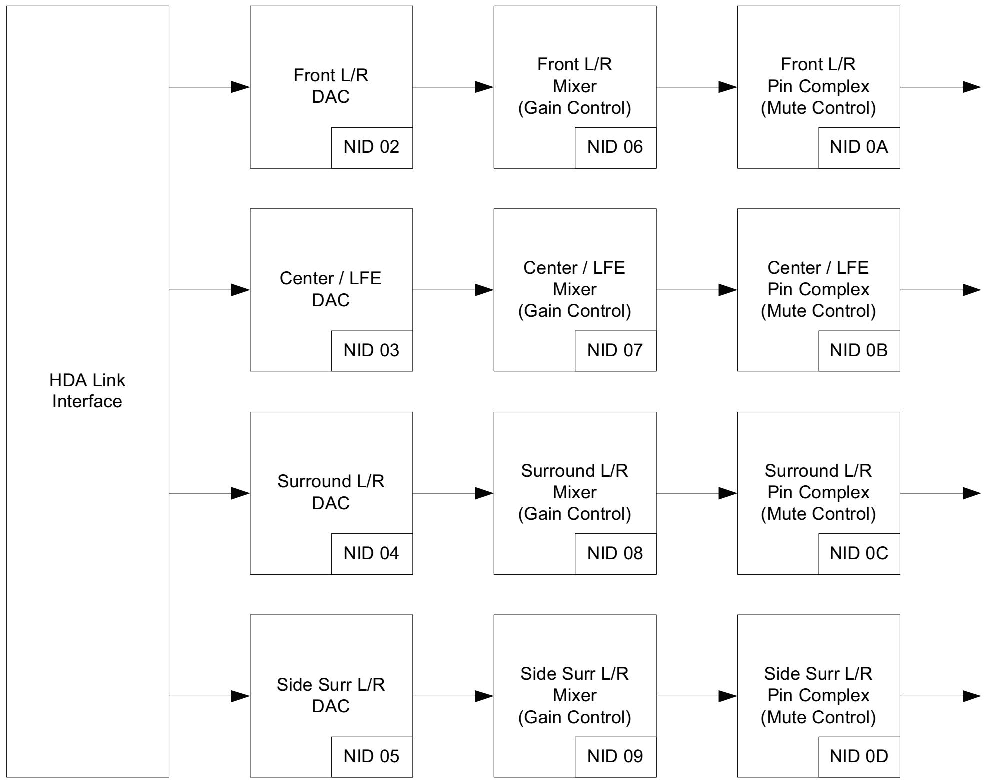



**FIGURE 10. HD AUDIO SYSTEM TOPOLOGY**

## Sample Rate Converters (SRC)

The D2-6 family ICs support internal asynchronous sample rate conversion to align input audio streams to a single rate compatible with the DSP processing rate and PWM switch rate. D2-6 device family has four independent rate estimators, allowing up to four asynchronous stereo inputs (eight channels) to be sample rate converted and processed simultaneously. The sample rate converter has a measured SNR that exceeds 140dB and a THD+N that exceeds -125dB.

## DSP

The majority of the D2-6 family audio processing functions as well as system control occur within the DSP core. The core is a 24-bit fixed-point digital signal processor, tightly integrated with its own DMA, interrupt control, memory, and control interfaces. Software configurable processing blocks and signal routings are implemented within the DSP, allowing a wide range of functionality and system implementations through the programmed definitions that are read into memory upon device initialization. Signal flows through the device are buffered and processed through hardware specific-function blocks (such as the sample rate converter) and allow considerable overall signal processing capability through interface to the DSP.

## Clocks And PLL

The clock generation contains a low jitter PLL critical for low noise PWM output and a precise master clock source for the ADC, sample rate conversion, and the audio data paths. The serial audio interfaces can function as either a master or a slave.

The PLL block contains the following components:

- Low noise crystal oscillator
- Low jitter PLL clock multiplier
- Power-on reset generator
- Brown out detectors on the CVDD and RVDD supplies
- System reset generation logic
- Clock generators for the DSP, S/PDIF transmitter, ADC, and MCLK output pin

The PLL block is completely managed by the system firmware. The system clock is provided by the crystal oscillator block, using either a fundamental mode crystal or a clock input to the XTALI pin. If the clock input is used, it must be a 1.8V signal level. The input signal on the XTALI pin is analog buffered and driven onto the OSCOUT pin for use in driving the XTALI input of other D2-6 family controllers.

The PLL uses the signal on the XTALI pin as the reference clock. The reference clock frequency is multiplied by an integer multiple of 4 to 15 to get the PLL output clock. The PLL output is used to time the PWM outputs and to generate the DSP clock. During system start-up, before the PLL has been configured and locked, the PLL is bypassed and the system operates at XTALI speed.

The power-on reset circuit senses the rise of the PLLVDD supply. When the supply reaches the sense threshold, the power-on reset pulse is generated. If the PLLVDD supply droops below the sense threshold, the reset pulse occurs when the supply rises above the threshold. The power-on reset signal drives the nRSTOUT output pin low.

The two power supply brown out detectors monitor the CVDD and PWMVDD power rails. If the power rail droops below the threshold, the brown out detector activates and drives the nRSTOUT output pin low.

The system reset generation logic is activated by a low level on the nRESET input pin or by the power-on reset sensor pulse. Upon de-assertion of nRESET a sequential counter ensures sufficient time and clock cycle count for the internal synchronous logic to reset.

Multiple D2-6 family ICs are capable of running on a common timebase. Multiple D2-6 family ICs synchronize themselves onto a single crystal oscillator so that all ICs run at identical frequencies.

### DSP CLOCK SPEED AND MEMORY CAPACITY SUPPORT

The D2-6 family devices are offered in part number-specific devices that support multiple DSP clock speeds and memory capacity. Depending on the device part number, the D2-6 operates up to clock rates of 147.456MHz or 159.744MHz, and offers memory capacity of 24k/24k/32k or 40k/40k, 56k of X/Y/P memory space.

The higher speed and larger memory devices support designs requiring higher processing capacity, while the lower speed devices provide cost optimization to systems not requiring the additional audio processing and decode capability.

Refer to "D2-6 Family Device Feature Set Offering" on page 3 for the device part numbers and definitions of clock speed and memory capacity.

## Hardware I/O Functions

The D2-6 family provides programmable I/O pins used for various hardware functions of the system design. Pin functions are defined by the product firmware, and may be different from one design to another.

### GENERAL-PURPOSE (GPIO) I/O PINS,

Eight dedicated General Purpose I/O (GPIO) pins are available for system use. These are controlled only by the D2-6 device family firmware.

### TIMERS

A timer block consisting of three separate general purpose timers provides programmed control of event or count down timing functions. The timer functions are controlled through the firmware, where these timers can operate as timed pulse generators, as pulse-width modulators, or as event counters to capture an event or to measure the width or period of a connected signal. These timers are connected to the three timer pins (TIO[0:2]), which are also assignable as I/O by firmware.

### POWER SUPPLY SYNCHRONIZATION

The PSSYNC pin provides a power supply synchronization signal for switching power supplies. Firmware configures PSSYNC to the frequency and duty cycle needed by the system switching regulator. The proper configuration eliminates audio output tones generated if the switching power supply is not locked to the amplifier switching.

### POWER SUPPLY ANTI-PUMP

The D2-6 family supports designs to correct for power supply pumping that occurs in half-bridge output stage topologies. The PUMPHI and PUMPLO pins provide a differential PWM signal pair that drive an anti-pump correction stage. The dead time and duty cycle are adjustable to eliminate the power supply DC offset.

## Amplifier Protection

The D2-6 family supports individual PWM channel protection through individual protection input pins. These PROTECT pins are primarily intended for protecting the PWM powered output stages. The protection inputs are activated by either a pulse or level driven into the pin. Firmware configures the input processing logic to properly interpret the input signal as rising edge triggered, falling edge triggered, high level, or low level.

The protection input signal is generated by specialized sensing circuits. There are several kinds of sensing circuits for detecting current, temperature, or voltage. A powered PWM output stage or a power supply pump driver typically uses an overcurrent sensor. This sensor detects power FET current, load current, or both. These circuits are unique to the specific power stage design, and may be embedded inside an integrated power stage. Temperature and voltage sensing are accomplished in a variety of ways and usually create a DC level representing a fault condition.

The D2-6 family designs incorporate a variety of protection strategies to prevent damage from the high voltages, currents, and temperatures present in class-D amplifier designs. This protection is also effective against user-induced faults, such as clipping, output overload, or output shorts, including both shorted outputs or short-to-ground faults.

The D2-92xx IC works in conjunction with specific surrounding parts to provide continuous system monitoring for destructive events. These events include:

- Output overcurrent
- Output short-circuit
- Over-temperature (thermal event)
- Power supply brown out
- Shoot-through overcurrent

Protection features and their details are firmware application dependent.

Firmware functions running on the D2-6 family can be assigned to observe the temperature at critical points in the hardware and automatically respond to excessive temperature. Depending on the specific implementation, this response can be as simple as turning on an optional fan to reduce temperature, or managing the audio signal to reduce power consumption.

### GRACEFUL OVERCURRENT AND SHORT-CIRCUIT

Overcurrent sensing requires a current sensor in the power device to be protected, usually a powered PWM output. The typical sensor creates a pulse that is active when the current exceeds a specified threshold.

The D2-6 family ICs observe the overcurrent protection inputs and provide graceful protection for the output stage. The hardware is configured to provide immediate current reduction, cycle-by-cycle output clipping, output signal control, and output stage deactivation depending on the severity and duration of high current events. The combination of hardware features and firmware monitoring allows the system to differentiate between an overcurrent situation or a more serious short-circuit condition.

### THERMAL PROTECTION

The D2-6 family ICs can connect to an optional low-cost thermal sensing circuit and monitor temperatures in the system. Firmware monitoring can record the system temperature and provide system responses including enabling a fan and managing the audio output signal.

## Device Operation

### RESET AND INITIALIZATION

The D2-6 family ICs must be reset after power up to begin proper operation, and in normal system hardware configurations, the reset occurs automatically using the reset hardware circuitry. The chips contain power rail sensors, brown out detectors, on the 3.3V and 1.8V power supplies. These brown out sensors asserts and hold an internal power-on reset, which disables the device until the power supplies are at a safe level for the DSP to start. These same brownout sensors detect a power supply voltage droop while the system is active and provide a safe amplifier shutdown.

### POWER SEQUENCING

The CVDD and RVDD (including PWMVDD) supplies should be brought up together to avoid high current transients that could fold back a power supply regulator. The ADCVDD and PLLVDD may be brought up separately. Best practice would be for all supplies to feed from regulators with a common power source. Typically this can be achieved by using a single 5V power source and regulating the 3.3V and 1.8V supplies from that 5V source.

### RESET

The D2-6 family ICs have one reset input: the nRESET pin. The nRESET input pin (active low, non-reset high) is effectively a power-on system reset. All internal state logic, except internal test hardware, is initialized by nRESET. While reset is active the system is held in the reset condition. The reset condition is defined as all internal reset signals being active, the crystal oscillator is running, and the PLL disabled.

At the de-assertion of nRESET, the chip captures the boot mode selection and begins the boot process.

## Booting and Boot Modes

### CODE INITIALIZATION AND BOOT MODES

The D2-6 family includes a fully-programmable DSP with internal boot ROM. The boot ROM's primary function is to download a second-stage boot image from one of several possible peripheral sources:

- $I^2C$ interface EEPROM
- $I^2C$ interface slave
- SPI ROM
- SPI interface slave
- HDA bus

The specific boot mode is selected based on the state of the IRQD, IRQC, IRQB, and IRQA pins at the time of reset de-assertion. The boot ROM code has been designed to handle both encrypted and non-encrypted boot images from any of the above storage locations. Boot modes are shown in Table 6 on page 27.

The system requires external firmware to boot the internal DSP. Internal ROM within the D2-6 family initiates the boot process to read the boot records and firmware, to load into the internal D2-6 family memory.

There are multiple boot modes provided on the D2-6 devices, as shown in Table 6. The mode is selected by a hardware pull-up or pull-down connection to each of the four boot mode (IRQ[D:A]) pins. (Modes not listed are reserved.) Boot sources include:

- $I^2C$ EEPROM
- SPI EEPROM or SPI flash
- $I^2C$ slave (to external microcontroller)
- SPI slave (to external microcontroller)
- Asynchronous UART (RS-232 for PC Communication mode as well as D2-6 family Device to Device Communication mode)
- HD audio bus
- Combo mode with $I^2C$ EEPROM or SPI

TABLE 6. BOOT MODES

| MODE | IRQ[D:A] | M/S | XTALI RANGE | INTERFACE SPEED | DESCRIPTION | USAGE |
|---|---|---|---|---|---|---|
| 0 | 0000 | S | N/A | per Master | $I^2C$ port 1 slave boot at address 88 | System |
| 1 | 0001 | M | 24.576 MHz | 400kb/s (See Note 18) | Combo Master - ROM on $I^2C$ port 0 or SPI | System |
| 2 | 0010 | M | 24.576MHz | 1.53MHz | ROM on SPI (EE or FLASH) (Copy of Mode 1 for pin compatibility) | System |
| 3 | 0011 | S | N/A | per Master | SPI slave boot | System |
| 7 | 0111 | S | 24.576MHz | 384kb/s | Fast asynchronous SCI boot | Multi-IC |
| B | 1011 | S | 24.576 MHz | 9600 b/s | Asynchronous SCI interface boot (RS232 Compatible) | System |
| C | 1100 | M | 24.576MHz | 1.53MHz (See Note 18) | HDA enabled, Combo Master - ROM on SPI (EE or FLASH) | System |
| D | 1101 | M | 24.576MHz | 400kb/s | Copy of mode C for pin compatibility | System |
| E | 1110 | M | 24.576MHz | per Master | HDA boot | System |
| F | 1111 | M | 24.576 MHz | 400Kb/s | 2-wire ROM on GPIO port (SCL= GPIO1,SDA = GPIO0) | System/ Failsafe |

NOTE:

18. For the “per Master” and “N/A” entries above, there is a maximum transfer rate that is a fraction of XTALI speed. This maximum transfer rate is peripheral port specific.

### APPLICATION FIRMWARE LOAD

The application firmware is loaded either by the boot code or by a multi-step process. Direct boot code loading occurs when the selected boot mode successfully finds a boot image on the expected peripheral interface and the image is successfully loaded in memory. A multi-step boot is one in which the boot code loads a program that manages the system boot.

## Control Interfaces

### $I^2C$ 2-WIRE INTERFACE

The D2-6 family ICs have two separate $I^2C$ 2-wire compatible ports. One is typically used for the external microcontroller interface, and the other for D2-6 family IC communication to EEPROMs, or other compatible peripheral chips. Both $I^2C$ interfaces are multi-master capable.

Registers are accessed through the $I^2C$ control interface. Because the $I^2C$ bus has multiple slaves, the desired $I^2C$ target device must be addressed. The specific $I^2C$ channel control address is defined within the firmware that is loaded into the D2-6 family at boot and initialization time. Typical addresses used in various reference designs use the address of 0xB2, but the actual address should be confirmed based on the firmware design being used in the application.

### SERIAL PERIPHERAL INTERFACE (SPI™)

The Serial Peripheral Interface (SPI) is an alternate serial interface to the $I^2C$ interfaces. As a master, this interface supports port extenders, EEPROMs, Flash, and various control interfaces for more complex chips. As a slave, this provides an alternate method for customers to communicate with the system.

### MULTI-CONTROLLER IC COMMUNICATION

The D2-6 family ICs are capable of communicating and synchronizing data and control information across multiple D2-6 family ICs. This communication is to facilitate matrix mixing of all input channels in a system and to allow precise phase alignment of the output audio. Systems designs are capable of achieving outputs phase aligned to within 1/2 sample at 192kHz. One D2-6 family IC acts as the timing master, so all other D2-6 family ICs must then operate as timing slaves. The setting of each of the D2-6 family ICs is system-configuration specific and is detailed in the specific RDP documentation.

### AUDIO SYNCHRONIZATION

Multiple D2-6 family ICs can be connected together and synchronized for controlling events to meet phase alignment requirements.

Control Protocols provide for an external device communication with the D2-6 family firmware while the amplifier is running. The D2-6 family firmware has a peripheral device driver that establishes communication with the external controller device. The D2-6 family is always a slave. Communication can occur through the HDA, $I^2C$, and SPI ports. However control is provided through only the $I^2C$, and HDA ports, and control through the SPI port is not supported.

### CONTROL REGISTER SUMMARY

The control register interface provides a mechanism for an external controller to manipulate the amplifier signal flow, and provides access to the internal registers.

Each system design has its own firmware-dependent register Application Programming Interface (API) and its own unique signal flow. The control register definitions, bit fields, and data format for each register are specified in that firmware API.

## READING AND WRITING CONTROL REGISTERS

Registers and memory spaces are defined within the D2-6 family firmware for specific internal operation and control. In typical reference designs, the highest-order byte of the register address (Bits 23:16) determines the internal address space used for control read or write access, and the remaining 16 bits (Bits 15:0) describe the actual address within that space. Refer to the descriptions of the actual reference design firmware being used in the application for specific definitions.

All reads or writes to registers (shown in Figures 11 and 12) begin with a Start Condition, followed by the Device Address byte, three Register Address bytes, three Data bytes, and a Stop Condition.

Register writes through the I$^2$C interface are initiated by setting the read/write bit that is within the device address byte. The device write function as, shown in Figure 11, executes the following nine steps as the I$^2$C bus master:

1. I$^2$C START command
2. Transmit device I$^2$C address with W
3. Transmit mode byte
4. Transmit upper memory address byte
5. Transmit lower memory address byte
6. Transmit data upper byte
7. Transmit data middle byte
8. Transmit data lower byte
9. I$^2$C STOP command

All reads to registers require two steps. First, the master must send a dummy write, which consists of sending a Start, followed by the device address with the write bit set, and three register address bytes. Next, the master must send a repeated Start, following with the device address with the read/write bit set to read, and then read the next three data bytes. The master must Acknowledge (ACK) the first two read bytes and send a Not Acknowledge (NACK) on the third byte received and a Stop condition to complete the transaction. The device's control interface acknowledges each byte by pulling SDA low on the bit immediately following each write byte. The device read function, as shown in Figure 12, executes the following 11 steps as the I$^2$C bus master:

1. I$^2$C START command
2. Transmit device I$^2$C address with W
3. Transmit mode byte
4. Transmit upper memory address byte
5. Transmit lower memory address byte
6. Repeat START command
7. Transmit device I$^2$C address with R
8. Receive data upper byte
9. Receive data middle byte
10. Receive data lower byte
11. I$^2$C STOP command or NACK

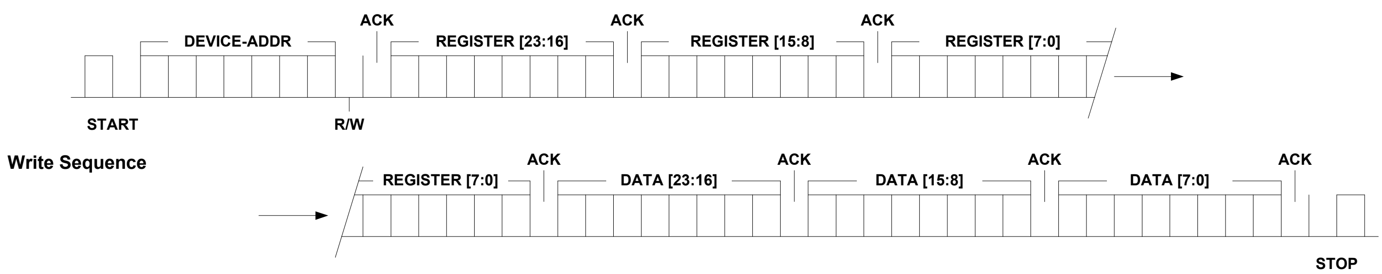



**FIGURE 11. I$^2$C WRITE SEQUENCE OPERATION**

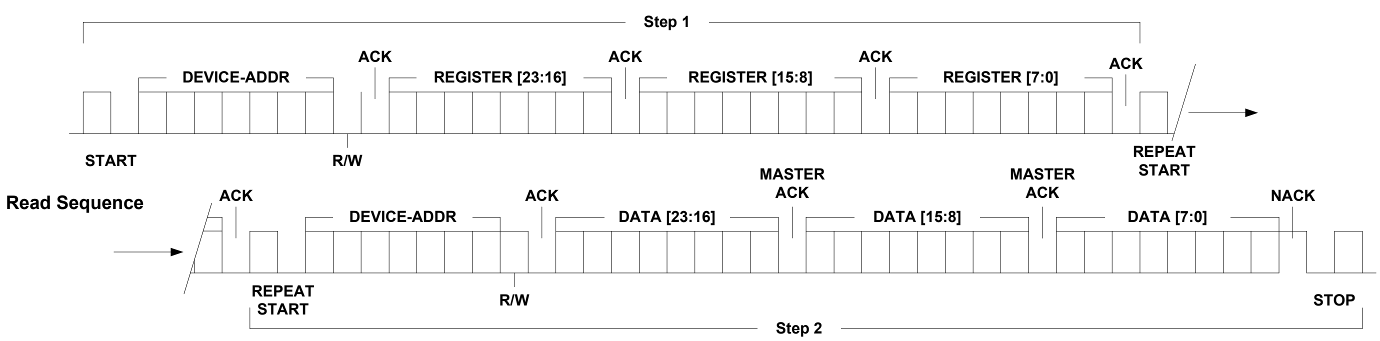



**FIGURE 12. I$^2$C READ SEQUENCE OPERATION**

# Audio Processing Functions

Each system design has its own firmware-dependent signal flow. This signal flow may be generic, or specifically designed for a particular amplifier application and consists of input elements connected to various signal processing blocks, routing the audio data to an output element. The input elements consist of chip peripherals used for audio input ($I^2S$ input, S/PDIF Digital receiver, and ADC). The output elements include the chip $I^2S$ output, S/PDIF Digital transmitter, and PWM outputs.

Typical audio processing blocks include gain stages, mixers, tone controls, compressors, limiters, equalizers, routers, loudness contour, crossover filters, delays, as well as audio enhancement features provided within the specific application firmware.

The input and output elements are configured by the firmware application and the scope of I/O selection is generally specific to the hardware of the particular application.

The signal processing blocks contain one or more parameters that define the signal transfer characteristic of the block and a mechanism for choosing the source and destination data locations. The signal flow is created by connecting together the signal processing blocks in the proper order to achieve the overall system audio processing function.

## Firmware Functions

D2-6 family ICs contain a DSP supporting powerful audio processing algorithms. Some of the standard audio algorithms that are typically supported in all firmware loads. Other algorithms are specific system design and firmware load dependent.

Additional features support multiple system capabilities such as:

- Automatic power-on amplifier calibration
- Parameter control and status reporting
- Integrated power supply control and clock synchronization
- Automatic power supply high-voltage rail anti-pump control
- Automatic negative rail generation and bring-up control (for select half-bridge designs where a ± rail is not already supplied)
- Automatic cycle-by-cycle temperature sensing and system response
- Automatic cycle-by-cycle current sensing and system response
- Input audio signal sensing and pop-free power-on/off using D2 Audio DSP's patented "Green Mode" algorithm with adjustable threshold
- Dynamic adjustment of efficiency vs. distortion vs. output power level using D2 Audio DSP's patented "DynaTiming" algorithm
- AM radio interference avoidance mode allows for dynamic switching of PWM engines when system microcontroller is in AM Radio model

## Input Source Selection

A source selection register specifies the action of a signal multiplexer, which implements a simple switching function. The selected input is routed to the block output unaltered. All non-selected inputs are ignored. Selections typically include $I^2S$ inputs, S/PDIF Digital inputs, HD Audio inputs, and ADC inputs.

## Master Volume

A master volume function alters the level on all channels simultaneously by applying the same gain/attenuation function to each. A single parameter controls all channels.

## Channel Attenuation

A channel attenuation function alters the level of a single channel. A single parameter is provided for each channel.

## Equalization

An equalization processing block consists of a single input and output, and is characterized by how many frequency bands are supported. Typical equalizers have 3-bands or 5-bands, although multiple combinations are directly supported. Each frequency band has three parameters - the center frequency, the filter Q, and the filter gain.

## Tone Control

Tone control provide simple bass and treble processing to the audio signal. Each tone processing block includes two first-order (6dB/octave) shelving filters, one each for bass and treble. Filters include programmable corner frequency and gain settings.

## Excursion Control

Excursion processing provides dynamic control of the subwoofer response. Three audio processing control adjustments are provided for frequency settings, and three adjustments are provided for Q parameter settings.

## Mixer

Mixer configuration blocks have multiple input channels and as many output channels as required by the system implementation. The mixer has an input gain parameter for each input to every mixing node. (for example, an 8-input mixer with 12 outputs incorporates a total of 96 independent gain adjustment parameters). The minimum gain parameter value is infinite attenuation, or mute.

## Mixers

An input mixer provides a two-input, two-output mixing and routing path. All inputs can be mixed at adjustable gain into any combination of outputs. Programmable settings are continuously adjustable from unity (0 dB) gain, through full cut-off.

## Compressor/Limiter

The compressor/limiter processor is used to gracefully limit the dynamic range of the audio signal. This is useful to prevent the amplifier from clipping or to limit the amplifier output power. Each compressor/limiter has configurable compression ratio, threshold, attack and release time, as well as makeup gain.

## Upward Compressor

Upward compressors provide audio compression and limiting functions but also provide an increase of signal level to inputs below the threshold setting. Upward compressors have configurable expansion ratio, threshold, attack and release time, as well as makeup gain. Controls are supported for global settings, gate adjustment, and for low-level expansion.

Upward compressors support two inputs. One input receives the audio that is processed by the compressor and passed to its output. A separate side chain input is the reference input for the processing algorithms.

## Delay

A delay block simply adds delay to the audio signal. A single delay parameter is used.

## Crossover

Low-pass and high-pass filter blocks add frequency filtering to the audio paths, providing appropriate signal processing for speaker crossover functionality, including bi-amplified solutions, and subwoofer low-pass filtering.

## High/Low-Pass Filters

High-Pass and Low-Pass filter blocks are provided for each of the five output channels downstream of the router and stereo mixer. These provide a flexible crossover function for all the output channels, including provision for defining the subwoofer channel's frequency response.

Filters are implemented as cascaded elements, with elements allocated for high-pass as well as for low-pass functionality, with complete flexibility of assignment. Pre-defined filter types including Butterworth, Bessel, and Linkwitz-Riley implementations are also provided.

## Routers

Routers provide individual audio path selection to any one of available input channels. The router performs path assignment only. It does not have a provision for gain or signal level adjustment.

## Loudness Contour

Loudness contour provides adjustment to allow for dynamically and automatically enhancing the frequency response of the audio program material relative to the master volume Level setting. The loudness contour models the frequency response correction as defined by the Fletcher/Munson audio response curve. It provides for amplitude or volume changes to those signals to which the ear does not respond equally at very low listening levels.

## Audio Processing Enhancements and Decoding

Depending on the device part number and design-specific firmware definitions, the D2-6 family devices support a variety of processing, decoding, virtualization, and pre/post processing feature sets, as well as options for DSP clock speed and memory capacity. Features and processing support are shown in "D2-6 Family Device Feature Set Offering" on page 3.

## Sound Enhancement Algorithm Processing

The D2 Audio DSP Sound enhancement algorithm audio processing provides a full set of enhancements to audio that greatly add to the quality and listening experience of sound in wide scopes of consumer devices. The D2 Audio DSP Sound Enhancement Algorithms use psycho-acoustic processing that create a rich-sounding environment from small speakers, and synthesizes the sound and quality equivalent to more complex systems. It is especially suited to consumer products that include televisions, docking stations, and mini hi-fi stereo products.

The D2-6 family includes enhanced sound enhancement algorithm processing that includes:

- 2 Channel stereo spatialization
- Bass Enhancement
- Content/configuration EQ presets
- Improved vocal clarity
- Automatic room audio setup/equalization/optimization
- Automatic loudspeaker setup/equalization/correction

The D2 Audio DSP sound enhancement algorithms are completely included within the D2-6 family devices.

# Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

| DATE | REVISION | CHANGE |
|---|---|---|
| Mar 19, 2019 | FN7838.4 | Changed the title from: D2-7xx83 to: D2-6 Family Audio SOC<br>Added Related Literature section.<br>Updated Applications and Features sections on page 1.<br>Updated Figure 1.<br>Updated Ordering Information table by removing retired parts and adding D2-74383-LR.<br>Changed throughout: “D2Audio™” to “D2 Audio DSP”; “DAE-3” to “D2-3 Family”; “DAE-6” and “D2-7xx83” to “D2-6 Family”; “Digital Audio Engine” to “Digital Audio Processor”; “SoundSuite” to “Sound Enhancement Algorithm”; removed “DTS®Studio Sound II”<br>Page 3, table 1:<br>- Added “DTS® Digital Surround Decoder” to the algorithm support column on page 3 for D2-74383-LR part.<br>- Added a note for “algorithm support” column.<br>Figure 5 on page 16, changed “D2AudioTM SoundSuite” to “D2 Sound Enhancement Algorithm”; for the lower block about Post-processing, changed the text to the following: “Post-Processing (D2 Sound Enhancement Algorithms for tone and equalization control)<br>Changed Audio Enhancement Features bullet points on page 30.<br>Removed Mark Levinson MightyCat™ Processing section.<br>Updated Application Markets section.<br>Removed About Intersil section on page 31<br>Updated to Renesas disclaimer and moved to end of datasheet. |
| Apr 28, 2016 | FN7838.3 | Updated the Ordering Information table on page 2.<br>Updated Table 1 on page 3 Algorithm Support column for D2-71583-LR, D2-74583-LR and D2-71683-LR.<br>Replaced the Products section with the About Intersil section.<br>Added Dolby and DTS disclaimers. |
| Sept 20, 2011 | FN7838.2 | Revise/add available device part numbers and related descriptions. |
| Jun 23, 2011 | FN7838.1 | Initial release. |

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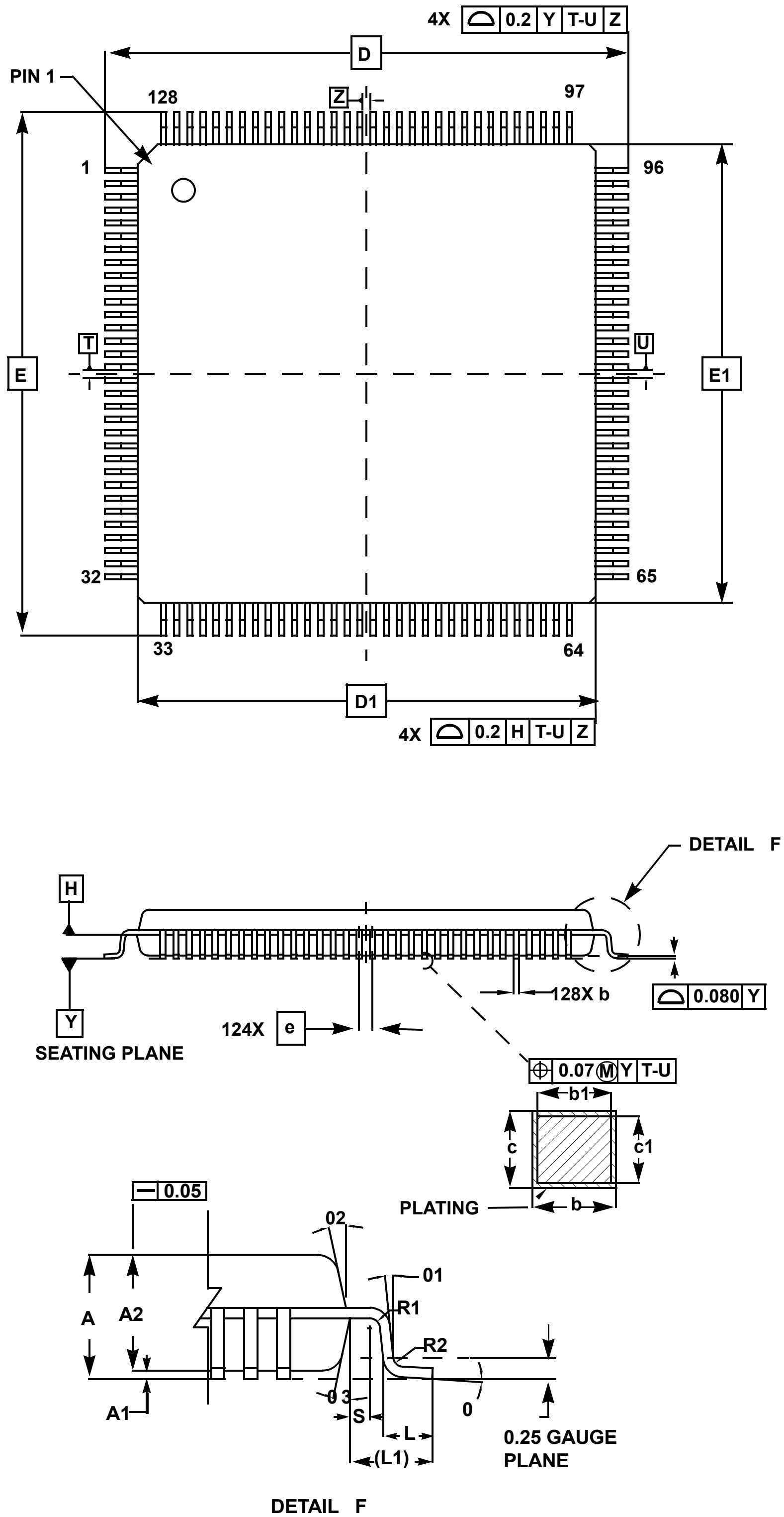
# Package Outline Drawing

For the most recent package outline drawing, see Q128.14x14.




## Q128.14x14

**128 LEAD LOW PLASTIC QUAD FLATPACK PACKAGE .4 MM PITCH (LQFP)**

| SYMBOL | MILLIMETERS | | | NOTES |
|---|---|---|---|---|
| | MIN | NOM | MAX | |
| A | - | | 1.60 | - |
| A1 | 0.05 | | 0.15 | - |
| A2 | 1.35 | 1.40 | 1.45 | - |
| b | 0.13 | 0.16 | 0.23 | 4 |
| b1 | 0.13 | - | 0.19 | - |
| c | 0.09 | - | 0.20 | - |
| c1 | 0.09 | - | 0.16 | - |
| D | 16 BSC | | | - |
| D1 | 14 BSC | | | 3 |
| E | 16 BSC | | | - |
| E1 | 14 BSC | | | 3 |
| L | 0.45 | 0.60 | 0.75 | - |
| L1 | 1.00 REF | | | - |
| R1 | 0.08 | - | - | - |
| R2 | 0.08 | - | 0.20 | - |
| S | 0.20 | - | - | - |
| 0 | 0° | 3.5° | 7° | - |
| 01 | 0° | - | - | - |
| 02 | 11° | 12° | 13° | - |
| 03 | 11° | 12° | 13° | - |
| N | 128 | | | - |
| e | 0.40 BSC | | | - |

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NOTES:

1. Dimensions are in millimeters. Dimensions in ( ) for Reference Only.
2. Dimensions and tolerances per AMSEY14.5M-1994.
3. Dimensions D1 and E1 are excluding mold protrusion. Allowable protrusion is 0.25 per side. Dimensions D1 and E1 are exclusive of mold mismatch and determined by datum plane H.
4. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar cannot be located at the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.

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