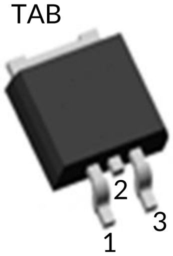
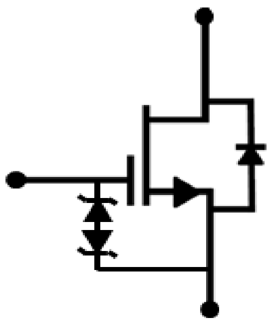
DATASHEET

UJ3C065080B3

650V-80mΩ SiC FET

Rev. B, April 2022





Part Number	Package	Marking
UJ3C065080B3	D^2PAK-3L	UJ3C065080B3

RoHS COMPLIANT | Pb LEAD FREE | HF HALOGEN FREE

Description

This SiC FET device is based on a unique ‘cascode’ circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device’s standard gate-drive characteristics allows for a true “drop-in replacement” to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the D^2PAK-3L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads , and any application requiring standard gate drive.

Features

- Typical on-resistance $R_{DS(on),typ}$ of 80mΩ
- Maximum operating temperature of 175°C
- Excellent reverse recovery
- Low gate charge
- Low intrinsic capacitance
- ESD protected: HBM class 2 and CDM class C3

Typical applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		650	V
Gate-source voltage	V_{GS}	DC	-25 to +25	V
Continuous drain current [1]	I_D	T_C = 25°C	25	A
		T_C = 100°C	18.2	A
Pulsed drain current [2]	I_{DM}	T_C = 25°C	65	A
Single pulsed avalanche energy [3]	E_{AS}	L=15mH, I_{AS} =2.1A	33	mJ
Power dissipation	P_{tot}	T_C = 25°C	115	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 175	°C
Reflow soldering temperature	T_{solder}	reflow MSL 1	260	°C

1. Limited by $T_{J,max}$
2. Pulse width t_p limited by $T_{J,max}$
3. Starting T_J = 25°C

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			1	1.3	°C/W

Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	V_{GS}=0V, I_D=1mA	650			V
Total drain leakage current	I_{DSS}	V_{DS}=650V, V_{GS}=0V, T_J=25°C		6	100	μA
		V_{DS}=650V, V_{GS}=0V, T_J=175°C		40		
Total gate leakage current	I_{GSS}	V_{DS}=0V, T_J=25°C, V_{GS}=-20V / +20V		6	± 20	μA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS}=12V, I_D=20A, T_J=25°C		80	100	mΩ
		V_{GS}=12V, I_D=20A, T_J=125°C		111		
		V_{GS}=12V, I_D=20A, T_J=175°C		141		
Gate threshold voltage	$V_{G(th)}$	V_{DS}=5V, I_D=10mA	4	5	6	V
Gate resistance	R_G	f=1MHz, open drain		4.5		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current [1]	I_S	T_C=25°C			25	A
Diode pulse current [2]	$I_{S,pulse}$	T_C=25°C			65	A
Forward voltage	V_{FSD}	V_{GS}=0V, I_F=10A, T_J=25°C		1.5	2	V
		V_{GS}=0V, I_F=10A, T_J=175°C		1.75		
Reverse recovery charge	Q_{rr}	V_R=400V, I_F=20A, V_{GS}=0V, R_{G_EXT}=20Ω di/dt=1600A/μs, T_J=150°C		111		nC
Reverse recovery time	t_{rr}			16		ns

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value Min	Value Typ	Value Max	Units
Input capacitance	C_{iss}	V_{DS}=100V, V_{GS}=0V f=100kHz		1500		pF
Output capacitance	C_{oss}	V_{DS}=100V, V_{GS}=0V f=100kHz		104		pF
Reverse transfer capacitance	C_{rss}	V_{DS}=100V, V_{GS}=0V f=100kHz		2.6		pF
Effective output capacitance, energy related	$C_{oss(er)}$	V_{DS}=0V to 400V, V_{GS}=0V		77		pF
Effective output capacitance, time related	$C_{oss(tr)}$	V_{DS}=0V to 400V, V_{GS}=0V		176		pF
C_{OSS} stored energy	E_{oss}	V_{DS}=400V, V_{GS}=0V		6.2		μJ
Total gate charge	Q_G	V_{DS}=400V, I_D=20A, V_{GS} = -5V to 15V		51		nC
Gate-drain charge	Q_{GD}	V_{DS}=400V, I_D=20A, V_{GS} = -5V to 15V		11		nC
Gate-source charge	Q_{GS}	V_{DS}=400V, I_D=20A, V_{GS} = -5V to 15V		19		nC
Turn-on delay time	$t_{d(on)}$	V_{DS}=400V, I_D=20A, Gate Driver =-5V to +15V, Turn-on $R_{G,EXT}$=1Ω, Turn-off $R_{G,EXT}$=20Ω Inductive Load, FWD: UJ3D06510TS, T_J=150°C		18		ns
Rise time	t_r	V_{DS}=400V, I_D=20A, Gate Driver =-5V to +15V, Turn-on $R_{G,EXT}$=1Ω, Turn-off $R_{G,EXT}$=20Ω Inductive Load, FWD: UJ3D06510TS, T_J=150°C		13		ns
Turn-off delay time	$t_{d(off)}$	V_{DS}=400V, I_D=20A, Gate Driver =-5V to +15V, Turn-on $R_{G,EXT}$=1Ω, Turn-off $R_{G,EXT}$=20Ω Inductive Load, FWD: UJ3D06510TS, T_J=150°C		59		ns
Fall time	t_f	V_{DS}=400V, I_D=20A, Gate Driver =-5V to +15V, Turn-on $R_{G,EXT}$=1Ω, Turn-off $R_{G,EXT}$=20Ω Inductive Load, FWD: UJ3D06510TS, T_J=150°C		11		ns
Turn-on energy	E_{ON}	V_{DS}=400V, I_D=20A, Gate Driver =-5V to +15V, Turn-on $R_{G,EXT}$=1Ω, Turn-off $R_{G,EXT}$=20Ω Inductive Load, FWD: UJ3D06510TS, T_J=150°C		85		μJ
Turn-off energy	E_{OFF}	V_{DS}=400V, I_D=20A, Gate Driver =-5V to +15V, Turn-on $R_{G,EXT}$=1Ω, Turn-off $R_{G,EXT}$=20Ω Inductive Load, FWD: UJ3D06510TS, T_J=150°C		62		μJ
Total switching energy	E_{TOTAL}	V_{DS}=400V, I_D=20A, Gate Driver =-5V to +15V, Turn-on $R_{G,EXT}$=1Ω, Turn-off $R_{G,EXT}$=20Ω Inductive Load, FWD: UJ3D06510TS, T_J=150°C		147		μJ

Typical Performance Diagrams

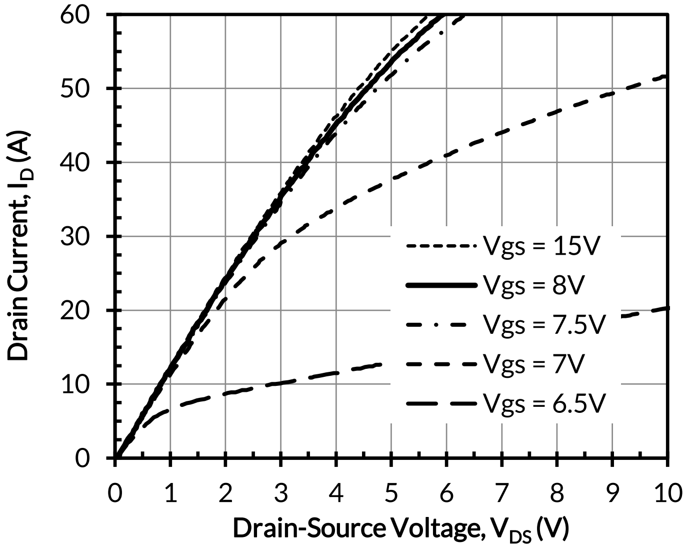


Figure 1. Typical output characteristics at T_J = - 55°C, tp < 250µs

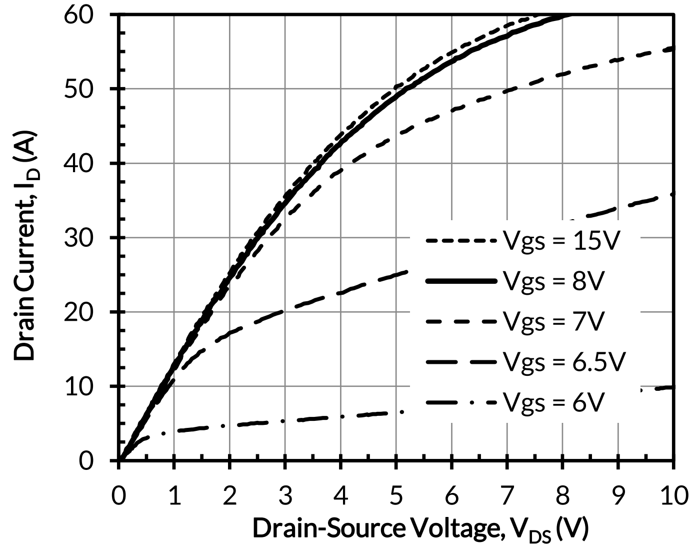


Figure 2. Typical output characteristics at T_J = 25°C, tp < 250µs

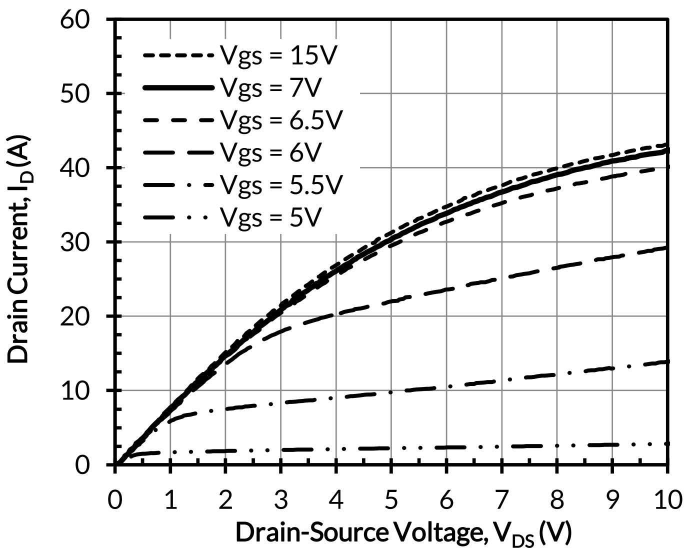


Figure 3. Typical output characteristics at T_J = 175°C, tp < 250µs

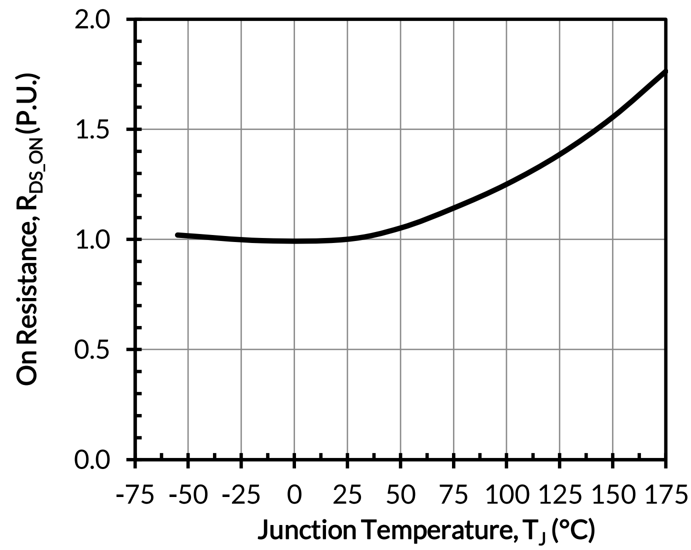


Figure 4. Normalized on-resistance vs. temperature at V_{GS} = 12V and I_D = 20A

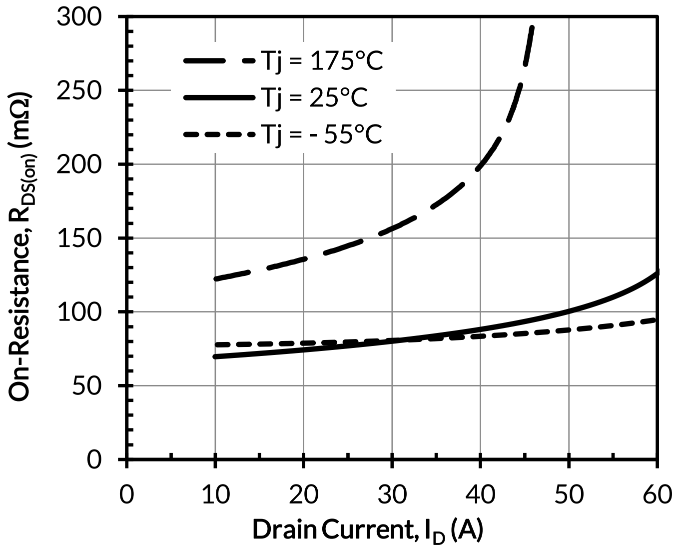


Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

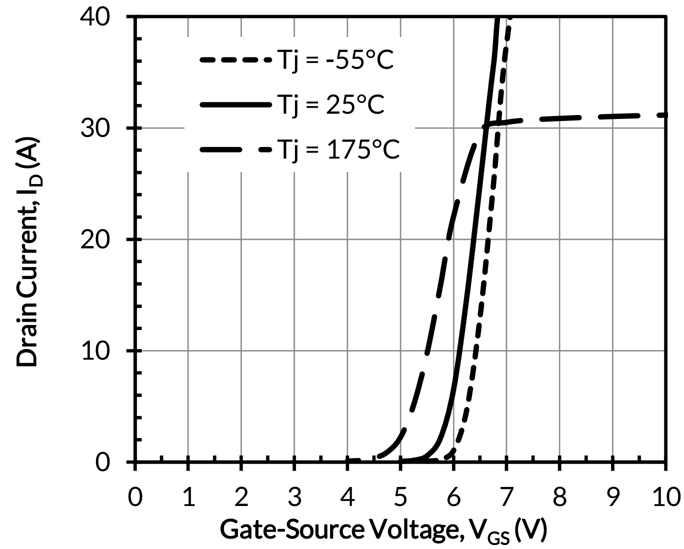


Figure 6. Typical transfer characteristics at V_{DS} = 5V

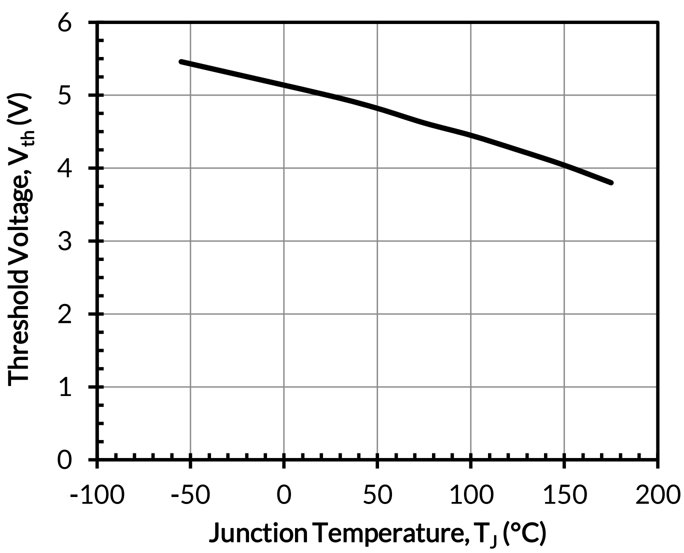


Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_D = 10mA

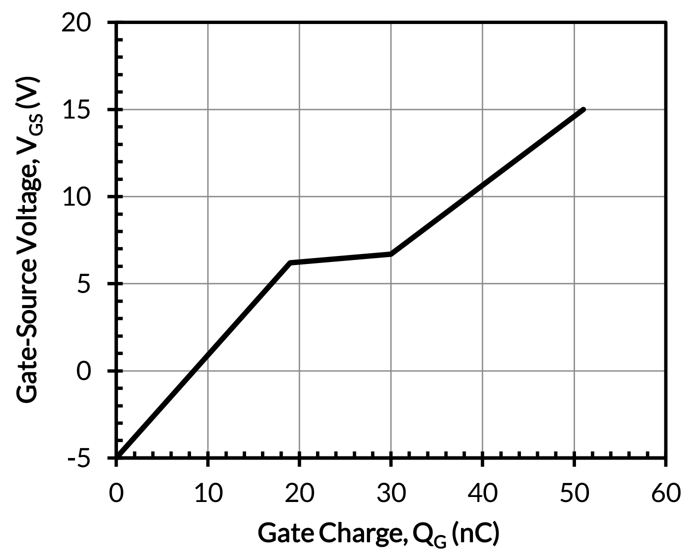


Figure 8. Typical gate charge at V_{DS} = 400V and I_D = 20A

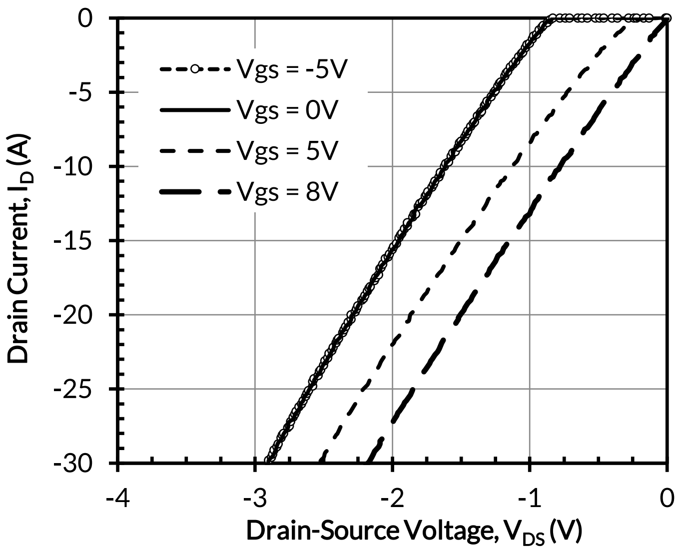


Figure 9. 3rd quadrant characteristics at T_J = -55°C

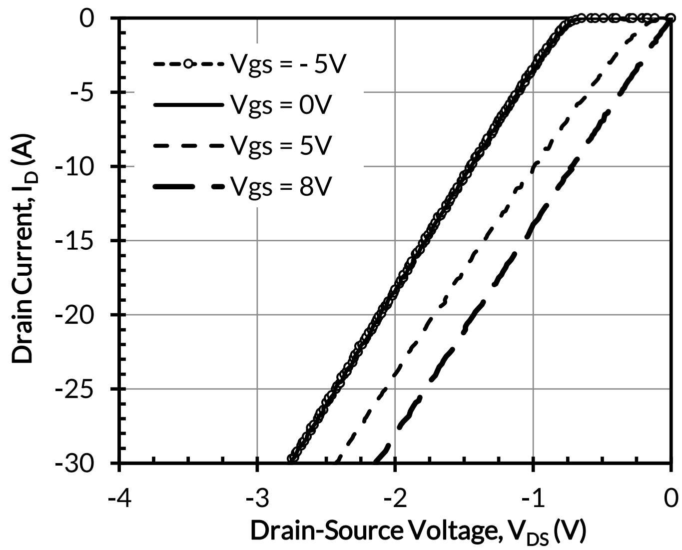


Figure 10. 3rd quadrant characteristics at T_J = 25°C

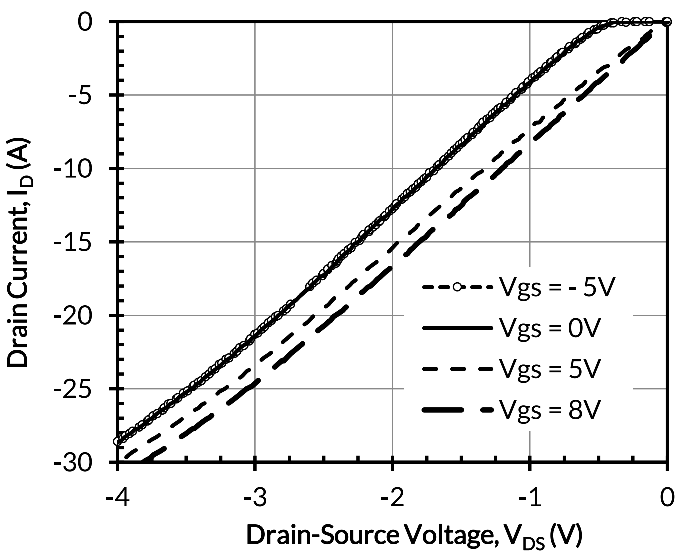


Figure 11. 3rd quadrant characteristics at T_J = 175°C

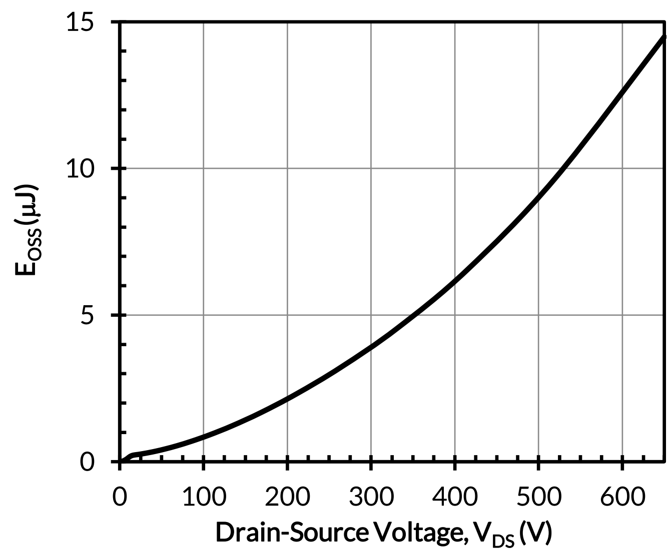


Figure 12. Typical stored energy in C_{OSS} at V_{GS} = 0V

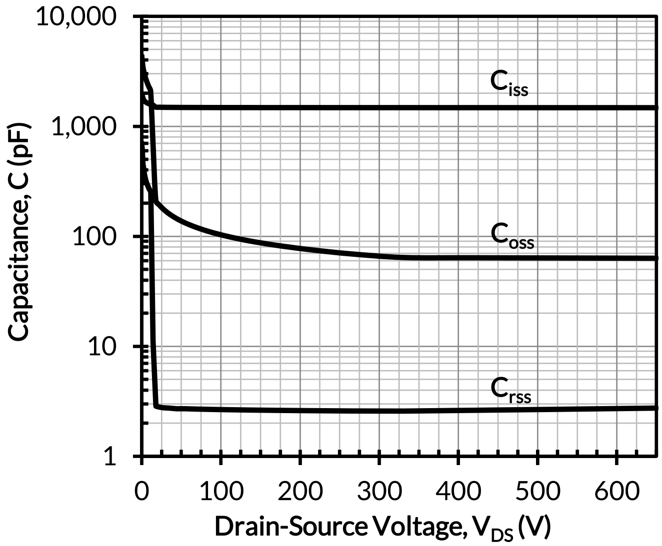


Figure 13. Typical capacitances at f = 100kHz and V_{GS} = 0V

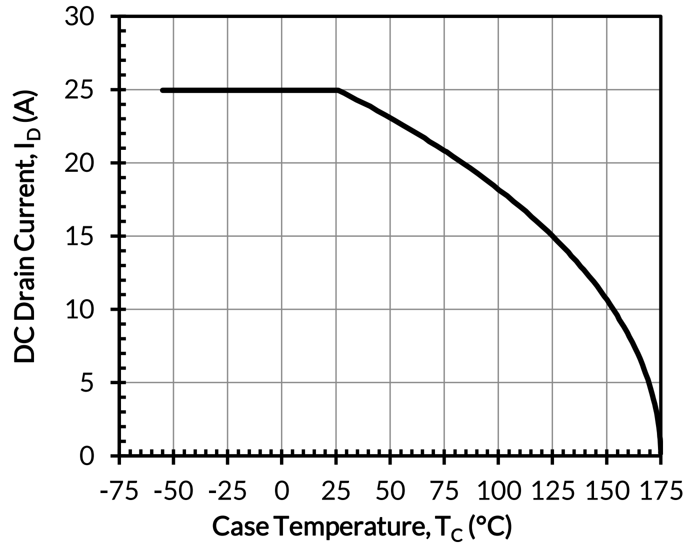


Figure 14. DC drain current derating

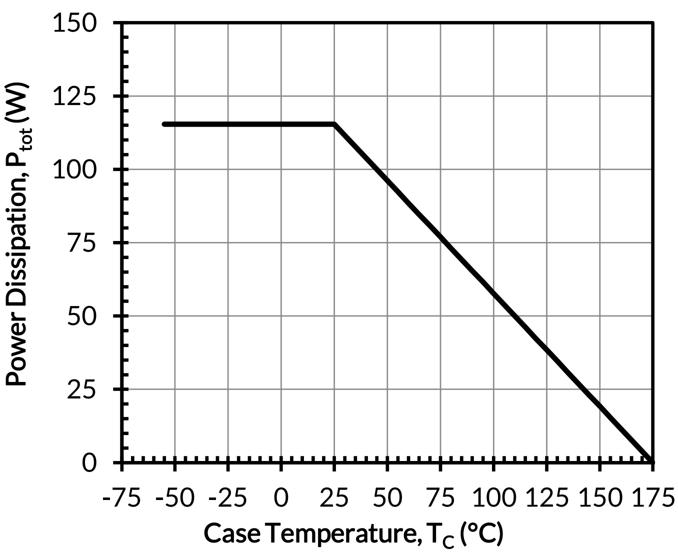


Figure 15. Total power dissipation

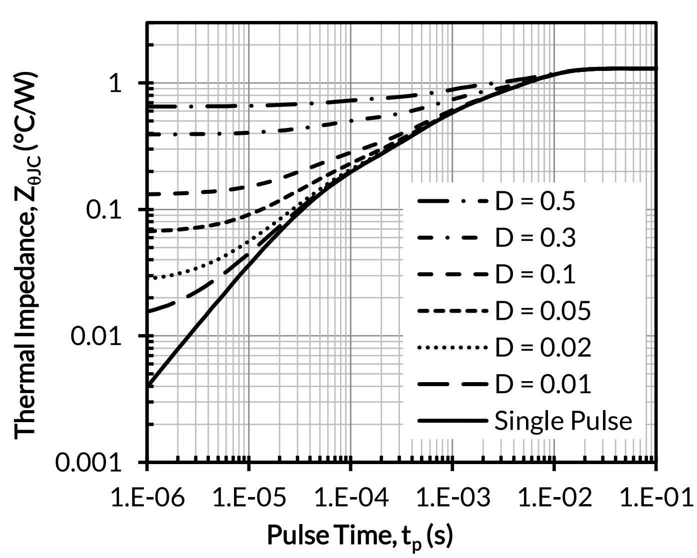


Figure 16. Maximum transient thermal impedance

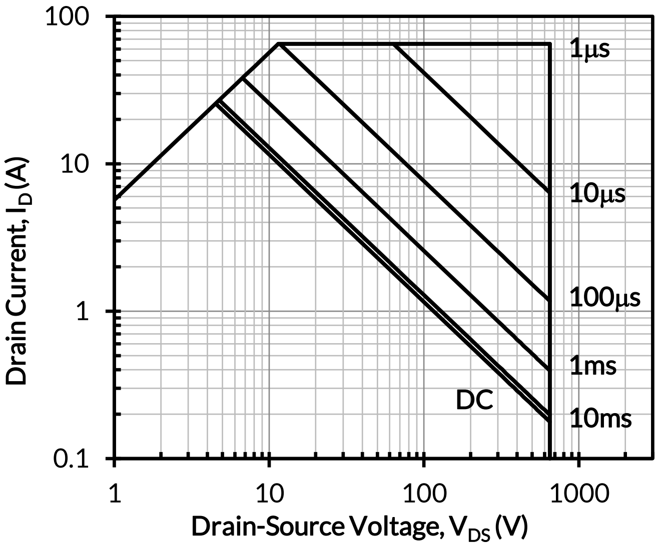


Figure 17. Safe operation area at T_C = 25°C, D = 0, Parameter t_p

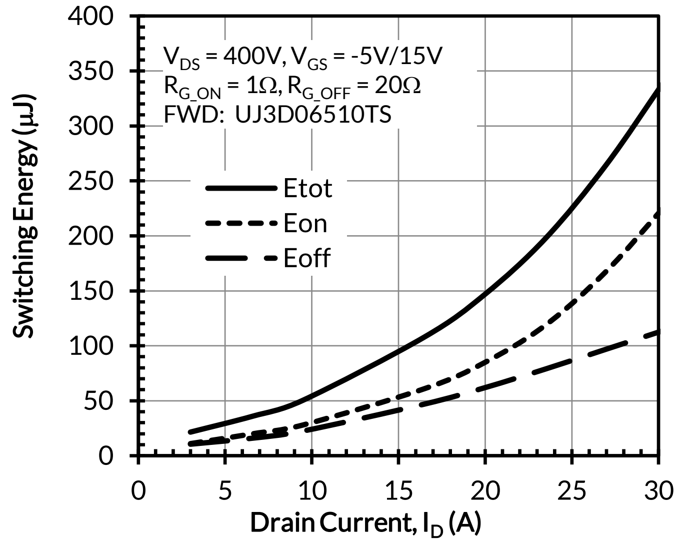


Figure 18. Clamped inductive switching energy vs. drain current at T_J = 150°C

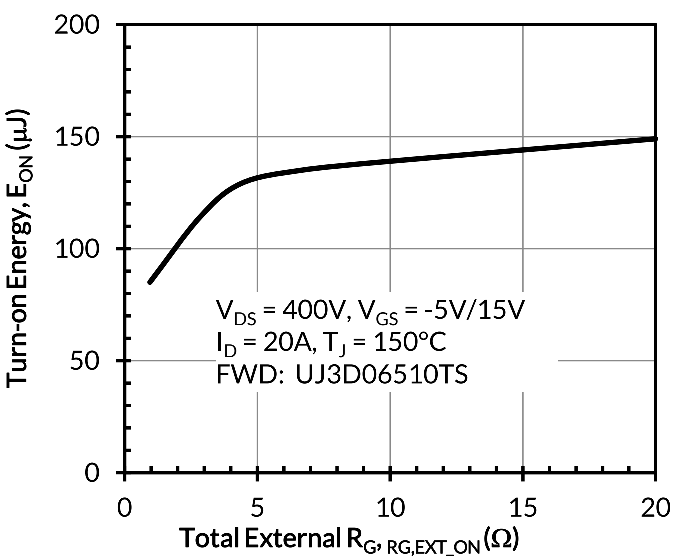


Figure 19. Clamped inductive switching turn-on energy vs. R_{G,EXT_ON}

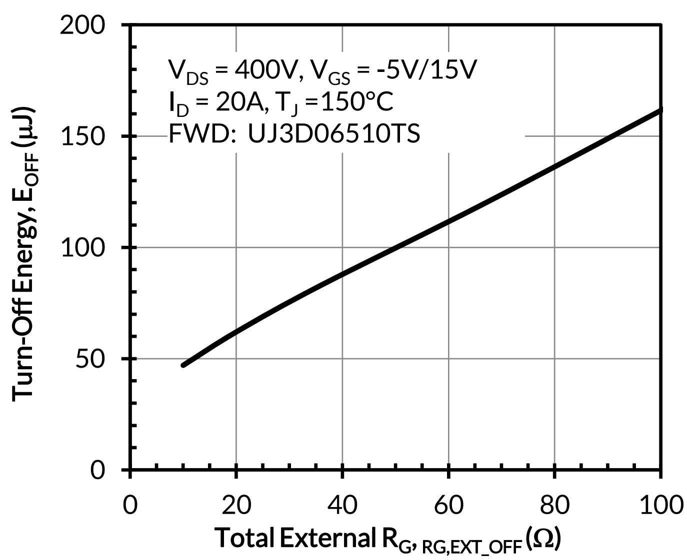


Figure 20. Clamped inductive switching turn-off energy vs. R_{G,EXT_OFF}

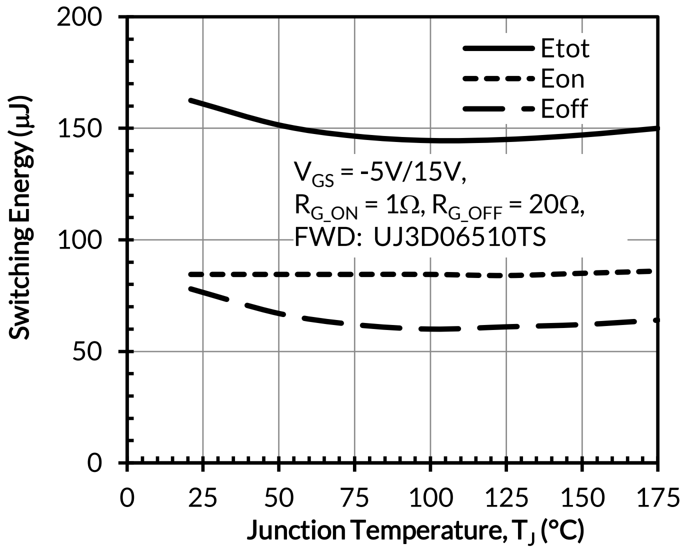


Figure 21. Clamped inductive switching energy vs. junction temperature at V_{DS} = 400V and I_D = 20A

Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.unitedsic.com.
A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the UnitedSiC website at www.unitedsic.com

Important notice