ASC Bridge Board

Evaluation Board User Guide

FPGA-EB-02025-2.1

November 2018

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ASC	Analog Sense and Control
FPGA	Field Programmable Gate Array
GPIO	General Purpose Input/Output
I^2C	Inter-Integrated Circuit
PWM	Pulse Width Modulation

1. Introduction

This guide describes the ASC Bridge Board, an interface board that connects up to three ASC Breakout Boards to either the MachXO3™-9400 Development Board or the ECP5™ Versa Development board for rapid prototyping and testing platform and hardware management applications. Throughout this document, the phrase *ASC Breakout Board* refers to a Platform Manager 2 evaluation board that is known by several names. The silkscreen on the board itself is *PM2 ASC EVAL BOARD*, the ordering part number is *LPTM-ASC-B-EVN*, and on the Lattice web site, the product name is *L-ASC10 Breakout Board*. The ASC Bridge Board does not contain any programmable logic nor does it have a USB connector for power or programming. The ASC Bridge Board is primarily an interconnect between the ASC Breakout Boards and either the MachXO3-9400 Development Board or the ECP5 Versa Development Board.

The content of this user guide includes descriptions of on-board jumper settings, tables detailing the inter-board connections, a complete set of schematics and the bill of materials for the ASC Bridge Board.

Complete descriptions of the MachXO3 FPGA, ECP5 FPGA, and L-ASC10 devices are found in the MachXO3 Family Data Sheet (FPGA-DS-02032), ECP5 and ECP5-5G Family Data Sheet (FPGA-DS-02012), and L-ASC10 Data Sheet (FPGA-DS-02038).

For full descriptions of the MachXO3-9400 Development Board, ECP5 Versa Development Board and L-ASC10 Breakout Board, see the MachXO3-9400 Development Board User Guide (FPGA-EB-02004), ECP5 Versa Development Board User Guide (FPGA-EB-02021), and ASC Breakout Board User Guide (FPGA-EB-02023).

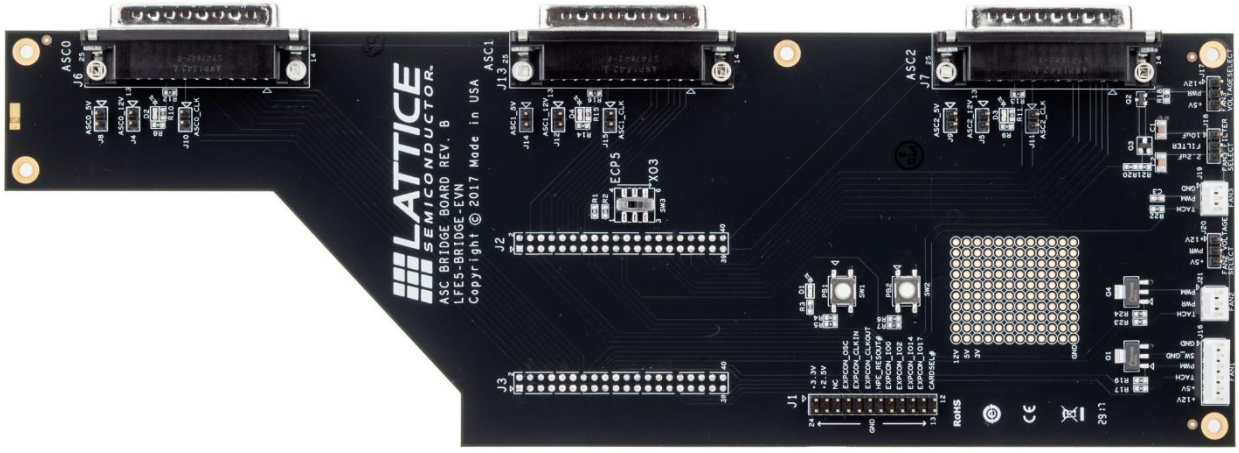

Figure 1.1. ASC Bridge Board, Top Side

2. Features

The ASC Bridge Board features the following on board components and circuits:

- 0.1-inch pitch through hole prototype area
- Three fan connectors with PWM (pulse width modulation) drive circuitry
- Two tactile push buttons
- Connectors for up to three ASC Breakout Boards
- Expansion header for additional FPGA I/Os
- *Versa* connectors to mate with either the MachXO3-9400 Development Board or the ECP5 Versa Development Board.

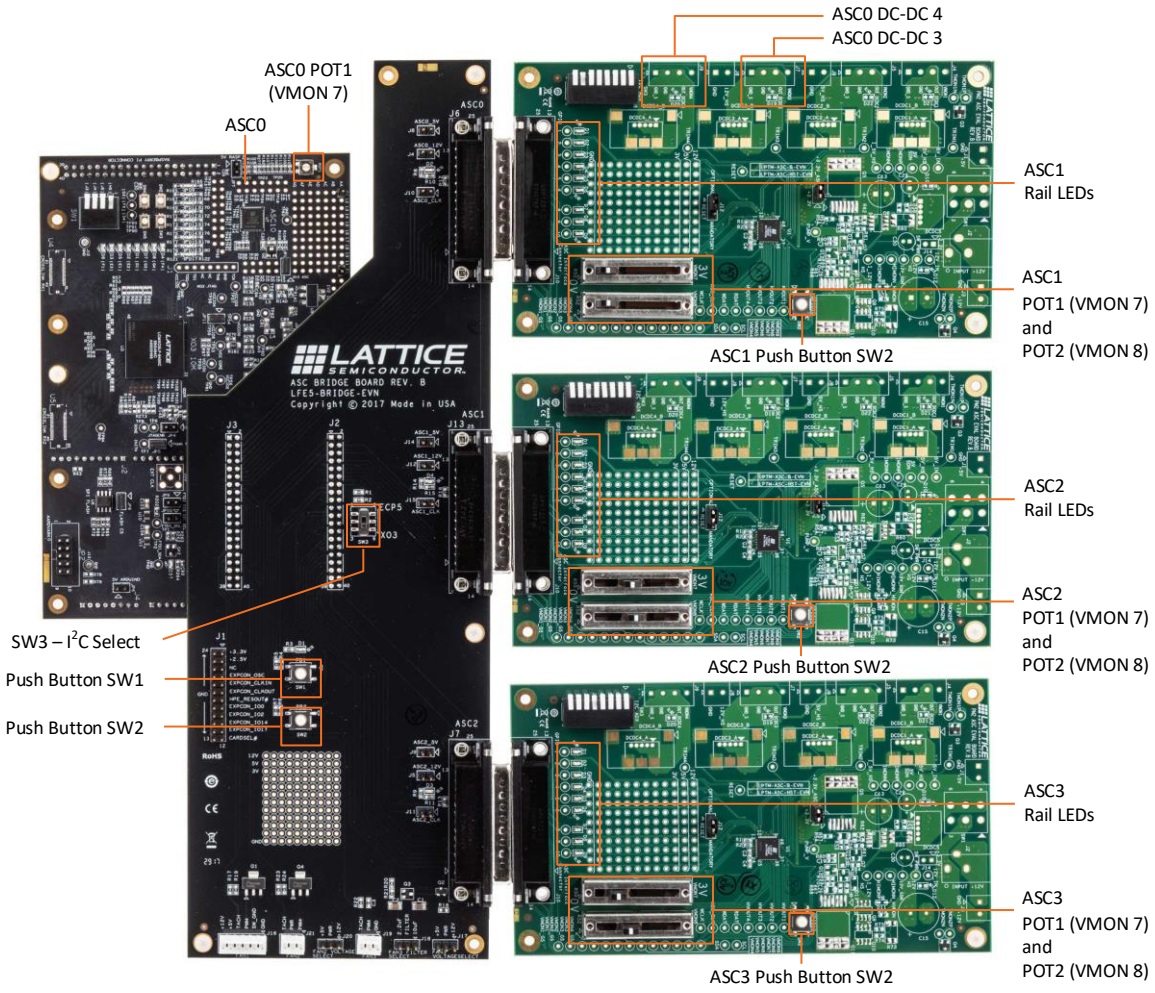

Figure 2.1. MachXO3-9400 Evaluation Board Connected to the Three ASC Breakout Boards

3. Setting Up the Board

To set up the board:

1. Attach four of the included nylon standoffs to the ASC Bridge Board (only one standoff is needed at the narrow edge of the board).
2. Attach two of the included nylon standoffs to the outside edge of each ASC Breakout Board.
3. Connect the ASC Bridge Board using the *Versa* connectors (J2 and J3) to either the MachXO3-9400 Development Board or the ECP5 Versa Development Board.
4. Connect the ASC Breakout Board(s) using J6, J7 and J13 as shown in Figure 2.1. The number of ASC Breakout Boards to install is based on the design requirement.
5. Slide SW3 to the MachXO3 position if the MachXO3-9400 Development Board is connected.

   Note: SW3 can also remain in the MachXO3 position for new ECP5 designs as long as the I^2C pins are mapped according to Table D.4 in Appendix D. SW3 only needs to be in the ECP5 position to support a legacy demo design. SW3 swaps the SDA and SCL signals on the ASC Bridge Board (see Figure A.2 in Appendix A).

4. Applying Power to the Board

The 3.3 V system power is supplied by either the MachXO3-9400 Development Board or the ECP5 Versa Development Board. Depending on your design requirement, the 5 V and 12 V power can be applied through the ASC Breakout Board (after the Hot Swap and/or Trim circuits have been populated).

Refer to the either the MachXO3-9400 Development Board User Guide (FPGA-EB-02004) or the ECP5 Versa Development Board User Guide (FPGA-EB-02021), and ASC Breakout Board User Guide (FPGA-EB-02023) on how to connect these power supplies. When using the 5 V and 12 V power supply, only one ASC Breakout Board is needed to connect to the power source. By shorting jumpers J8, J9, and J14, the 5 V supply connects to the other ASC Breakout Boards. Jumpers J4, J5, and J12 will do the same for the 12 V supply.

Note: The ASC Breakout Board may be populated with user supplied 3.3 V voltage regulator (DCDC5). When setting up the platform, be sure that only one board is supplying the 3.3 V power to prevent power supply contention.

5. System Clock

The 8 MHz system source clock comes from the ASC0 device. When using the MachXO3-9400 Development Board, no clock jumpers need to be installed on the ASC Bridge Board; the ASC0 device is located on the MachXO3-9400 Development Board and the clock signal is hard-wired to the MachXO3.

When using the ECP5 Versa Development board, the ASC0 device can be plugged-in to any of the ASC connectors. Shorting one of the jumpers, J10, J11, J15, enables the ASC0 ASCCLK to connect to ECP5 device. It is recommended to connect only one jumper.

Table 5.1. ASC0 ASCCLK Jumper Setting

ASC Connector	ASC0 Clock Jumper
ASC0 Connector	J10
ASC1 Connector	J15
ASC2 Connector	J11

6. Electrical, Mechanical, and Environmental Specifications

The nominal board dimensions are 3.875 inches by 11.5 inches. Five 0.125 inch plated through holes are provided to allow installation of plastic or metal spacers to lift the board off the desktop to a uniform height.

- Operation temperature: 0°C to 55°C
- Storage temperature: –40°C to 75°C
- Humidity: <95% without condensation

7. J2 and J3 Female Header

J2 and J3 are 40-pin female headers that connect the signals from either the MachXO3-9400 Development Board or the ECP5 Versa Development Board to the ASC Bridge Board. The female header carries both signal and power. The connections for J2 and J3 are listed in Appendix C and Appendix D.

Note: The connections referenced in this document refer to the LFE5UM-45F-8BG381C device.

8. J6, J7 and J13 D-SUB25 Connector

The L-ASC10 Evaluation Board is connected to the ASC Bridge Board through D-SUB 25-pin connectors. These connectors carry both signal and power.

Table 8.1 through Table 8.3 show the connections between the D-SUB connectors to J2 and J3 connectors.

Table 8.1. J6 D-SUB 25 Connection

J6 Header Pin Number	ASC Pin Function	Header Connection	Header Pin Number
1	GND	—	—
2	WDAT	J3	13
3	RDAT	J3	9
4	WRCLK	J3	10
5	MANDATORY_RESET	J2	28
6	GND	—	—
7	I2C_WRITE_EN	J2	32
8	ASC_CLK	J3	5
9	3.3 V	—	—
10	N.C.	—	—
11	12 V	—	—
12	5 V	—	—
13	GND	—	—
14	ASC_12V_OC_SHUTDOWN	J3	14
15	ASC_12V_OC_SENSE	J3	12
16	GND	—	—
17	ASC_RESET	J3	7
18	I2C_SCL	J2	18
19	I2C_SDA	J2	16
20	ASC_5V_OC_SHUTDOWN	J3	8
21	ASC_5V_OC_SENSE	J3	6
22	ASC_BOARD_SENSE	J3	4
23	12 V	—	—
24	5 V	—	—
25	5 V	—	—

Table 8.2. J13 D-SUB 25 Connection

J13 Header Pin Number	ASC Pin Function	Header Connection	Header Pin Number
1	GND	—	—
2	WDAT	J2	11
3	RDAT	J2	9
4	WRCLK	J2	10
5	MANDATORY_RESET	J2	28
6	GND	—	—
7	I2C_WRITE_EN	J2	32
8	ASC_CLK	J2	13
9	3.3 V	—	—
10	N.C.	—	—
11	12 V	—	—
12	5 V	—	—
13	GND	—	—
14	ASC_12V_OC_SHUTDOWN	J2	14
15	ASC_12V_OC_SENSE	J2	12
16	GND	—	—
17	ASC_RESET	J2	7
18	I2C_SCL	J2	18
19	I2C_SDA	J2	16
20	ASC_5V_OC_SHUTDOWN	J2	8
21	ASC_5V_OC_SENSE	J2	6
22	ASC_BOARD_SENSE	J2	4
23	12 V	—	—
24	5 V	—	—
25	5 V	—	—

Table 8.3. J7 D-SUB 25 Connection

J7 Header Pin Number	ASC Pin Function	Header Connection	Header Pin Number
1	GND	—	—
2	WDAT	J2	27
3	RDAT	J2	31
4	WRCLK	J2	33
5	MANDATORY_RESET	J2	28
6	GND	—	—
7	I2C_WRITE_EN	J2	32
8	ASC_CLK	J3	5
9	3.3 V	—	—
10	N.C.	—	—
11	12 V	—	—
12	5 V	—	—
13	GND	—	—
14	ASC_12V_OC_SHUTDOWN	J2	25
15	ASC_12V_OC_SENSE	J2	29
16	GND	—	—
17	ASC_RESET	J2	35
18	I2C_SCL	J2	18
19	I2C_SDA	J2	16
20	ASC_5V_OC_SHUTDOWN	J2	37
21	ASC_5V_OC_SENSE	J2	39
22	ASC_BOARD_SENSE	J2	36
23	12 V	—	—
24	5 V	—	—
25	5 V	—	—

9. J1 Male Header

The J1 male header provides power pins and additional I/Os from either the MachXO3-9400 Development Board or the ECP5 Versa Development Board's expansion connector which are not connected to the ASC Breakout Board connectors.

Table 9.1. J1 Male Header Connections for use with MachXO3-9400 or ECP5 Versa Develpment Board

J1 Pin Number	Silkscreen Name	MachXO3-9400		ECP5-45		FPGA Board Signal Name
		Ball	Port	Ball	Port	
1	+3.3 V	—		—		—
2	+2.5 V	—		—		—
3	N.C.	—		—		—
4	EXPCON_OSC	(Note)[1]		(Note)[2]		EXPCON_OSC
5	EXPCON_CLKIN	A10	PT23B	A10	PT36A	EXPCON_CLKIN
6	EXPCON_CLKOUT	A21	PT44A	E11	PT42B	EXPCON_CLKOUT
7	HPE_RESOUT#	G9	PT21D	A8	PT18B	HPE_RESOUT#
8	EXPCON_IO0	F8	PT11C	A12	PT49A	EXPCON_IO0
9	EXPCON_IO2	F9	PT21C	B13	PT51A	EXPCON_IO2
10	EXPCON_IO14	C6	PT14C	A9	PT33A	EXPCON_IO12
11	EXPCON_IO17	D8	PT15B	B15	PT69A	EXPCON_IO16
12	CARDSEL#	C13	PT29C	A7	PT18A	CARDSEL#
13	GND	—		—		GND
14	GND	—		—		GND
15	GND	—		—		GND
16	GND	—		—		GND
17	GND	—		—		GND
18	GND	—		—		GND
19	GND	—		—		GND
20	GND	—		—		GND
21	GND	—		—		GND
22	GND	—		—		GND
23	GND	—		—		GND
24	GND	—		—		GND

Notes:

1. When using the MachXO3-9400 Development Board the J1 pin 4 signal EXPCON_OSC comes from either the on-board oscillator Y2 or from an off-board source using J10.
2. When using the ECP5 Versa Development Board the J1 pin 4 signal EXPCON_OSC comes from the on-board Lattice ispClock5406D device.

10. J16 Fan 1 Header

This fan connector supports either a 3-wire low-side drive fan or 4-wire fan.

Table 10.1. Fan 1 Header Connection

J16 Pin Number	Description	MachXO3-9400		ECP5-45		FPGA Board Signal Name
		Ball	Pad	Ball	Pad	
1	GND	—		—		—
2	PWM Switch to GND*	G15	PT42D	C7	PT11B	EXPCON_IO44
3	PWM	G15	PT42D	C7	PT11B	EXPCON_IO44
4	Fan Tachometer	G12	PT28A	C6	PT11A	EXPCON_IO45
5	+5 V	—		—		—
6	+12 V	—		—		—

***Note:** J16 pin 2 is buffered and inverted from the signal FAN1_PWM. See Figure A.4 in the Appendix A. Board Schematics section for additional details.

11. J21 Fan 2 Header

This fan connector supports a 3-wire low-side drive fan. The power pin on this connector is selectable between 5 V and 12 V through jumper J20. Shorting the jumper to the 1-2 location selects the 12 V option. The 5 V option is selected when the jumper in on the 2-3 location.

Table 11.1. Fan 2 Header Connection

J21 Pin Number	Description	MachXO3-9400		ECP5-45		FPGA Board Signal Name
		Ball	Pad	Ball	Pad	
1	PWM Switch to GND*	G15	PT42D	D8	PT13B	EXPCON_IO42
2	Fan Power	—		—		—
3	Fan Tachometer	F15	PT42C	E8	PT13A	EXPCON_IO43

***Note:** J21 pin 1 is buffered and inverted from the signal FAN2_PWM. See Figure A.4 in the Appendix A. Board Schematics section for additional details.

12. J19 Fan 3 Header

This fan connector supports a 3-wire high side drive fan. The power for this fan connector is selectable between 5 V and 12 V through jumper J17. Shorting the jumper to the 1-2 location selects the 12 V option. The 5 V option is selected when the jumper in on the 2-3 location. A hold-up capacitor is inserted in parallel with the fan to guarantee proper under speed detection. The ASC Bridge Board has a set of pre-populated capacitors connected through jumper J18. For fan PWM frequency less than 10 kHz, connect J18 to the 1-2 location. Connect J18 to the 2-3 location for fan PWM frequency between 10 kHz to 26.7 kHz. If the fan PWM frequency is greater than 40 kHz, leave J18 unconnected. For more information about fan control, please refer to TN1278, Temperature Monitoring and Fan Control with Platform Manager 2.

Table 12.1. Fan 3 Header Connection

J19 Pin Number	Description	MachXO3-9400		ECP5-45		FPGA Board Signal Name
		Ball	Pad	Ball	Pad	
1	GND	—		—		—
2	PWM Switch to Power*	E16	PT40C	B8	PT15B	EXPCON_IO40
3	Fan Tachometer	E13	PT28C	C8	PT15A	EXPCON_IO41

***Note:** J19 pin 2 is buffered from the signal FAN3_PWM. See Figure A.4 in the Appendix A. Board Schematics section for additional details.

13. Push Buttons

Two push-button switches are connected to FPGA I/O with a 10 kΩ pull-up resistor tied to the 3.3 V supply. Depressing the button drives a logic level “0” to the device.

Table 13.1. Momentary Push-Buttons

Push Button SW	MachXO3-9400		ECP5-45		FPGA Board Signal Name
	Ball	Pad	Ball	Pad	
SW1	C6	PT14C	A9	PT33A	EXPCON_IO12
SW2	D8	PT15B	B15	PT69A	EXPCON_IO16

14. LED Indicators

The D1 blue LED illuminates when 3.3 V power is applied to the ASC Bridge Board. The red LEDs, D2, D3, and D4 illuminate when the corresponding ASC Breakout Boards are installed on the ASC0, ASC1 or ASC2 connectors.

15. Demonstration Design

For all the latest demo designs and documentation, please see the Lattice web page for the ASC Bridge Board.

16. Known Issue

The silkscreen on the board is marked with *LFE5-BRIDGE-EVN*. However, the correct Ordering Part Number is *L-ASC-BRIDGE-EVN*.

References

For more information, refer to

- ECP5 and ECP5-5G Family Data Sheet (FPGA-DS-02012)
- L-ASC10 Data Sheet (FPGA-DS-02038)
- MachXO3-9400 Development Board User Guide (FPGA-EB-02004)
- ECP5 Versa Development Board User Guide (FPGA-EB-02021)
- ASC Breakout Board User Guide (FPGA-EB-02023)
- Temperature Monitoring and Fan Control with Platform Manager 2 (FPGA-TN-02080)
- Adding Scalable Power and Thermal Management to MachXO2 and MachXO3 Using L-ASC10 (AN6094)
- Adding Scalable Power and Thermal Management to ECP5 Using L-ASC10 (AN6095)

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
ASC Bridge Evaluation Board	L-ASC-BRIDGE-EVN*	

***Note:** The silkscreen on the board is marked with *LFE5-BRIDGE-EVN*. However, the correct Ordering Part Number is *L-ASC-BRIDGE-EVN*.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Appendix A. Board Schematics

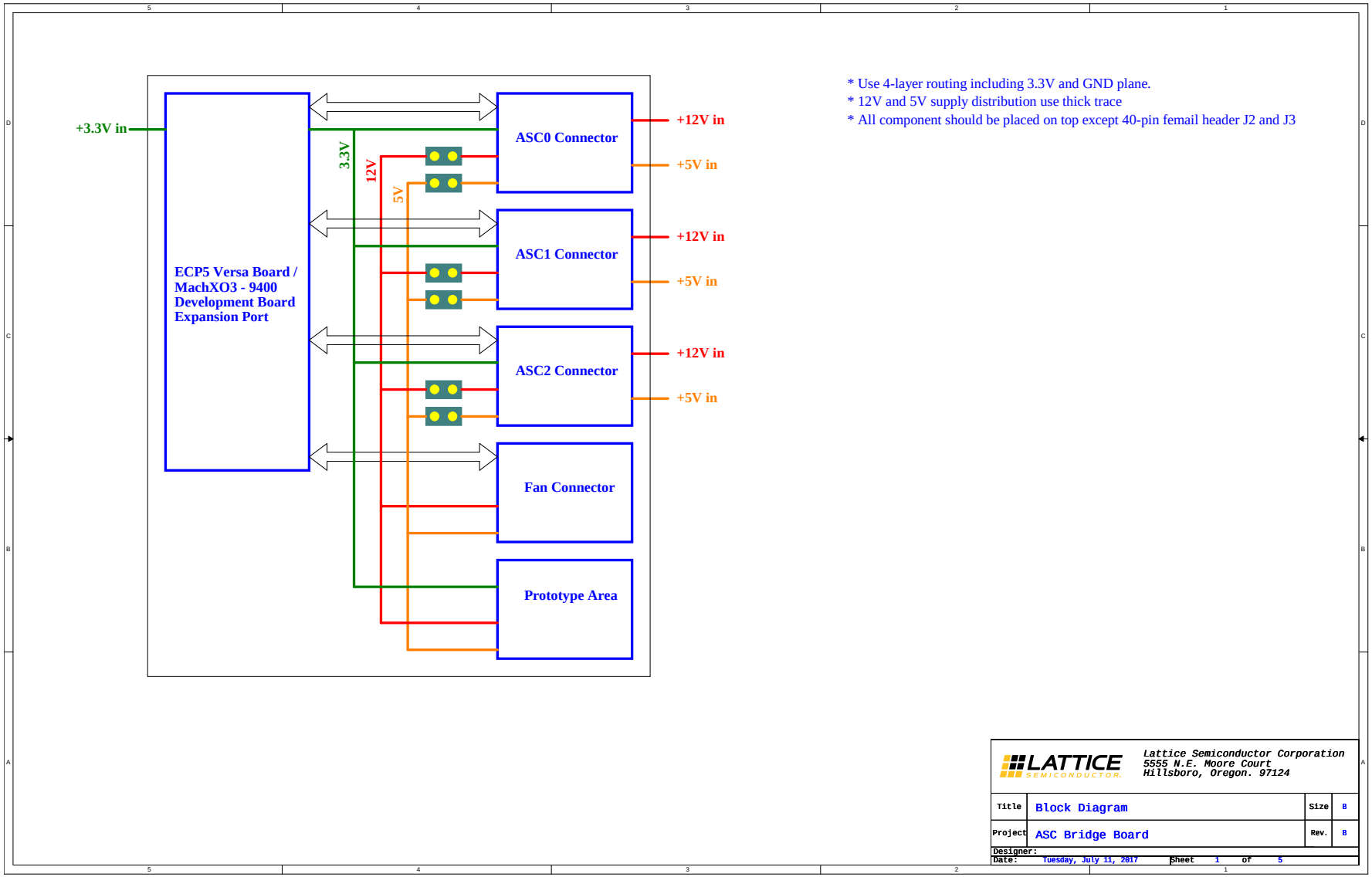

Figure A.1. ASC Bridge Board Block Diagram

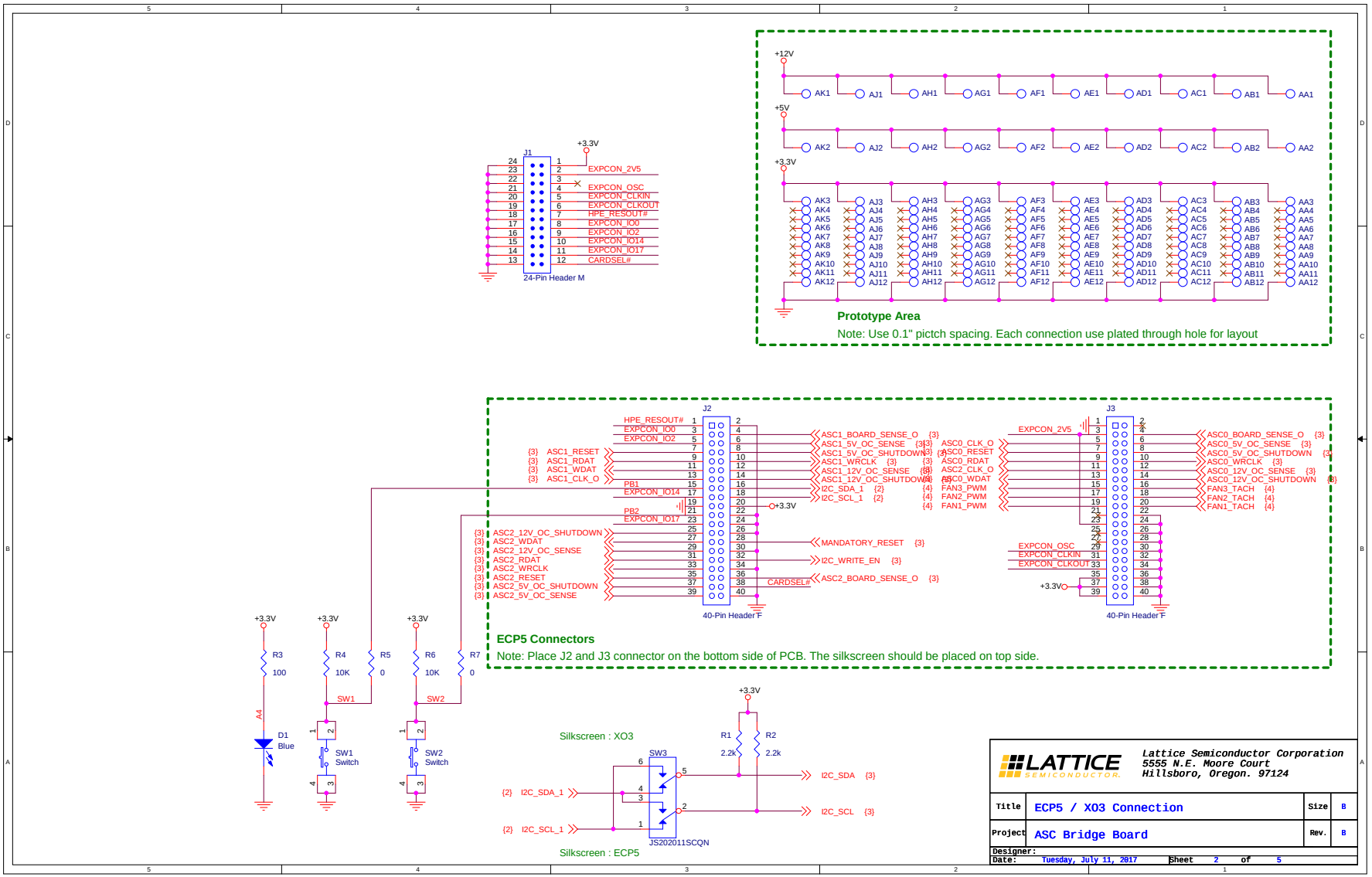

Figure A.2. ECP5 Connection

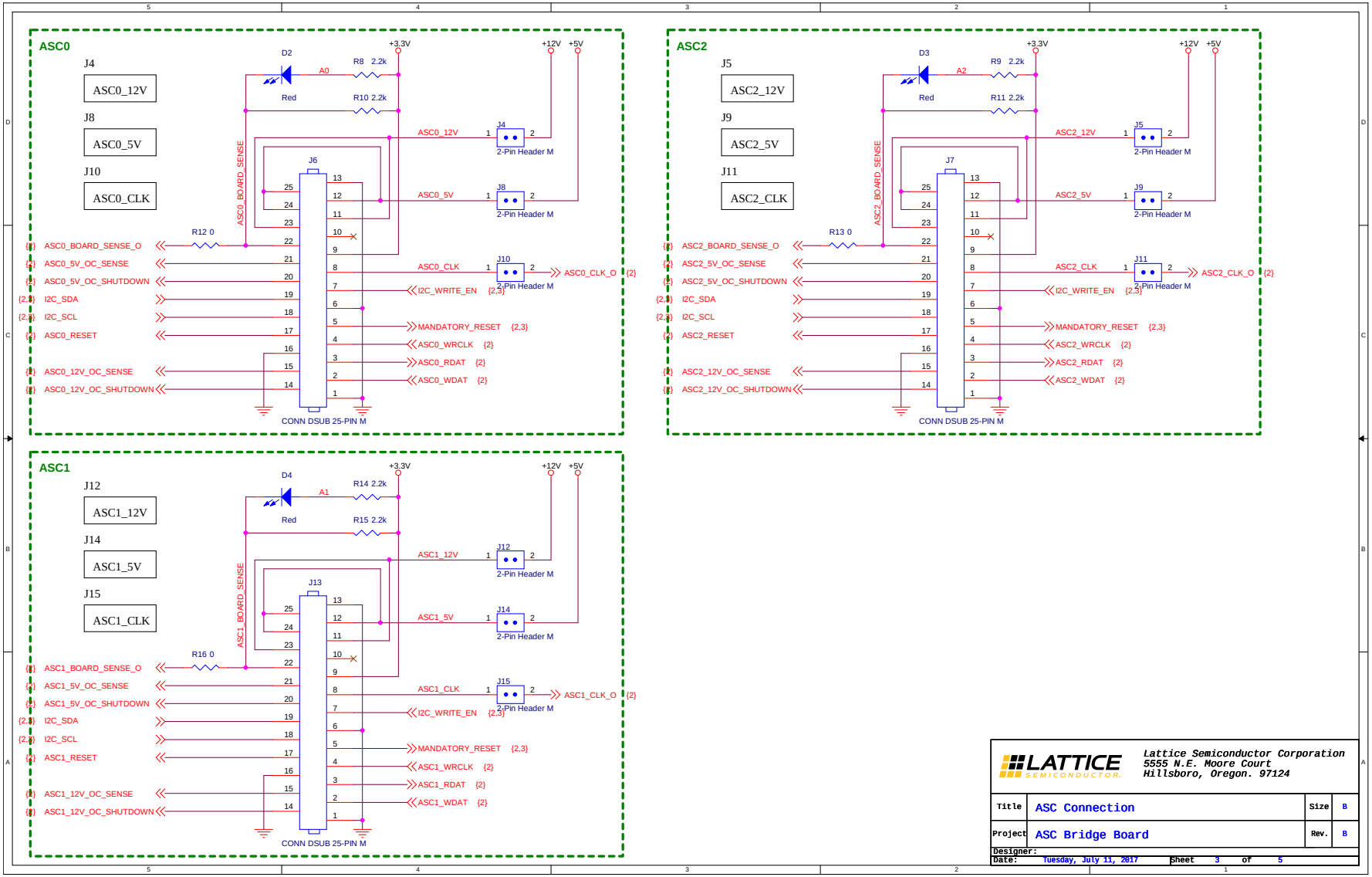

Figure A.3. ASC Connection

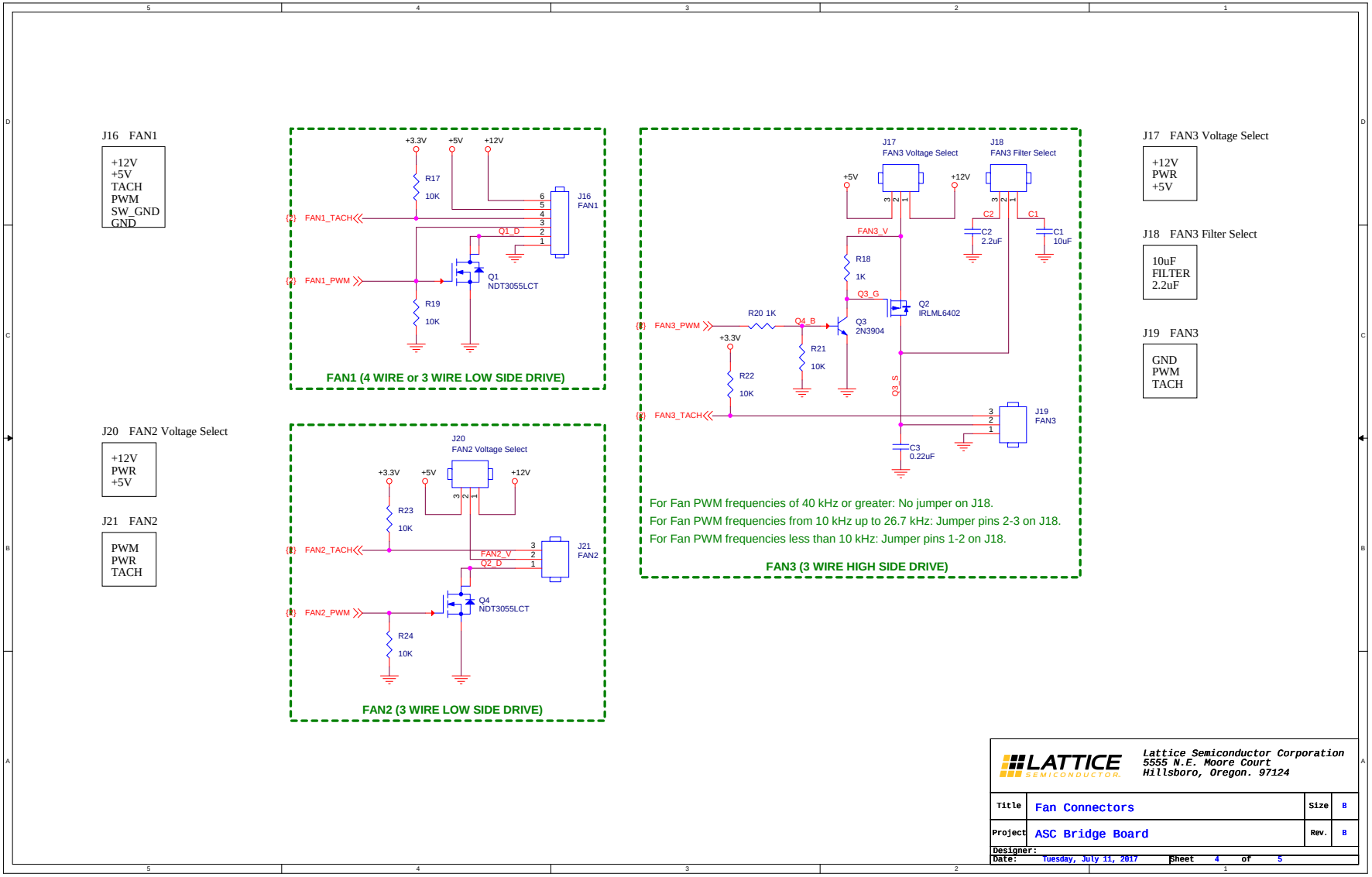

Figure A.4. Fan Connectors

Appendix B. Bill of Materials

Item	Quantity	Reference	Value	Manufacture	Mfr Part Number	Description
1	1	C1	10 uF	Kemet	C1206C106K4PACTU	CAP CER 10 uF 16 V 10% X5R 1206
2	1	C2	2.2 uF	Kemet	C1206C225K4RACTU	CAP CER 2.2 uF 16 V 10% X7R 1206
3	1	C3	0.22 uF	Murata	GRM188R71C224KA01D	CAP CER 0.22 uF 16 V 10% X7R 0603
4	1	D1	LED_blue	Lite-On	LTST-C193TBKT-5A	LED Blue 0603
5	3	D2,D3,D4	LED_red	Lite-On	LTST-C190KRKT	LED Red 0603
6	1	J1	Header_2x12	FCI	67997-224HLF	Male Header 24POS .100”
7	2	J2,J3	Header_2x20	TE Connectivity	2-534206-0	Female Header 40POS .100”
8	9	J4,J5,J8,J9,J10, J11,J12,J14,J15	Header_1x2	Molex	22284024	Male Header 2POS .100”
9	3	J6,J7,J13	DSUB_25	TE Connectivity	5747842-3	Male 25Pin DSUB Connector
10	1	J16	Header_Fan_1x6	Molex	22272061	Male Header 6POS .100”
11	1	J17,J18,J20	Header_1x3	Molex	22284034	Male Header 3POS .100”
12	1	J19,J21	Header_Fan_1x3	Molex	22272031	Male Header 3POS .100”
13	2	Q1,Q4	NDT3055LCT	Fairchild	NDT3055L	MOSFET N-CH 60 V 4 A SOT223
14	1	Q2	IRLML6402	International Rectifier	IRLML6402TRPBF	MOSFET P-CH 20 V 3.7ASOT-23
15	1	Q3	2N3904	Fairchild	MMBT3904	BJT NPN 40 V 0.2A SOT-23
16	8	R1,R2,R8,R9,R10, R11,R14,R15	2.2k	Panasonic	ERJ-3EKF2201V	RES 2.2 kΩ 1% 1/10 W 0603
17	1	R3	100	Panasonic	ERJ-3EKF1000V	RES 100 Ω 1% 1/10 W 0603
18	8	R4,R6,R17,R19, R21,R22,R23,R24	10K	Panasonic	ERJ-3EKF1002V	RES 10 kΩ 1% 1/10 W 0603
19	5	R5,R7,R12, R13,R16	0	Panasonic	ERJ-3GEY0R00V	RES 0.0 Ω 1/10 W 0603
20	1	R18	1K	Rohm	ESR03EZPJ102	RES 1 kΩ 5% 1/4 W 0603
21	1	R20	1K	Panasonic	ERJ-3EKF1001V	RES 1 kΩ 1% 1/10 W 0603
22	2	SW1,SW2	Switch	Panasonic	EVQ-Q2K03W	Tactile Switch 15 V 20 mA
23	10	bag	#4-40 by 1"	Keystone	1902E	Nylon Hex Standoff
24	10	bag	#4-40 by 1/4"	Essentra	NSP-4-40-01	Nylon Phillips Machine Screw

Appendix C. MachXO3 9400 Development Board and ASC Bridge Board Signals and Connections.

Table C.1. ASC1 (J4) – MachXO3-9400 Development Board and ASC Bridge Board Connections

Bridge Board Signal Name	Bridge Board J3 Pin	MachXO3 Board X2 Pin	MachXO3 Board Signal Name	MachXO3 Ball	Platform Designer Signal Name
ASC0_CLK_0	5		EXPCON_IO30	D14	N / A
ASC0_RESET	7		EXPCON_IO32	C17	ASC1_RSTN_I
ASC0_RDAT	9		EXPCON_IO34	C18	rdat_1
ASC0_WDAT	13		EXPCON_IO38	D18	wdat_1
ASC0_WRCLK	10		EXPCON_IO35	D16	wrclk_1
ASC0_BOARD_SENSE	4		EXPCON_IO29	E12	User Defined
ASC0_5V_OC_SENSE	6		EXPCON_IO31	C15	User Defined
ASC0_5V_OC_SHUTDOWN	8		EXPCON_IO33	D15	User Defined
ASC0_12V_OC_SENSE	12		EXPCON_IO37	D17	User Defined
ASC0_12V_OC_SHUTDOWN	14		EXPCON_IO39	C20	User Defined

Table C.2. ASC2 (J13) – MachXO3-9400 Development Board and ASC Bridge Board Connections

Bridge Board Signal Name	Bridge Board J2 Pin	MachXO3 Board X3 Pin	MachXO3 Board Signal Name	MachXO3 Ball	Platform Designer Signal Name
ASC1_CLK_0	13		EXPCON_IO10	F10	N / A
ASC1_RESET	7		EXPCON_IO4	E7	ASC2_RSTN_I
ASC1_RDAT	9		EXPCON_IO6	D5	rdat_2
ASC1_WDAT	11		EXPCON_IO8	D6	wdat_2
ASC1_WRCLK	10		EXPCON_IO7	C3	wrclk_2
ASC1_BOARD_SENSE	4		EXPCON_IO1	G8	User Defined
ASC1_5V_OC_SENSE	6		EXPCON_IO3	F7	User Defined
ASC1_5V_OC_SHUTDOWN	8		EXPCON_IO5	E6	User Defined
ASC1_12V_OC_SENSE	12		EXPCON_IO9	C4	User Defined
ASC1_12V_OC_SHUTDOWN	14		EXPCON_IO11	C5	User Defined

Table C.3. ASC3 (J7) – MachXO3-9400 Development Board and ASC Bridge Board Connections ctions

Bridge Board Signal Name	J2 Pin X3 Pin	J3 Pin X2 Pin	MachXO3 Board Signal Name	MachXO3 Ball	Project Designer Signal Name
ASC2_CLK_0	—	11	EXPCON_IO36	C19	N / A
ASC2_RESET	35	—	EXPCON_IO25	D12	ASC3_RSTN_I
ASC2_RDAT	31	—	EXPCON_IO22	E11	rdat_3
ASC2_WDAT	27	—	EXPCON_IO19	E10	wdat_3
ASC2_WRCLK	33	—	EXPCON_IO24	F11	wrclk_3
ASC2_BOARD_SENSE	36	—	EXPCON_IO26	F12	User Defined
ASC2_5V_OC_SENSE	39	—	EXPCON_IO28	C14	User Defined
ASC2_5V_OC_SHUTDOWN	37	—	EXPCON_IO27	D13	User Defined
ASC2_12V_OC_SENSE	29	—	EXPCON_IO21	G11	User Defined
ASC2_12V_OC_SHUTDOWN	25	—	EXPCON_IO18	D9	User Defined

Table C.4. Miscellaneous – MachXO3-9400 Development Board and ASC Bridge Board Connections

Bridge Board Signal Name	J2 Pin X3 Pin	J3 Pin X2 Pin	MachXO3 Board Signal Name	MachXO3 Ball	Project Designer Signal Name
I2C_SDA	16	—	EXPCON_IO13	B12	SCL
I2C_SCL	18	—	EXPCON_IO15	A12	SDA
I2C_WRITE_EN[1]	32	—	EXPCON_IO23	D11	—
PB1 (SW1)	15	—	EXPCON_IO12	C6	User Defined
PB2 (SW2)	21	—	EXPCON_IO16	D8	User Defined
MANDATORY_RESET	28	—	EXPCON_IO20	C9	User Defined
FAN1_PWM	—	15	EXPCON_IO40	E16	User Defined
FAN1_TACH	—	20	EXPCON_IO45	G12	User Defined
FAN2_PWM	—	17	EXPCON_IO42	F13	User Defined
FAN2_TACH	—	18	EXPCON_IO43	F15	User Defined
FAN3_PWM	—	19	EXPCON_IO44	G15	User Defined
FAN3_TACH	—	16	EXPCON_IO41	E13	User Defined
EXPCON_OSC	—	29	EXPCON_OSC[2]	—	—
EXPCON_CLKIN	—	31	EXPCON_CLKIN	A10	—
EXPCON_CLKOUT	—	33	EXPCON_CLKOUT	A21	—
HPE_RESOUT#	1	—	HPE_RESOUT#	G9	—
EXPCON_IO0	3	—	EXPCON_IO0	F8	User Defined
EXPCON_IO2	5	—	EXPCON_IO2	F9	User Defined
EXPCON_IO14	17	—	EXPCON_IO14	D7	User Defined
EXPCON_IO17	23	—	EXPCON_IO17	C8	User Defined
CARDSEL#	38	—	CARDSEL#	C13	User Defined

Notes:

1. If I2C_WRITE_EN is not used, remove R4 on the ASC Breakout Boards to isolate their GPIO1 (LED1) signals; the I2C_WRITE_EN signal is bussed to all three ASC connectors on the ASC Bridge board.
2. J10 or Y2 Oscillator.

Appendix D. ECP5 Versa Development Board and ASC Bridge Board Signals and Connections

Table D.1. ASC0 (J4) –ECP5 Versa Development Board and ASC Bridge Board Connections

Bridge Board Signal Name	Bridge Bd. J3 Pin	ECP5 Bd. X3 Pin	ECP5 Versa Board Signal Name	ECP5 Ball	Platform Designer Signal Name
ASC0_CLK_0	5		EXPCON_IO30	B12	N / A
ASC0_RESET	7		EXPCON_IO32	E6	ASC0_RSTN_I
ASC0_RDAT	9		EXPCON_IO34	E7	rdat_0
ASC0_WDAT	13		EXPCON_IO38	E9	wdat_0
ASC0_WRCLK	10		EXPCON_IO35	D7	wrclk_0
ASC0_BOARD_SENSE	4		EXPCON_IO29	B19	User Defined
ASC0_5V_OC_SENSE	6		EXPCON_IO31	B9	User Defined
ASC0_5V_OC_SHUTDOWN	8		EXPCON_IO33	D6	User Defined
ASC0_12V_OC_SENSE	12		EXPCON_IO37	B6	User Defined
ASC0_12V_OC_SHUTDOWN	14		EXPCON_IO39	D9	User Defined

Table D.2. ASC1 (J13) – ECP5 Versa Development Board and ASC Bridge Board Connections

Bridge Board Signal Name	Bridge Bd. J2 Pin	ECP5 Bd. X4 Pin	ECP5 Versa Board Signal Name	ECP5 Ball	Platform Designer Signal Name
ASC1_CLK_0	13		EXPCON_IO10	D11	N / A
ASC1_RESET	7		EXPCON_IO4	D13	ASC1_RSTN_I
ASC1_RDAT	9		EXPCON_IO6	A14	rdat_1
ASC1_WDAT	11		EXPCON_IO8	D14	wdat_1
ASC1_WRCLK	10		EXPCON_IO7	C14	wrclk_1
ASC1_BOARD_SENSE	4		EXPCON_IO1	A13	User Defined
ASC1_5V_OC_SENSE	6		EXPCON_IO3	C13	User Defined
ASC1_5V_OC_SHUTDOWN	8		EXPCON_IO5	E13	User Defined
ASC1_12V_OC_SENSE	12		EXPCON_IO9	E14	User Defined
ASC1_12V_OC_SHUTDOWN	14		EXPCON_IO11	C10	User Defined

Table D.3. ASC2 (J7) – ECP5 Versa Development Board and ASC Bridge Board Connections

Bridge Board Signal Name	J2 Pin X4 Pin	J3 Pin X3 Pin	ECP5 Versa Board Signal Name	ECP5 Ball	Project Designer Signal Name
ASC2_CLK_0		11	EXPCON_IO36	B11	N / A
ASC2_RESET	35	—	EXPCON_IO25	C17	ASC2_RSTN_I
ASC2_RDAT	31	—	EXPCON_IO22	C16	rdat_2
ASC2_WDAT	27	—	EXPCON_IO19	E15	wdat_2
ASC2_WRCLK	33	—	EXPCON_IO24	B17	wrclk_2
ASC2_BOARD_SENSE	36	—	EXPCON_IO26	A17	User Defined
ASC2_5V_OC_SENSE	39	—	EXPCON_IO28	A18	User Defined
ASC2_5V_OC_SHUTDOWN	37	—	EXPCON_IO27	B18	User Defined
ASC2_12V_OC_SENSE	29	—	EXPCON_IO21	B16	User Defined
ASC2_12V_OC_SHUTDOWN	25	—	EXPCON_IO18	D15	User Defined

Table D.4. Miscellaneous – ECP5 Versa Development Board and ASC Bridge Board Connections

Bridge Board Signal Name	J2 Pin X4 Pin	J3 Pin X3 Pin	ECP5 Versa Board Signal Name	ECP5 Ball	Project Designer Signal Name
I2C_SDA[1]	16	—	EXPCON_IO13	B10	SCL
I2C_SCL[1]	18	—	EXPCON_IO15	E12	SDA
I2C_WRITE_EN[2]	32	—	EXPCON_IO23	D16	—
PB1 (SW1)	15	—	EXPCON_IO12	A9	User Defined
PB2 (SW2)	21	—	EXPCON_IO16	B15	User Defined
MANDATORY_RESET	28	—	EXPCON_IO20	A16	User Defined
FAN1_PWM	—	19	EXPCON_IO40	C7	User Defined
FAN1_TACH	—	20	EXPCON_IO45	C6	User Defined
FAN2_PWM	—	17	EXPCON_IO42	D8	User Defined
FAN2_TACH	—	18	EXPCON_IO43	E8	User Defined
FAN3_PWM	—	15	EXPCON_IO44	B8	User Defined
FAN3_TACH	—	16	EXPCON_IO41	C8	User Defined
EXPCON_OSC[3]	—	29	EXPCON_OSC	—	—
EXPCON_CLKIN	—	31	EXPCON_CLKIN	A10	—
EXPCON_CLKOUT	—	33	EXPCON_CLKOUT	E11	—
HPE_RESOUT#	1		HPE_RESOUT#	A8	—
EXPCON_IO0	3		EXPCON_IO0	A12	User Defined
EXPCON_IO2	5		EXPCON_IO2	B13	User Defined
EXPCON_IO14	17	—	EXPCON_IO14	D12	User Defined
EXPCON_IO17	23	—	EXPCON_IO17	C15	User Defined
CARDSEL#	38	—	CARDSEL#	A7	User Defined

Notes:

1. SDA and SCL signal mapping shown are for SW3 (I^2C Select) in the MachXO3 position.
2. If I2C_WRITE_EN is not used, remove R4 on the ASC Breakout Boards to isolate their GPIO1 (LED1) signals; the I2C_WRITE_EN signal is bussed to all three ASC connectors on the ASC Bridge board.
3. ispCLOCK5406D BANK_2P (U13 pin 27).

Revision History

Revision 2.1, November 2018

Section	Change Summary
Known issue	Added this section.
Ordering Information	Corrected part number to *L-ASC-BRIDGE-EVN* and added note to table.
Revision History	Corrected document number to FPGA-EB-02025.

Revision 2.0, September 2018

Section	Change Summary
All	• Changed document number from EB102 to FPGA-EB-02025. • Changed document template. • Applied minor editorial changes.
	Added MachXO3 support.
Ordering Information	Added this section.
Appendix A. Board Schematics	Updated version of schematic drawings to Rev. B.

Revision 1.0, July 2015

Section	Change Summary
All	Initial release

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