ZERO DELAY, LOW SKEW BUFFER

ICS574

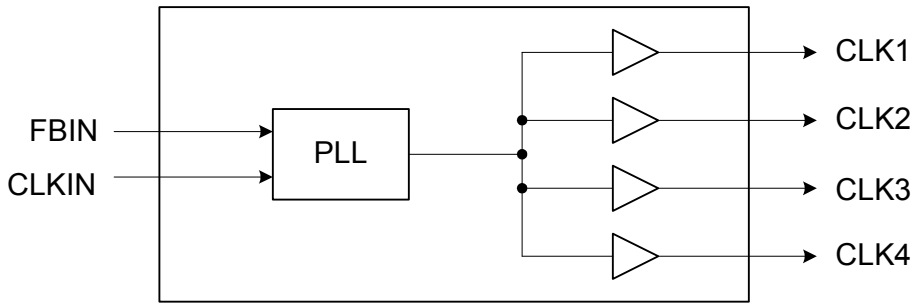
Description

The ICS574 is a low jitter, low-skew, high performance PLL-based zero delay buffer for high speed applications. Based on IDT's proprietary low jitter Phase Locked Loop (PLL) techniques, the device provides four low skew outputs at speeds up to 160 MHz at 3.3 V. When one of the outputs is connected directly to FBIN, the rising edge of each output is aligned with the rising edge of the input clock. External delay elements connected in the feedback loops will cause the outputs to occur before the inputs by the amount of propagation delay of the external element.

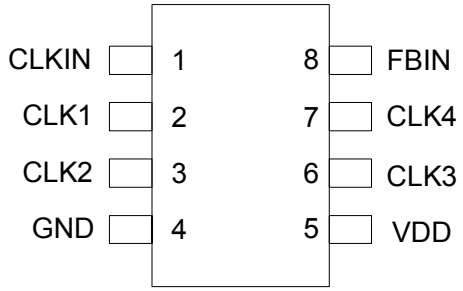
Features

- Packaged in 8 pin narrow SOIC, Pb (lead) free
- Zero input-to-output delay
- Four 1X outputs
- Output to output skew is less than 150 ps
- Output clocks up to 160 MHz at 3.3 V
- External feedback path for output edge placement
- Spread Smart™ technology works with spread spectrum clock generators
- Full CMOS outputs with 18 mA output drive capability at TTL levels at 3.3 V
- Advanced, low power, sub-micron CMOS process
- Operating voltage from 3.0 to 5.5 V
- Industrial temperature version available

Block Diagram



Pin Assignment



Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	CLKIN	Input	Clock input. Connect to input clock source.
2, 3, 6, 7	CLK1:4	Output	Clock Outputs (4).
4	GND	Power	Connect to ground.
5	VDD	Power	Power supply. Connect both pins to same voltage (either 3.3 V or 5 V).
8	FBIN	Input	Feedback input.

External Components

The ICS574 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.1µF should be connected between VDD and GND on pins 4 and 5, as close to the device as possible. A series termination resistor of 33Ω may be used close to the pin for each clock output to reduce reflections.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS574. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD (referenced to ground)	-0.5 V to 7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Electrostatic Discharge (MII-STD-883)	2000 V (minimum)
Ambient Operating Temperature	-40° C to +85° C
Soldering Temperature (10 seconds max.)	260° C
Junction Temperature	150° C
Storage Temperature	-65 to +150° C

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Supply Voltage	VDD		3		5.5	V
Input High Voltage	V_{IH}		VDD/2+1			V
Input Low Voltage	V_{IL}				VDD/2-1	V
Output High Voltage, CMOS level	V_{OH}	I_{OH} = -5 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -18 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 18 mA			0.4	V
IDD Operating Supply Current		No load (Note 2)		36		mA
Short Circuit Current	I_{OS}	Each output		±65		mA
Input Capacitance	C_{IN}			7		pF

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency, clock	f_{IN}	FBIN from CLK4	20		160	MHz
Output Frequency, clock		FBIN from CLK4	20		160	MHz
Output Clock Rise Time		0.8 to 2.0 V, 15 pF load			1.5	ns
Output Clock Fall Time		2.0 to 0.8 V, 15 pF load			1.5	ns
Output Clock Duty Cycle, 3.3 V		At 1.4 V	40	50	60	%
Device-to-device Skew, equally loaded		Rising edges at VDD/2			700	ps
Outpu-to-output Skew, equally loaded		Rising edges at VDD/2			150	ps
Maximum Absolute Jitter				170		ps
Cycle-to-cycle Jitter, 15 pF loads		66.67 MHz outputs			250	ps

Notes:
1. Stresses beyond those listed in Absolute Maximum Ratings can permanently damage the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximum Ratings may affect device reliability.
2. With CLKIN = 160 MHz, FBIN to CLK4.

Using Spread Spectrum Input Clocks

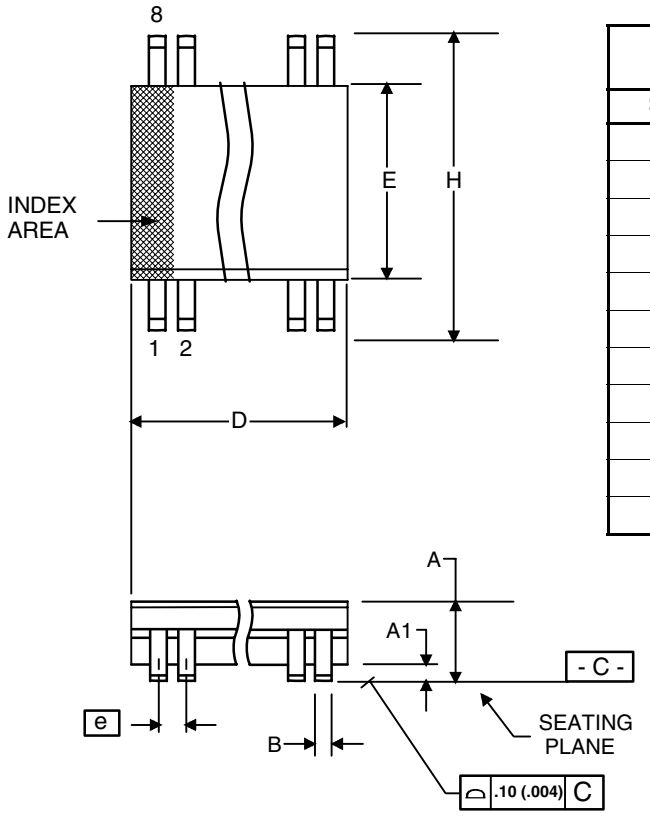
The ICS574 uses IDT's Spread Smart technology, allowing it to accurately track (pass through) any clocks that implement spread spectrum techniques.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W
Thermal Resistance Junction to Top of Case	Ψ_{JT}	Still air		20		°C/W

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
574MLF	574MLF	Tubes	8-pin SOIC	0 to +70° C
574MLFT		Tape and Reel	8-pin SOIC	0 to +70° C
574MILF	574MILF	Tubes	8-pin SOIC	-40 to +85° C
574MILFT		Tape and Reel	8-pin SOIC	-40 to +85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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