FMMT411FDBW

NPN LOW VOLTAGE AVALANCHE TRANSISTOR IN DFN2020-3

Description

The DIODES™ FMMT411FDBW is a silicon planar bipolar transistor designed for operating in avalanche mode. Tight process control and low inductance packaging combine to produce high on-current pulses with fast edges.

Applications

- Laser diode drivers for ranging and measurement (LIDAR)
- Radar systems
- Fast edge switch generator
- High-speed pulse generators

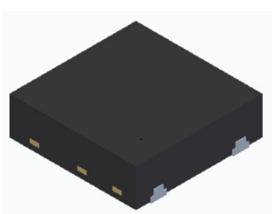
Features

- I_{USB} = 35A typical
- BV_{CBO} > 80V
- BV_{CEO} > 15V
- Specifically Designed for Low Voltage Avalanche Mode Operation
- Low Profile 0.62mm High Package for Thin Applications
- Sidewall Tin Plating for Wettable Flanks in AOI
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen- and Antimony-Free. "Green" Device (Note 3)**
- **An automotive-compliant part is available under separate datasheet (DIODES™ FMMT411FDBWQ)**

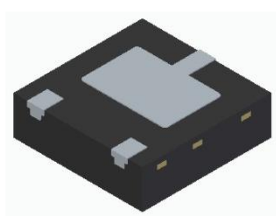
Mechanical Data

- Package: W-DFN2020-3/SWP (Type A)
- Nominal Package Height: 0.62mm
- Package Material: Molded Plastic. "Green" Molding Compound. UL Flammability Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin, Solderable per MIL-STD-202, Method 208 (e3)
- Weight: 0.01 grams (Approximate)

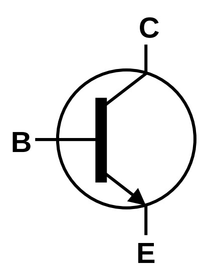
W-DFN2020-3/SWP (Type A)



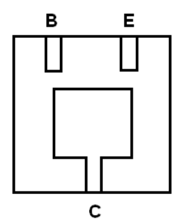
Top View



Bottom View



Device Symbol



Bottom View
Pin-Out

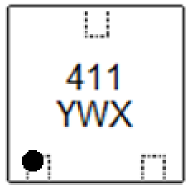
Ordering Information (Note 4)

Part Number	Package	Marking	Reel Size (inches)	Tape Width (mm)	Packing	
					Qty.	Carrier
FMMT411FDBW-7	W-DFN2020-3	411	7	8	3000	Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" an Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

U-DFN2020-3 (Type A)



411 = Product Type Marking Code
Y = Year: 0~9
W = Week: A~Z: 1~26 Week;
a~z; 27~52 Week; z Represents
52 and 53 Week
X = A~Z: Internal Code

Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	80	V
Collector-Emitter Voltage	V_{CES}	80	V
Collector-Emitter Voltage	V_{CEO}	15	V
Emitter-Base Voltage	V_{EBO}	7	V
Continuous Collector Current	I_C	5	A

Thermal Characteristics (@ T_A = +25°C, unless otherwise specified.)

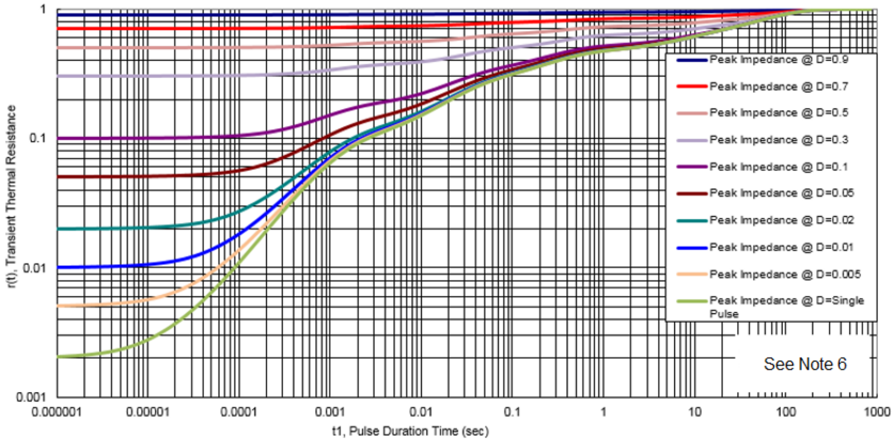
Characteristic		Symbol	Value	Unit
Power Dissipation	(Note 5)	P_D	0.82	W
	(Note 6)	P_D	1.8	W
Thermal Resistance, Junction to Ambient	(Note 5)	$R_{\theta JA}$	154	°C/W
	(Note 6)	$R_{\theta JA}$	67	°C/W
Thermal Resistance, Junction to Case	(Note 5)	$R_{\theta JC}$	32	°C/W
	(Note 6)	$R_{\theta JC}$	12	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

ESD Ratings (Note 7)

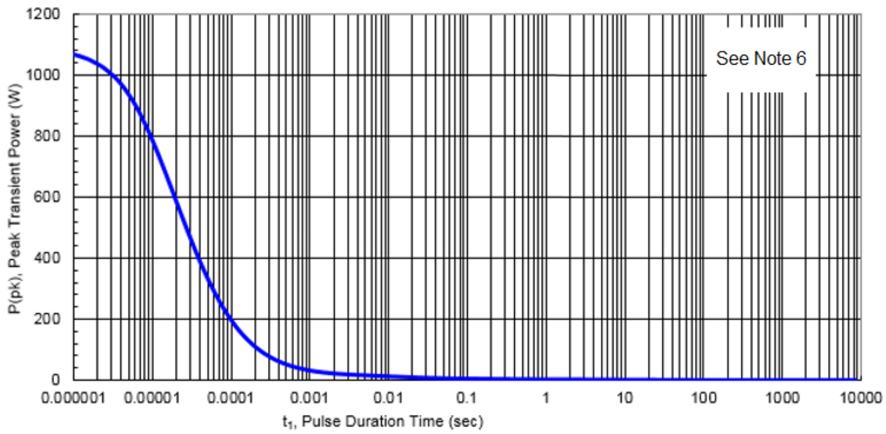
Characteristic	Symbol	Value	Unit	JEDEC Class
Electrostatic Discharge - Human Body Model	ESD HBM	4,000	V	3A
Electrostatic Discharge - Machine Model	ESD MM	400	V	C

Notes:
5. For a device mounted with the collector lead on MRP single-sided 1.6mm FR-4 PCB; device is measured under still air conditions whilst operating in a steady-state.
6. For a device mounted with the collector lead on 25mm x 25mm 2oz copper that is on a single-sided 1.6mm FR-4 PCB; device is measured under still air conditions whilst operating in a steady-state.
7. Refer to JEDEC specification JESD22-A114 and JESD22-A115.

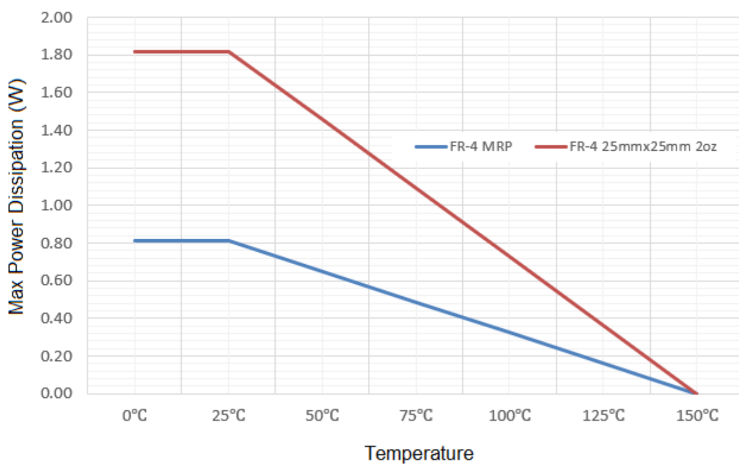
Thermal Characteristics and Derating information



Transient Thermal Resistance



Single Pulse Maximum Power Dissipation



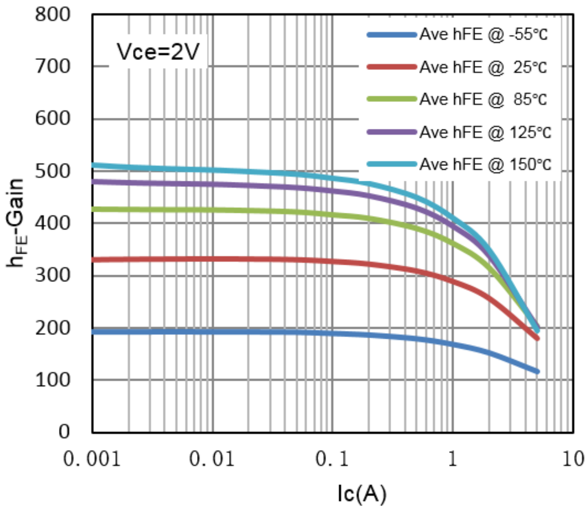
Derating Curve

Electrical Characteristics (@ T_A = +25°C, unless otherwise specified.)

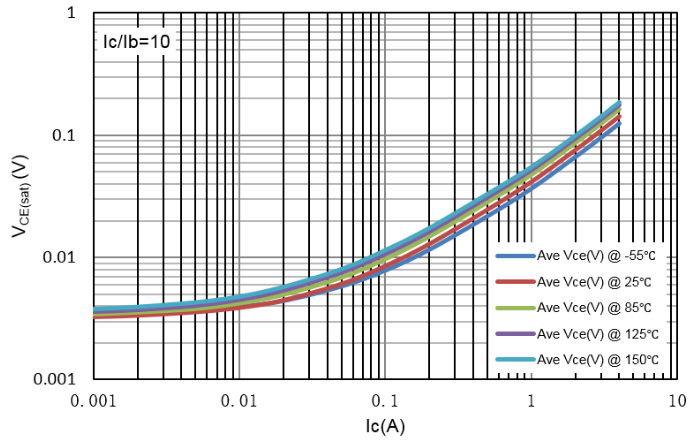
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
Collector-Base Breakdown Voltage	BV_{CBO}	80	—	—	V	I_C = 100µA
Collector-Emitter Breakdown Voltage	BV_{CES}	80 75	—	—	V	I_C = 100µA T_J = -50°C to +150°C
Collector-Emitter Breakdown Voltage	BV_{CEO}	15	—	—	V	I_C = 100µA
Emitter-Base Breakdown Voltage	BV_{EBO}	7	—	—	V	I_E = 100µA
Collector Cutoff Current	I_{CBO}	—	—	100 10	nA µA	V_{CB} = 75V V_{CB} = 75V, T_J = +100°C
Emitter Cutoff Current	I_{EBO}	—	—	20	nA	V_{EB} = 6V
Static Forward Current Transfer Ratio (Note 8)	h_{FE}	100	—	—	—	I_C = 10mA, V_{CE} = 10V
Collector-Emitter Saturation Voltage (Note 8)	$V_{CE(sat)}$	—	—	100	mV	I_C = 10mA, I_B = 1mA
Base-Emitter Saturation Voltage (Note 8)	$V_{BE(sat)}$	—	—	800	mV	I_C = 10mA, I_B = 1mA
Current in Second Breakdown (Pulsed)	I_{USB}	—	35	—	A	V_{CE} = 70V, C_{CE} = 470pF
Input Capacitance	C_{ibo}	—	49	—	pF	V_{EB} = 0.5V. f = 1MHz
Output Capacitance	C_{obo}	—	17	—	pF	V_{CB} = 20V, I_E = 0 f = 1MHz
Transition Frequency	f_T	80	110	—	MHz	V_{CE} = 20V, I_C = 10mA, f = 20MHz
Turn-On Time	$t_{d(on)}$	—	59	—	ns	V_{CE} = 10V, I_C = 100mA I_{B1} = 10mA, I_{B2} = -10mA
	t_r	—	37	—	ns	
Turn-Off Time	$t_{d(off)}$	—	320	—	ns	
	t_f	—	25	—	ns	

Note: 8. Measured under pulsed conditions. Pulse width ≤ 300µs. Duty cycle ≤ 2%.

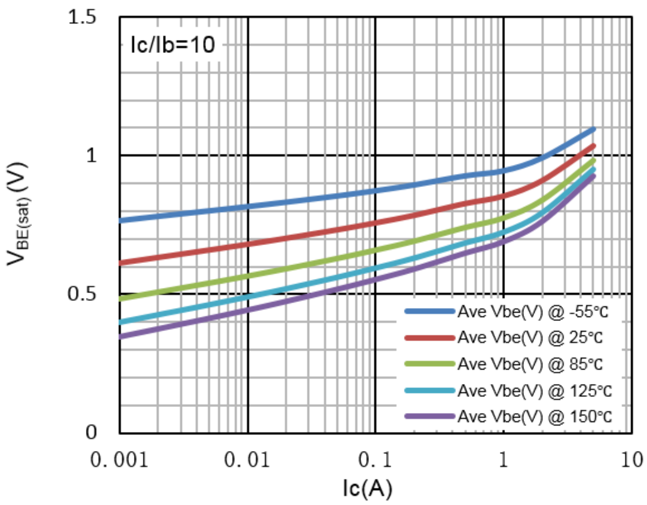
Typical Characteristics



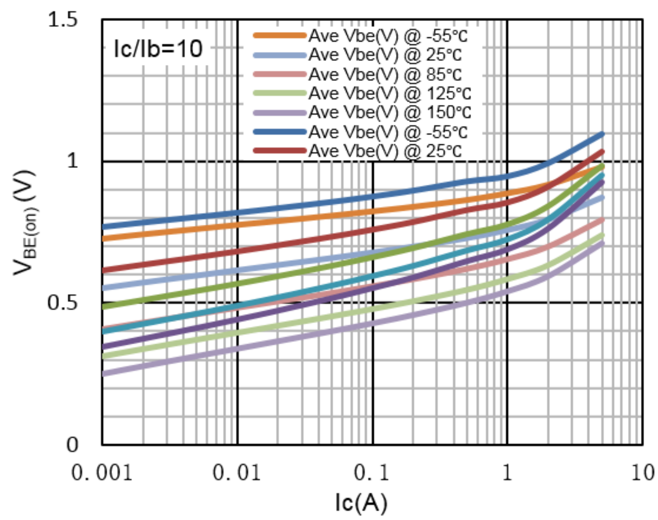
h_{FE} vs I_C



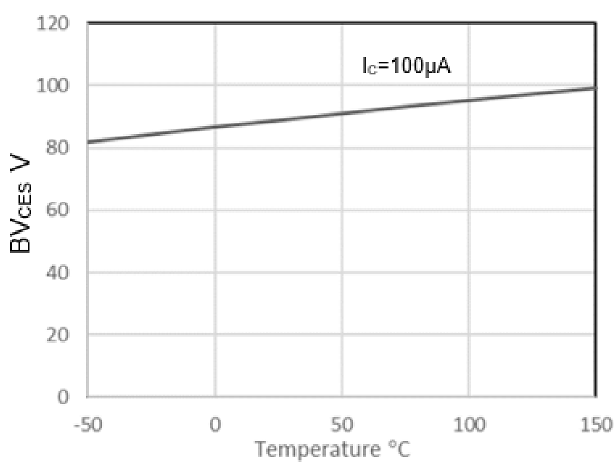
$V_{CE(sat)}$ vs I_C



$V_{BE(sat)}$ vs I_C



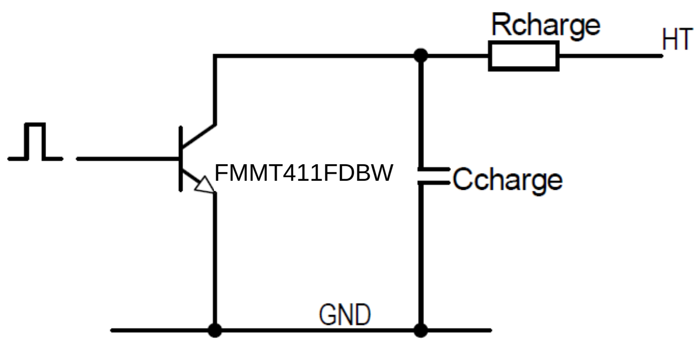
$V_{BE(on)}$ vs I_C



BV_{CES} vs Temperature

Application Considerations

In a typical circuit a large pulse is applied to the base and the resultant energy is enough to cause the onset of avalanche multiplication. Once breakdown has been established it will continue until the energy in the breakdown region is insufficient to maintain the condition, or the crystal lattice is permanently damaged. It is important therefore to limit the total energy expended during breakdown. The typical method of achieving avalanche uses the circuit shown below, wherein the energy per cycle is set by the charge voltage and capacitance value.



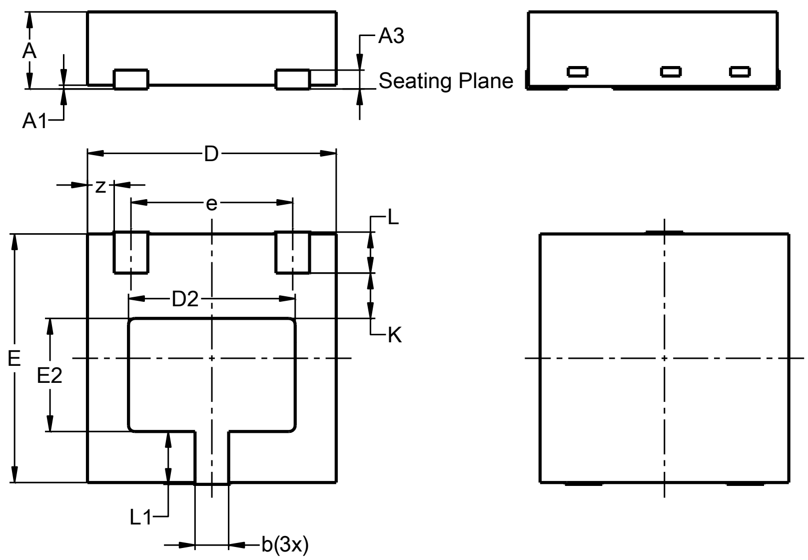
The effect of parasitic inductance in the circuit must be considered. Excessive inductance will reduce the current pulse height and slew current pulse edges. Loop area enclosed by the power circuit and track lengths should be minimized.

Thermal limitations must also be observed to ensure the transistor junction temperature is not exceeded. Avalanche power dissipation can be calculated from the energy per pulse and the pulse frequency, but PCB thermal resistance depends on many factors such as design, layout, and proximity of other components; so thermal performance should be verified by measurement.

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-DFN2020-3/SWP (Type A)



W-DFN2020-3 /SWP (Type A)			
Dim	**Min**	**Max**	**Typ**
A	0.57	0.67	0.62
A1	0.00	0.05	0.03
A3	—	—	0.152
b	0.22	0.32	0.27
D	1.95	2.05	2.00
D2	1.24	1.44	1.34
D4	0.56	0.76	0.66
E	1.95	2.05	2.00
E2	0.81	1.01	0.91
e	—	—	1.30
k	—	—	0.365
L	0.28	0.38	0.33
L1	0.375	0.475	0.425
z	—	—	0.215
All Dimensions in mm			

Suggested Pad Layout

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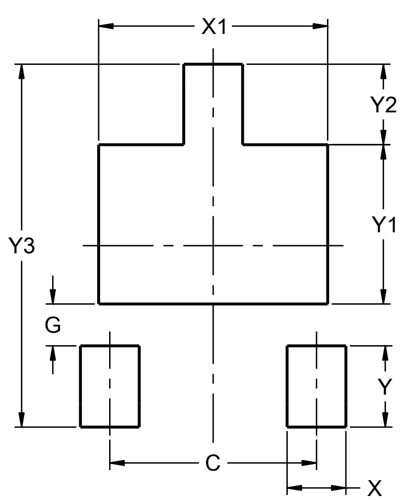
W-DFN2020-3/SWP (Type A)



Dimensions	Value (in mm)
C	1.300
G	0.265
X	0.370
X1	1.440
Y	0.515
Y1	1.010
Y2	0.510
Y3	2.300

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