3-Channel, 12-Bit, PWM LED Driver with Buck DC/DC Converter and Differential Signal Interface

Check for Samples: TLC5970

FEATURES

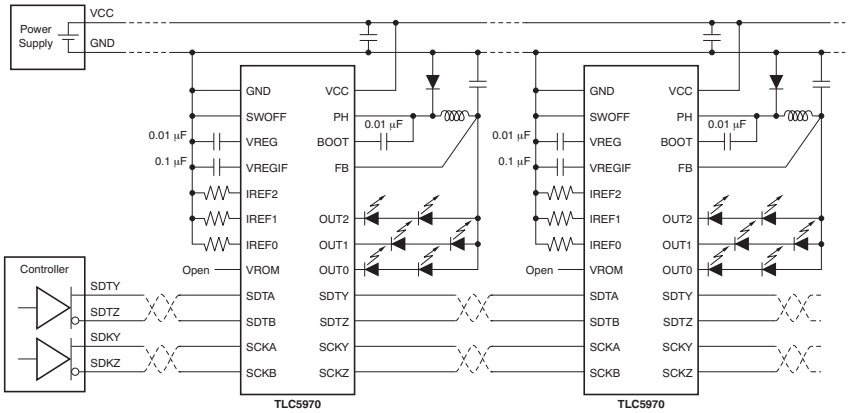
- **3-Channel, Constant-Current Sink Output**
- **Current Capability: 150 mA per channel**
- **Grayscale (GS) Control with PWM: 12-bit (4096 steps)**
- **Dot Correction (DC): 7-bit (128 steps)**
- **Global Brightness Control (BC): 7-bit (128 steps)**
- **EEPROM for Dot Correction Storage**
- **Input Voltage: Up to 36 V**
- **LED Supply Voltage: Up to 17 V with Auto LED Anode Voltage Control**
- **Constant-Current Accuracy:**
  - **Channel-to-Channel = ±0.5% (typ)**
  - **Device-to-Device = ±3% (typ)**
- **Data Transfer Rate: 20 MHz**
- **Differential Signal Interface for Long Distance Cascading**
- **Unlimited Device Cascading**
- **Auto Display Repeat/Auto Data Refresh**
- **Internal/External Selectable GS Clock**
- **Thermal Shutdown (TSD)**
- **Package: QFN-28**

APPLICATIONS

- **Full-Color Static LED Displays for Building Wall**
- **Long Distance and Large Area Illumination**

DESCRIPTION

The TLC5970 is a three-channel, constant-current sink driver with a buck dc/dc converter and a differential signal interface. Each channel has individually adjustable currents with 4096 PWM grayscale (GS) steps and 128 constant-current sink steps for dot correction (DC). The dot correction adjusts the brightness variations between LEDs. The DC data can be stored in the internal EEPROM. Also, current through all three channels can be controlled by global brightness control (BC) data with 128 steps. GS control, DC, and BC are accessible via a differential signal interface. The maximum current value for each channel is set by a single external resistor. The TLC5970 contains a dc/dc buck converter. The dc/dc converter improves system efficiency, reduces system level currents, and allows thinner gauge wiring by optimizing the LED anode voltage to keep the LED cathode voltage to 1 V. The TLC5970 proivdes overtemperature protection by turning all output drivers off when the IC temperature is too high (exceeds +138°C).



Typical Application Circuit Example

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLC5970	QFN-28 6.0 mm × 6.0 mm	TLC5970RHPR	Tape and Reel, 3000
		TLC5970RHPT	Tape and Reel, 250

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at ti.com.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Over operating free-air temperature range, unless otherwise noted.

		VALUE		UNIT
		MIN	MAX	
Supply voltage	V_{CC}	–0.3	+40	V
Input voltage	BOOT	–0.3	+50	V
	BOOT-PH difference	–0.3	+10	V
	FB	–0.3	+18	V
	IREF0 to IREF2, SWOFF	–0.3	VREG + 0.3	V
	SDTA, SDTB, SCKA, SCKB	–10	+15	V
	VROM	–0.3	+21	V
Output voltage	PH (steady-state)	–0.6	+40	V
	PH (transient < 10 ns)		–1.2	V
	OUT0 to OUT2	–0.3	+18	V
	SDTY, SDTZ, SCKY, SCKZ	–10	+15	V
	VREG, VREGIF	–0.3	+6	V
Output current	PH (dc)		–800	mA
	PH (peak)		–2	A
	OUT0 to OUT2		+180	mA
	SDTY, SDTZ, SCKY, SCKZ	–35	+35	mA
Electrostatic discharge rating	Human body model (HBM) SDTA, SDTB, SCKA, SCKB, SDTY, SDTZ, SCKY, SCKZ		4	kV
	Human body model (HBM) Other pins		2	kV
	Charged device model (CDM) SDTA, SDTB, SCKA, SCKB, SDTY, SDTZ, SCKY, SCKZ		1000	V
	Charged device model (CDM) Other pins		500	V
Operation junction temperature	$T_{J\ (max)}$		+150	°C
Storage temperature	T_{stg}	–55	+150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TLC5970 RHP 28	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	26.7	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	11.7	
θ_{JB}	Junction-to-board thermal resistance	5.3	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	5.2	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	1.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

DISSIPATION RATINGS

PACKAGE	DERATING FACTOR ABOVE T_A = +25°C	POWER RATING T_A < +25°C	POWER RATING T_A = +70°C	POWER RATING T_A = +85°C
QFN-28 Bottom side heat sink soldered(1)	33.2 mW/°C	4149 mW	2655 mW	2157 mW

(1) The package thermal impedance is calculated in accordance with JESD51-5.

RECOMMENDED OPERATING CONDITIONS

At T_A = –40°C to +85°C, unless otherwise noted.

			TLC5970			UNIT
			MIN	NOM	MAX	
DC CHARACTERISTICS						
V_{CC}	Supply voltage		10		36	V
V_{CC1}		VCC = SWOFF = VREG = VREFIF = FB (no buck conver operation mode)	4.75		5.5	V
V_I	Voltage at input terminal	FB (buck converter operation mode)	7		17	V
V_{I1}		SDTA, SDTB, SCKA, SCKB	–7		12	V
V_{I2}		VROM for data writing	18.5	19	19.5	V
V_{ID}	Differential voltage at input terminal(1)	SDTA-SDTB, SCKA-SCKB	–12		12	V
V_{IH}	High level input voltage	SWOFF	0.7 × VREG		VREG	V
V_{IL}	Low level input voltage	SWOFF	GND		0.3 × VREG	V
V_O	Voltage at output terminal	OUT0 to OUT2			17	V
I_{OLC}	Constant output sink current	OUT0 to OUT2			150	mA
I_{OH}	High level output current	SDTY, SDTZ, SCKY, SCKZ	–30			mA
I_{OL}	Low level output current	SDTY, SDTZ, SCKY, SCKZ			30	mA
T_A	Operating free-air temperature		–40		+85	°C
T_J	Operating junction temperature		–40		+125	°C
AC CHARACTERISTICS						
f_{CLK}	Data shift clock frequency	SCKA-SCKB			20	MHz
T_{WH}/T_{WL}	Pulse duration	SCKA-SCKB	12			ns
T_{SU}	Setup time	(SDTA-SDTB)-(SCKA-SCKB) ↑	5			ns
T_H	Hold time	(SDTA-SDTB)-(SCKA-SCKB) ↑	3			ns
N_{ROM}	Number of EEPROM write cycles	At each address			10	Times

(1) Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.

ELECTRICAL CHARACTERISTICS

At V_{CC} = 10 V to 36 V and T_A = –40°C to +85°C. Typical values at V_{CC} = 24 V, FB = 17 V, and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5970			UNIT
			MIN	TYP	MAX	
BUCK DC/DC CONVERTER BLOCK						
R_{DSON}	High-side MOS switch on-resistance	At PH pin. VCC = 10 V to 36V, I_O = 500mA, VBOOT = VCC + 9 V, PH high-side MOS switch is on		300	770	MΩ
R_{DSOFF}	High-side MOS switch off-resistance	At PH pin. VCC = 36 V, PH = 0 V, PH high-side MOS switch is off	1			MΩ
V_{BOOT}	Boot regulator output voltage	At BOOT pin. VCC = 10 V, IBOOT = –10 mA, PH high-side MOS switch is off	8			V
V_{BOOT1}		At BOOT pin. VCC = 36 V, PH = 0 V, IBOOT = no load, PH high-side MOS switch is off			10	V
V_{SCP}	Short-circuit protection detection	At FB pin	3.75	4	4.25	V
I_{FB}	Input current	At FB pin. SDTA/SCKA = 0 V, SDTB/SCKB = 3 V, SDTY/SDTZ/SCKY/SCKZ/PH/BOOT = open, FB = 7 V to 17 V, V_{OUTn} = 1.0 V, GSn = 000h, DCn = BC = 7Fh, R_{IREF} = 15 kΩ, internal oscillator mode, and auto repeat mode		18	29	mA
I_{FB1}		At FB pin. SDTA/SCKA = 0 V, SDTB/SCKB = 3 V, SDTY/SDTZ/SCKY/SCKZ/PH/BOOT = open, FB = 7 V to 17 V, V_{OUTn} = 1.0 V, GSn = 000h, DCn = BC = 7Fh, R_{IREF} = 2 kΩ, internal oscillator mode, and auto repeat mode		19	30	mA
I_{FB2}		At FB pin. SDTA/SDTB = 10 MHz, SCKA/SCKB = 20 MHz with 0 V to 3 V swing, SDTY-SDTZ/SCKY-SCKZ = RL_{DIF} = 10 kΩ, CL_{DIF} = 15 pF, PH/BOOT = open, FB = 7 V to 17 V, V_{OUTn} = 1.0 V, GSn = FFFh, DCn = BC = 7Fh, R_{IREF} = 2 kΩ, internal oscillator mode, and auto repeat mode		36	60	mA
I_{FB3}		At FB pin. SDTA/SDTB = 10 MHz, SCKA/SCKB = 20 MHz with 0 V to 3 V swing, SDTY-SDTZ/SCKY-SCKZ = RL_{DIF} = 2 × 51 Ω, CL_{DIF} = 50 pF, PH/BOOT = open, FB = 7 V to 17 V, V_{OUTn} = 1.0 V, GSn = FFFh, DCn = BC = 7Fh, R_{IREF} = 2 kΩ, internal oscillator mode, and auto repeat mode		65	115	mA
I_{FB4}		At FB pin. SDTA/SDTB = 10 MHz, SCKA/SCKB = 20 MHz with 0 V to 3 V swing, SDTY-SDTZ/SCKY-SCKZ = RL_{DIF} = 2 × 51 Ω, CL_{DIF} = 50 pF, PH/BOOT = open, FB = 7 V to 17 V, V_{OUTn} = 1.0 V, GSn = FFFh, DCn = BC = 7Fh, R_{IREF} = 1 kΩ, internal oscillator mode, and auto repeat mode		68	130	mA

ELECTRICAL CHARACTERISTICS (continued)

At V_{CC} = 10 V to 36 V and T_A = –40°C to +85°C. Typical values at V_{CC} = 24 V, FB = 17 V, and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5970			UNIT
			MIN	TYP	MAX	
LED DRIVER BLOCK						
I_{OLC}	Constant output current	At OUT0 to OUT2 pins. OUTn are on, DCn = BC = 7Fh, V_{OUT} = 1 V, R_{IREF} = 1 kΩ	136	151	166	mA
I_{OLKG}	Leakage output current	At OUT0 to OUT2 pins. OUTn are off, DCn = 7Fh, BC = 7Fh, V_{OUT} = 17 V, R_{IREF} = 1 kΩ			0.1	µA
ΔI_{OLC}	Constant-current error (channel-to-channel)(1)	At OUT0 to OUT2 pins. OUTn are on, DCn = BC = 7Fh, V_{OUT} = 1 V, R_{IREF} = 1 kΩ		±0.5	±3	%
ΔI_{OLC1}	Constant-current error (device-to-device)(2)	At OUT0 to OUT2 pins. OUTn are on, DCn = BC = 7Fh, V_{OUT} = 1 V, R_{IREF} = 1 kΩ		±3	±6	%
ΔI_{OLC2}	Line regulation(3)	OUT0 to OUT2 are on, DCn = BCn = 7Fh, V_{OUT} = 1 V, R_{IREF} = 1 kΩ, VREG = 3.3 V to 5.5 V		±0.5	±2	%/V
ΔI_{OLC3}	Load regulation(4)	OUT0 to OUT2 are on, DCn = BCn = 7Fh, V_{OUT} = 1 V to 3 V, R_{IREF} = 1 kΩ		±1	±2	%/V
V_{IREF}	Reference voltage output	IREF0 to IREF2, R_{IREF} = 1 kΩ	1.17	1.20	1.23	V

(1) The deviation of each output from the average of OUT0–OUT2 constant-current. Deviation is calculated by the formula:

$$\Delta\,(\%) = \left(\frac{I_{OUTn}}{\frac{(I_{OUT0} + I_{OUT1} + I_{OUT2})}{3}} - 1 \right) \times 100$$

(2) The deviation of the OUT0–OUT2 constant-current average from the ideal constant-current value. Deviation is calculated by the following formula:

$$\Delta\,(\%) = \left(\frac{\frac{(I_{OUT0} + I_{OUT1} + I_{OUT2})}{3} - (\text{Ideal Output Current})}{\text{Ideal Output Current}} \right) \times 100$$

Ideal current is calculated by the formula:

$$I_{OUT(IDEAL)} = 125 \times \left(\frac{1.20}{R_{IREF}} \right)$$

(3) Line regulation is calculated by this equation:

$$\Delta\,(\%/V) = \left(\frac{(I_{OUTn} \text{ at VREG} = 5.5\text{ V}) - (I_{OUTn} \text{ at VREG} = 3\text{ V})}{(I_{OUTn} \text{ at VREG} = 3.0\text{ V})} \right) \times \frac{100}{5.5\text{ V} - 3\text{ V}}$$

(4) Load regulation is calculated by the equation:

$$\Delta\,(\%/V) = \left(\frac{(I_{OUTn} \text{ at } V_{OUTn} = 3\text{ V}) - (I_{OUTn} \text{ at } V_{OUTn} = 1\text{ V})}{(I_{OUTn} \text{ at } V_{OUTn} = 1\text{ V})} \right) \times \frac{100}{3\text{ V} - 1\text{ V}}$$

ELECTRICAL CHARACTERISTICS (continued)

At V_{CC} = 10 V to 36 V and T_A = –40°C to +85°C. Typical values at V_{CC} = 24 V, FB = 17 V, and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5970			UNIT
			MIN	TYP	MAX	
DIFFERENTIAL INTERFACE BLOCK						
V_{ITP}	Positive-going input threshold voltage	At SDTA-SDTB or SCKA-SCKB pins. Common-mode, V_{IB} = 1.5 V (see Figure 4)			0.2	V
V_{ITN}	Negative-going input threshold voltage	At SDTA-SDTB or SCKA-SCKB pins. Common-mode, V_{IB} = 1.5 V (see Figure 4)	–0.2			V
V_{ITHYS}	Hysteresis voltage ($\lvert V_{ITP} - V_{ITN} \rvert$)	Common-mode	30	50	110	mV
I_I	Input current	At SDTA/SDTB/SCKA/SCKB pins. V_{IH} = 12 V (other inputs at 0 V), VCC = 24 V		2	3	mA
I_{I1}		At SDTA/SDTB/SCKA/SCKB pins. V_{IH} = 12 V (other inputs at 0 V), VCC = 0 V		2	3	mA
I_{I2}		At SDTA/SDTB/SCKA/SCKB pins. V_{IH} = –7 V (other inputs at 0 V), VCC = 24 V	–3	–1.2		mA
I_{I3}		At SDTA/SDTB/SCKA/SCKB pins. V_{IH} = –7 V (other inputs at 0 V), VCC = 0 V	–3	–1		mA
V_{OD}	Differential output voltage	At SDTY-SDTZ or SCKY-SCKZ pins. 1/2 × RL_{DIF} = 51 Ω (see Figure 6)	1	1.8	3	V
ΔV_{OD}	Change in magnitude of differential output voltage(5)	At SDTY-SDTZ or SCKY-SCKZ pins. 1/2 × RL_{DIF} = 51 Ω (see Figure 6)	–0.2		0.2	V
V_{OC}	Steady-state common-mode output voltage	At SDTY-SDTZ or SCKY-SCKZ pins. 1/2 × RL_{DIF} = 51 Ω (see Figure 6)	1.5	V_{REG}/2	3	V
ΔV_{OC}	Change in magnitude of steady-state common-mode output voltage(5)	At SDTY-SDTZ or SCKY-SCKZ pins. 1/2 × RL_{DIF} = 51 Ω (see Figure 6)	–0.2		0.2	V
R_{INT}	Internal resistor between differential input pair	At SDTA-SDTB or SCKA-SCKB pins. A pins = 0 V, B pins = 1.8 V		10		kΩ
I_O	Output current with power off	At SDTY-SDTZ or SCKY-SCKZ pins. VCC = 0 V, –7 V ≤ SDTY/SDTZ/SCKY/SCKZ ≤ 12 V, 1 pin sweep, all other outputs are open	–10	±1	20	µA

(5) ΔV_{OD} and ΔV_{OC} are the changes in the steady-state magnitude of V_{OD} and V_{OC}, respectively, that occur when the output data change from a high level to a low level.

ELECTRICAL CHARACTERISTICS (continued)

At V_{CC} = 10 V to 36 V and T_A = –40°C to +85°C. Typical values at V_{CC} = 24 V, FB = 17 V, and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5970			UNIT
			MIN	TYP	MAX	
WHOLE BLOCK						
V_{REG}	Internal power-supply voltage	At VREG pin. C_{REG} = 0.01 µF, GSn = 000h	4.75	5.0	5.25	V
V_{REG1}		At VREGIF pin. C_{REG1} = 0.1 µF, RL_{DIF} = 2 × 51 Ω	4.75	5.0	5.25	V
V_{STR}	Undervoltage lockout	At VREG pin, VREG rising	3.8	4.1	4.4	V
V_{HYS}	Undervoltage lockout hysteresis	At VREG pin	250	350	450	mV
I_{CC}	Supply current	At VCC pin. SDTA/SCKA = 0 V, SDTB/SCKB = 3 V, SDTY/SDTZ/SCKY/SCKZ/PH/BOOT = open, PH not switching, V_{OUTn} = 1.0 V, GSn = 000h, DCn = BC = 7Fh, R_{IREF} = 15 kΩ, internal oscillator mode, and auto repeat mode		4.0	7.5	mA
I_{CC1}		At VCC pin. SDTA/SCKA = 0 V, SDTB/SCKB = 3 V, SDTY/SDTZ/SCKY/SCKZ/PH/BOOT = open, PH not switching, V_{OUTn} = 1.0 V, GSn = 000h, DCn = BC = 7Fh, R_{IREF} = 2 kΩ, internal oscillator mode, and auto repeat mode		7.5	10	mA
I_{CC2}		At VCC pin. SDTA/SDTB = 10 MHz, SCKA/SCKB = 20 MHz with 0 V to 3 V swing, SDTY-SDTZ/SCKY-SCKZ = RL_{DIF} = 10 kΩ, CL_{DIF} = 15 pF, PH/BOOT = open, PH is full switching, V_{OUTn} = 1.0 V, GSn = FFFh, DCn = BC = 7Fh, R_{IREF} = 2 kΩ, internal oscillator mode, and auto repeat mode		8.5	25	mA
I_{CC3}		At VCC pin. SDTA/SDTB = 10 MHz, SCKA/SCKB = 20 MHz with 0 V to 3 V swing, SDTY-SDTZ/SCKY-SCKZ = RL_{DIF} = 2 × 51 Ω, CL_{DIF} = 50 pF, PH/BOOT = open, PH is full switching, V_{OUTn} = 1.0 V, GSn = FFFh, DCn = BC = 7Fh, R_{IREF} = 2 kΩ, internal oscillator mode, and auto repeat mode		8.5	25	mA
I_{CC4}		At VCC pin. SDTA/SDTB = 10 MHz, SCKA/SCKB = 20 MHz with 0 V to 3 V swing, SDTY-SDTZ/SCKY-SCKZ = RL_{DIF} = 2 × 51 Ω, CL_{DIF} = 50 pF, PH/BOOT = open, PH is full switching, V_{OUTn} = 1.0 V, GSn = FFFh, DCn = BC = 7Fh, R_{IREF} = 1 kΩ, internal oscillator mode, and auto repeat mode		15	35	mA
I_{I4}	Input current	At SWOFF pin. V_{IH} = +5 V, V_{IL} = GND	–2		1000	µA
I_{I5}		At VROM pin. V_{IH} = +19.0 V		5	10	mA
T_{TSD}	Thermal shutdown trip point	Rising junction temperature(6)	+150	+162	+175	°C
T_{HYST}	Thermal shutdown hysteresis	Junction temperature(6)	+5	+10	+20	°C
T_{PTD}	Pre thermal shutdown trip point	Rising junction temperature(6)	+125	+138	+150	°C
T_{HYSP}	Pre thermal shutdown hysteresis	Junction temperature(6)	+4	+8	+16	°C

(6) Not tested, specified by design.

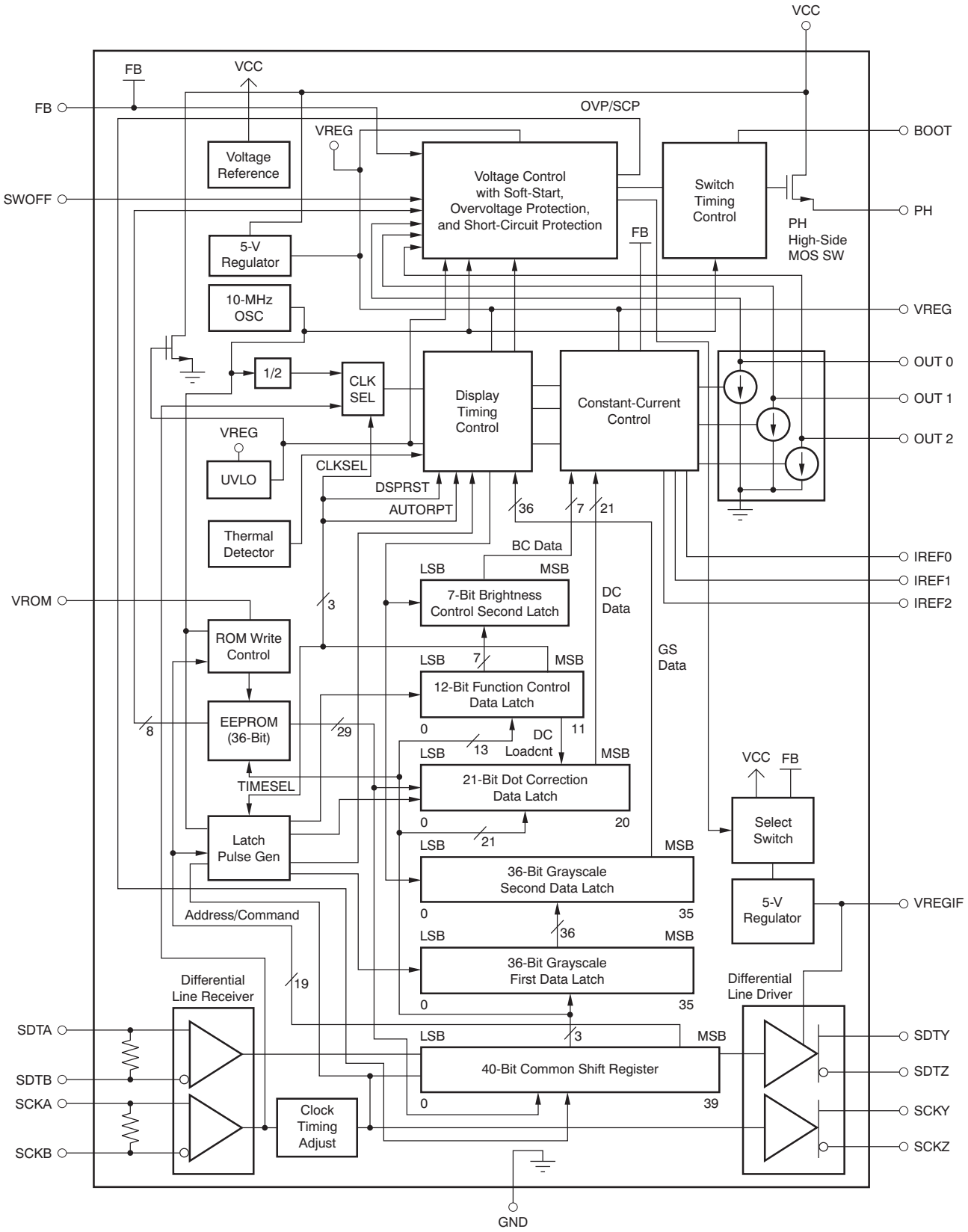
SWITCHING CHARACTERISTICS

At V_{CC} = 10 V to 36 V, T_A = –40°C to +85°C, R_{IREF} = 1 kΩ, and V_{LED} = 5.0 V. Typical values at V_{CC} = 24 V and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5970			UNIT
			MIN	TYP	MAX	
t_{R0}	Rise time	At SDTY, SDTZ, SCKY, or SCKZ pins. RL_{DIF} = 2 × 51 Ω, CL_{DIF} = 50 pF, SDTA-SDTB = SCKA-SCKB = 20 MHz, measured at 0.4 V differential point (see Figure 10 and Figure 11)			15	ns
t_{R1}		At OUTn pins. DCn/BC = 7Fh, RL_{LED} = 27 Ω, CL_{LED} = 15 pF (see Figure 12)		10	15	ns
t_{F0}	Fall time	At SDTY, SDTZ, SCKY, or SCKZ pins. RL_{DIF} = 2 × 51 Ω, CL_{DIF} = 50 pF, SDTA-SDTB = SCKA-SCKB = 20 MHz, measured at 0.4 V differential point (see Figure 10 and Figure 11)			15	ns
t_{F1}		At OUTn pins. DCn/BC = 7Fh, RL_{LED} = 27 Ω, CL_{LED} = 15 pF (see Figure 12)		10	35	ns
t_{D0}	Propagation delay time	(SCKA-SCKB)↑ – (SDTY-SDTZ) , RL_{DIF} = 2 × 51 Ω, CL_{DIF} = 50 pF, DSI mode = 2 (see Figure 10)	20	30	60	ns
t_{D0A}		(SCKA-SCKB)↑ – (SDTY-SDTZ) , RL_{DIF} = 2 × 51 Ω, CL_{DIF} = 50 pF, DSI mode = 1 (see Figure 10)	30	50	90	ns
t_{D0B}		(SCKA-SCKB) ↓ – (SDTY-SDTZ) , RL_{DIF} = 2 × 51 Ω, CL_{DIF} = 50 pF, DSI mode = 0 (see Figure 11)	20	30	55	ns
t_{D1}		(SCKA-SCKB)↑ – (SCKY-SCKZ)↑, RL_{DIF} = 2 × 51 Ω, CL_{DIF} = 50 pF, DSI mode = 2 (see Figure 10)	13	19	33	ns
t_{D1A}		(SCKA-SCKB)↑ – (SCKY-SCKZ)↑, RL_{DIF} = 2 × 51 Ω, CL_{DIF} = 50 pF, DSI mode = 1 (see Figure 10)	13	19	33	ns
t_{D1B}		(SCKA-SCKB)↑↓ – (SCKY-SCKZ)↑↓, RL_{DIF} = 2 × 51 Ω, CL_{DIF} = 50 pF, DSI mode = 0 (see Figure 11)	13	20	30	ns
t_{D2} (1)		(SCKY-SCKZ)↑ – (SDTY-SDTZ), RL_{DIF} = 2 × 51 Ω, CL_{DIF} = 50 pF, DSI mode = 2	5	11	30	ns
t_{D2A} (1)		(SCKY-SCKZ)↑ – (SDTY-SDTZ), RL_{DIF} = 2 × 51 Ω, CL_{DIF} = 50 pF, DSI mode = 1	15	31	60	ns
t_{D3}		(SCKA-SCKB) ↑ – OUT0 turns on/off (see Figure 12)	12	30	60	ns
t_{D4}		(SCKA-SCKB) ↑ – OUT1 turns on/off (see Figure 12)	35	70	140	ns
t_{D5}		(SCKA-SCKB) ↑ – OUT2 turns on/off (see Figure 12)	55	110	220	ns
t_W	Shift clock output one pulse width	(SCKY-SCKZ)↑ – (SCKY-SCKZ) ↓ with DSI mode 1 or mode 2 (see Figure 10)	12	25	35	ns
t_{W_ERR}	Shift clock output pulse width error	High-level pulse width of (SCKA-SCKB) – high-level pulse width of (SCKY-SCKZ) with DSI mode 0 (see Figure 11)	–10		10	ns
f_{OSC}	Internal oscillator frequency		8	10	12	MHz
f_{SW}	High-side MOS switching maximum frequency	At PH pin	1	1.25	1.5	MHz
t_{DTY0}	On-duty cycle	At PH pin. EEPROM data = 7h	83	86	90	%
t_{DTY1}		At PH pin. EEPROM data = 0h	15	18	21	%
t_{SCP}	Short-circuit detection time	VFB < VSCP		2.4	4.0	µs

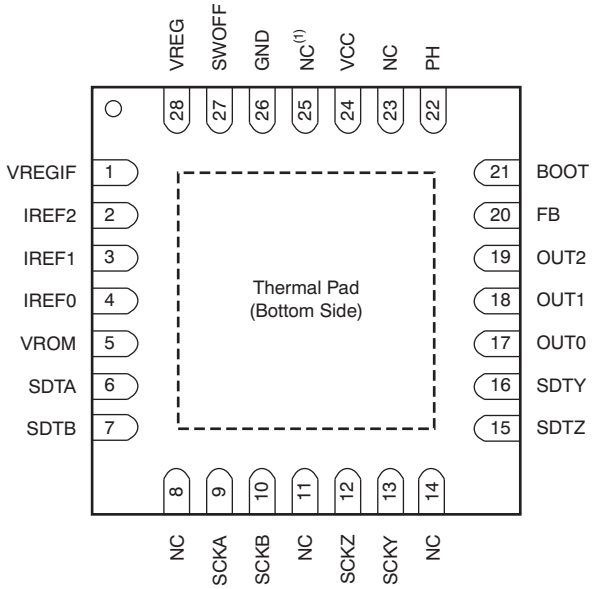
(1) The propagation delays are calculated by $t_{D2} = t_{D0} – t_{D1}$, $t_{D2A} = t_{D0A} – t_{D1A}$.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS

RHP PACKAGE
QFN-28
(TOP VIEW)



(1) NC = not connected

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	PIN NO.		
SDTA	6	I	Noninverting serial data input
SDTB	7	I	Inverting serial data input
SCKA	9	I	Noninverting data shift clock input. All data in the Common Shift Register are shifted to the MSB side by 1 bit and synchronized to the rising edge of the differential clock generated by SCKA and SCKB. The differential data made by SDTA and SDTB are shifted into the Common Shift Register LSB at the same time.
SCKB	10	I	Inverting data shift clock input. All data in the shift register are shifted to the MSB side by 1 bit synchronized to the rising edge of the differential clock generated by SCKA and SCKB. The differential data made by SDTA and SDTB are shifted into the Common Shift Register LSB at the same time.
SDTY	16	O	Noninverting serial data output
SDTZ	15	O	Inverting serial data output
SCKY	13	O	Noninverting serial data shift clock output
SCKZ	12	O	Inverting serial data shift clock output
SWOFF	27	I	Disable buck converter. When SWOFF is connected to VREG, the buck converter is not operated and the OVP/SCP flag is not set even if the device is in an error condition. When SWOFF is low, the buck converter is operated. This terminal is internally pulled down to GND by approximately a 10 kΩ resistor.
VROM	5		EEPROM writing power supply. When this pin level is 19 V, EEPROM can be programmed for dot correction data. This pin must be open in normal operation. This terminal is pulled down to GND by approximately a 10 kΩ resistor internally.
IREF0	4	I/O	The resistors connected from IREF0, IREF1, and IREF2 to GND set the maximum sink current for OUT0, OUT1, and OUT2, respectively.
IREF1	3	I/O	
IREF2	2	I/O	
OUT0	17	O	Constant-current sink output. Multiple outputs can be tied together to increase the constant-current capability.
OUT1	18	O	
OUT2	19	O	
VREG	28	O	Internal regulator output. This pin requires a 0.01 µF decoupling capacitor to ground. This output cannot be used for any other function and no current can be pulled from this output.
VREGIF	1	O	Internal regulator output for the differential interface circuit. This pin requires a 0.1 µF decoupling capacitor. This output cannot be used for any other function and no current can be pulled from this output.
FB	20	I	Feedback voltage input for the converter and power-supply for differential signal interface output and LED driver. Connect this pin to the dc/dc converter output voltage. The FB pin must not be opened, otherwise higher voltage than the absolute maximum voltage is generated.
PH	22	O	Source of the high-side power MOSFET. Connected to an external inductor and diode.
BOOT	21	I/O	Boost capacitor for the high-side power MOSFET gate driver. A capacitor is connected between BOOT and PH.
VCC	24	—	Power-supply voltage
GND	26	—	Power ground
NC	8, 11, 14, 23, 25		No internal connection. These pins are not electrically connected to the IC. They should be soldered to the PCB. Connecting these pins to ground provides improved thermal performance.
Thermal pad	—	—	The RHP package thermal pad is electrically connected to ground inside the package. This pad must be connected to the ground plane on the PCB for best thermal performance and for mechanical reasons. This pad cannot be connected to any other voltage other than ground. See the mechanical drawings at the end of this document for more information.

PARAMETRIC MEASUREMENT INFORMATION

PIN EQUIVALENT INPUT/OUTPUT SCHEMATICS

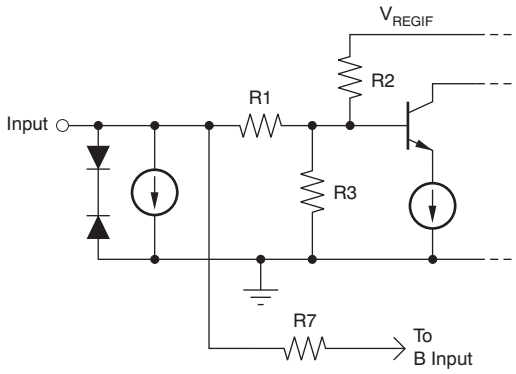


Figure 1. SDTA/SCKA

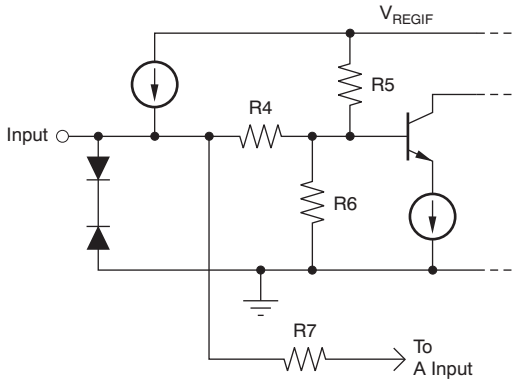


Figure 2. SDTB/SCKB

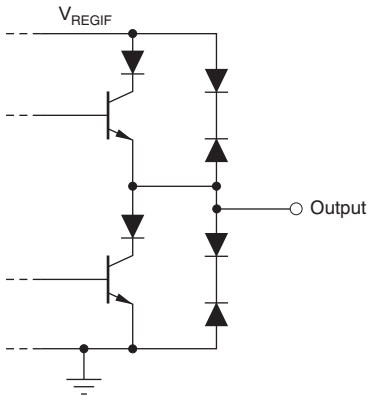


Figure 3. SDTY/SCKY, SDTZ/SCKZ

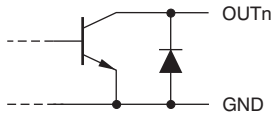


Figure 4. OUT0 Through OUT2

TEST CIRCUITS

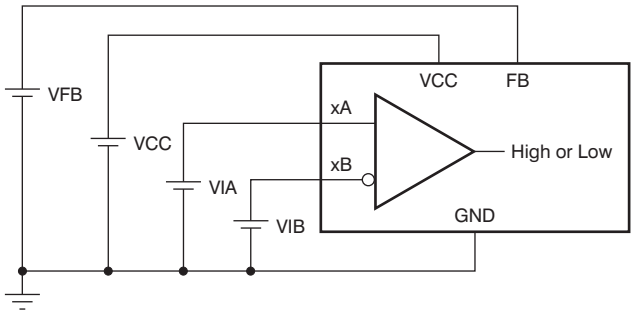


Figure 5. Receiver Test Circuit for SDTA/B and SCKA/B

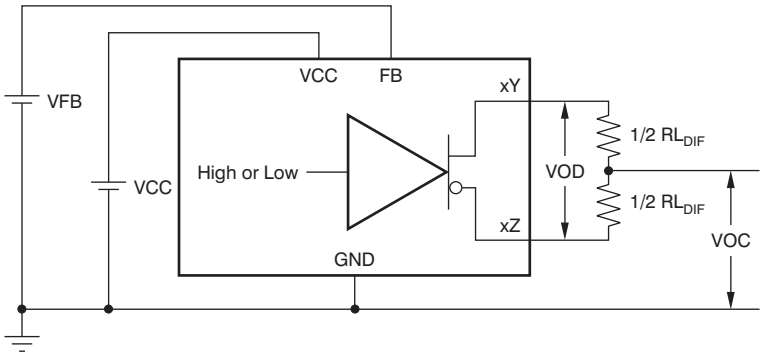
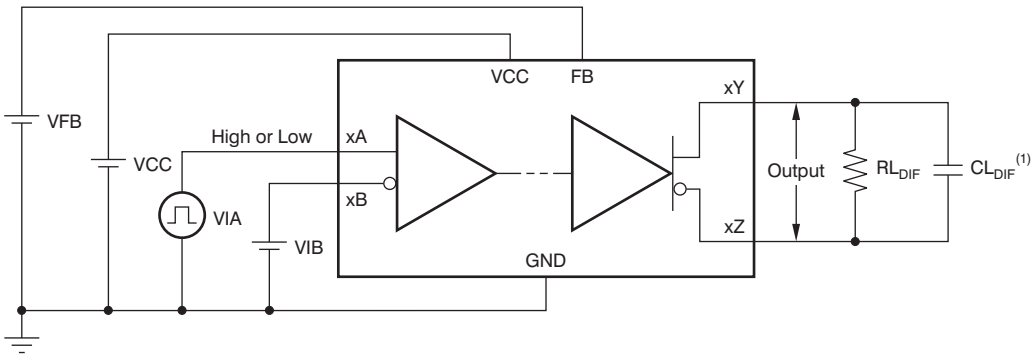


Figure 6. Driver V_{OD} and V_{OC} Test Circuit for SDTY/Z and SCKY/Z



(1) CL_{DIF} includes probe and jig capacitance.

Figure 7. Rise/Fall Time and Propagation Delay Test Circuit for SDTY/Z and SCKY/Z

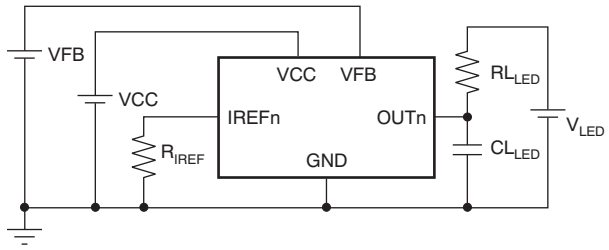


Figure 8. Rise/Fall Time Test Circuit for OUTn

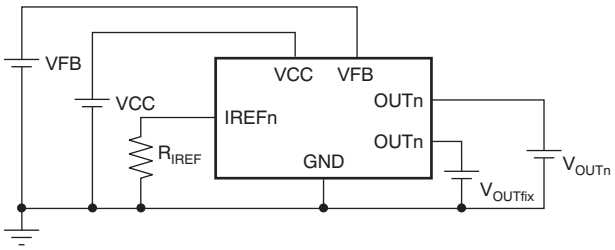


Figure 9. Constant-Current Test Circuit for OUTn

TIMING DIAGRAMS

T_{SU}, T_H, t_{D0}, t_{D0A}, t_{D1}, t_{D1A}, t_W, t_{R0}, t_{F0}

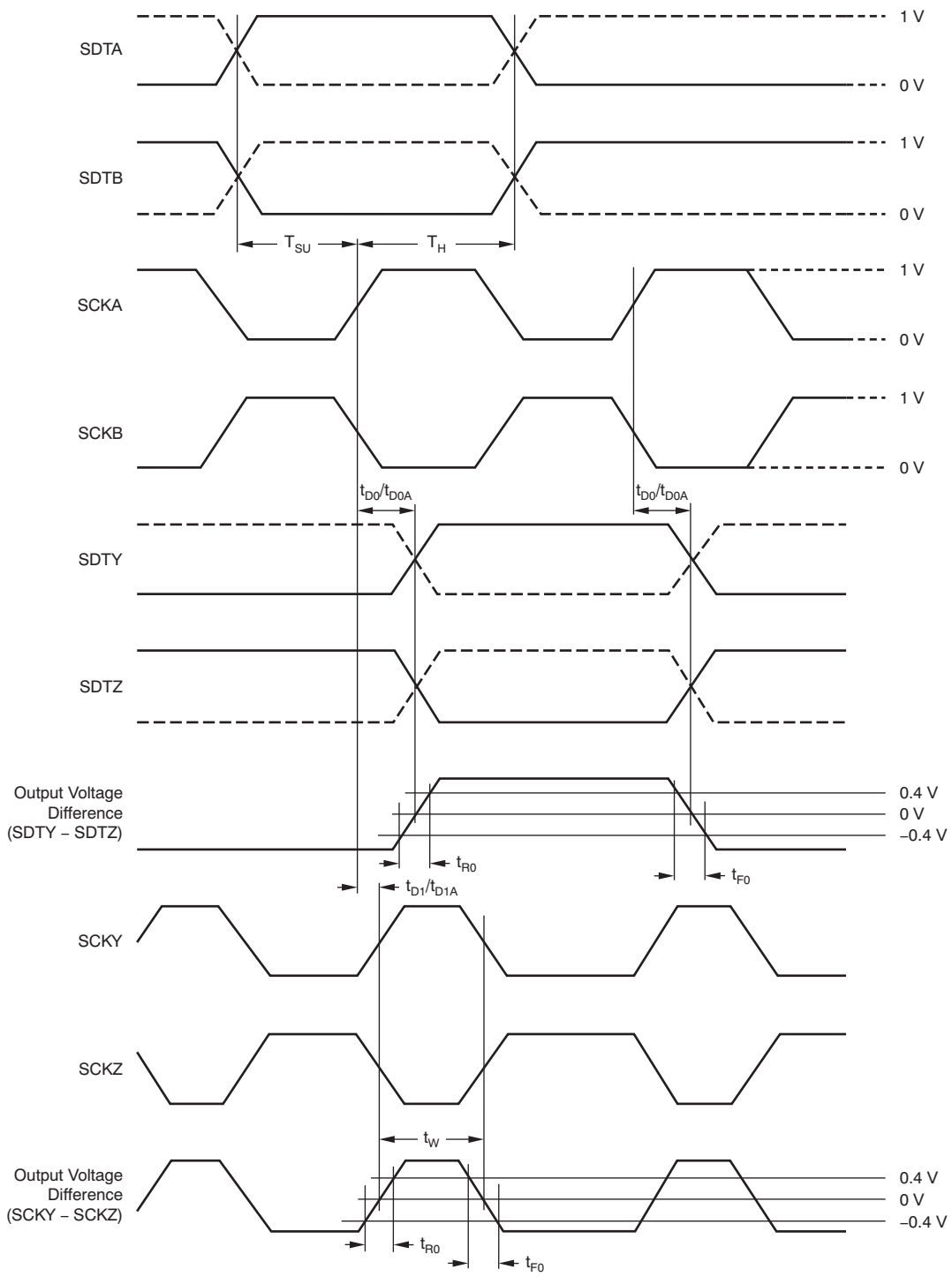
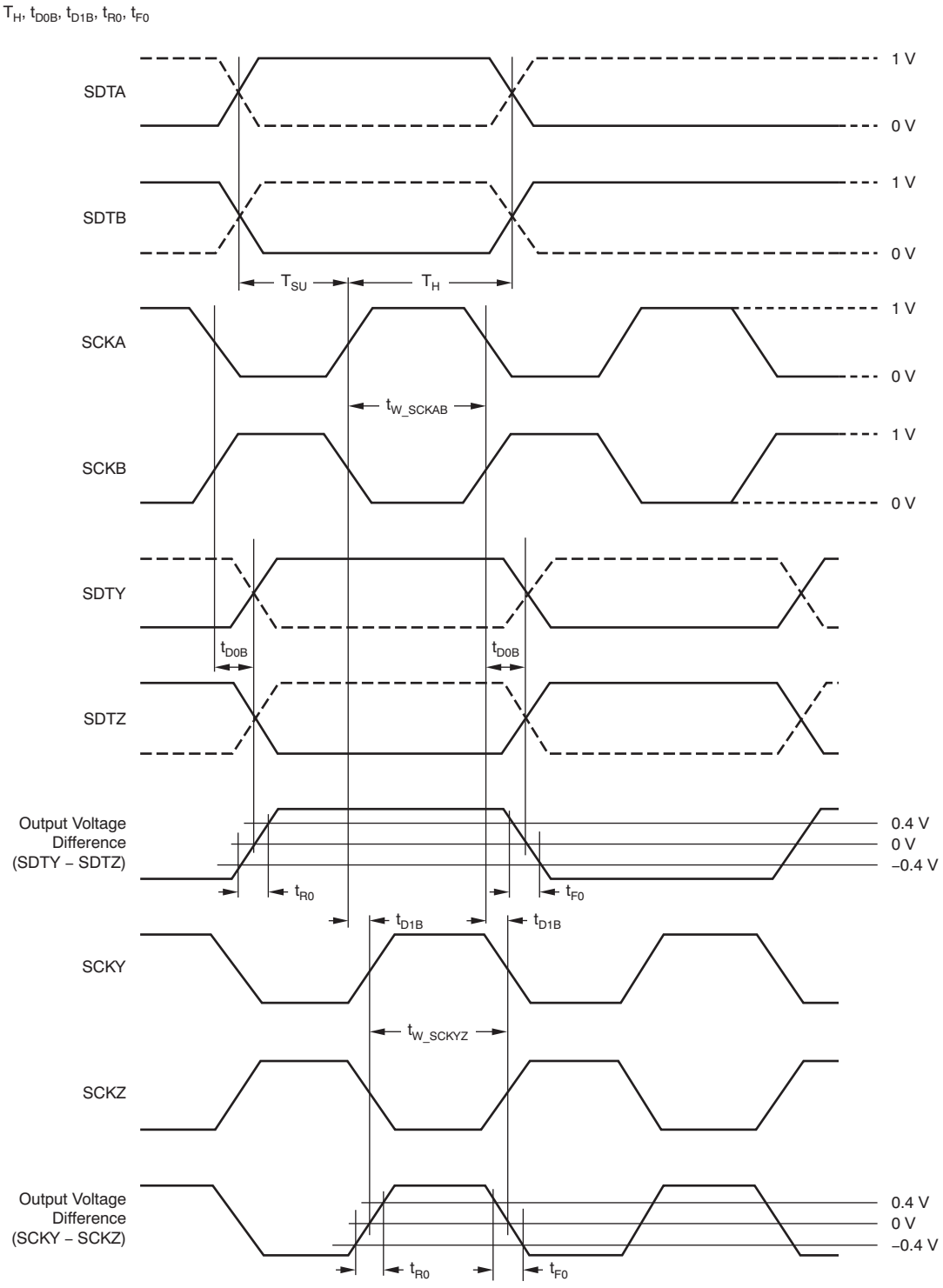


Figure 10. Input/Output Timing 1 (DSI Mode = 1 or 2)



(1) $t_{W\_ERR} = t_{W\_SCKYZ} - t_{W\_SCKAB}$.

Figure 11. Input/Output Timing 2 (DSI Mode = 0)(1)

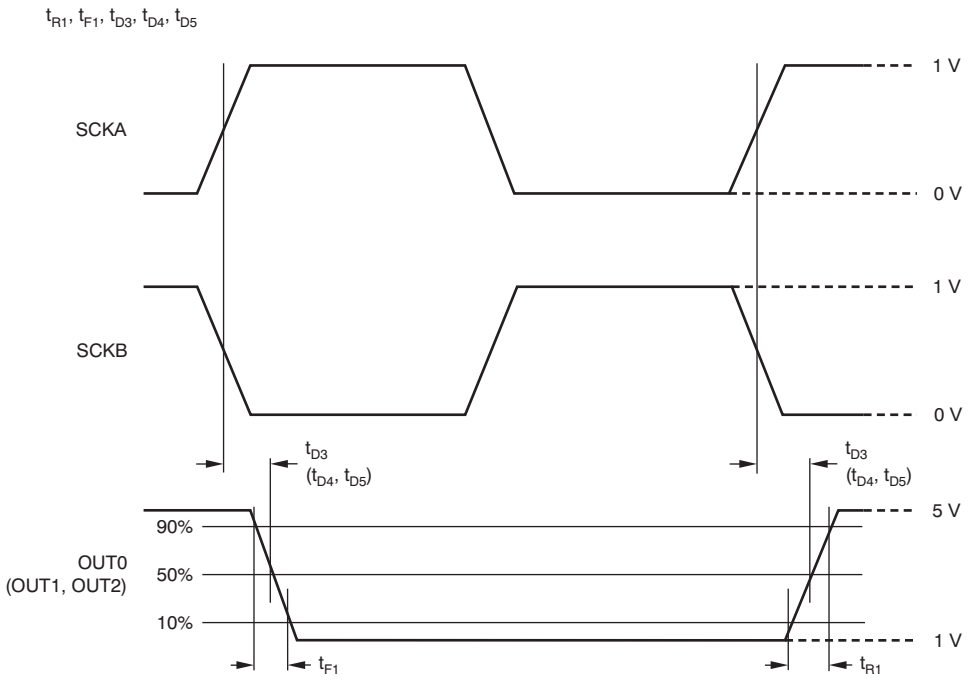


Figure 12. Output Timing

TYPICAL CHARACTERISTICS

At T_A = +25°C and VCC = 24 V, unless otherwise noted.

REFERENCE RESISTOR vs OUTPUT CURRENT

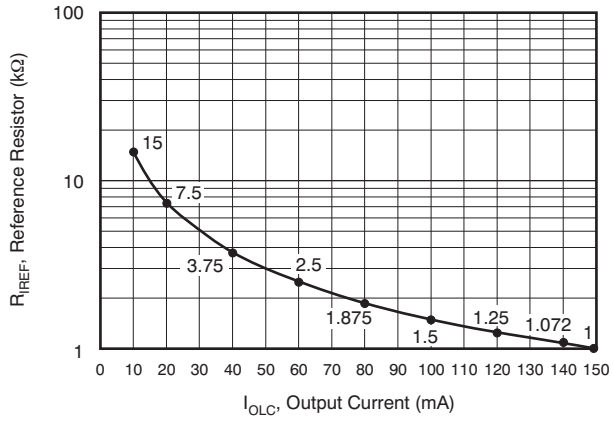


Figure 13.

POWER DISSIPATION vs FREE-AIR TEMPERATURE

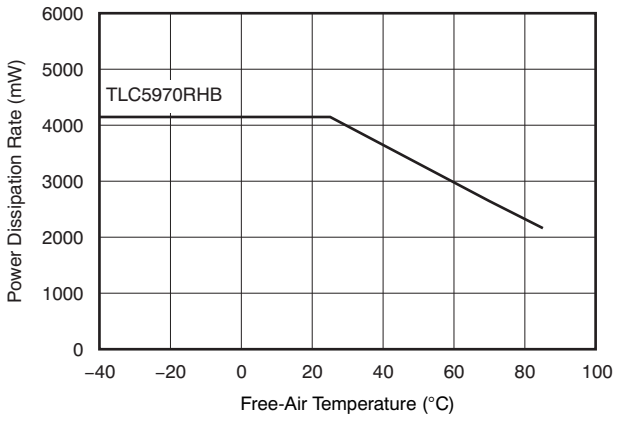


Figure 14.

OUTPUT CURRENT vs OUTPUT VOLTAGE

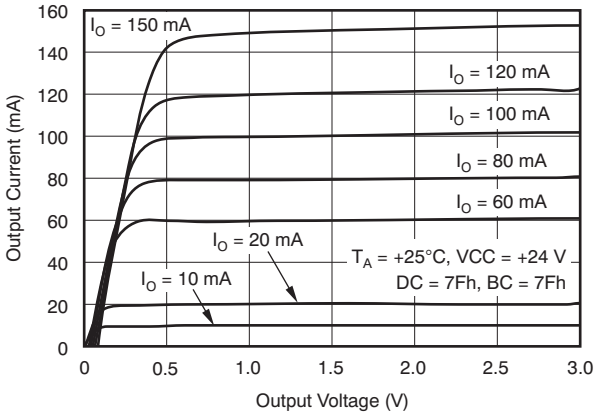


Figure 15.

DOT CORRECTION LINEARITY

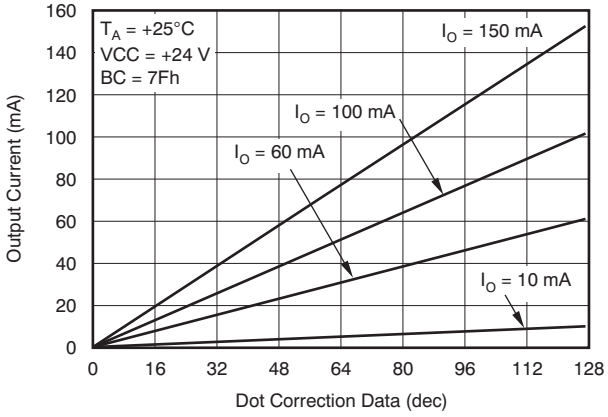


Figure 16.

GLOBAL BRIGHTNESS LINEARITY

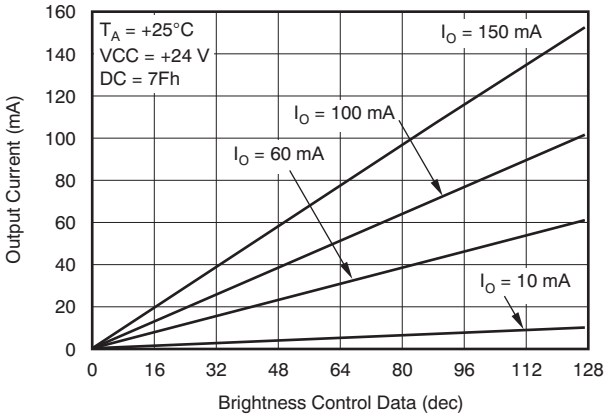


Figure 17.

CONSTANT-CURRENT OUTPUT VOLTAGE WAVEFORM

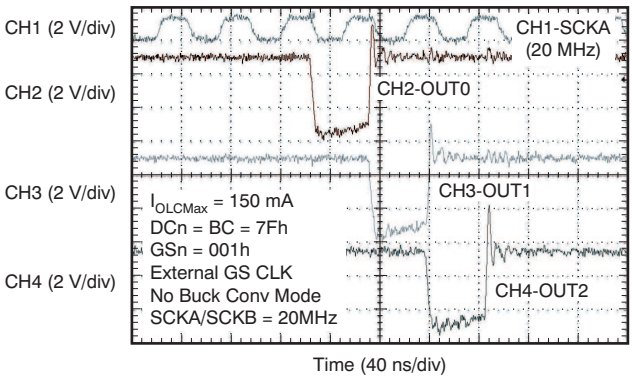


Figure 18.

APPLICATION INFORMATION

MAXIMUM CONSTANT SINK CURRENT VALUE

The TLC5970 maximum constant sink current value for each channel, I_{OLCMax}, is determined by an external resistor, R_{IREF}, placed between IREFn and GND. IREFn determines the maximum current of OUTn, where *n* represents outputs 0, 1, or 2. The R_{IREF} resistor value is calculated with Equation 1:

$$R_{IREF}\ (k\Omega) = \frac{V_{IREF}\ (V)}{I_{OLCMax}\ (mA)} \times 125 \quad (1)$$

Where:

V_{IREF} = the internal reference voltage on the IREF pin (1.20 V, typically).

I_{OLCMax} is the largest current for each output. Each output sinks the I_{OLCMax} current when it is turned on, the dot correction is set to the maximum value of 7Fh (127d), and global brightness control data are 7Fh (127d). Each output sink current can be reduced by lowering the output dot correction and brightness control values.

R_{IREF} must be between 1 kΩ (typical) and 15 kΩ (typical) to keep I_{OLCMax} between 10 mA and 150 mA. The output may be unstable when I_{OLCMax} is set lower than 10 mA. Output currents lower than 10 mA can be achieved by setting I_{OLCMax} to 10 mA or higher and then using dot correction and global brightness control. The constant sink current versus external resistor, R_{IREF}, characteristics are shown in Figure 13 and Table 1.

Table 1. Maximum Constant Current versus External Resistor Value

I_{OLCMax} (mA)	R_{IREF} (kΩ, Typical)
150	1.00
140	1.07
120	1.25
100	1.50
80	1.88
60	2.50
40	3.75
20	7.50
10	15.0

DOT CORRECTION (DC) AND GLOBAL BRIGHTNESS CONTROL (BC) FUNCTION (CURRENT CONTROL)

The TLC5970 has the capability to adjust the output current of each channel (OUT0 to OUT2) individually. This function is called *dot correction* (DC). The DC data are seven bits long, which allows each channel output current to be adjusted in 128 steps from 0% to 100% of the maximum output current, I_{OLCMax}. The DC data are entered into the TLC5970 via the serial interface and can be stored into the internal EEPROM. When the IC is powered on, DC data are automatically loaded into the DC data latch from the EEPROM.

The TLC5970 also has the capability to adjust all output currents at the same time. This function is called *global brightness control* (BC). The BC data are seven bits long, which allows all three output channel currents to be adjusted in 128 steps from 0% to 100% of the maximum output current, I_{OLCMax}. The BC data are entered into the TLC5970 via the serial interface. The brightness control data cannot be stored into EEPROM. When IC is powered on, BC data are automatically set to 7Fh (127d).

Equation 2 determines each output (OUTn) sink current:

$$I_{OUTn}\ (mA) = I_{OLCMax}\ (mA) \times \left[\frac{DCn}{127d}\right] \times \left[\frac{BC}{127d}\right]$$

Where:

I_{OLCMax} = the maximum channel current for each channel determined by R_{IREFn}

DCn = the decimal dot correction value for each OUTn in the DC latch (DCn = 0d to 127d)

BC = the decimal brightness control value in the brightness control latch (BC = 0d to 127d) (2)

DC, BC, and function current control data are shown in Table 2, Table 3, and Table 4, respectively.

Table 2. DC Data versus Current Ratio and Set Current Value

DC DATA (Binary)	DC DATA (Decimal)	DC DATA (Hex)	BC DATA (Hex)	SET CURRENT RATIO TO MAXIMUM CURRENT (%)	150 mA I_{OLCMax} (mA, Typical)	10 mA I_{OLCMax} (mA, Typical)
000 0000	0	00	7F	0	0	0
000 0001	1	01	7F	0.8	1.18	0.08
000 0010	2	02	7F	1.6	2.36	0.16
—	—	—	—	—	—	—
111 1101	125	7D	7F	98.4	147.64	9.84
111 1110	126	7E	7F	99.2	148.82	9.92
111 1111	127	7F	7F	100.0	150.00	10.00

Table 3. BC Data versus Current Ratio and Set Current Value

BC DATA (Binary)	BC DATA (Decimal)	BC DATA (Hex)	DC DATA (Hex)	SET CURRENT RATIO TO MAXIMUM CURRENT (%)	150 mA I_{OLCMax} (mA, Typical)	10 mA I_{OLCMax} (mA, Typical)
000 0000	0	00	7F	0	0	0
000 0001	1	01	7F	0.8	1.18	0.08
000 0010	2	02	7F	1.6	2.36	0.16
—	—	—	—	—	—	—
111 1101	125	7D	7F	98.4	147.64	9.84
111 1110	126	7E	7F	99.2	148.82	9.92
111 1111	127	7F	7F	100.0	150.00	10.00

Table 4. DC and BC Data versus Current Ratio and Set Current Value

BC DATA (Hex)	DC DATA (Hex)	SET CURRENT RATIO TO MAXIMUM CURRENT (%)	150 mA I_{OLCMax} (mA, Typical)	10 mA I_{OLCMax} (mA, Typical)
00	00	0	0	0
01	01	0	0.01	0
02	02	0.01	0.04	0
—	—	—	—	—
7D	7D	96.88	145.31	9.69
7E	7E	98.43	147.65	9.84
7F	7F	100.0	150.00	10.00

GRAYSCALE (GS) FUNCTION (PWM CONTROL)

The OUTn PWM control is controlled by a 12-bit grayscale counter that is clocked on each rising edge of either the internal oscillator or the shift clock signal generated by the differential signal, SCKA and SCKB. When bit 9 in the Function Control Data Latch is '0', the internal oscillator drives the PWM grayscale counter. When bit 9 is '1', SCKA and SCKB drive the grayscale counter. The OUTn that are programmed with a non-zero grayscale value (GSn) turn on at the first rising edge of the selected clock after the internal latch pulse generation. After the internal latch latch pulse goes high, the 12-bit grayscale counter counts the clock rising edges. Each OUTn stays on until the grayscale counter value is larger than the output GSn value. OUTn turns off on the rising edge of the clock.

When the IC powers up, all data in the Grayscale Data Latch are set to '0'. Therefore, GSn data must be written into the Grayscale Data Latch to turn on OUTn. Equation 3 determines each OUTn on-time (t_{OUT_ON}):

$$t_{OUT\_ON}\ (ns) = t_{GSCLK}\ (ns) \times GSn$$

Where:

t_{GSCLK} = Twice the period of the internal oscillator frequency if the internal clock is selected. One period of the shift clock frequency is generated by the differential signal if the external clock is selected.

GSn = the programmed grayscale value for OUTn (GSn = 0d to 4095d) (3)

AUTO DISPLAY REPEAT

Auto display repeat, DSPRPT, allows OUTn to continuously turn on for multiple PWM cycles without the need to continuously reprogram the PWM grayscale registers. When Auto Repeat is enabled, bit 8 in the Function Control Data Latch is '1' and OUTn automatically turns on again at the next rising clock of the internal oscillator. When Auto Display Repeat is disabled by setting the control bit to '0', OUTn do not turn on again until an internal latch pulse is generated and another GS clock pulse goes high. This timing is shown in Figure 19 and Figure 20.

Table 5. GS Data versus OUTn On-Duty and OUTn On-Time

GS DATA (Binary)	GS DATA (Decimal)	GS DATA (Hex)	OUTn ON-DUTY RATIO AGAINST MAXIMUM CODE (%)	OUTn ON-TIME WHEN 5 MHz INTERNAL OSCILLATOR IS SELECTED FOR GS CLOCK (µs, Typical)
0000 0000 0000	0	000	0	0
0000 0000 0001	1	001	0.02	0.20
0000 0000 0010	2	002	0.05	0.40
—	—	—	—	—
0111 1111 1111	2047	7FF	49.99	409.4
1000 0000 0000	2048	800	50.01	409.6
1000 0000 0001	2049	801	50.04	409.8
—	—	—	—	—
1111 1111 1101	4093	FFD	99.95	818.6
1111 1111 1110	4094	FFE	99.98	818.8
1111 1111 1111	4095	FFF	100.00	819.0

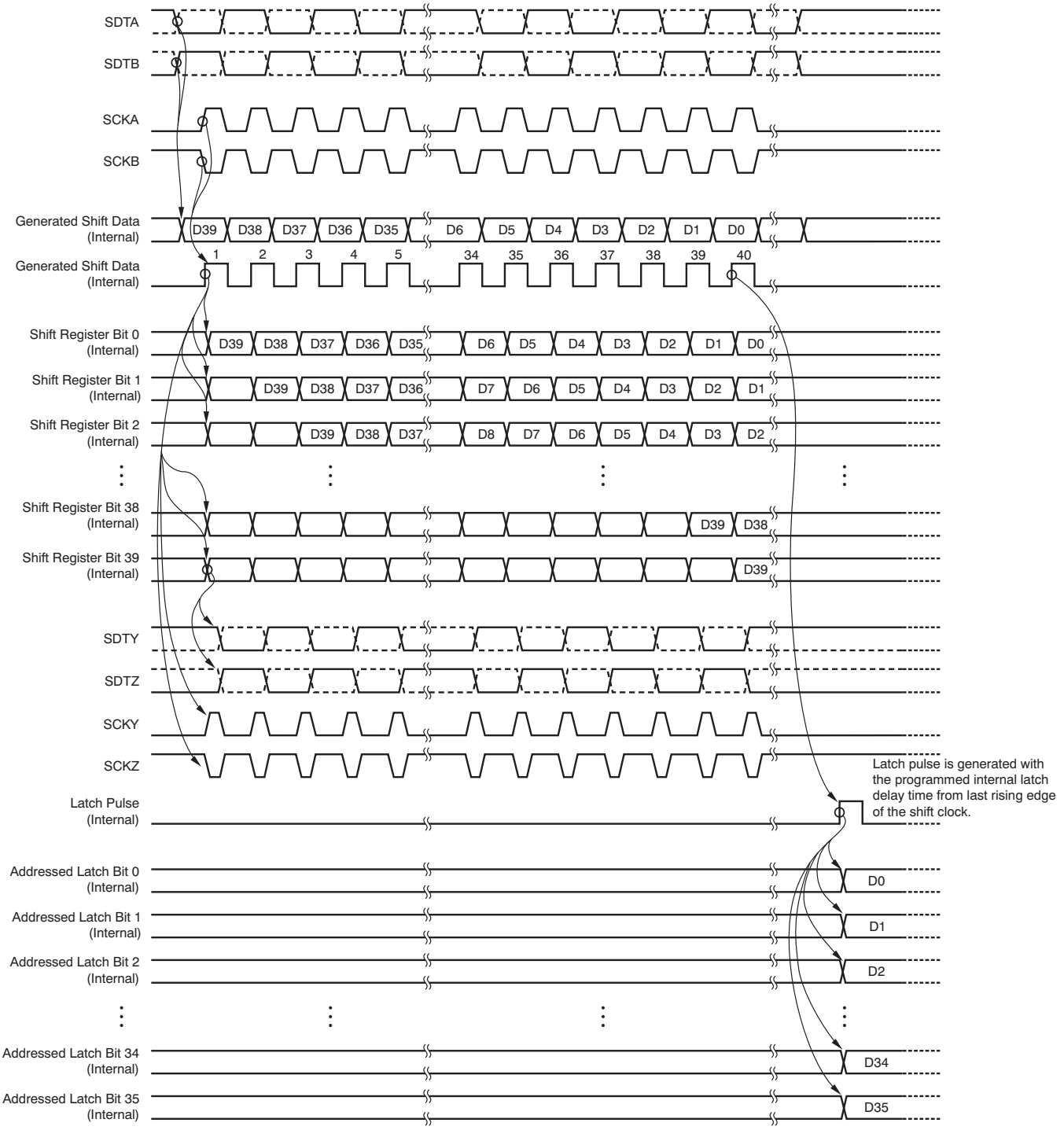


Figure 19. Serial Data Input/Output Timing Diagram 1

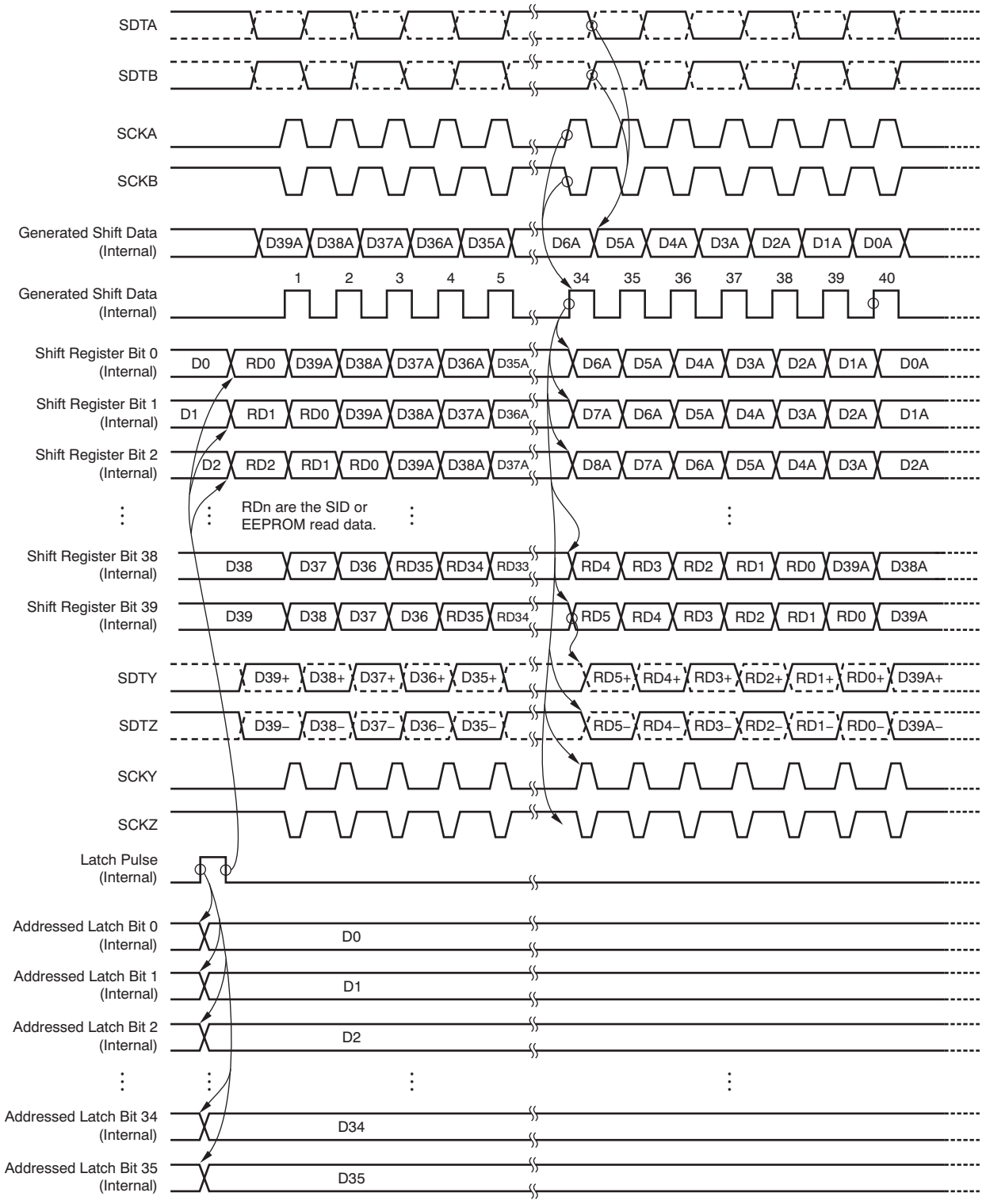


Figure 20. Serial Data Input/Output Timing Diagram 2 (SID/EEPROM Data Read)

DIFFERENTIAL SIGNAL INTERFACE

This device has a differential signal receiver and differential signal driver. These differential components provide very reliable, high-quality signal integrity over long distances. This integrity allows very large distances between the display pixels without the need for additional drive circuitry. The drivers are enabled one second after the IC powers up. A 10-kΩ resistor is internally mounted between SDTA and SDTB/SCKA and SCKB. Table 6 shows a truth table of the differential signal interface receiver and driver.

Table 6. Differential Signal Interface Truth Table

RECEIVER (SDTA-SDTB, SCKA-SCKB)		DRIVER (SDTY-SDTZ, SCKY-SCKZ)		
DIFFERENTIAL INPUTS (VID = SDTA/SCKA – SDTB/SCKB)	INTERNAL INPUT DATA	DRIVER INPUT	DIFFERENTIAL OUTPUTS	
			SDTY/SCKY	SDTZ/SCKZ
VID ≥ 0.2 V	High	Low	Low	High
–0.2 V < VID < 0.2 V	Undefined			
VID ≤ –0.2 V	Low	High	High	Low
Open input	Low			

BUCK DC/DC CONVERTER

The buck converter operates with the Pulse Frequency Mode (PFM).The buck converter controls the LED anode voltage to keep the LED cathode voltage to approximately 1 V for high efficiency and reduces the system power-supply current. The LED anode voltage is controlled by the buck converter in this manner:

1. After the IC powers on, the LED anode voltage charges up to the FB voltage set by EEPROM with a soft-start squence. The maximum time of the soft-start sequence is 800 ms.
2. The LED then turns on and comparators check the OUTn voltage when all LED are turned on at the 32nd GSCLK. If the lowest voltage in OUT0 to OUT2 is below 0.9 V when all OUTn are on at 32nd GSCLK, the buck converter target voltage is changed by one step to a higher voltage at the rising edge of the 33rd GSCLK. If the lowest voltage in OUT0 to OUT2 is above 1.1 V, the buck converter target voltage changes by one step to a lower voltage. If the lowest voltage in OUT0 to OUT2 is between 0.9 V and 1.1 V, then the buck converter target voltage remains at the previous voltage.
3. If the highest voltage in OUT0 to OUT2 exceeds 4.0 V at the 32nd GSCLK rising edge when all OUTn are on, then the buck converter target voltage does not change to a higher voltage side.

Parameter Selection for Buck Converter

The following steps select the parameters for the buck converter.

1. PH on-time selection:

$$\text{Calculated PH On-Duty Ratio1 (\%)} = \frac{\text{VFB Minimum Voltage}}{\text{VCC Maximum Input Voltage}} \times 100$$

Where:

VFB = the number of LEDs in series × LED minimum forward voltage (V_F) + 1.0 V (4)

Select the closest and smaller number in Table12, then calculate PH on-duty ratio1 (%).

Example: VCC = 24 V (typical) and 25 V (maximum). LED forward voltage (V_F) = 3.2 V (minimum) and 3.5 V (typical). Two LEDs are connected in series.

Thus, VFB = 2 × 3.2 + 1 = 7.4 V. The PH on-duty ratio1 (%) = 7.4/25 = 29.6%. Therefore, 29% code ('1h') should be selected for PH on-duty.

So, the selected PH on-duty in the EEPROM write data latch is 29%.

2. Inductor value and current selection:

$$\text{PH On-Duty Ratio2 (\%)} = \frac{\text{VFB Maximum Voltage}}{\text{VCC Minimum Input Voltage}} \times 100 \quad (5)$$

Example: VCC = 23 V (minimum), 24 V (typical), and 25 V (maximum). LED forward voltage (V_F) = 3.2 V (minimum), 3.5 V (typical), and 3.8 V (maximum). Two LEDs are connected in series.

Thus, VFB = 2 × 3.8 + 1 = 8.6 V. The PH on-duty ratio 2 (%) = 8.6/23 = 37.4% in this case.

Calculate inductor peak current (mA):

$$\text{Inductor Peak Current (mA)} = \frac{\frac{I_{OUT} + \text{IFBn}}{\left(\frac{\text{Selected PH On-Duty}}{\text{PH On-Duty Ratio2}}\right)} \times 2}{\frac{\eta}{100}} \quad (6)$$

Where:

I_{OUT} (mA) = Total current of LEDs connected to OUT0/1/2.

IFBn (mA) = Maximum input current of IFB pin.

η (%) = Efficiency of TLC5970 buck converter (recommended to use 90).

Example: In case all LED currents are set to 60 mA by the 2.50-kΩ external resistor and total current is 180 mA. IFB3 in this data sheet is used when the differential interface output drives the next TLC5970 without a resistor between SDTA/SDTB and SCKA/SCKB. Therefore:

$$I_{LPK}\text{ (mA)} = \frac{\frac{\frac{180 + 115}{29}}{37.4} \times 2}{\frac{90}{100}} = 845.5\text{ mA} \quad (7)$$

A 25% margin for inductor variation is required. Thus, I_{LPK} = 845.5 × 1.25 = 1057 mA. The maximum inductor current should be larger than 1057 mA. However, the TLC5970 PH peak current must be less than 2 A in any case.

3. Calculate inductor value (μH) for minimum inductor value:

$$\text{Inductor Value (}\mu\text{H)} = \text{VCC Voltage (V, Minimum)} \times \frac{1}{\text{Maximum PH Switching Frequency (MHz, Maximum)}} \times \frac{\text{Selected PH On-Duty (\%)}}{I_{LPH}\text{ (mA)} \times 1000} \quad (8)$$

(9)

Example: VCC = 23 V (minimum), 24 V (typical), and 25 V (maximum). Maximum PH switching frequency is 1.5 MHz. The selected PH on-duty ratio as calculated by Equation 4 is 29%. I_{LPK} (mA) is 1057 mA as calculated by Equation 6.

$$\begin{aligned}\text{Therefore, the inductor value (}\mu\text{H)} &= 23 \times \frac{1}{1.5} \times \frac{0.29}{1057 \times 1000} \\ &= 23 \times 0.67 \times \frac{0.29}{1057 \times 1000} \\ &= 4.2\ \mu\text{H}\end{aligned} \quad (10)$$

4. Calculate inductor peak current that should be selected:

   The TLC5970 PH peak current must be less than 2 A and I_{LPK} must not be greater than 2 A in any case.

$$\text{Inductor Peak Current (A)} = \text{VCC (V, Maximum)} \times \frac{1}{\text{Maximum PH Switching Frequency (MHz, Maximum)}} \times \frac{\text{Selected PH On-Duty}}{\text{Inductor Value } (\mu\text{H})} < 2 \text{ A} \tag{11}$$

   Example: In this case, 25 × 0.67 × 0.29/4.2 = 1.15 A. So the inductor value is correct.

   As the result of the above calculation, the inductor value should be selected over 4.2 µH and the inductor peak current should be over 1.15 A.

Figure 21 shows a block diagram of the buck dc/dc converter; Figure 22 details the buck dc/dc converter operation. Figure 23 and Figure 24 illustrate the timings of the external and internal GS clock mode for PWM operation, respectively.

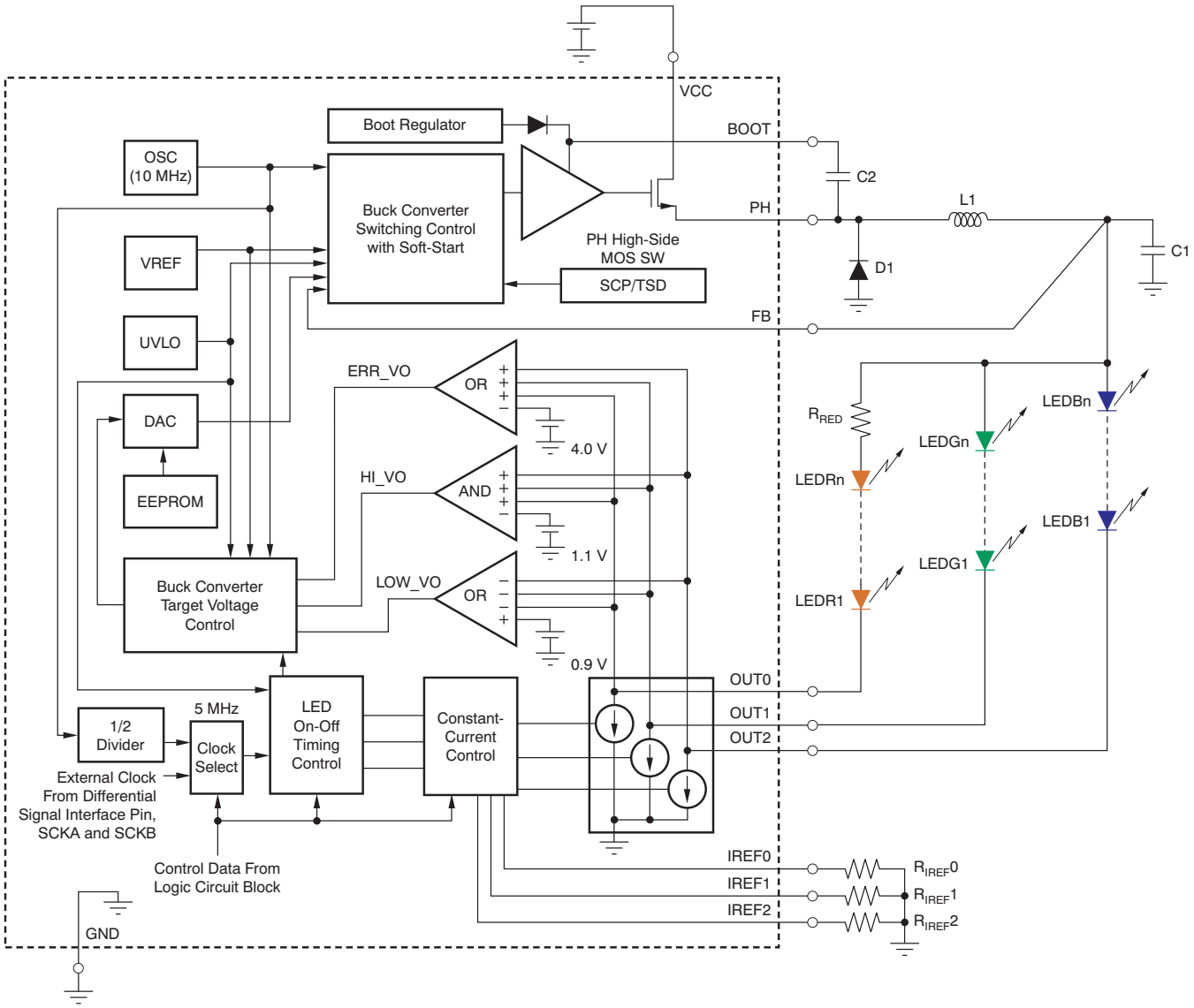


Figure 21. Buck DC/DC Converter Operation

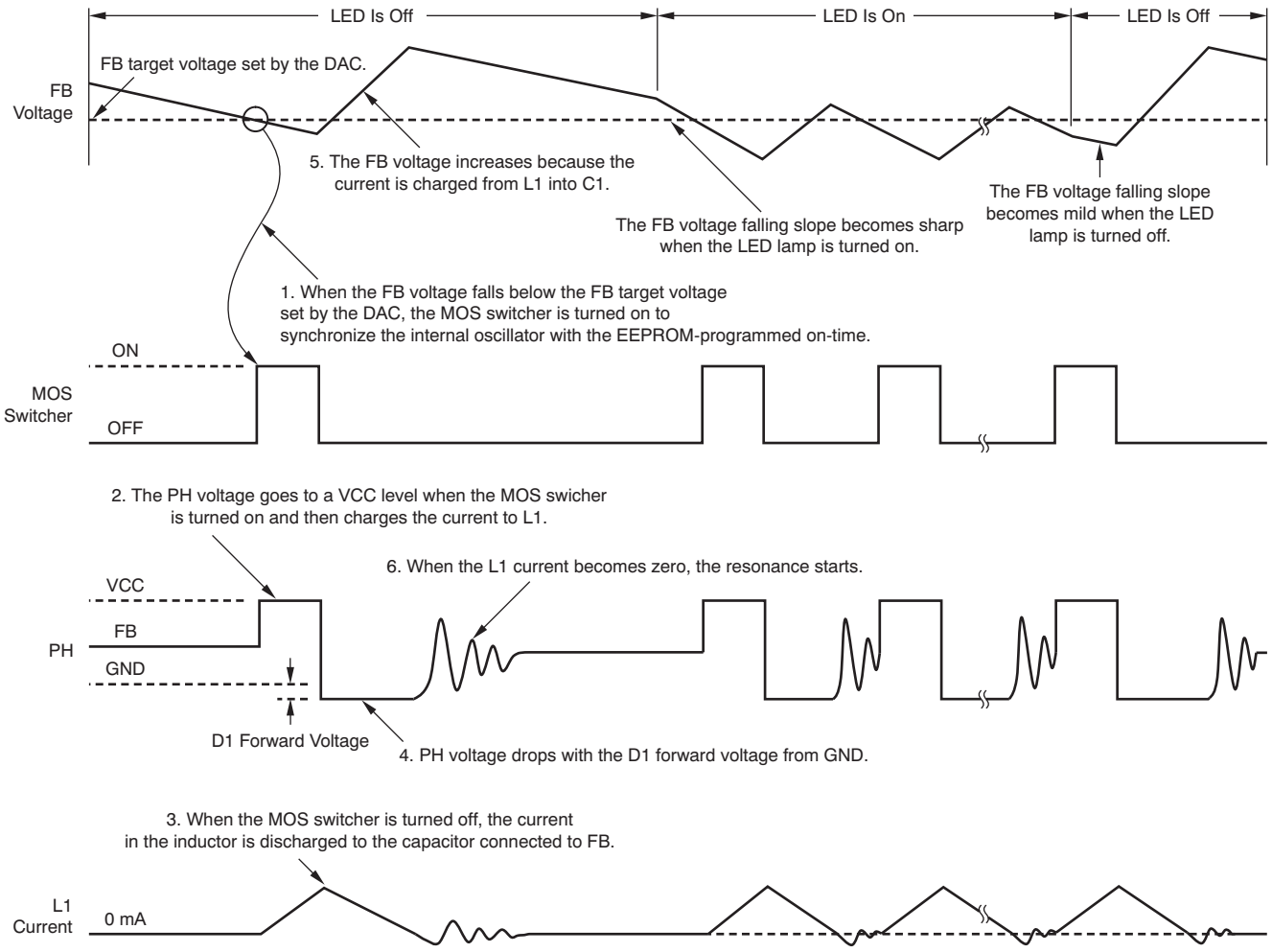


Figure 22. Buck DC/DC Converter Block Diagram

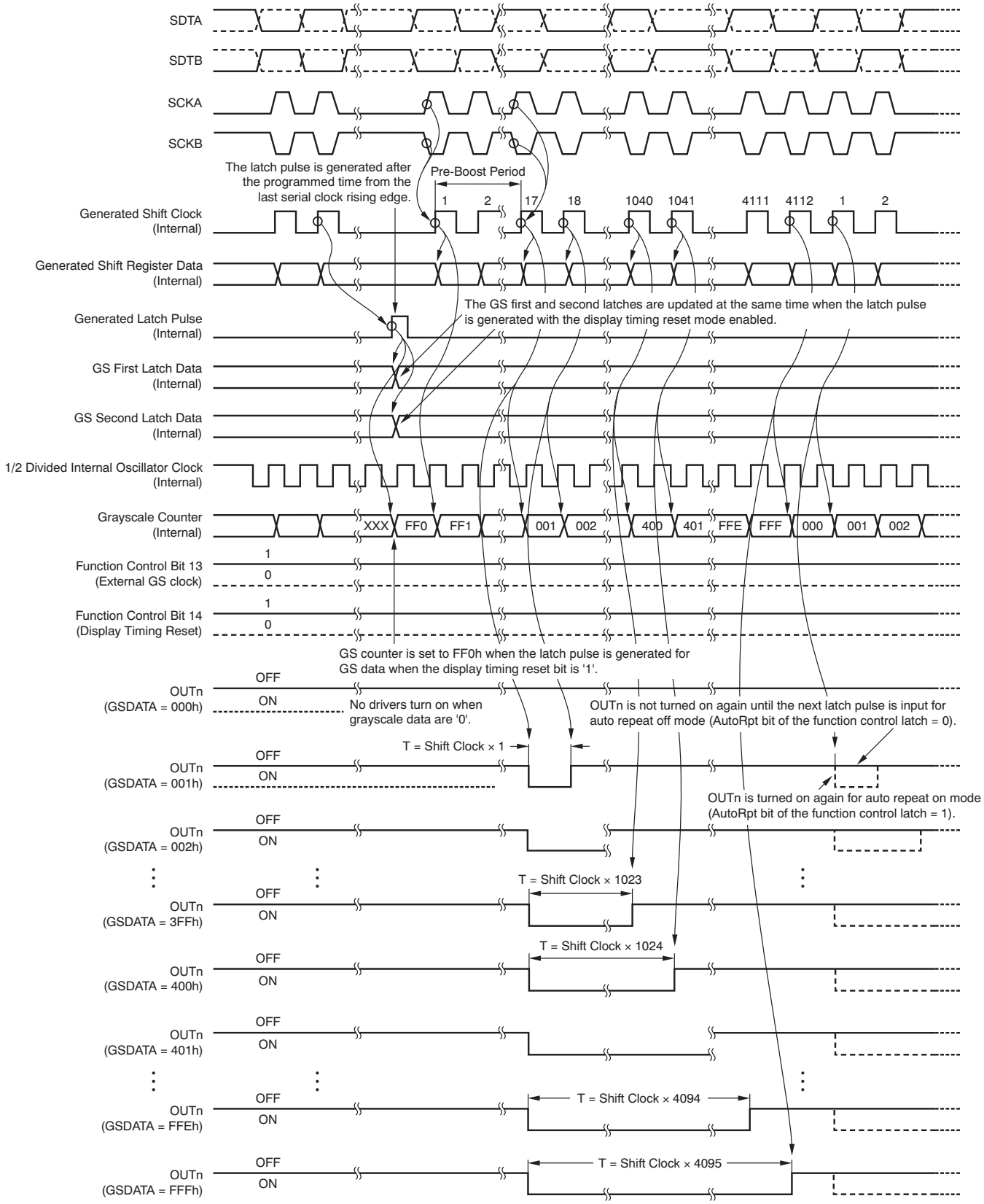


Figure 23. PWM Operation (External GS Clock Mode)

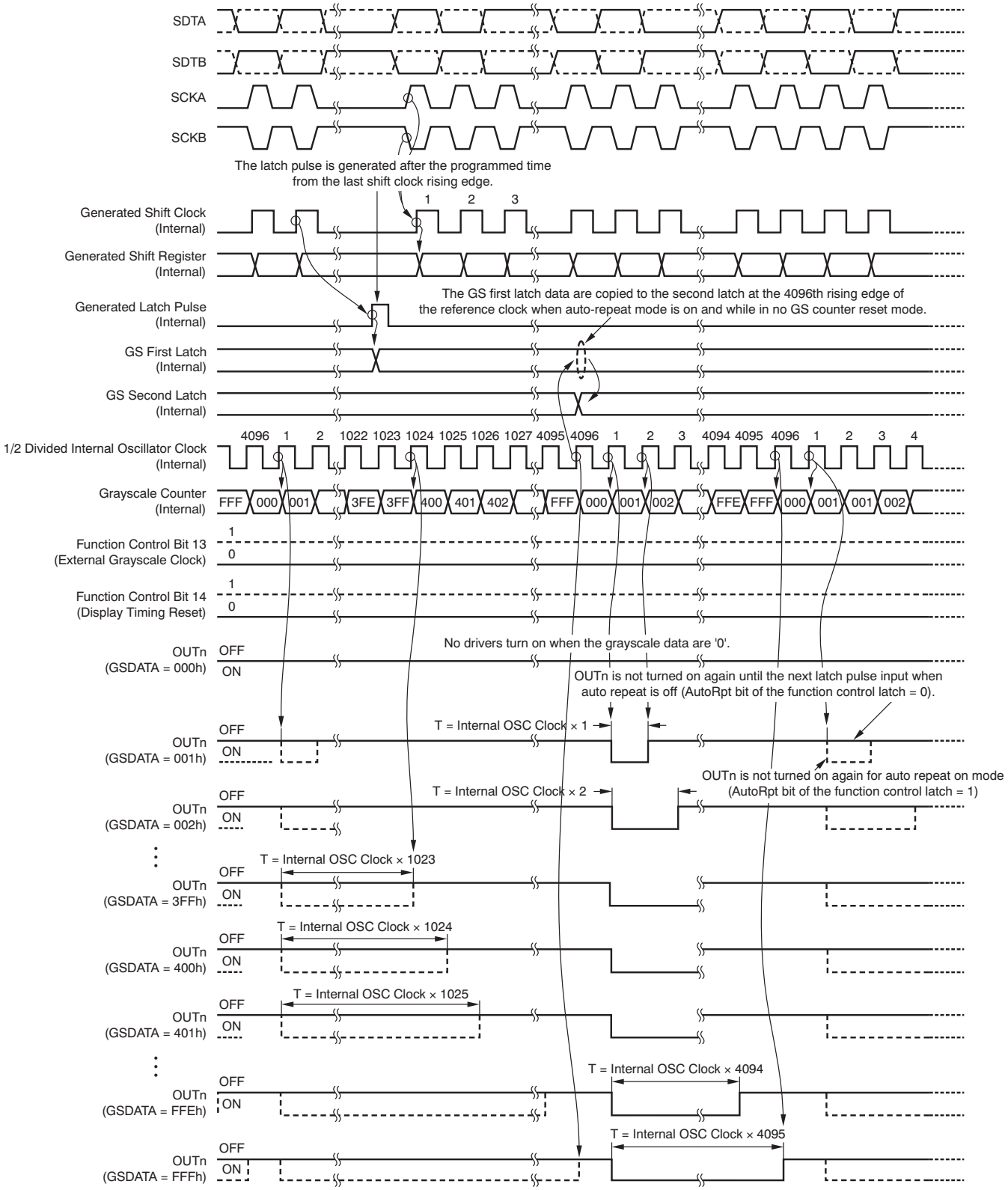


Figure 24. PWM Operation (Internal GS Clock Mode)

REGISTER AND DATA LATCH CONFIGURATION

The TLC5970 has five writable data latches, two readable registers, and one error release address. All data written into or read from these registers and data latches go through the differential signal interfaces and the 40-bit Common Shift Register. The first four most significant bits (MSBs) in the 40-bit Common Shift Register are used to define which internal latch the data are transferred into. Data in the 40-bit Common Shift Register are automatically transferred into an internal latch or data from the internal latch are automatically transferred into the 40-bit Common Shift Register when the TLC5970 generates the internal latch signal. Figure 25 shows the shift register and data latch configurations. Table 7 lists the assignment of latch addresses.

Table 7. Register/Data Latch Address Assignment

ADDRESS (4-Bit)			READ/WRITE	SELCTED DATA LATCH/FUNCTION
BINARY	DECIMAL	HEX		
0000	0	0	W	Grayscale (GS) data latch. These data control LED brightness by PWM.
0001-1000	1-8	1-8	—	No assigned latch. Data are not transferred when these addresses are selected.
1001	9	9	W	Restart operation. If the TLC5970 is disabled because of overvoltage protection (OVP) or short-circuit protection (SCP), writing any value to the Restart Operation latch enables the TLC5970. Writing to this latch has no effect if the TLC5970 is operating normally. The system should diagnose and correct any problems that have caused OVP or SCP before writing to this latch to restart the IC.
1010	10	A	R	Status Information Data (SID) Register. Writing any value to this register causes the SID data to be loaded into the 40-bit Common Shift Register.
1011	11	B	R	EEPROM Data Read Register. Writing any value to this register causes the EEPROM data to be loaded into the 40-bit Common Shift Register.
1100	12	C	W	EEPROM1 Write Data Latch (write command = A5h). The data in this latch program the PH on-duty, VFB target voltage, differential interface timing mode. and Internal latch pulse delay time. In order to properly program the EEPROM with this data, bits 35-28 must contain A5h (1010101b).
1101	13	D	W	EEPROM Write Data Latch 2 (write commend = 5Ah). The data in this latch program the default Dot Correction. In order to properly program the EEPROM with this data, bits 35-28 must contain 5Ah (0101010b).
1110	14	E	W	Dot Correction (DC) Data Latch. The data in this latch contain OUTn DC data. When the IC is powered up, the data stored in EEPROM2 are automatically written to this latch.
1111	15	F	W	Function Control (FC) and Brightness Control (BC) Data Latch. These data control several IC functions. This latch also contains the Brightness Control data.

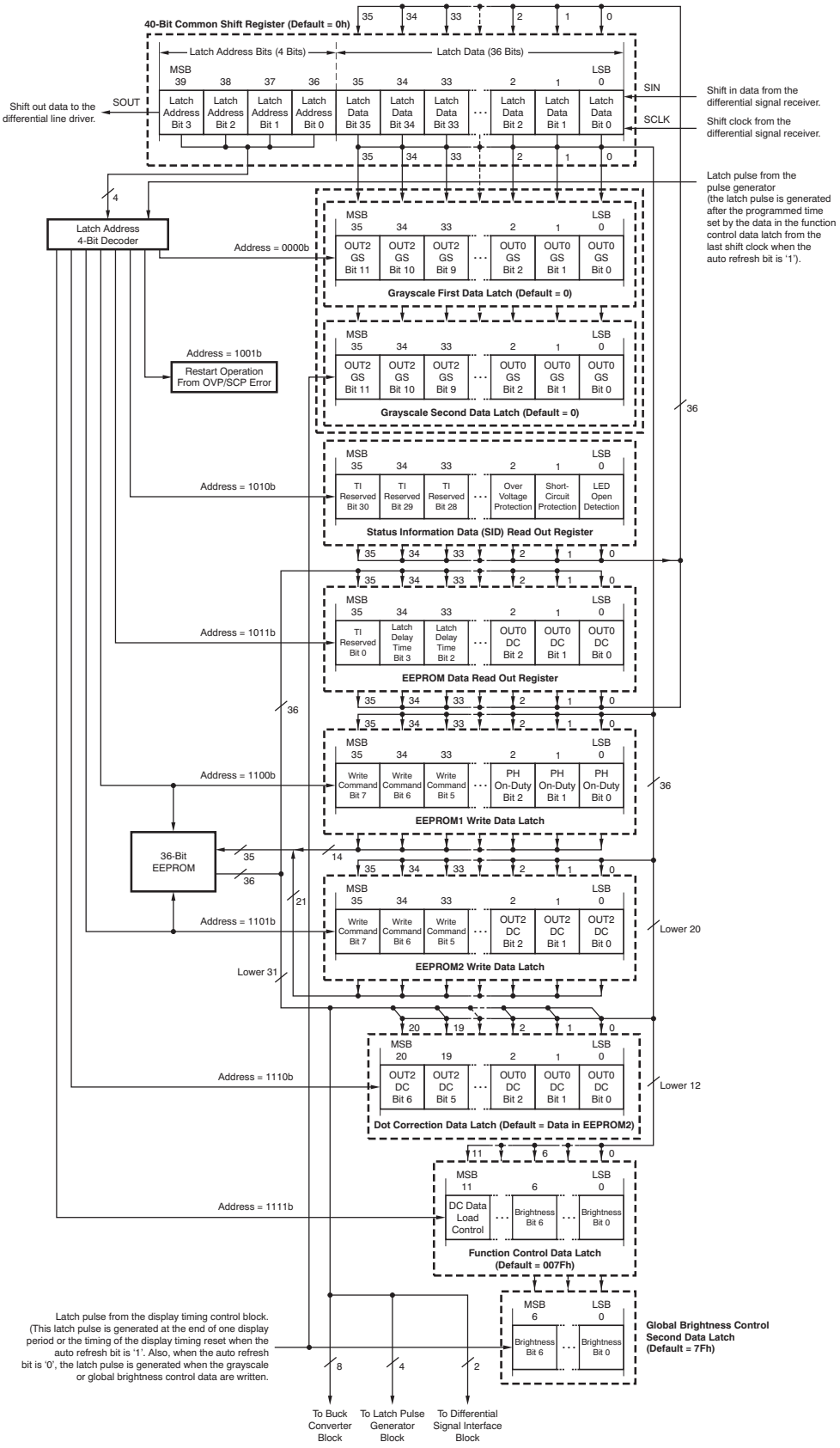


Figure 25. Register and Data Latch Configuration

Grayscale (GS) First/Second Data Latch (Register Address = 0000b)

The GS Latch is 36 bits long. The second GS Latch controls the pulse width modulation (PWM) for each OUTn. The first GS Latch holds the data written through the differential signal interface. If the Auto Data Refresh bit in the Function Control Latch is '1', the data in the first latch are copied to the second latch at the rising edge of the 4096th grayscale clock. If the Auto Data Refresh bit is '0', both the first and second GS Latches are updated at the same time from the data written into the differential signal interface. When the IC is powered on, both latches are reset to all '0'. At startup, GS data should not be programmed until after the Function Control Data Latch is programmed because the PWM control automatically starts when data are written into the second GS Latch.

Table 8 and Figure 26 show the GS Data Latch bit assignments. Table 5 shows an example of OUTn duty cycle ratios for different GS data.

Table 8. Grayscale Data Latch Bit Assignment

BIT NUMBER	BIT NAME	DESCRIPTION
11-0	GSOUT0	Grayscale data for OUT0 (data = 000h to FFFh, default = 000h = LED off)
23-12	GSOUT1	Grayscale data for OUT1 (data = 000h to FFFh, default = 000h = LED off)
35-24	GSOUT2	Grayscale data for OUT2 (data = 000h to FFFh, default = 000h = LED off)

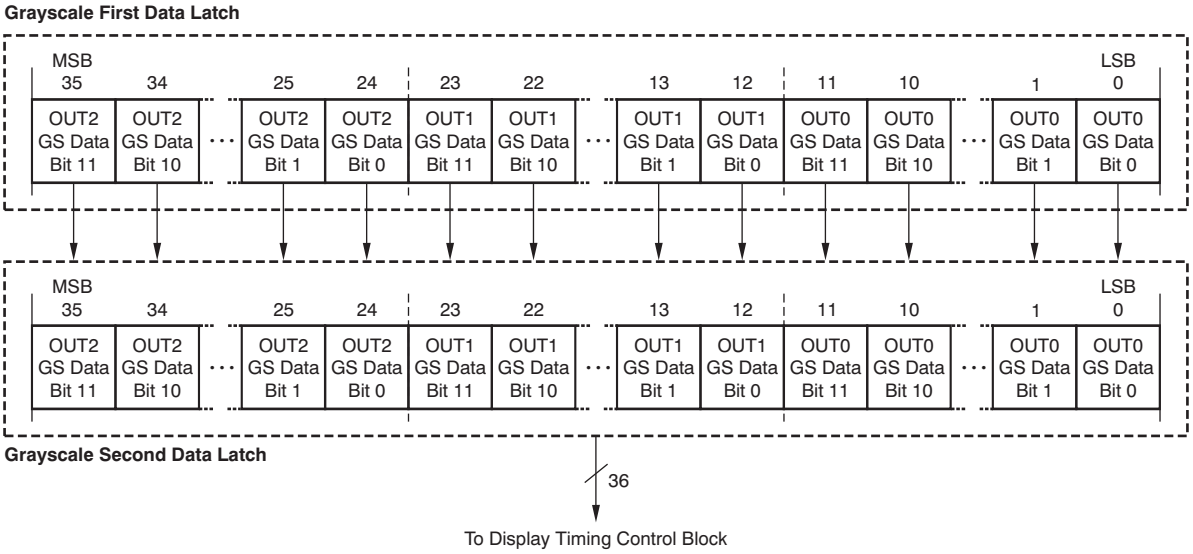


Figure 26. GS Data Latch Bit Assignment

Function Control (FC) and Global Brightness Control (BC) First/Second Data Latch

(Register Address = 1111b)

The FC and BC first Data Latch total bit length is 15 bits. The BC second latch bit length is seven bits. The FC data are used to set the function mode; the BC second data latch sets the current ratio of each constant-current output. The BC first latch holds the data written through the differential signal interface, and the latched data in the first latch are copied to the second latch at the rising edge of the 4096th GS clock when the auto data refresh bit is set to '1' in the FC latch. The first and second latch data are updated at the same time by the data written through the differential signal interface when the auto data refresh bit is set to '0'. When the IC is powered on, the FC data should be set before the GS data setting because the PWM control starts as soon as the GS data (except '0') are written into this second latch.

The data bit assignments are shown in Table 9 and Figure 27. OUTn set the current ratio in select BC data; see Table 3.

Table 9. Global Brightness Control and Function Control Data Latch Bit Assignment

BIT NUMBER	BIT NAME	DESCRIPTION
6-0	BCDATA	Global brightness control (BC) data for all outputs (default = 7Fh)
7	DATRFH	Auto data refresh (default = 0) 0 = Disabled; the GS and BC first and second data latches are simultaneously updated by the internal data latch pulse. 1 = Enabled; the GS and BC second data latches are updated with the data in the first latch at the 4096th rising edge of the grayscale clock or the display timing reset timing.
8	DSPRPT	Auto display repeat (default = 0) 0 = Disabled; all OUTn on/off controls are not repeated. The output is turned on and off one time only after the GS clock counter is reset. 1 = Enabled; all OUTn on/off controls are repeated according to the 4096th GS clock after the GS clock counter is reset.
9	EXTCLK	External grayscale clock select (default = 0) 0 = Internal clock is selected; each OUTn on/off control timing is synchronized with the internal clock. 1 = External clock is selected; each OUTn on/off timing control is synchronized with the shift clock generated by the differential signal with the SCKA and SCKB input pin.
10	TMGRST	Display timing reset (default = 0) 0 = Disabled; the GS clock counter is not reset and all OUTn are not forced off when the internal latch pulse is generated for GS data writing. This bit is always '0' when the internal clock is selected. 1 = Enabled; the GS clock counter is reset and all OUTn are forced off whenever an internal latch pulse is generated for GS data writing. This bit can be set to '1' only when the external clock is selected.
11	DCENA	Dot Correction (DC) data write control (default = 0) 0 = Disabled; the DC data latch is fixed to the DC data in the EEPROM and DC data cannot be changed. 1 = Enabled; the DC data latch is not fixed to the DC data in the EEPROM and the data in the DC data latch can be changed via serial interface.
35-12	—	No assigned bit (24-bit data). No function has not been assigned to these bits. If any data are written to these bits, device operation is not affected.

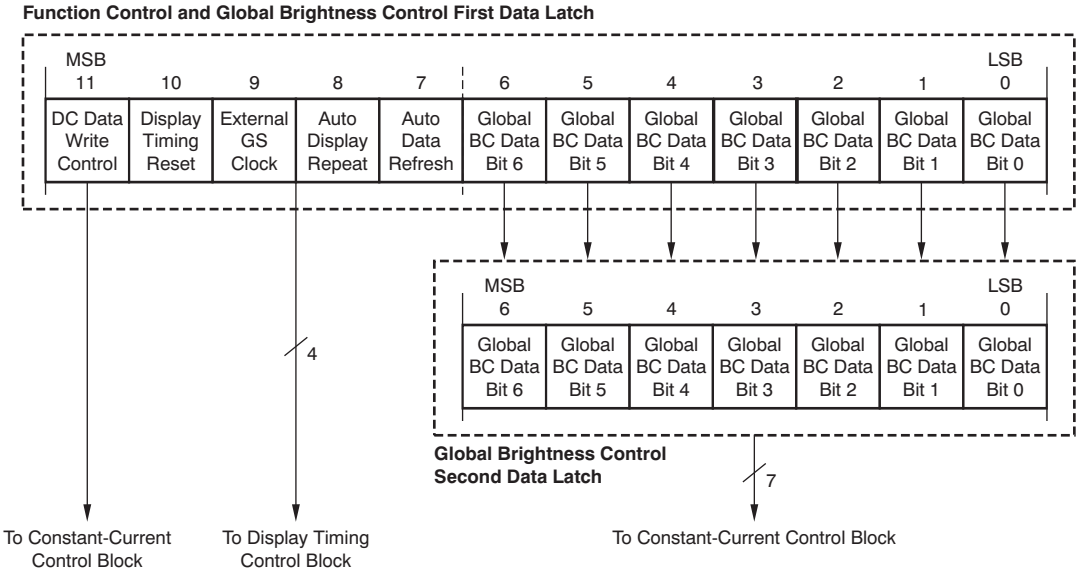


Figure 27. Function Control Data Latch Bit Assignment

Dot Correction (DC) Data Latch (Register Address = 1110b)

This data latch bit length is 21 bits. These data are used to set the current ratio of each constant-current output. When the IC is powered on, the DC data latch is set to the data in the DC data EEPROM. When the DC data write control bit is '1', the data can be changed by data written through the differential signal interface. The data bit assignments are shown in Table 10 and Figure 28.

Table 10. Dot Correction Data Latch Bit Assignment

BIT NUMBER	BIT NAME	DESCRIPTION
6-0	DCOUT0	Dot correction data for OUT0 (data = 00h to 7Fh, default = EEPROM data)
13-7	DCOUT1	Dot correction data for OUT1 (data = 00h to 7Fh, default = EEPROM data)
20-14	DCOUT2	Dot correction data for OUT2 (data = 00h to 7Fh, default = EEPROM data)
35-21	—	No assigned bit (24-bit data). No function has not been assigned to these bits. If any data are written to these bits, device operation is not affected.

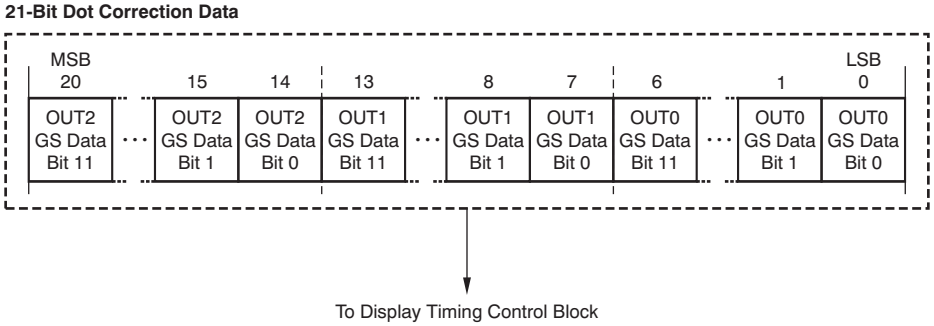


Figure 28. Dot Correction Data Latch Bit Assignment

EEPROM1 and EEPROM2 Write Data Latch

Each data latch bit length is 36 bits. The EEPROM1 write data latch sets the buck converter maximum on-duty ratio, VFB target voltage, and the EEPROM differential interface mode. The EEPROM2 write data latch is used to set the EEPROM DC default value.

EEPROM1 Write Data Latch (Register Address = 1100b)

The data bit assignments of the EEPROM write data latch 1 are shown in Table 11 and Figure 29.

Table 11. EEPROM1 Write Data Latch Bit Assignment

BIT NUMBER	BIT NAME	DESCRIPTION
2-0	ONDUTY	PH on-duty (data = 0h to 7h, factory default = 0h)
7-3	FBVOLT	FB target voltage (data = 00h to 1Fh, factory default = 00h)
9-8	DSIMOD	Differential signal interface (DSI) timing mode (data = 0h to 3h, factory default = 0h)
13-10	LATTIM	Internal latch generation delay time (data = 0h to Fh, factory default = Fh)
27-14	—	No EEPROM bits (14-bit data). The data cannot be stored in these bits even if data are written to these bits.
35-28	WRCMD1	Write command. When data are written to the EEPROM1 write data latch, these data must be A5h (10100101b).

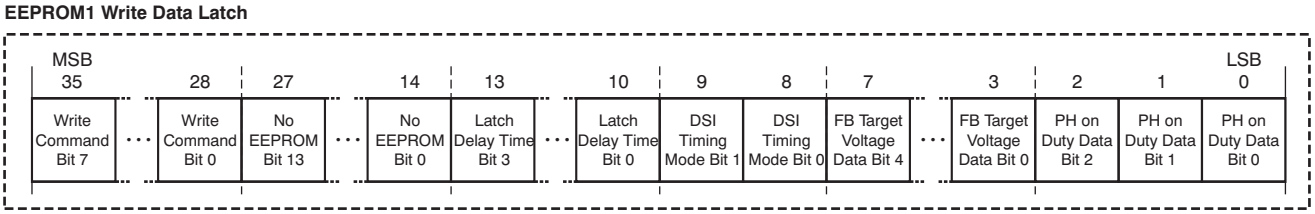


Figure 29. EEPROM1 Write Data Latch Bit Assignment

Maximum On-Duty Data for Buck Converter

The TLC5970 buck converter always operates with the Pulse Frequency Modulation (PFM) mode. Therefore, the PH on-duty should be set to the value calculated by Table 12 to avoid inductor current saturation at the inductor.

Table 12. Maximum On-Duty Selection Truth Table

ON-DUTY DATA (Binary)	ON-DUTY DATA (Decimal)	ON-DUTY DATA (Hex)	ON-DUTY AT PH (%, Typical)
000	0	0	18
001	1	1	30
010	2	2	42
011	3	3	55
100	4	4	67
101	5	5	80
110	6	6	86
111	7	7	86

FB Target Voltage

These bits select the target voltage of the FB pin. The FB pin is connected to the LED anode side. The set data should be determined by Equation 12. Also, the set data should be set to the higher voltage of the three-color LED line. The buck converter chargeup FB voltage to the FB target voltage (VFB) is set by these bits with a soft-start sequence after the IC is powered on.

VFB (V) = Typical LED forward voltage × the number of LED in series + 1 V.

VFB set data can be calculated by Equation 12:

$$\text{FB Set Data for VFB} = \frac{(\text{VFB} - 7) \times 31}{10} \quad (12)$$

FB voltage (VFB) can be calculated by Equation 13:

$$\text{FB Voltage (V)} = \frac{10 \times \text{FB Set Data}}{31} + 7 \quad (13)$$

Table 13 lists the FB voltage set by FB set data.

Table 13. FB Target Voltage Selection Truth Table

FB DATA (Binary)	FB DATA (Decimal)	FB DATA (Hex)	TARGET FB VOLTAGE (V)	FB DATA (Binary)	FB DATA (Decimal)	FB DATA (Hex)	TARGET FB VOLTAGE (V)
0 0000	0	00	7.0	1 0000	16	10	12.2
0 0001	1	01	7.3	1 0001	17	11	12.5
0 0010	2	02	7.6	1 0010	18	12	12.8
0 0011	3	03	8.0	1 0011	19	13	13.1
0 0100	4	04	8.3	1 0100	20	14	13.5
0 0101	5	05	8.6	1 0101	21	15	13.8
0 0110	6	06	8.9	1 0110	22	16	14.1
0 0111	7	07	9.3	1 0111	23	17	14.4
0 1000	8	08	9.6	1 1000	24	18	14.7
0 1001	9	09	9.9	1 1001	25	19	15.1
0 1010	10	0A	10.2	1 1010	26	1A	15.4
0 1011	11	0B	10.5	1 1011	27	1B	15.7
0 1100	12	0C	10.9	1 1100	28	1C	16.0
0 1101	13	0D	11.2	1 1101	29	1D	16.4
0 1110	14	0E	11.5	1 1110	30	1E	16.7
0 1111	15	0F	11.8	1 1111	31	1F	17.0

Differential Signal Interface (DSI) Timing Mode

These bits select a differential interface timing mode from three types of timing modes, as shown in Table 14.

Table 14. DSI Timing Mode Selection Truth Table

DSIMOD DATA (Binary)	DSIMOD DATA (Decimal)	DSIMOD DATA (Hex)	SELECTED MODE
00	0	0	Mode 0 (factory default)
01	1	1	Mode 1
10	2	2	Mode 2
11	3	3	Mode 2

Mode 0 is a low-frequency transfer mode. Maximum transfer frequency is lowest in the timing modes but it is easy to transfer the data over long distances without transmission errors because this mode can control the data hold time for the next connected device. The SCKY/SCKZ output level is controlled by the SCKA/SCKB level. SCKY/SCKZ go to a high level when the SCKA/SCKB level is high. The SCKY/SCKZ output level is controlled by the SCKA/SCKB level. SCKY/SCKZ go to a low level when the SCKA/SCKB level is low. The SDTY/SDTZ data change after 30 ns (typical) from when the SCKA/SCKB falling clock is input.

Mode 1 is the middle frequency transfer mode. Maximum transfer frequency and transmission distance are mean between mode 0 and mode 2. The SDTY/SDTZ data change after 50 ns (typical) from when the SCKA/SCKB rising clock is input.

Mode 2 is the high-frequency transfer mode. Maximum transfer frequency is highest in the three timing modes. This mode should be used for short distance data transmission. SDTY/SDTZ data change after 30 ns (typical) from when the SCKA/SCKB rising clock is input. The timing diagram for each mode is shown in Figure 30 to Figure 32.

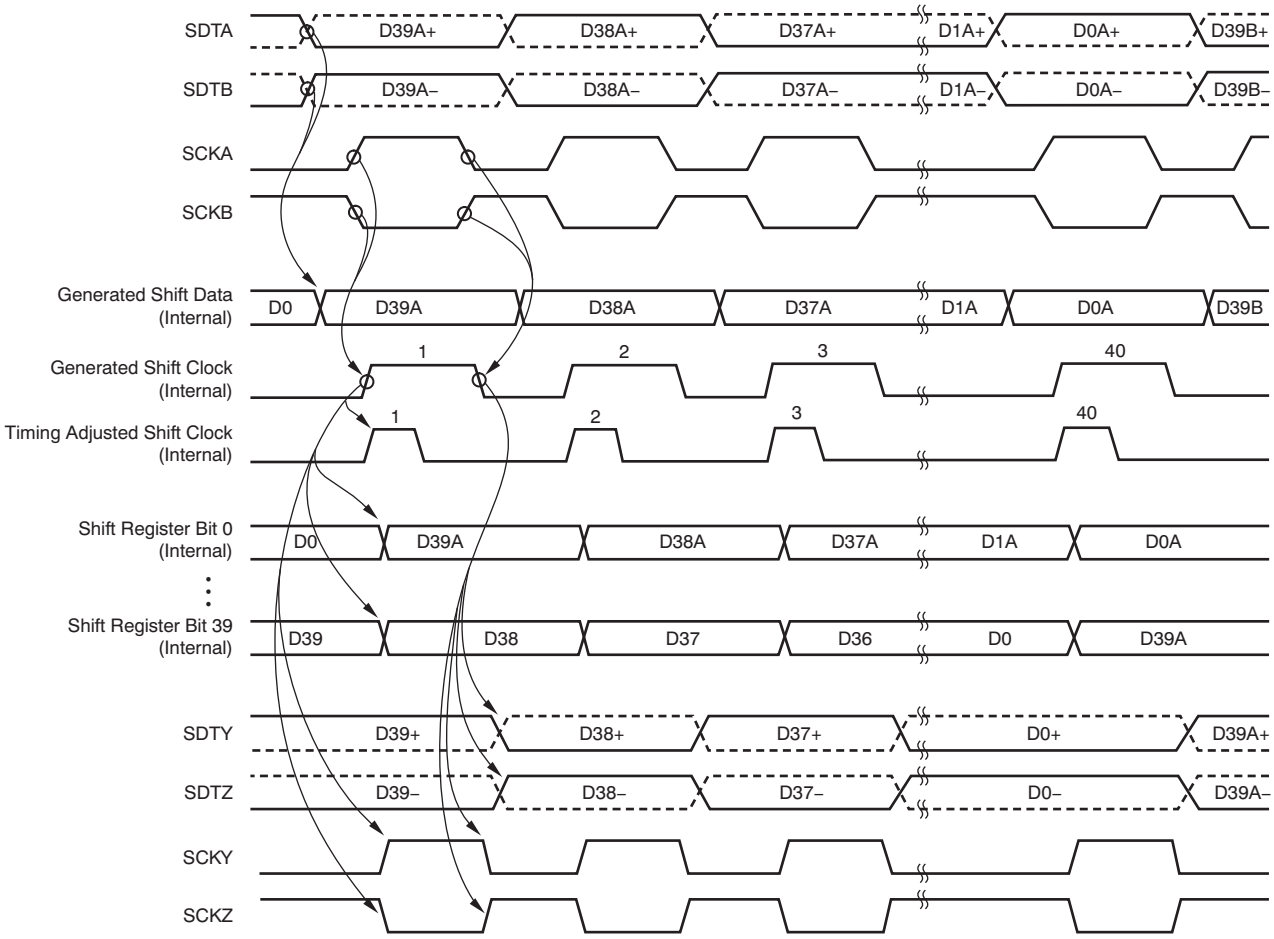


Figure 30. DSI Timing Mode 0

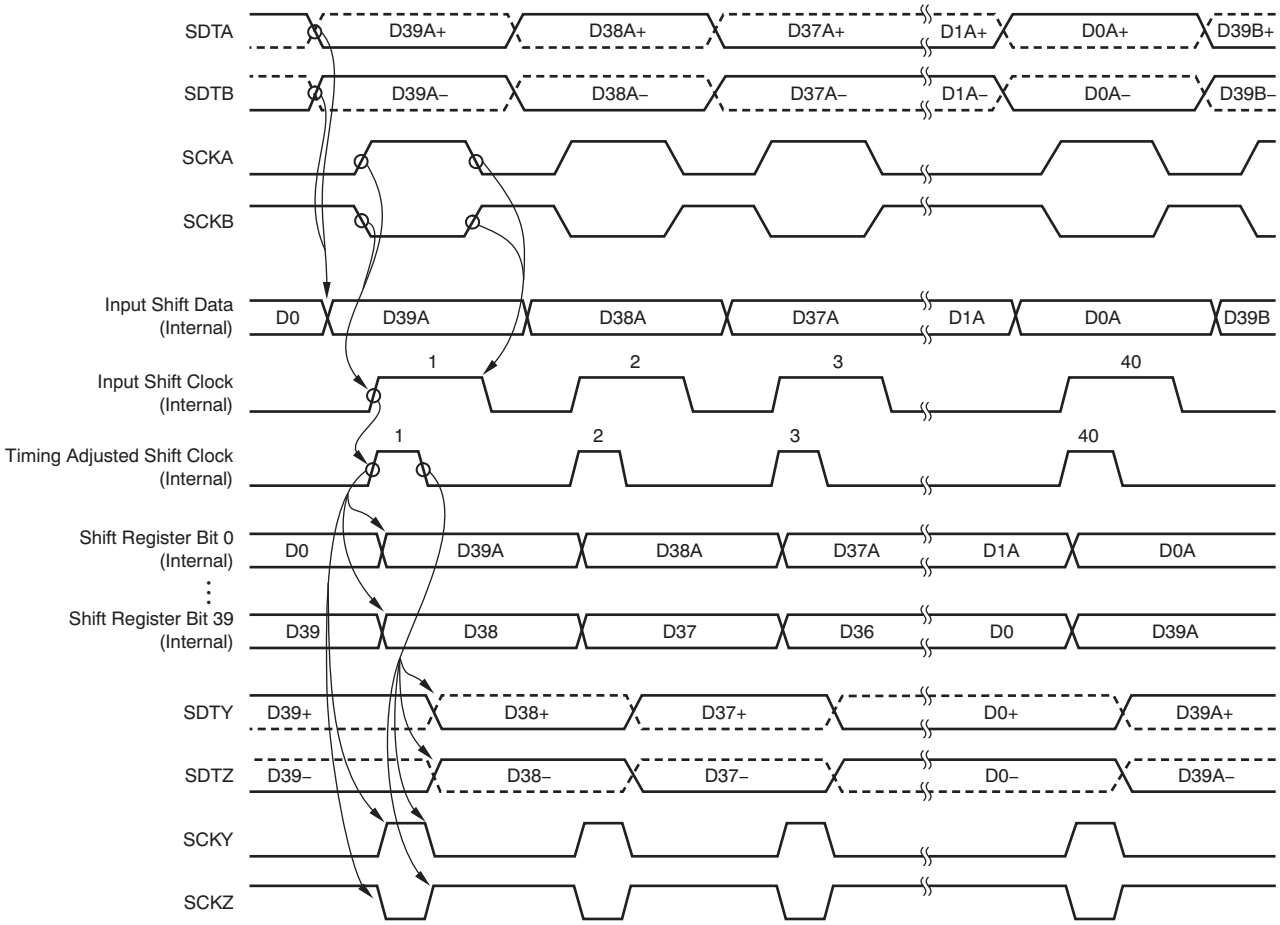


Figure 31. DSI Timing Mode 1

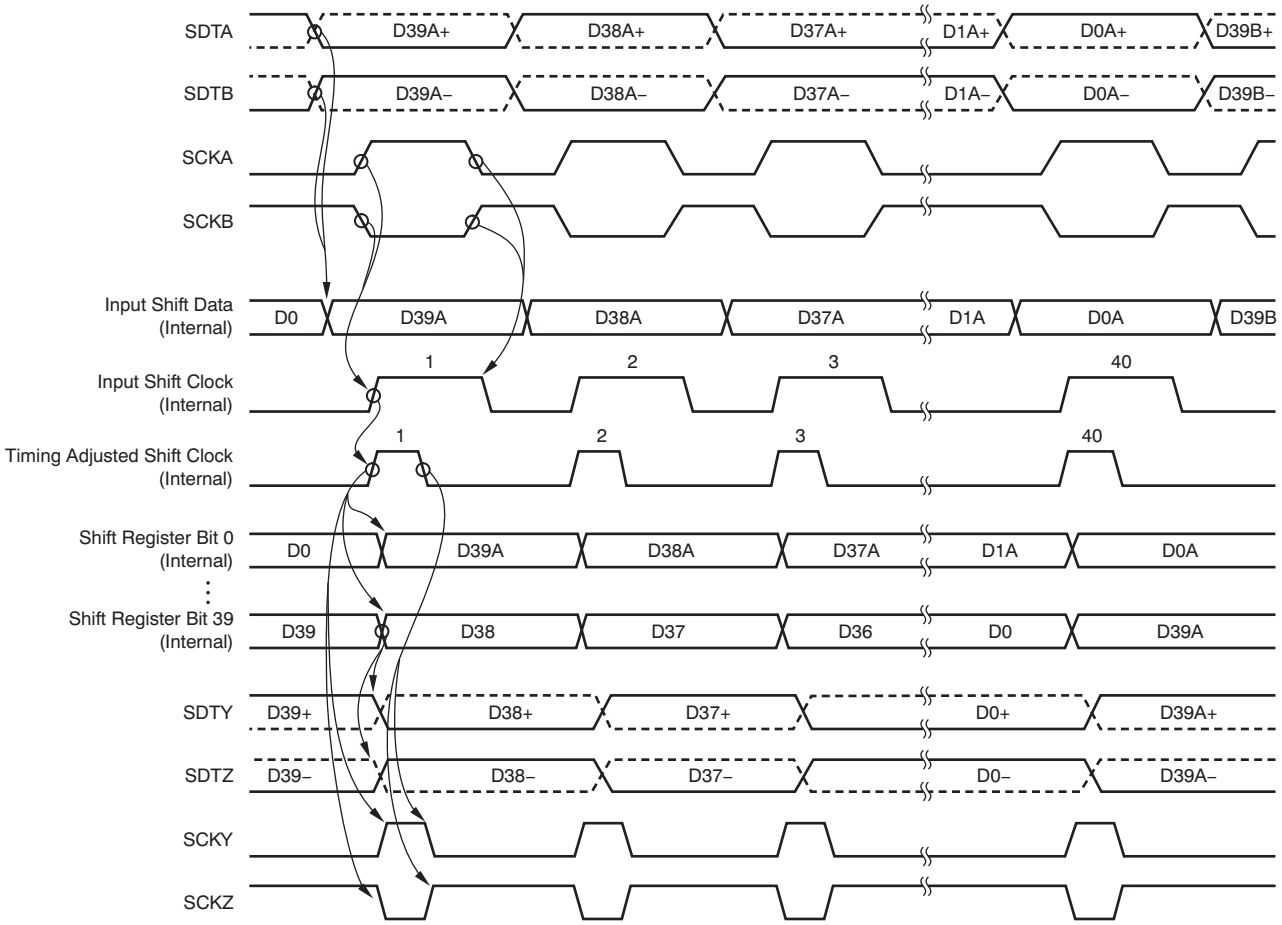


Figure 32. DSI Timing Mode 2

Internal Latch Pulse Delay Time

Shifted in lower 36-bit data in the 40-bit shift register is latched into the latch selected by the higher four bits of the shift register after the programmed time by the following code is passed from the last rising edge of SCLK. The next SCLK rising edge for new data inputs must be input after over two clocks of the internal oscillator clock period from the shift register is latched.

Table 15. Internal Latch Pulse Delay Time Selection Truth Table

FB DATA (Binary)	FB DATA (Decimal)	FB DATA (Hex)	INTERNAL LATCH PULSE DELAY TIME (µs)	
			MINIMUM	MAXIMUM
0000	0	0	0.3	0.8
0001	1	1	0.6	1.3
0010	2	2	1.3	2.3
0011	3	3	2.6	4.3
0100	4	4	5.3	8.3
0101	5	5	10	16
0110	6	6	21	33
0111	7	7	42	65
1000	8	8	85	129
1001	9	9	170	257
1010	10	A	341	513
1011	11	B	682	1025
1100	12	C	1365	2049
1101	13	D	2730	4097
1110	14	E	5461	8193
1111	15	F	10922	16385

EEPROM2 Write Data Latch (Register Address = 1101b)

The EEPROM2 write data latch data bit assignments are shown in Table 16 and Figure 33.

Table 16. EEPROM2 Write Data Latch Bit Assignment

BIT NUMBER	BIT NAME	DESCRIPTION
6-0	DCOUT0	Dot correction data for OUT0 (data = 00h to 7Fh, factory default = 7Fh)
13-7	DCOUT1	Dot correction data for OUT1 (data = 00h to 7Fh, factory default = 7Fh)
20-14	DCOUT2	Dot correction data for OUT2 (data = 00h to 7Fh, factory default = 7Fh)
27-21	—	No EEPROM bits (7-bit data). Data cannot be stored in these bits even if data are written to these bits.
35-28	WRCMD2	Write command. When data are written to the EEPROM1 write data latch, these data must be 5Ah (01011010b).

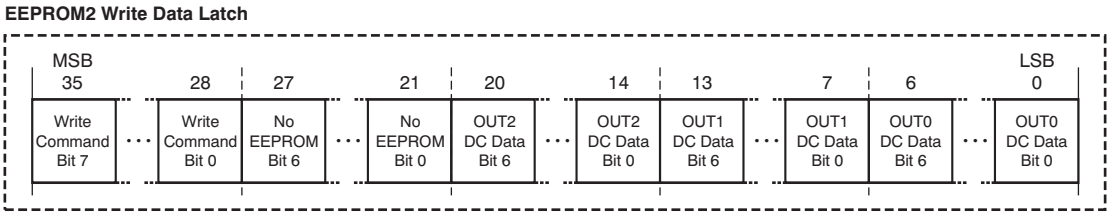


Figure 33. EEPROM2 Write Data Latch Bit Assignment

EEPROM Data Write Procedure

The DC data and the maximum on-duty data can be programmed into the EEPROM with the following procedure:

1. Turn on the VCC power supply.
2. Set the VROM pin voltage to 19 V ± 0.5 V. The supply current is 5 mA (typical). The buck converter stops while the VROM pin is held at the voltage.
3. Write the data for EEPROM write data latch 1 with the address. Write the command and the write data to EEPROM data latch address.
4. Wait for more than 40 ms without data transfer. The maximum wait time is unlimited.
5. Stop supplying 19 V to the VROM pin and release the pin.
6. Write the grayscale data to turn on the LED and check LED brightness.
7. If the brightness must be adjusted, send new dot correction data to the DC data latch for brightness adjust.
8. Check the brightness again.
9. Repeat steps 8 and 9 to determine the best DC data.
10. Write the best DC data to the EEPROM write data latch 2 using steps 3 to 5 in this sequence.

Readout Register

EEPROM Data Readout Register (Register Address = 1011b)

When any data are written to this register address, the programed data in the EEPROM are loaded to the lower 36 bits in the 40-bit shift register from this readout register (register address = 1011b). The higher 4-bit data in the 40-bit shift register are not changed from 1011b. The loaded data can be read out from SDTY and SDTZ and syncronized by the shift clock generated from SCKA and SCKB. The data bit assignments are shown in Table 17 and Figure 34.

Table 17. EEPROM Data Readout Register Bit Assignment

BIT NUMBER	BIT NAME	DESCRIPTION
6-0	RDDC0	Dot correction data for OUT0 in EEPROM (7-bit data)
13-7	RDDC1	Dot correction data for OUT1 in EEPROM (7-bit data)
20-14	RDDC2	Dot correction data for OUT2 in EEPROM (7-bit data)
23-21	RDONDTY	On-duty (4-bit data)
28-24	RDVFB	FB target voltage (5-bit data)
30-29	RDDSI	DSI mode (2-bit data)
34-31	RDDLY	Internal data latch pulse delay time (4-bit data)
35	RDRSV	TI reserved data (1-bit data, no fixed data)

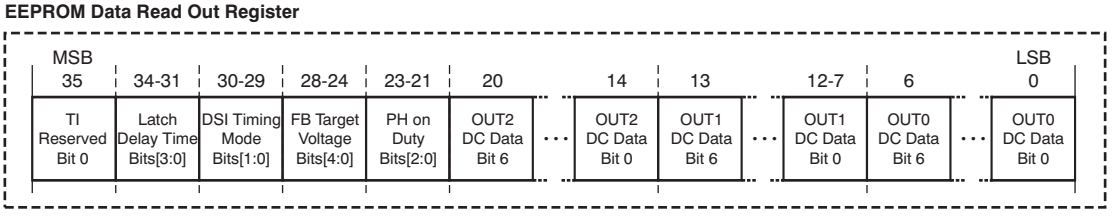


Figure 34. EEPROM Data Readout Register Bit Assignment

Status Information Data (SID) Readout Register (Register Address = 1010b)

When any data are written to this register address, the status of five error detections are loaded to the lower 36 bits in the 40-bit shift register from this readout register (register address = 1010b). The higher 4-bit data in the 40-bit shift register are not changed from 1010b. The loaded data can be readout from SDTY and SDTZ and syncronized by the shift clock generated from SCKA and SCKB. The data bit assignments are are shown in Table 18 and Figure 35.

Table 18. SID Readout Register Bit Assignment

BIT NUMBER	BIT NAME	DESCRIPTION
0	LOD	LED open detection (LOD) error flag 0 = All OUTn are either connected to the LED lamp or are not connected to the LED lamp. When all OUTn are not connected to LED lamp, the OVP flag is set to '1'. 1 = One or two OUTn are not connected to the LED lamp. This bit is set to '1' when the voltage of OUTn connected to the LED lamp is greater than approximately 4 V. Also, this bit is set to '1' when the SWOFF pin is connected to VREG.
1	SCP	Short-Circuit Protection (SCP) error flag 0 = The buck converter is operating normally. Also, this bit is set to '0' when SWOFF is connected to VREG. 1 = The buck converter is not operated by the SCP.
2	OVP	Overvoltage Protection (OVP) flag 0 = The buck converter is operating normally. Also, this bit is set to '0' when SWOFF is connected to VREG. 1 = The buck converter is not operated by the OVP.
3	PTD	Pre-Thermal Shutdown (PTD) log 0 = The LED driver has been in normal operation after the previous readout register reading. 1 = The LED driver has stopped operating due to the device temperature exceeding the PTD detect temperature after the previous readout register reading. This log is held until these register data are readout.
4	TSD	Thermal Shutdown (TSD) log 0 = The buck converter/LED driver/interface has been in normal operation after the previous readout register reading. 1 = The buck converter/LED driver/interface has stopped operating due to the device temperature exceeding the TSD detect temperature after the previous readout register reading. This flag is held until these register data are readout.
35-5	—	TI reserved data (31-bit data, no fixed data)

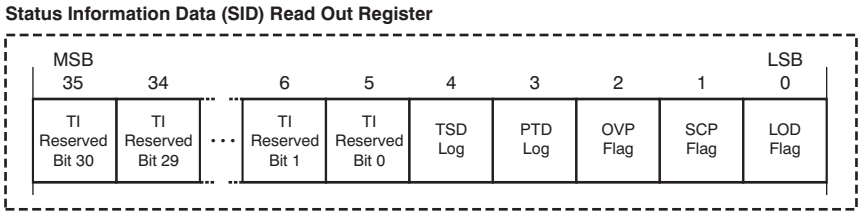


Figure 35. SID Readout Register Bit Assignment

DEVICE PROTECTION

When the Short-Circuit Protection (SCP) and Overvoltage protection (OVP) are operating, the buck converter stops. Afterwards, the buck converter is restarted with a soft-start when any data are written to the restart operation address, 1001b. The TLC5970 has an LED Open Detection (LOD) and four device protections as listed:

1. **LED open detection (LOD):** When SWOFF is connected to GND, the LOD can detect if one or two LEDs are opened or if OUTn is shorted to GND. The LOD flag is set to '1' in the readout data register when LEDs open or when OUTn is shorted to GND. If all LEDs are opened, the OVP flag comes up because the OUT0-OUT2 voltage is not pulled up. When SWOFF is connected to the VREG level, the LOD flag is set to '1' when the voltage of any OUTn is less than approximately 0.3 V at the 33rd GS clock from when OUTn is turned on. Also, the LOD data are kept until the next 33rd GS clock. Therefore, GS data must be set at 33d (decimal data) or more to ensure the correct LOD data.
2. **Short-Circuit Protection (SCP):** The SCP detects if the buck converter output is overloaded or if the FB line is open. SCP operates in this manner:
   (a) The SCP circuit observes the FB pin voltage.
   (b) If the FB is under 4 V (typical), then the SCP timer starts to count the number of times the PH switches.
   (c) When the SCP timer counts to 4, if FB voltage is still below 4 V, the SCP circuit stops the buck converter and the LED driver from operating. Also, the buck converter target voltage is set to the FB voltage programmed in the EEPROM at same time.
   (d) The SCP flag is set in the readout register.
   (e) The differential interface can be used even if buck converter is not operating.

   It is required to write any data to the address 1001b to restart the device operation.
3. **Overvoltage Protection (OVP):** The OVP detects if the buck converter target voltage is set to the maximum code. Also, the OVP detects when all LEDs are opened. The OVP does not work when the SWOFF signal level is high. Therefore, the OVP flag in the SID is always '0'. The OVP circuit operates in this manner:
   (a) The OVP circuit checks that the internal digital-to-analog converter (DAC) code is at the 33rd GS clock.
   (b) If the DAC code is not the maximum code, the OVP period counter is reset. If the DAC code is the maximum code, then the OVP period counter is counted up.
   (c) When the OVP period counter becomes 4, the OVP circuit stops the LED driver from operating and sets the DAC code to the FB voltage programmed in the EEPROM. Then the buck converter operation does not stop.
   (d) The OVP flag is set to '1' in the readout register.
   (e) The differential interface can be used even if the buck converter is not operating.
   (f) The LED driver cannot be controlled again until any data are written to the address 1001b to clear the OVP flag.
4. **Pre-Thermal Shutdown (PTD):** The PTD stops the LED driver operation at T_{PTD} (T_{PTD} = +138°C, typical) device temperature to avoid the device temperature from becoming higher. PTD operation follows this logic:
   (a) The LED driver (OUT0to OUT2) is forced off.
   (b) Set the PTD flag in the readout register.
   (c) Start the LED driver control again when the device temperature drops below $T_{PTD} – T_{HYSP}$ (T_{HYSP} = +8°C, typical).
5. **Thermal Shutdown (TSD):** The TSD stops the buck coverter/LED driver/differential interface operation at T_{TSD} (T_{TSD} = +168°C, typical) device temperature to prevent the device temperature from becoming too high. TSD operation follows this sequence:
   (a) The buck converter switching/LED driver (OUT0 to OUT2)/differential interface are forced off.
   (b) The TSD flag is set in the readout register.
   (c) Buck converter target voltage is set to the FB voltage programmed in the EEPROM.
   (d) Differential interface operation starts again when the device temperature drops below $T_{TSD} – T_{HYST}$ (T_{HYST} = +10°C, typical). Then the buck converter starts to operate.

PRE-BOOST FUNCTION

The TLC5970 has a pre-boost function. This function increases the DAC code of the buck converter a few steps from the 16th GS clock before the LED turns on to prevent the output voltage from decreasing much. The pre-boost is finished at the 33rd GS clock rising edge. After the GS counter is reset, the first 16 GS clocks are spent for the pre-boost and the LED is turned on from the 17th clock. Therefore, 4112 GS clocks are needed to display the full GS data in the first period in auto repeat mode. In no auto repeat mode, 4112 GS clocks are always needed for one display period.

UNDERVOLTAGE LOCKOUT (UVLO)

An undervoltage lockout (UVLO) circuit is implemented to keep the device disabled when VREG is lower than the UVLO start voltage. The following list describes each functional block status during a UVLO condition:

- The buck converter control block, constant-current timing control, and oscillator are initialized.
- The 40-bit data shift register is set to all '0'.
- Each data latch is set to the default value except for the DC latch.
- The data in the EEPROM is set to the DC data latch.
- The power-supply source for the differential interface is connected to VCC.
- FB voltage is discharged to GND.

NOISE REDUCTION

Large surge currents would flow through the IC and the board if all three LED channels are fully turned on simultaneously at the start of each grayscale cycle. These large surge currents could introduce detrimental noise and electromagnetic Interference (EMI) into other circuits. The TLC5970 turns on/off each OUTn with approximately a 40-ns time difference to reduce the switching noise and LED anode voltage drop.

APPLICATION CIRCUITS

The TLC5970 can be used to increase the LED drive current for high-current LEDs with the high-current LED operating mode (Figure 36) or with the parallel operating mode (Figure 37). In the parallel operating mode, the external clock mode should be used to avoid flickering that can occur in an unsyncronized internal clock.

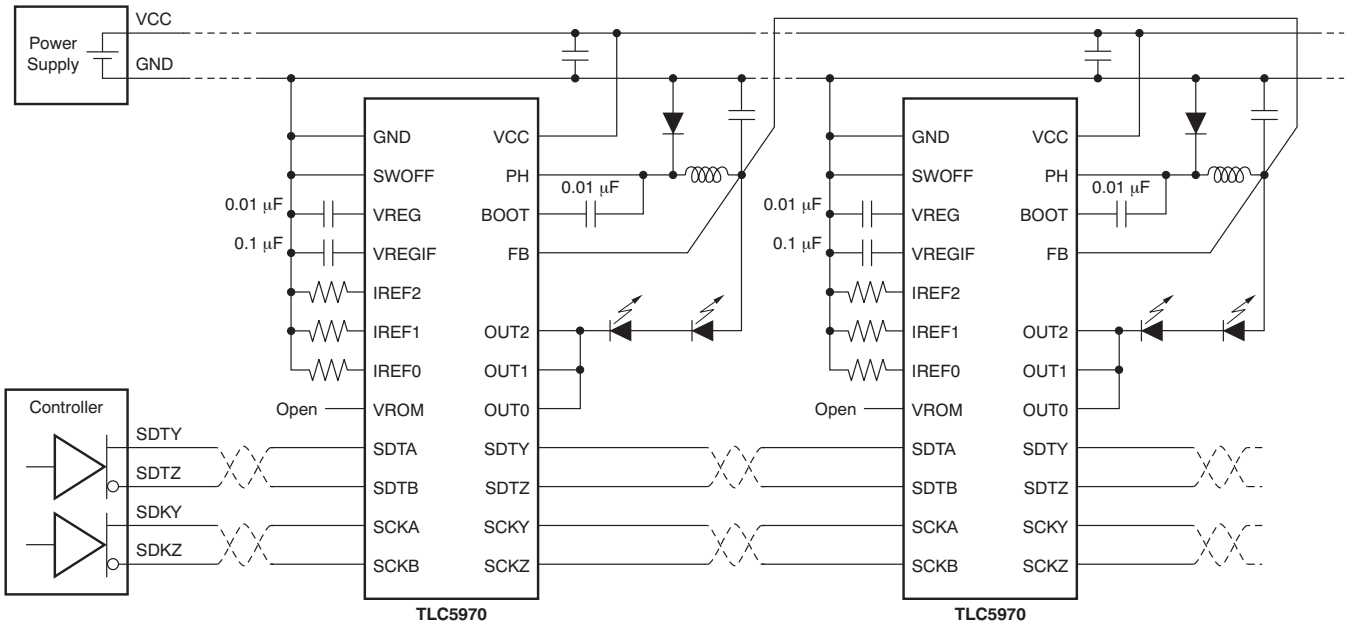


Figure 36. High-Current LED Operating Mode

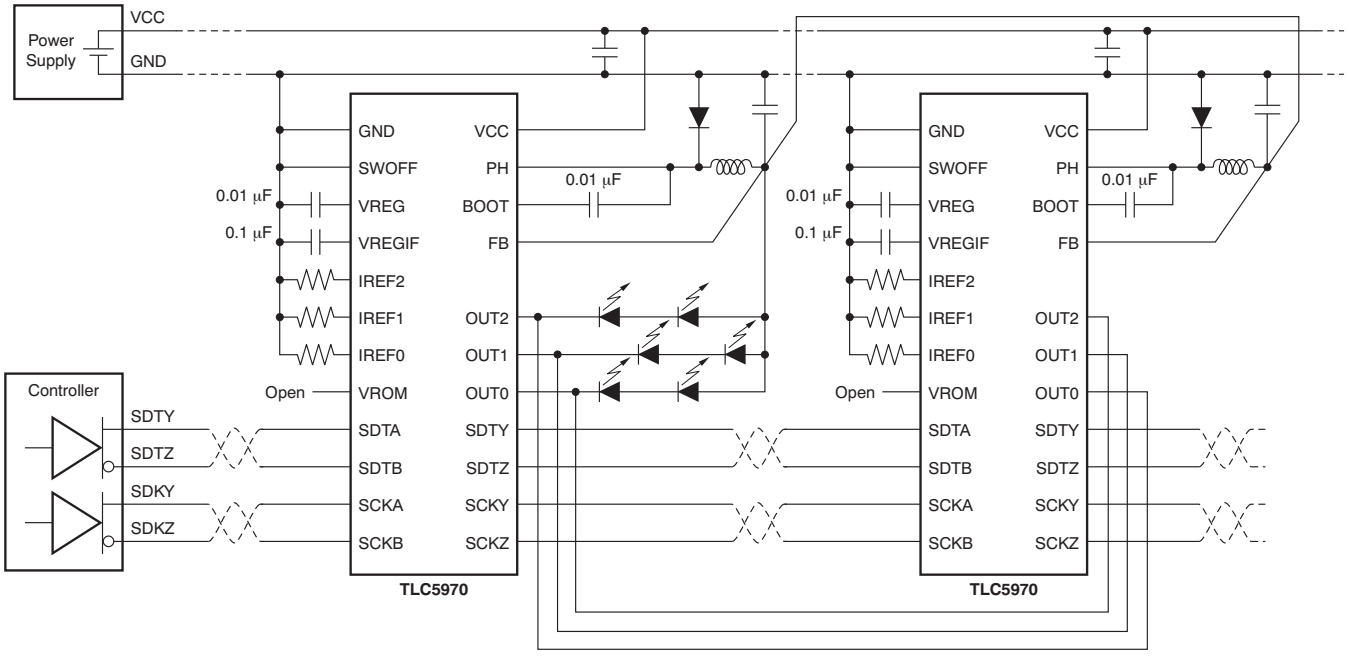


Figure 37. Parallel Operating Mode

The TLC5970 can be used to drive several LED lamps for small-current LEDs with the master-slave operation mode (Figure 38). In this operating mode, BC data and DC data in the master device should not be set to '0' to hold the LED anode (FB) voltage.

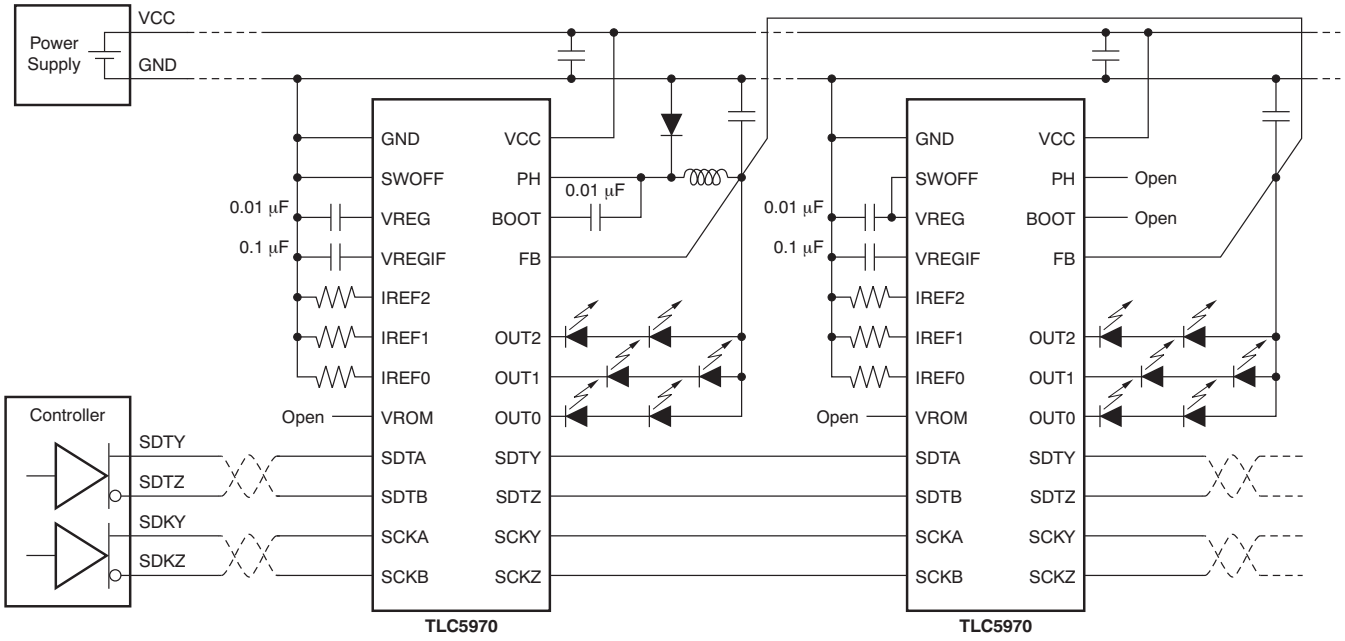


Figure 38. Master/Slave Operating Mode

The TLC5970 can be used as a 5 V single power-supply LED without a buck converter operating mode, as shown in Figure 39.

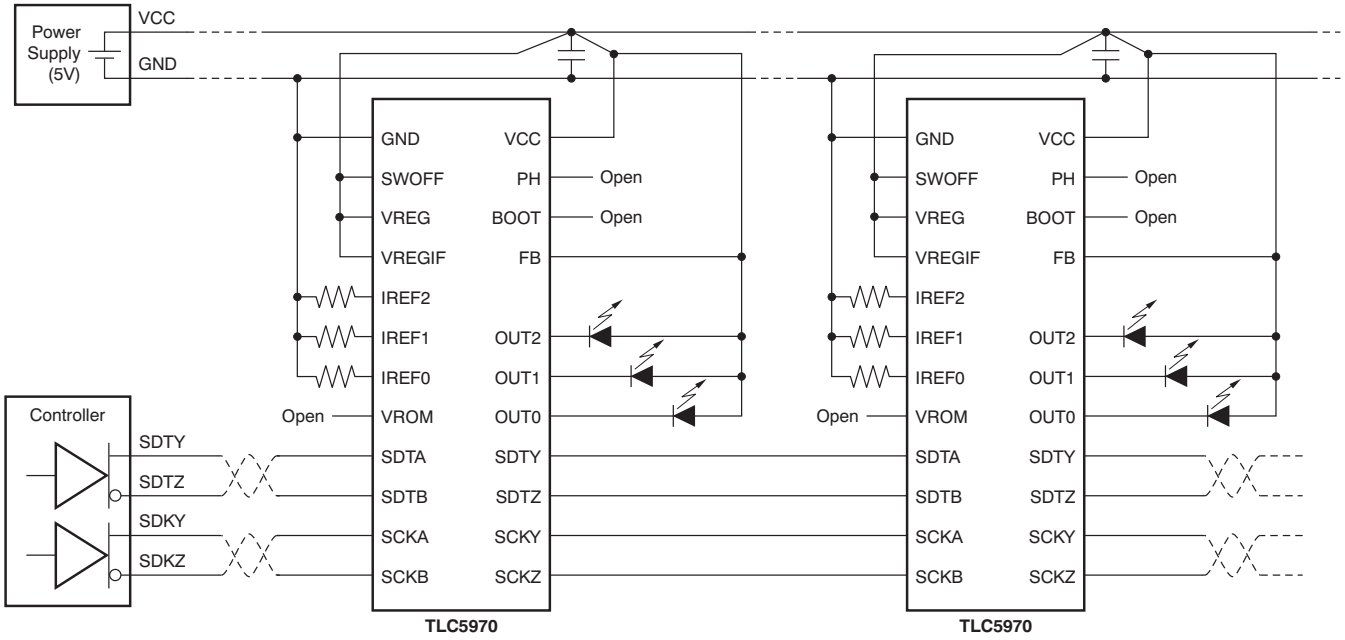


Figure 39. No Buck Converter Operating Mode

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2010) to Revision A **Page**

- Deleted information regarding HTTSOP-32 package of device throughout document. This device package will not be produced 1
- Deleted footnote 2 and information regarding HTSSOP-32 package from Ordering Information table 2
- Deleted footnote 2 and information regarding HTSSOP-32 package from Dissipation Ratings table 3
- Deleted DAP (HTSSOP-32) pinout drawing 11
- Deleted information regarding HTSSOP-32 package from the Terminal Functions table 12
- Added conditions to *Typical Characteristics* section 19
- Deleted information regarding HTSSOP-32 package from Figure 14 19
- Updated Figure 18 19

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC5970RHPR	OBSOLETE	VQFN	RHP	28		TBD	Call TI	Call TI	-40 to 85	5970	
TLC5970RHPT	OBSOLETE	VQFN	RHP	28		TBD	Call TI	Call TI	-40 to 85	5970	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

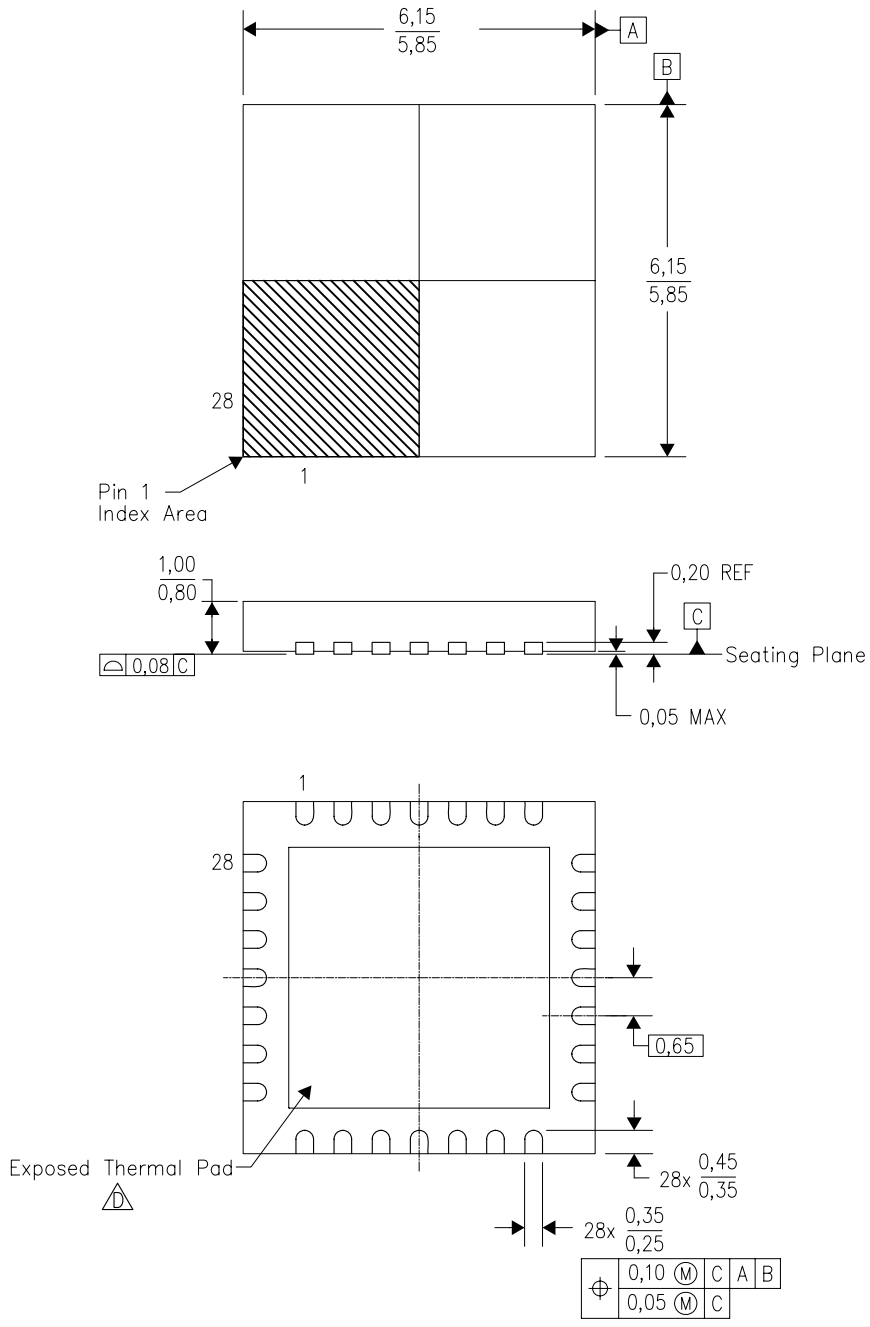
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

RHP (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

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