

MOSFET – Power, Single, N-Channel, Logic Level, SO-8FL

30 V, 0.67 mΩ, 370 A



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NTMFS4C020N

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Optimized for 4.5 Gate Drive
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	30	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	I_D 370 A
		$T_C = 25^\circ\text{C}$	P_D 161 W
Power Dissipation $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_A = 25^\circ\text{C}$	I_D 57 A
		$T_A = 25^\circ\text{C}$	P_D 3.84 W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)			
Power Dissipation $R_{\theta JA}$ (Notes 1, 2, 3)			
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM} 900	A
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Source Current (Body Diode)	I_S	110	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 35 \text{ A}$)	E_{AS}	862	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

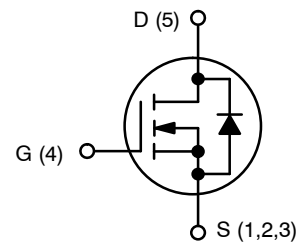
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

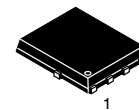
Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta JC}$	0.93	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	39	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
30 V	0.67 mΩ @ 10 V	370 A
	0.78 mΩ @ 6.5 V	
	0.95 mΩ @ 4.5 V	

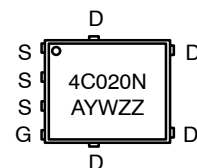


N-CHANNEL MOSFET



SO-8 FLAT LEAD CASE 488AA STYLE 1

MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4C020NT1G	SO-8 FL (Pb-Free)	1500 / Tape & Reel
NTMFS4C020NT3G	SO-8 FL (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			16.3		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 24 V	T _J = 25 °C		1	μA
			T _J = 125°C		100	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V			100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	1.3		2.2	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J			5.8		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 30 A		0.56	0.67	mΩ
		V _{GS} = 6.5 V, I _D = 30 A		0.56	0.78	
		V _{GS} = 4.5 V, I _D = 30 A		0.76	0.95	
Forward Transconductance	g _{FS}	V _{DS} = 3 V, I _D = 30 A		183		S
Gate Resistance	R _G	T _A = 25 °C		1.0	2.5	Ω

CHARGES AND CAPACITANCES

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 15 V		10144	15250	pF
Output Capacitance	C _{OSS}			5073	7610	
Reverse Transfer Capacitance	C _{RSS}			148	350	
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 15 V; I _D = 30 A		63	105	nC
Threshold Gate Charge	Q _{G(TH)}			18	36	
Gate-to-Source Charge	Q _{GS}			29	58	
Gate-to-Drain Charge	Q _{GD}			13	26	
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 15 V, I _D = 30 A		139	230	nC

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 4.5 V, V _{DS} = 15 V, I _D = 15 A, R _G = 3.0 Ω		29		ns
Rise Time	t _r			68		
Turn-Off Delay Time	t _{d(OFF)}			53		
Fall Time	t _f			36		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 10 A	T _J = 25°C		0.73	1.1	V
			T _J = 125°C		0.55		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 30 A		87		ns	
Charge Time	t _a			43			
Discharge Time	t _b			44			
Reverse Recovery Charge	Q _{RR}				147		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

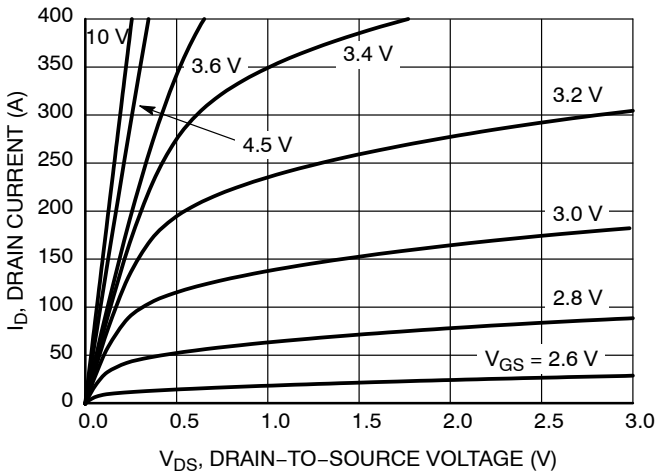


Figure 1. On-Region Characteristics

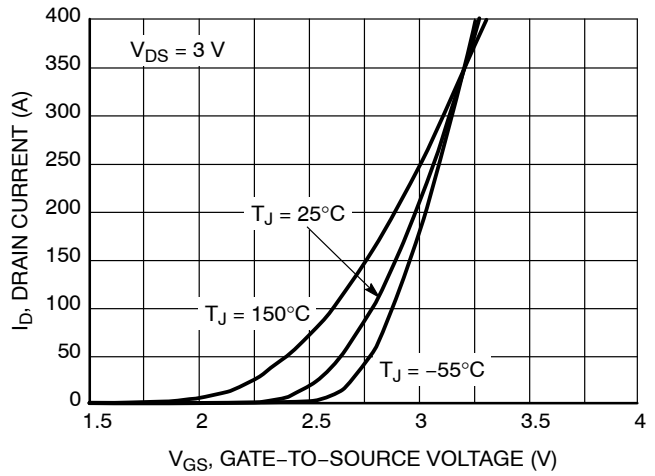


Figure 2. Transfer Characteristics

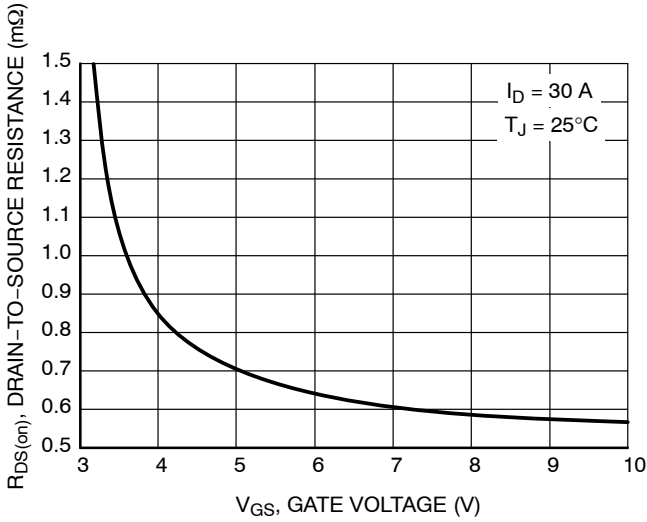


Figure 3. On-Resistance vs. Gate-to-Source Voltage

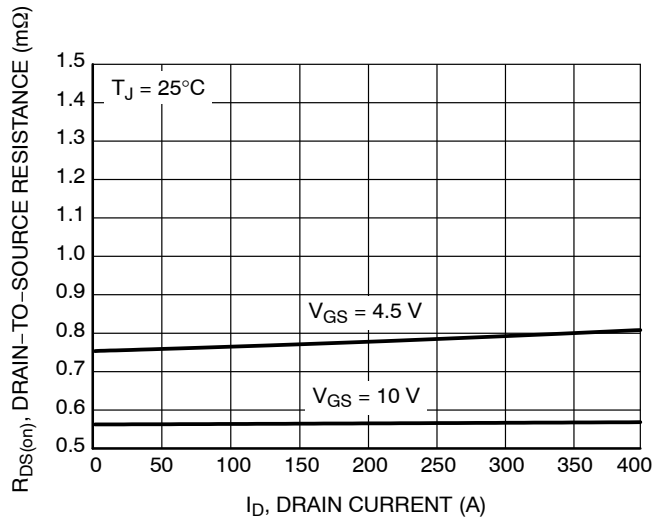


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

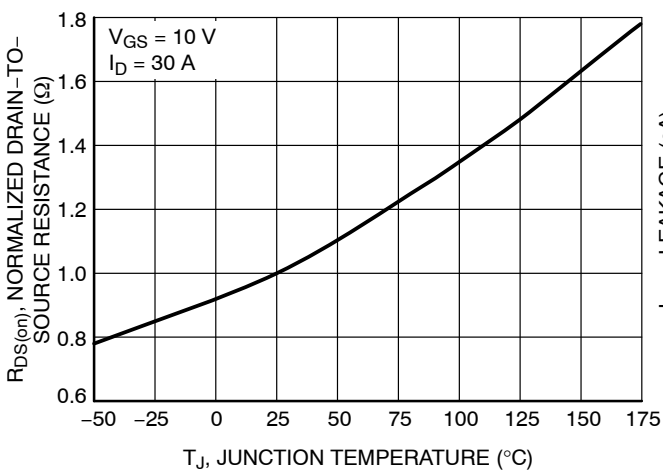


Figure 5. On-Resistance Variation with Temperature

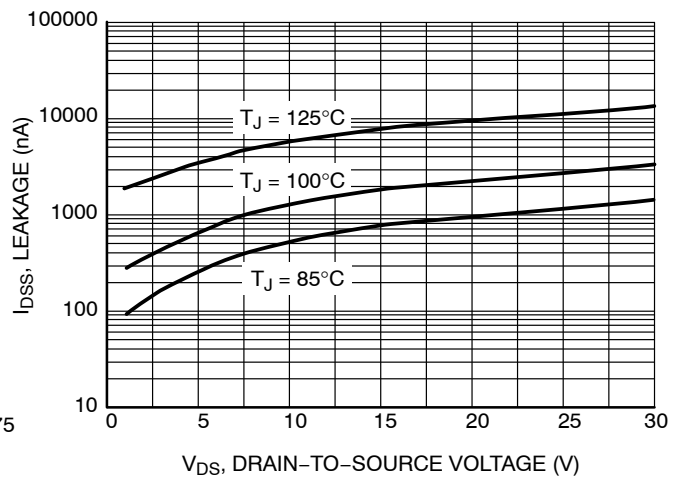


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

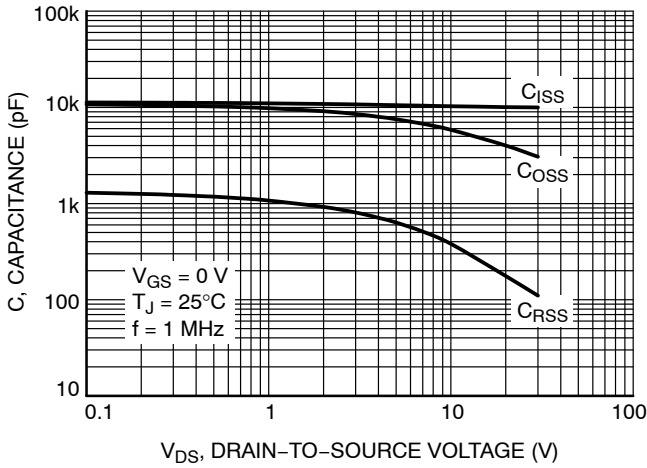


Figure 7. Capacitance Variation

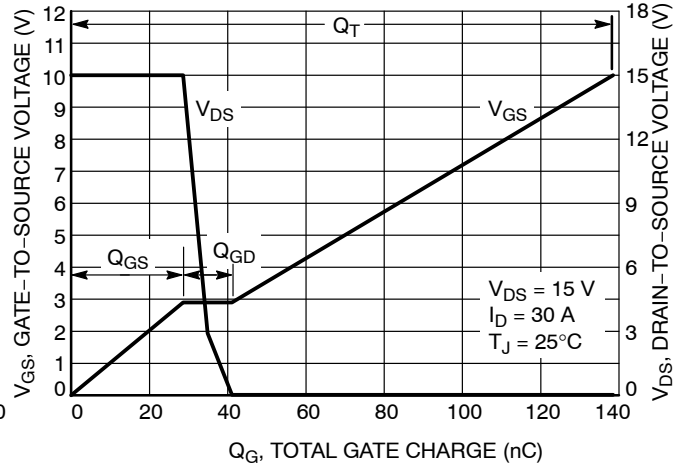


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

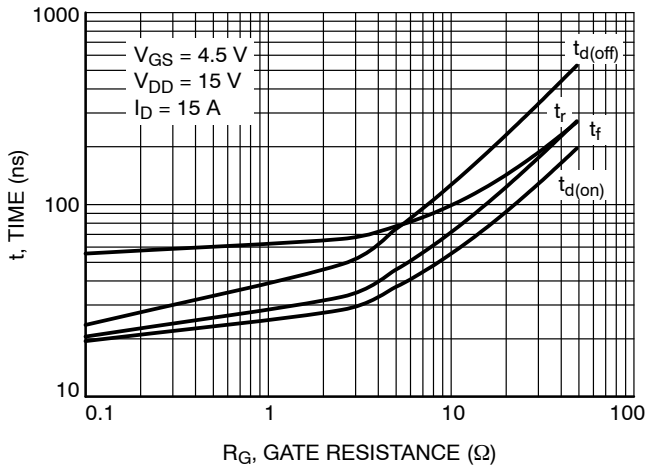


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

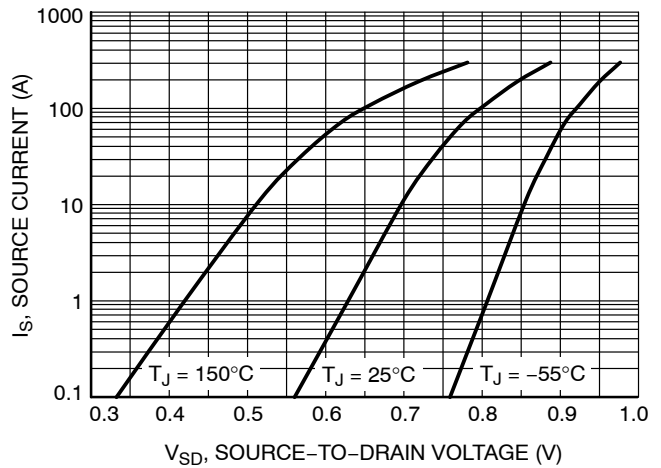


Figure 10. Diode Forward Voltage vs. Current

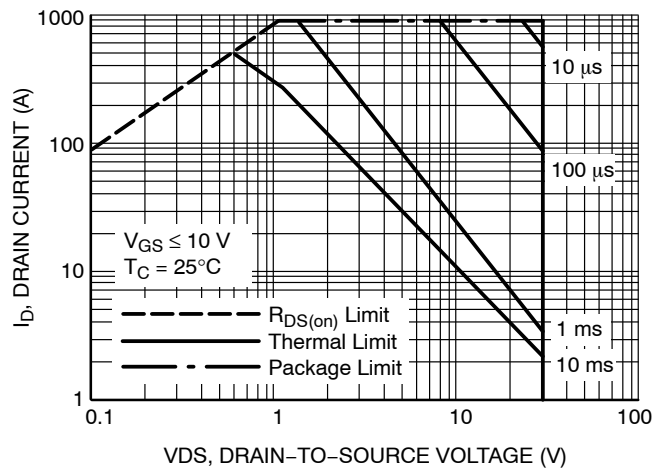


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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TYPICAL CHARACTERISTICS

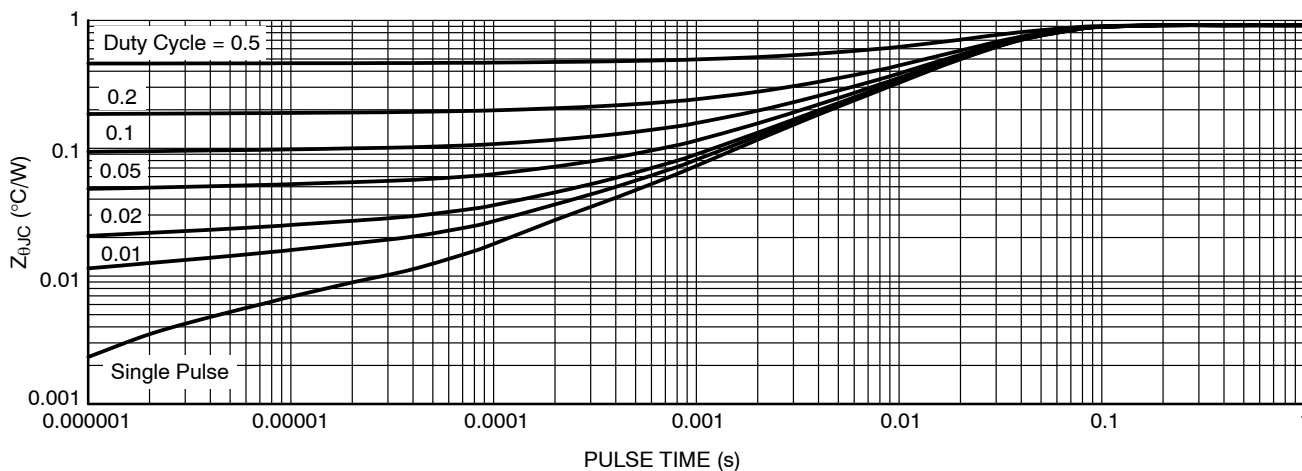


Figure 12. Thermal Resistance

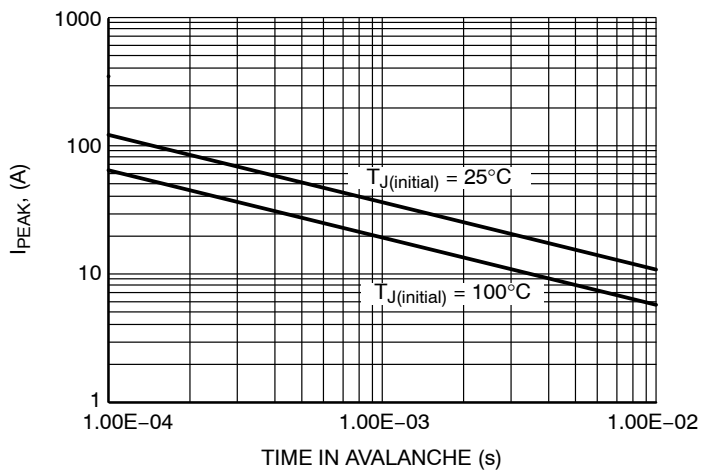


Figure 13. Avalanche Characteristics

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



1
SCALE 2:1

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



- STYLE 1:
1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN

- STYLE 2:
1. ANODE
 2. ANODE
 3. ANODE
 4. NO CONNECT
 5. CATHODE

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN5 5x6, 1.27P (SO-8FL)	PAGE 1 OF 1

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