19-4445; Rev 0; 2/09

EVALUATION KIT AVAILABLE

DC-DC Converter with Integrated Scan Driver, VGL Controller, Op Amp, and LDO for TFT LCD

General Description

The MAX17103 includes a high-performance step-up regulator, a 350mA low-dropout linear regulator, a high-speed operational amplifier, a negative linear regulator controller, and a high-voltage, level-shifting scan driver. The device is optimized for thin-film transistor (TFT) liquid-crystal display (LCD) applications.

The step-up DC-DC converter provides the regulated supply voltage for panel source driver ICs. The high 1.2MHz switching frequency allows the use of ultra-small inductors and ceramic capacitors. The current-mode control architecture provides fast-transient response to pulsed loads typical of source driver loads. The step-up regulator features an adjustable soft-start and an adjustable cycle-by-cycle current limit.

The high-current operational amplifier is designed to drive the LCD backplane (VCOM). The amplifier features high output current (±200mA), fast slew rate (50V/µs), wide bandwidth (12MHz), and rail-to-rail inputs and outputs.

The low-voltage LDO linear regulator has an integrated 0.8Ω pass element and can provide at least 350mA. The output voltage is accurate within ±1%.

The high-voltage, level-shifting scan driver is designed to drive the TFT panel gate drivers. Its three outputs can swing up to 40V (max) to swiftly drive capacitive loads. To save power, the two complementary outputs are designed to allow charge sharing during state changes.

The MAX17103 is available in a 32-pin, 5mm x 5mm, thin QFN package with a maximum thickness of 0.8mm for thin LCD panels.

Applications

Notebook Computer Displays

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17103ETJ+	-40°C to +85°C	32 Thin QFN-EP*
AUO-P1721.14	-40°C to +85°C	32 Thin QFN-EP*

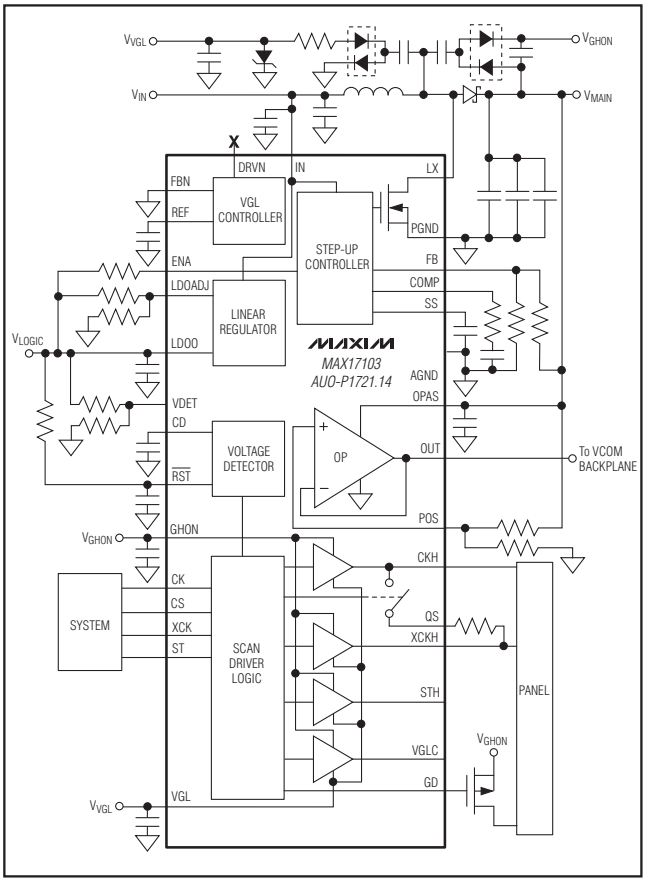
+Denotes lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Pin Configuration appears at end of data sheet.

Features

- **2.3V to 5.5V IN Supply Voltage Range**
- **1.2MHz Current-Mode Step-Up Regulator**
  - **Fast-Transient Response**
  - **High-Accuracy Reference (1%)**
  - **Integrated 16V, 2A, 200mΩ MOSFET**
  - **High Efficiency (> 85%)**
  - **Adjustable Cycle-by-Cycle Current Limit**
- **High-Performance Operational Amplifier**
  - **200mA Output Short-Circuit Current**
  - **50V/µs Slew Rate**
  - **12MHz, -3dB Bandwidth**
- **Low-Dropout Linear Regulator**
  - **High-Accuracy Output Voltage (1.0%)**
- **High-Voltage Drivers with Scan Logic**
  - **+35V to -15V Outputs**
  - **40V (Max) Swing**
- **Linear Regulator Controller for Gate-Off Supply**
- **Thermal-Overload Protection**
- **32-Pin, 5mm x 5mm, Thin QFN Package**

Simplified Operating Circuit



DC-DC Converter with Integrated Scan Driver, VGL Controller, Op Amp, and LDO for TFT LCD

ABSOLUTE MAXIMUM RATINGS

IN, $\overline{RST}$ to AGND .....-0.3V to +7.5V
FB, FBN, CD, ENA, VDET, SS, CS, ST, CK, XCK to AGND.....-0.3V to (V_{IN} + 0.3V)
LDOADJ, LDOO, COMP, REF to AGND.....-0.3V to (V_{IN} + 0.3V)
PGND to AGND .....-0.3V to +0.3V
LX, OPAS to PGND.....-0.3V to +18V
DRVN to AGND.....-20V to (V_{IN} + 0.3V)
GHON to PGND.....-0.3V to +40V
VGL to PGND ..... -20V to +0.3V
GHON to VGL.....-0.3V to +45V
GD to PGND .....-0.3V to (V_{GHON} + 0.3V)
GD to VGHON .....-15V to +0.3V
VGLC, STH, CKH, XCKH.....(-0.3V + V_{VGL}) to (V_{GHON} + 0.3V)
OUT, POS to PGND.....-0.3V to (V_{OPAS} + 0.3V)
POS to OUT .....-7.5V to +7.5V
OUT Maximum Continuous Output Current.....±75mA
GHON, STH, VGL, CKH, and XCKH RMS Current Rating 120mA
LX, PGND RMS Current Rating.....1.6A
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN (derate 24.9mW/°C above +70°C).....1990mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +3V, Circuit of Figure 1, V_{OPAS} = +8.5V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IN Input-Voltage Range		2.3		5.5	V
IN Undervoltage Lockout	V_{IN} rising, typical hysteresis = 150mV	1.80	2.00	2.20	V
IN Standby Current	V_{ENA} = 0, V_{IN} = 5.5V, V_{GHON} = 4V, V_{GL} = 0		0.7	2	mA
GHON Standby Current	V_{ENA} = 0, V_{IN} = 5.5V, V_{GHON} = 4V, V_{GL} = 0		100	200	µA
OPAS Shutdown Current	V_{ENA} = 0, V_{IN} = 5.5V, V_{GHON} = 4V, V_{GL} = 0		10	30	µA
IN Quiescent Current	V_{FB} = 1.3V, LX not switching		1	2.5	mA
	V_{FB} = 1.2V, LX switching		2	4	
Duration to Trigger Fault Condition			160		ms
Thermal Shutdown	Temperature rising		+160		°C
REFERENCE					
REF Output Voltage	No external load	1.227	1.240	1.252	V
REF Load Regulation	0 < I_{LOAD} < 50µA				mV
REF Sink Current	In regulation	-20		+10	µA
STEP-UP REGULATOR					
Output-Voltage Range		V_{IN}		15	V
Frequency		1000	1200	1400	kHz
Oscillator Maximum Duty Cycle		91	94	97	%
FB Regulation Voltage	No load	1.227	1.240	1.252	V
FB Fault Trip Level	Falling edge	1.05	1.10	1.15	V
Overvoltage Protection	OPAS rising (Note 1)	16.5	17	18	V
FB Load Regulation	0 < I_{LOAD} < full load, transient only		-0.5		%
FB Line Regulation	V_{IN} = 2.5V to 5.5V, T_A = +25°C		0.1	0.15	%/V
	V_{IN} = 2.5V to 5.5V, T_A = 0°C to +85°C			0.2	
FB Input Bias Current	V_{FB} = 1.3V, T_A = +25°C		65	200	nA
FB Transconductance	ΔI = ±2.5µA at COMP, FB = COMP	75	160	280	µS
FB Voltage Gain	FB to COMP		700		V/V
LX Current Limit	V_{FB} = 1.2V, duty cycle = 60%, R_{ENA} = 10kΩ, V_{LDOO} = 2.5V	1.6	2	2.4	A

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3V, Circuit of Figure 1, V_{OPAS} = +8.5V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LX On-Resistance	I_{LX} = 1A		0.200	0.500	Ω
LX Leakage Current	V_{LX} = 13.5V, T_A = +25°C		10	20	µA
Current-Sense Transresistance		0.10	0.20	0.30	V/A
Soft-Start Pullup Current		2	4	6	µA
GATE-OFF LINEAR REGULATOR CONTROLLER					
FBN Fault Trip Level	V_{FBN} rising	370	420	470	mV
FBN Regulation Voltage	I_{DRVN} = 100µA	-20		+20	mV
FBN Line-Regulation Error	V_{IN} = 2.5V to 5.5V, I_{DRVN} = 100µA	-6	0	+6	mV
FBN Input Bias Current	V_{FBN} = 0, T_A = +25°C	-200		+200	nA
FBN Effective Load Regulation Error (Transconductance)	V_{DRVN} = -10V, I_{DRVN} = 50µA to 1mA		11	25	mV
DRVN Source Current	V_{FBN} = 300mV, V_{DRVN} = -10V	1	4	10	mA
DRVN Off-Leakage Current	V_{FBN} = 0, V_{DRVN} = -15V, T_A = +25°C		10	20	µA
Startup Delay from V_{FB} = 90%			32		ms
Soft-Start Period			3		ms
GD SWITCH CONTROL					
GD Pulldown Resistor	UVLO or $\overline{RST}$ asserted			100	Ω
GD Pullup Resistor	UVLO and $\overline{RST}$ unasserted			100	Ω
GD Low Voltage Level	UVLO or $\overline{RST}$ asserted, V_{GHON} > 11V	V_{GHON} - 12	V_{GHON} - 11	V_{GHON} - 8	V
GD High Voltage Level	UVLO and $\overline{RST}$ unasserted, V_{GHON} > 8V			V_{GHON}	V
VCOM BUFFER					
Supply Voltage (V_{OPAS})		6		15	V
Input Bias Current	V_{POS} = V_{OPAS}/2, T_A = +25°C	-50		+50	nA
OPAS Supply Current	V_{POS} = V_{OPAS}/2, no load		3	5	mA
Output-Voltage Swing High	I_{OUT} = 100µA	V_{OPAS} - 20	V_{OPAS} - 5		mV
	I_{OUT} = 75mA	V_{OPAS} - 1.5	V_{OPAS} - 1.3		V
Output-Voltage Swing Low	I_{OUT} = 100µA		2	20	mV
	I_{OUT} = 75mA		1.5	1.8	V
Slew Rate	5V pulse at POS; both rising and falling edges	12	50		V/µs
-3dB Bandwidth	R_L = 10kΩ, C_L = 10pF		12		MHz
Short-Circuit Current	Short to V_{OPAS}/2, sourcing and sinking	115	200		mA
Input Offset Voltage		-15		+15	mV
Gain-Bandwidth Product			8		MHz
VOLTAGE DETECTOR					
Minimum V_{IN} Operating Voltage		1.6		5.5	V
VDET Input Bias Current	T_A = +25°C, VDET = 1.3V	-1		+1	µA
VDET Threshold	VDET falling, hysteresis = 50mV	1.078	1.1	1.122	V
Adjustable Delay Time Coefficient (K)	T = 120kΩ	80	120	160	kΩ
$\overline{RST}$ Sink Current	$V_{\overline{RST}}$ = 0.4V	1	8		mA

DC-DC Converter with Integrated Scan Driver, VGL Controller, Op Amp, and LDO for TFT LCD

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3V, Circuit of Figure 1, V_{OPAS} = +8.5V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LEVEL SHIFTERS					
GHON-to-VGL Voltage Range	V_{GHON} - V_{VGL}			40	V
GHON Input-Voltage Range		12		35	V
VGL Input-Voltage Range		-15		-3	V
GHON Supply Current	V_{GHON} = 23V, CK, XCK, ST are low		1	2.1	mA
VGL Supply Current	V_{VGL} = -6V, CK, XCK, ST are low		1	2	mA
CKH, XCKH, STH Output-Voltage Low	I_{OUT} = 10mA (5Ω typ)		V_{VGL} + 0.05	V_{VGL} + 0.25	V
CKH, XCKH, STH Output-Voltage High	I_{OUT} = 10mA (20Ω typ)	V_{GHON} - 0.5	V_{GHON} - 0.2		V
CKH, XCKH, STH Rise Time	C_{LOAD} = 5nF, CS = high, V_{GHON} = 25V, V_{VGL} = -15V, T_A = +25°C		0.75	0.25	µs
	T_A = 0°C to +85°C			2	
CKH, XCKH, STH Fall Time	C_{LOAD} = 5nF, CS = high, V_{GHON} = 25V, V_{VGL} = -15V		0.5	1	µs
CK-to-CKH, XCK-to-XCKH, ST-to-STH, Rising Edge Propagation Delay	C_{LOAD} = 100pF		60		ns
CK-to -CKH, XCK-to-XCKH, ST to STH, Falling Edge Propagation Delay	C_{LOAD} = 100pF		60		ns
CKH, XCKH Maximum Operating Frequency				100	kHz
VGLC Output-Voltage Low	I_{OUT} = 10mA		V_{VGL} + 0.07	V_{VGL} + 0.25	V
VGLC Output-Voltage High	I_{OUT} = 10mA	V_{GHON} - 0.5	V_{GHON} - 0.2		V
CHARGE-SHARING FUNCTION					
QS-to-CKH On-Resistance	V_{GHON} = 24V, V_{VGL} = -6V; V_{CKH} = V_{XCKH} = 10V, CS = low		200	400	Ω
CS-to-CKH/QS Propagation Delay			100		ns
GHON - QS Switch Leakage Current	CS = low, T_A = +25°C			1	mA
LOW-DROPOUT LINEAR REGULATOR					
Dropout Voltage	V_{IN} = 3.3V, V_{LDOADJ} = 1.1V, I_{OUT} = 0.35A		300	500	mV
LDOADJ Feedback Voltage		1.227	1.24	1.252	V
Current Limit	V_{IN} = 3.3V, V_{LDOADJ} = 1.0V	0.4	0.55	0.7	A
LDOADJ Line Regulation	V_{IN} = 2.8V to 5.5V, I_{OUT} = 100mA; V_{LDOO} = 2.5V		0.1	0.3	%/V
LDOADJ Load Regulation	I_{OUT} = 1mA to 300mA, V_{LDOO} = 2.5V		0.2	0.5	%/V
LDOADJ Input Bias Current	V_{LDOADJ} = 1.3V, T_A = +25°C		100	200	nA
DIGITAL INPUTS					
ENA, CS, CK, XCK, ST Input High		1.5			V
ENA, CS, CK, XCK, ST Input Low				0.6	V
CS, ST, CK, XCK Input Current	CK, XCK, ST = V_{IN}, T_A = +25°C	-1		+1	µA

ELECTRICAL CHARACTERISTICS

(V_{IN} = +3V, Circuit of Figure 1, V_{OPAS} = +8.5V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IN Input-Voltage Range	(Note 1)	2.3		5.5	V
IN Undervoltage-Lockout Threshold	V_{IN} rising, typical hysteresis = 150mV	1.80		2.20	V
IN Standby Current	V_{ENA} = 0, V_{IN} = 5.5V, V_{GHON} = 4V, V_{GL} = 0			2	mA
IN Quiescent Current	V_{FB} = 1.3V, LX not switching			2.5	mA
	V_{FB} = 1.2V, LX switching			4	
GHON Standby Current	V_{ENA} = 0, V_{IN} = 5.5V, V_{GHON} = 4V, V_{GL} = 0			200	µA
OPAS Shutdown Current	V_{ENA} = 0, V_{IN} = 5.5V, V_{GHON} = 4V, V_{GL} = 0			30	µA
REFERENCE					
REF Output Voltage	No external load	1.227		1.252	V
REF Load Regulation	0 < I_{LOAD} < 50µA			20	mV
REF Sink Current	In regulation			10	µA
STEP-UP REGULATOR					
Output-Voltage Range		V_{IN}		15	V
Frequency		1000		1400	kHz
Oscillator Maximum Duty Cycle		91		97	%
FB Regulation Voltage	No load, T_A = +25°C to +85°C	1.227		1.252	V
FB Fault Trip Level	Falling edge (Note 2)	1.05		1.15	V
FB Line Regulation	V_{IN} = 2.5V to 5.5V			0.2	%/V
FB Transconductance	ΔI = ±2.5µA at COMP, FB = COMP	75		280	µS
LX Current Limit	V_{FB} = 1.2V, duty cycle = 60%, R_{ENA} = 10kΩ, V_{LDOO} = 2.5V	1.6		2.4	A
LX On-Resistance	I_{LX} = 1A			0.5	Ω
Current-Sense Transresistance		0.10		0.30	V/A
Soft-Start Pullup Current		2		6	µA
GATE-OFF LINEAR-REGULATOR CONTROLLER					
FBN Fault Trip Level	V_{FBN} rising (Note 2)	370		470	mV
FBN Regulation Voltage	I_{DRVN} = 100µA	-20		+20	mV
FBN Line-Regulation Error	V_{IN} = 2.5V to 5.5V, I_{DRVN} = 100µA	-6		+6	mV
FBN Effective Load-Regulation Error (Transconductance)	V_{DRVN} = -10V, I_{DRVN} = 50µA to 1mA			25	mV
DRVN Source Current	V_{FBN} = 300mV, V_{DRVN} = -10V	1		10	mA
GD SWITCH CONTROL					
GD Pulldown Resistor	UVLO or $\overline{RST}$ asserted			100	Ω
GD Pullup Resistor	UVLO and $\overline{RST}$ unasserted			100	Ω
GD Low-Voltage Level	UVLO or $\overline{RST}$ asserted, V_{GHON} > 11V	V_{GHON} - 13.5		V_{GHON} - 8	V
GD High-Voltage Level	UVLO and $\overline{RST}$ unasserted, V_{GHON} > 8V			V_{GHON}	V

DC-DC Converter with Integrated Scan Driver, VGL Controller, Op Amp, and LDO for TFT LCD

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3V, Circuit of Figure 1, V_{OPAS} = +8.5V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCOM BUFFER					
Supply Voltage	V_{OPAS}	6		15	V
OPAS Supply Current	V_{POS} = V_{OPAS}/2, no load			5	mA
Output-Voltage Swing High	I_{OUT} = 100µA	V_{OPAS} - 0.02	V_{OPAS} - 0.005		V
	I_{OUT} = 75mA	V_{OPAS} - 1.5			
Output-Voltage Swing Low	I_{OUT} = 100µA			20	mV
	I_{OUT} = 75mA			1.8	V
Slew Rate		12			V/µs
Short-Circuit Current	Short to V_{OPAS}/2, sourcing	115			mA
	Short to V_{OPAS}/2, sinking	115			
Input Offset Voltage		-15		+15	mV
VOLTAGE DETECTOR					
Operating Voltage		1.6		5.5	V
VDET Input Bias Current	T_A = +25°C	-1		+1	µA
VDET Threshold	VDET falling, hysteresis = 50mV	-2%		+2%	V
Adjustable Delay Time Coefficient K	TD = k(Ω) x C(F)	80		160	kΩ
$\overline{RST}$ Sink Current	$V_{\overline{RST}}$ = 0.4V	1			mA
LEVEL SHIFTERS					
GHON-to-VGL Voltage Range	V_{GHON} - V_{VGL}			40	V
GHON Input-Voltage Range		12		35	V
VGL Input-Voltage Range		-15		-3	V
GHON Supply Current (V_{GHON} = 23V)	CK, XCK, ST are low			2	mA
VGL Supply Current (V_{VGL} = -6V)	CK, XCK, ST are low			2	mA
CKH, XCKH, STH Output-Voltage Low	I_{OUT} = 10mA (7Ω typ)			V_{VGL} + 0.25	V
CKH, XCKH, STH Output-Voltage High	I_{OUT} = 10mA (20Ω typ)	V_{GHON} - 0.5			V
CKH, XCKH, STH Rise Time	C_{LOAD} = 5nF, CS = high, V_{GHON} = 25V, V_{VGL} = -15V			2	µs
CKH, XCKH, STH Fall Time	C_{LOAD} = 5nF, CS = high, V_{GHON} = 25V, V_{VGL} = -15V			1	µs
CKH, XCKH Maximum Operating Frequency				100	kHz
VGLC Output-Voltage Low	I_{OUT} = 10mA			V_{VGL} + 0.25	V
VGLC Output-Voltage High	I_{OUT} = 10mA	V_{GHON} - 0.5			V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3V, Circuit of Figure 1, V_{OPAS} = +8.5V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGE-SHARING FUNCTION					
QS-to-CKH On-Resistance	V_{GHON} = 24V, V_{VGL} = -6V; V_{CKH} = V_{XCKH} = 10V, CS = low			400	Ω
GHON - QS Switch Leakage Current	CS = low			1	mA
LOW-DROPOUT LINEAR REGULATOR					
Dropout Voltage	V_{IN} = 3.3V, V_{LDOADJ} = 1.1V, I_{OUT} = 0.35A			500	mV
LDOADJ Feedback Voltage		1.227		1.252	V
Current Limit	V_{IN} = 3.3V, V_{LDOADJ} = 1.0V	0.4		0.7	A
LDOADJ Line Regulation	V_{IN} = 2.8V to 5.5V, I_{OUT} = 100mA; V_{LDOO} = 2.5V			0.3	%/V
LDOADJ Load Regulation	I_{OUT} = 1mA to 300mA, V_{LDOO} = 2.5V			0.5	%/V
DIGITAL INPUTS					
ENA, CS, CK, XCK, ST Input High Level		1.5			V
ENA, CS, CK, XCK, ST Input Low Level				0.6	V
CS, ST, CK, XCK Input Current	CK, XCK, ST = V_{IN}, T_A = +25°C	-1		+1	µA

Note 1: If V_{OPAS} exceeds the overvoltage threshold, the part stops switching. As soon as V_{OPAS} falls below the overvoltage theshold, LX is allowed to resume switching.

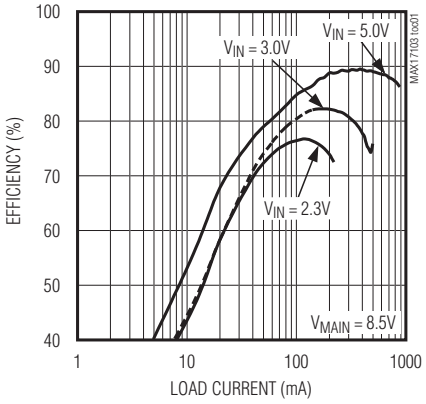
Note 2: T_A = -40°C specifications are guaranteed by design, not production tested.

DC-DC Converter with Integrated Scan Driver, VGL Controller, Op Amp, and LDO for TFT LCD

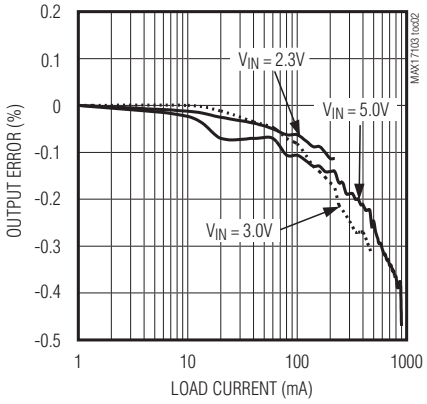
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

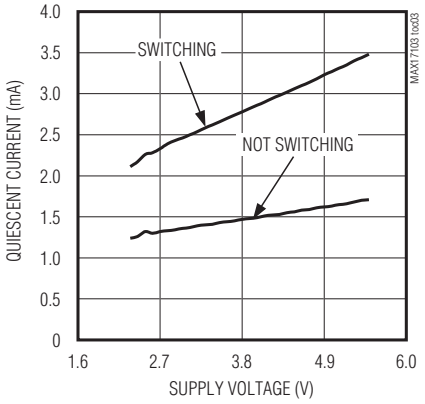
STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT



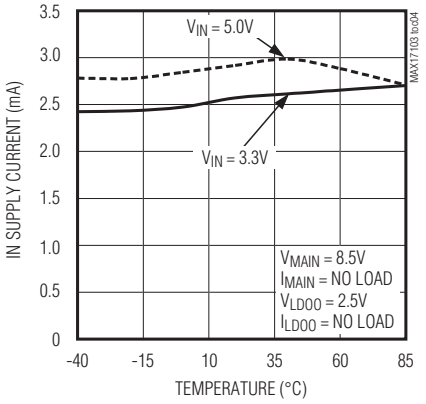
STEP-UP REGULATOR OUTPUT LOAD REGULATION vs. LOAD CURRENT



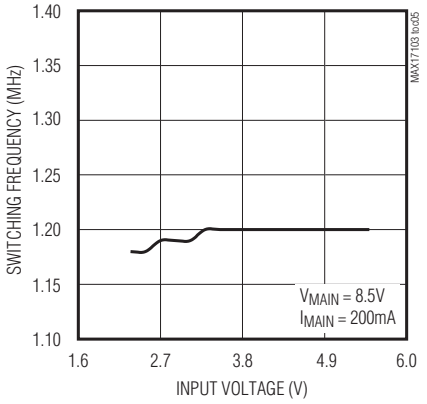
IN-SUPPLY QUIESCENT CURRENT vs. IN SUPPLY VOLTAGE



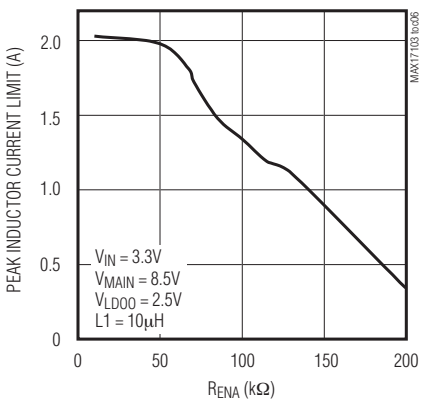
IN-SUPPLY CURRENT vs. TEMPERATURE



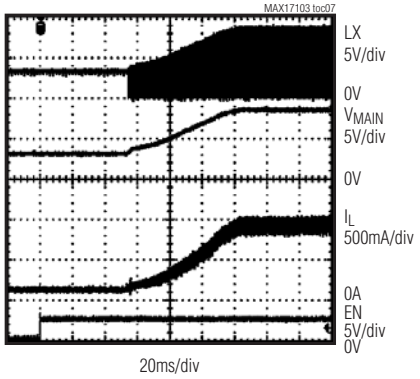
STEP-UP CONVERTER SWITCHING FREQUENCY vs. INPUT VOLTAGE



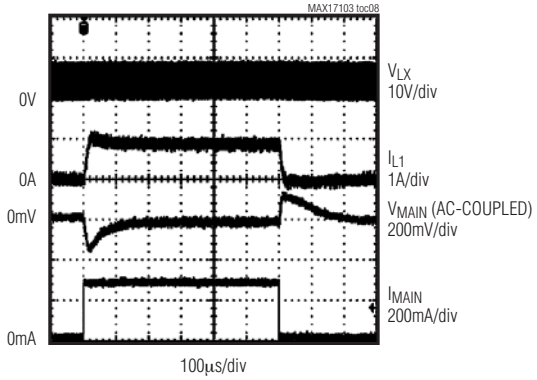
STEP-UP CONVERTER PEAK INDUCTOR CURRENT LIMIT vs. R_{ENA}



STEP-UP REGULATOR HEAVY-LOAD SOFT-START



STEP-UP REGULATOR LOAD-TRANSIENT RESPONSE (20mA TO 300mA)

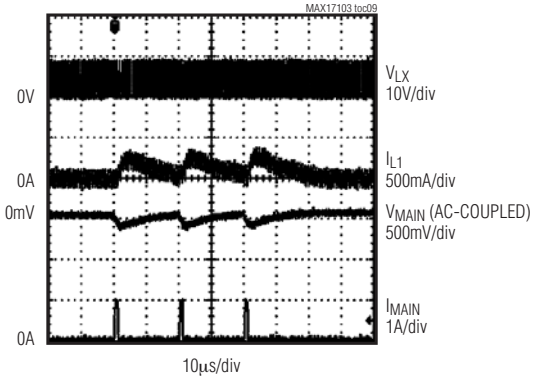


DC-DC Converter with Integrated Scan Driver, VGL Controller, Op Amp, and LDO for TFT LCD

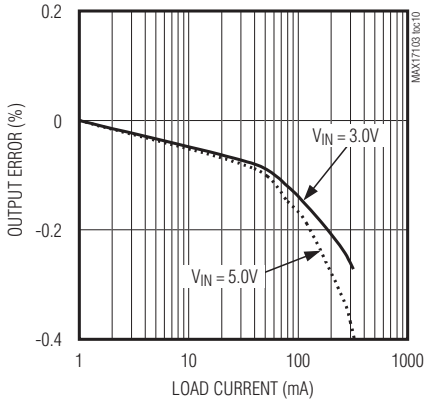
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

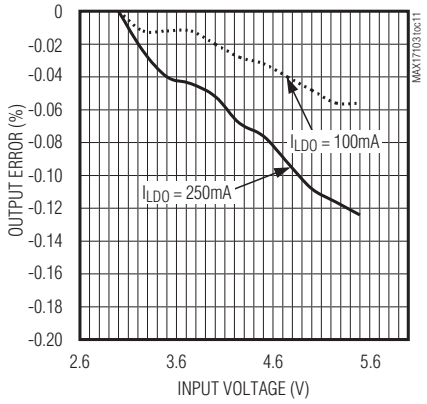
STEP-UP REGULATOR PULSED LOAD-TRANSIENT RESPONSE (20mA TO 1A)



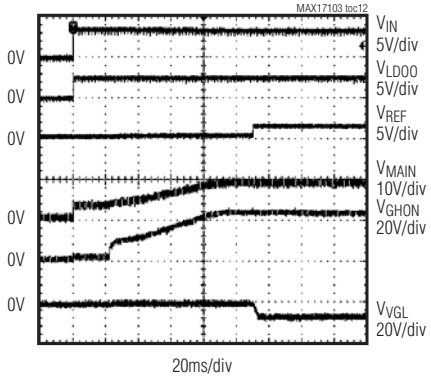
LDO OUTPUT LOAD REGULATION vs. LOAD CURRENT



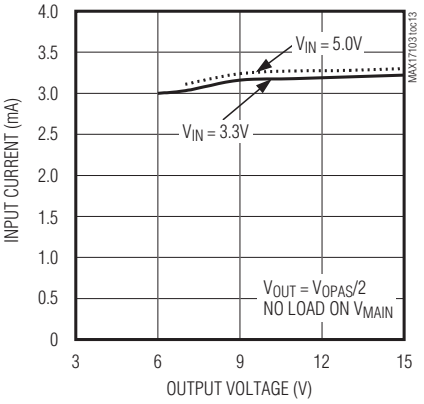
LDO LINE REGULATION vs. INPUT VOLTAGE



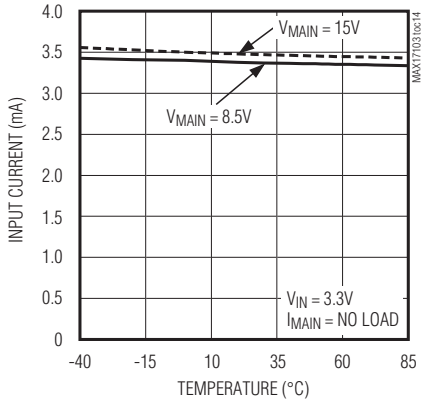
POWER-UP SEQUENCE



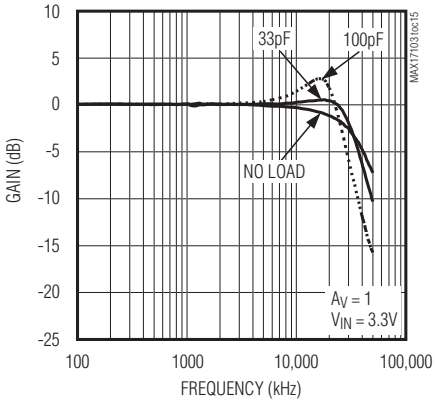
OPAS SUPPLY CURRENT vs. OPAS SUPPLY VOLTAGE



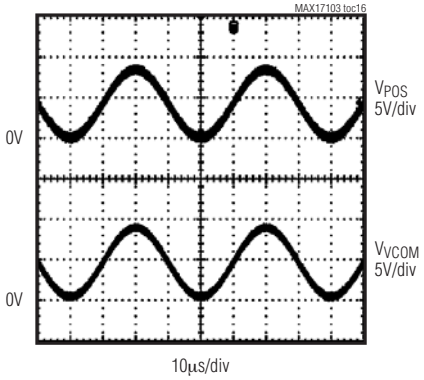
OPAS SUPPLY CURRENT vs. TEMPERATURE



OPERATIONAL AMPLIFIER FREQUENCY RESPONSE



OPERATIONAL AMPLIFIER RAIL-TO-RAIL INPUT/OUTPUT WAVEFORMS

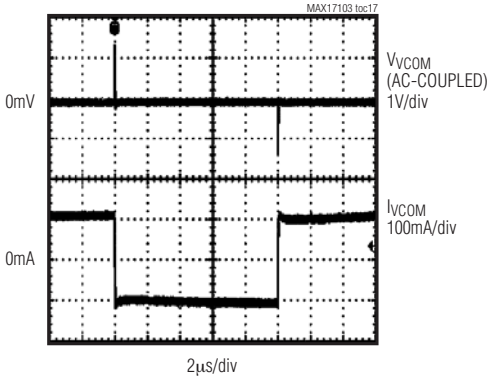


DC-DC Converter with Integrated Scan Driver, VGL Controller, Op Amp, and LDO for TFT LCD

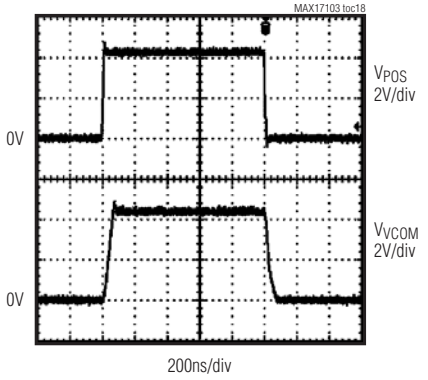
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

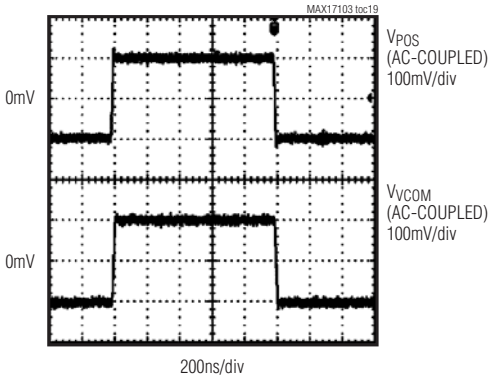
OPERATIONAL AMPLIFIER LOAD-TRANSIENT RESPONSE



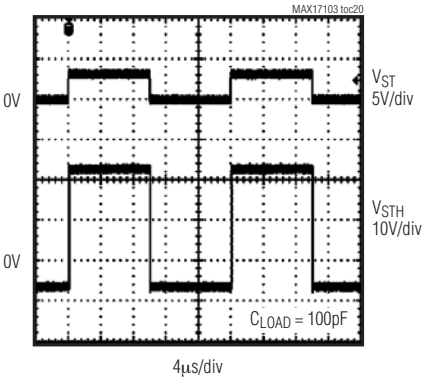
OPERATIONAL AMPLIFIER LARGE-SIGNAL STEP RESPONSE



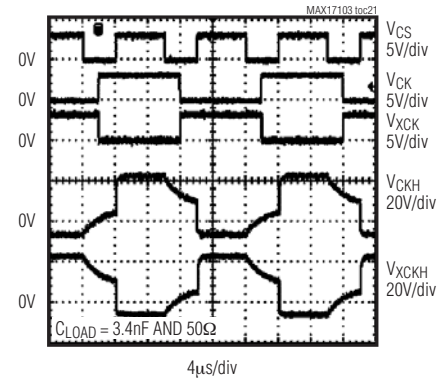
OPERATIONAL AMPLIFIER SMALL-SIGNAL STEP RESPONSE



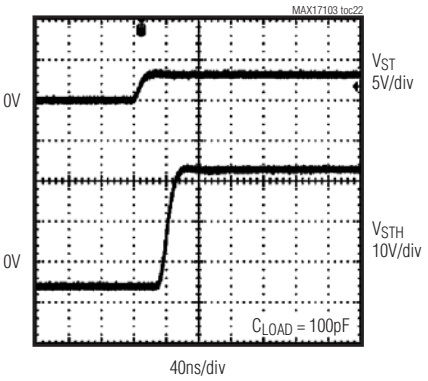
STH OUTPUT WAVEFORM WITH LOGIC INPUT



CKH AND XCKH OUTPUT WAVEFORMS WITH LOGIC INPUT



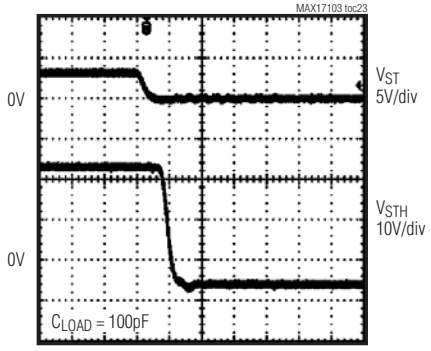
STH RISING EDGE PROPAGATION DELAY



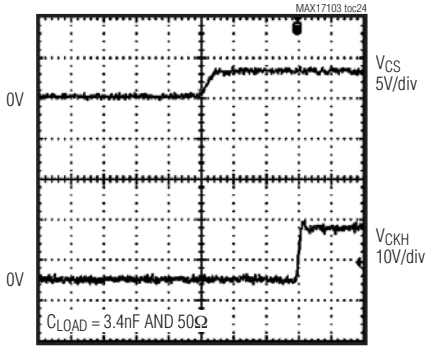
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

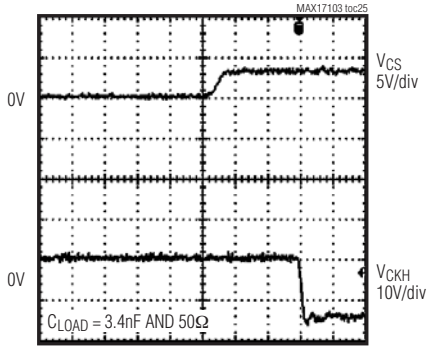
STH FALLING EDGE PROPAGATION DELAY



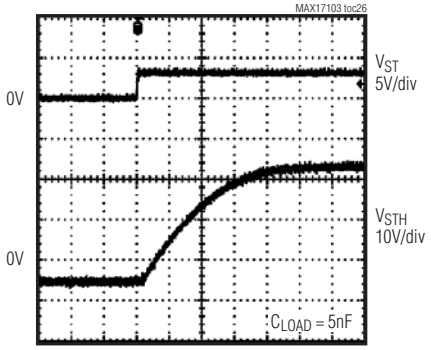
CS/CKH RISING EDGE PROPAGATION DELAY



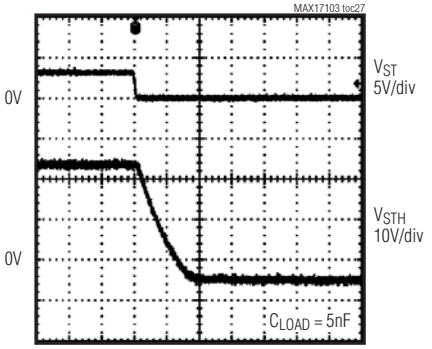
CS/CKH FALLING EDGE PROPAGATION DELAY



SCAN DRIVER OUTPUT RISE TIME



SCAN DRIVER OUTPUT FALL TIME



DC-DC Converter with Integrated Scan Driver, VGL Controller, Op Amp, and LDO for TFT LCD

Pin Description

PIN	NAME	FUNCTION
1	OPAS	Operational Amplifier Supply Input. Connect to V_{MAIN} (Figure 1) and bypass to AGND with a 0.1µF or greater ceramic capacitor.
2	POS	Operational Amplifier Noninverting Input
3	CS	Charge-Sharing Control Input. Charge sharing between the capacitive loads of CKH and XCKH occurs when CS is low.
4	XCK	Level-Shifter Input Signal. The XCK input controls the high-voltage XCKH output while CS is high.
5	CK	Level-Shifter Input Signal. The CK input controls the high-voltage CKH output while CS is high.
6	ST	Level-Shifter Input Signal. The ST input controls the high-voltage STH output.
7	GHON	Gate-On Supply. GHON is the positive supply voltage for the CKH, XCKH, STH, and VGLC high-voltage scan driver outputs. Bypass to PGND with a minimum of 0.1µF ceramic capacitor.
8	STH	Start Pulse Level-Shifter Output
9	CKH	Level-Shifter Output. Whenever CS is high, CKH toggles between its high state (connected to GHON) and its low state (connected to VGL) as commanded by the CK input. Whenever CS is low, the CKH and XCKH drivers are high impedance and the capacitive loads attached to their outputs are connected together through an internal switch between CK and QS, and an external resistor connected between the QS and XCKH (R_{CS}) to enable charge sharing between the two capacitive loads.
10	QS	Charge-Sharing Connection. Connect an external resistor between QS and XCKH.
11	XCKH	Level-Shifter Output. Whenever CS is high, XCKH toggles between its high state (connected to GHON) and its low state (connected to VGL) as commanded by the XCK input. Whenever CS is low, the CKH and XCKH drivers are high impedance and the capacitive loads attached to their outputs are connected together through an internal switch between CK and QS, and an external resistor connected between the QS and XCKH (R_{CS}) to enable charge sharing between the two capacitive loads.
12	VGLC	VGL Charge-Sharing Voltage Output
13	VGL	Gate-Off Supply. VGL is the negative supply voltage for the CKH, XCKH, STH, and VGLC high-voltage driver outputs. Bypass to PGND with a minimum of 1µF ceramic capacitor.
14	N.C.	No Connection
15	GD	Power-Off Sequence Control Output
16	$\overline{RST}$	Voltage Detector Open-Drain Output
17	REF	Reference Bypass Terminal. Bypass REF to AGND with a minimum of 0.22µF capacitor close to the pins.
18	FBN	Gate-Off Linear-Regulator Feedback Input. Connect FBN to the center of a resistive voltage-divider between the regulator output and REF to set the gate-off linear regulator output voltage.
19	DRVN	Gate-Off Linear-Regulator Base Drive. Open drain of an internal p-channel MOSFET. Connect DRVN to the base of an external npn pass transistor.
20	CD	Voltage-Detector $\overline{RST}$ Delay Set. Connect a capacitor to the CD pin to program the $\overline{RST}$ delay according to t_{DELAY} = 120kΩ x C_{CD} (F).

Pin Description (continued)

PIN	NAME	FUNCTION
21	VDET	Voltage Detector Input
22	SS	Step-Up Regulator Soft-Start Control
23	COMP	Compensation Pin for Error Amplifier. Connect a series RC from this pin to AGND. Typical values are 56kΩ and 1000pF.
24	FB	Step-Up Regulator Feedback Pin. Reference voltage is 1.24V nominal. Connect an external resistor-divider midpoint to FB and minimize trace area. Set V_{MAIN} according to V_{MAIN} = 1.24V (1 + R1/R2).
25	PGND	Power Ground. Source connection of the internal step-up regulator power switch.
26	LX	Switching Node. Connect inductor/catch diode here and minimize trace area for lowest EMI.
27	ENA	Chip-Enable Control and Overcurrent Protection (OCP) Set Input. When ENA = low, the step-up converter and op amp are disabled, but the LDO remains active and the level-shifter outputs are high impedance.
28	IN	Step-Up Regulator and Low-Dropout Regulator Supply Pin. Bypass IN to AGND with a 1µF or greater ceramic capacitor.
29	LDOO	Internal Linear Regulator Output. Bypass LDOO to AGND with a 1µF capacitor.
30	LDOADJ	Linear Regulator Feedback Input. Reference voltage is 1.24V nominal.
31	AGND	Analog Ground
32	OUT	Operational Amplifier Output
—	EP	Exposed Backside Pad. Connected to AGND.

DC-DC Converter with Integrated Scan Driver, VGL Controller, Op Amp, and LDO for TFT LCD

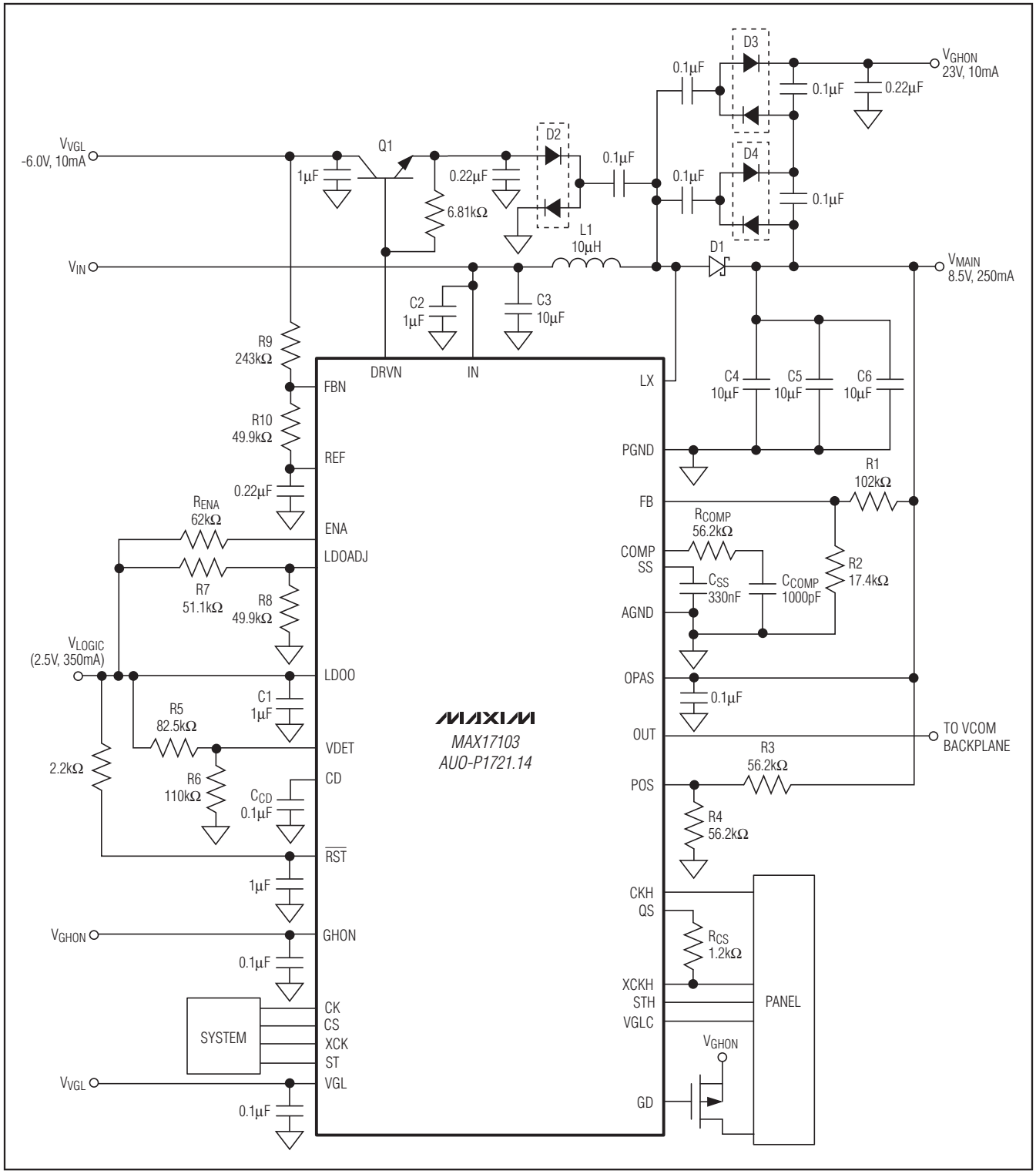


Figure 1. MAX17103 Typical Operating Circuit

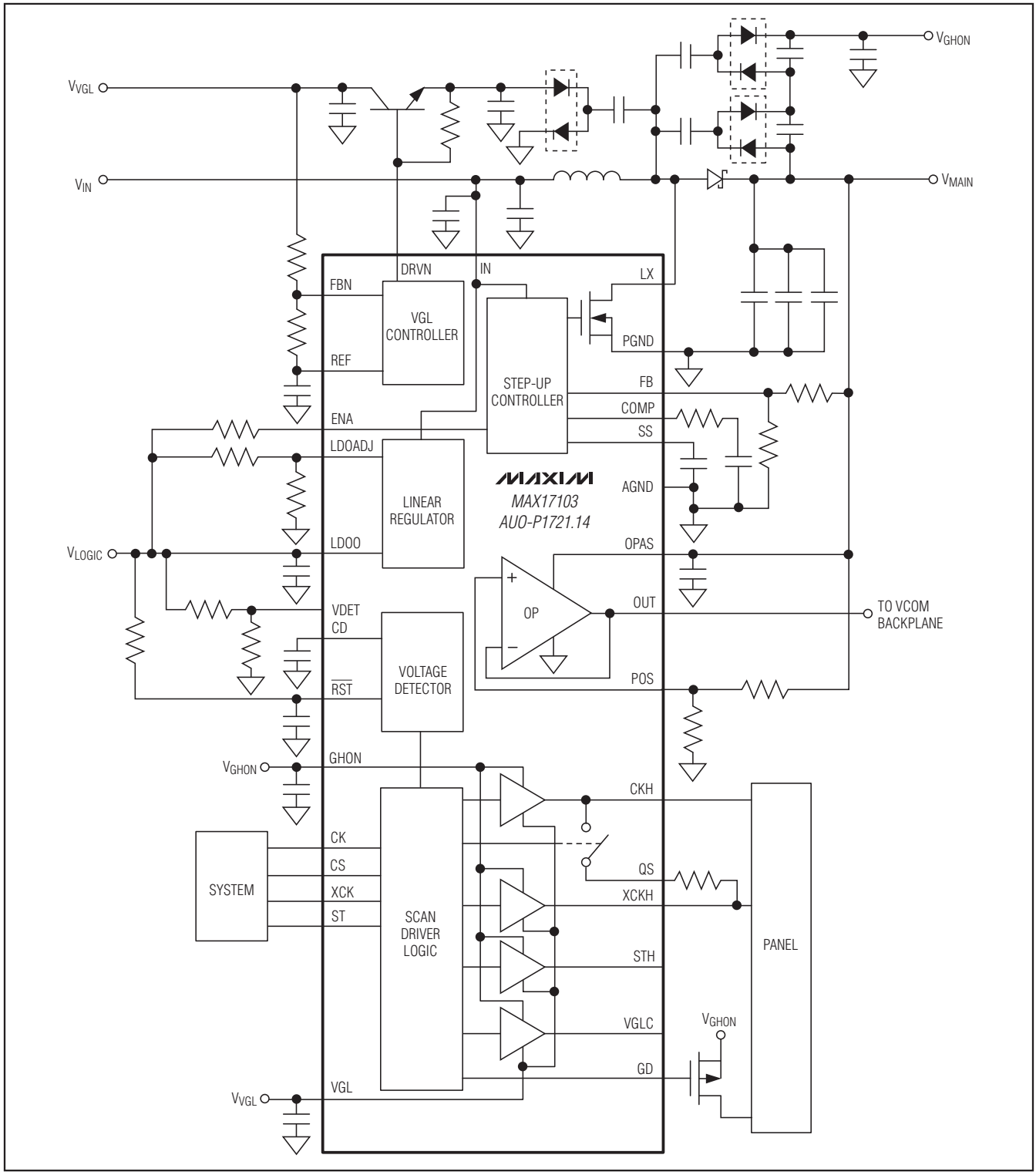


Figure 2. MAX17103 Functional Diagram

DC-DC Converter with Integrated Scan Driver, VGL Controller, Op Amp, and LDO for TFT LCD

Typical Application Circuit

The MAX17103 typical application circuit (Figure 1) generates a +8.5V source-driver supply and approximately +23V and -6V gate-driver supplies for TFT displays. The input-voltage range for the IC is from +2.3V to +5.5V, but the circuit in Figure 1 is designed to run from 2.5V to 3.6V. Table 1 lists the recommended components and Table 2 lists the component suppliers.

Table 1. Component List

DESIGNATION	DESCRIPTION
C1, C2	1µF ±10%, 16V X5R ceramic capacitors (0603) Murata GRM188R61C105K TDK C1608X5R1C105K
C3	10µF ±10%, 10V X5R ceramic capacitor (0805) TDK C2012X5R1A106K Murata GRM21BR61A106K
C4, C5, C6	10µF ±10%, 16V X5R ceramic capacitors (1206) Taiyo Yuden EMK316BJ106KL Murata GRM31CR61C106K
D1	1A, 30V Schottky diode (S-Flat) Central CMMSH1-40 Nihon EP10QY03 Toshiba CRS02(TE85L)
D2, D3, D4	200mA, 100V dual diodes (SOT23) Fairchild MMBD4148SE Central CMPD7000
L1	10µH, 1.85A, 74.4mΩ inductor (6mm x 6mm x 3mm) Sumida CDRH5D28RHPNP-100M
Q1	npn surface-mount transistor (SOT23) Diodes Inc. MMBT3904 Fairchild MMBT3904

Table 2. Component Suppliers

SUPPLIER	WEBSITE
Central Semiconductor Corp.	www.centralsemi.com
Diodes Inc.	www.diodes.com
Fairchild Semiconductor	www.fairchildsemi.com
Murata Electronics North America, Inc.	www.murata-northamerica.com
Nihon Inter Electronics Corp.	www.niec.co.jp
Sumida Corp.	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK Corp.	www.component.tdk.com
Toshiba America Electronic Components, Inc.	www.toshiba.com/taec

Detailed Description

The MAX17103 includes a high-performance, step-up regulator, a 350mA low-dropout (LDO) linear regulator, a high-speed operational amplifier, a negative linear-regulator controller, and a high-voltage, level-shifting scan driver. Figure 2 shows the MAX17103 functional diagram.

Step-Up Regulator

The step-up regulator employs a peak-current-mode control architecture with a fixed 1.2MHz switching frequency that maximizes loop bandwidth and provides a fast-transient response to pulsed loads found in source drivers of TFT LCD panels. The high switching frequency allows the use of low-profile inductors and ceramic capacitors to minimize the thickness of LCD panel designs. The integrated high-efficiency MOSFET reduces the number of external components required. The output voltage can be set from V_{IN} to 15V with an external resistive voltage-divider.

The regulator controls the output voltage and the power delivered to the output by modulating the duty cycle (D) of the internal power MOSFET in each switching cycle. The duty cycle of the MOSFET is approximated by:

$$D \approx \frac{V_{MAIN} - V_{IN}}{V_{MAIN}}$$

Figure 3 shows the block diagram of the step-up regulator. An error amplifier compares the signal at FB to 1.24V and changes the COMP output. The voltage at COMP determines the current trip point each time the internal MOSFET turns on. As the load varies, the error amplifier sources or sinks current to the COMP output accordingly to produce the inductor peak current necessary to service the load. To maintain stability at high duty cycles, a slope compensation signal is summed with the current-sense signal.

On the rising edge of the internal clock, the controller sets a flip-flop, turning on the n-channel MOSFET and applying the input voltage across the inductor. The current through the inductor ramps up linearly, storing energy in its magnetic field. Once the sum of the current-feedback signal and the slope compensation exceed the COMP voltage, the controller resets the flip-flop and turns off the MOSFET. Since the inductor current is continuous, a transverse potential develops across the inductor that turns on the diode (D1). The voltage across the inductor then becomes the difference between the output voltage and the input voltage. This discharge condition forces the current through the inductor to ramp back down, transferring the energy stored in the magnetic field to the output capacitor and the load. The MOSFET remains off for the rest of the clock cycle.

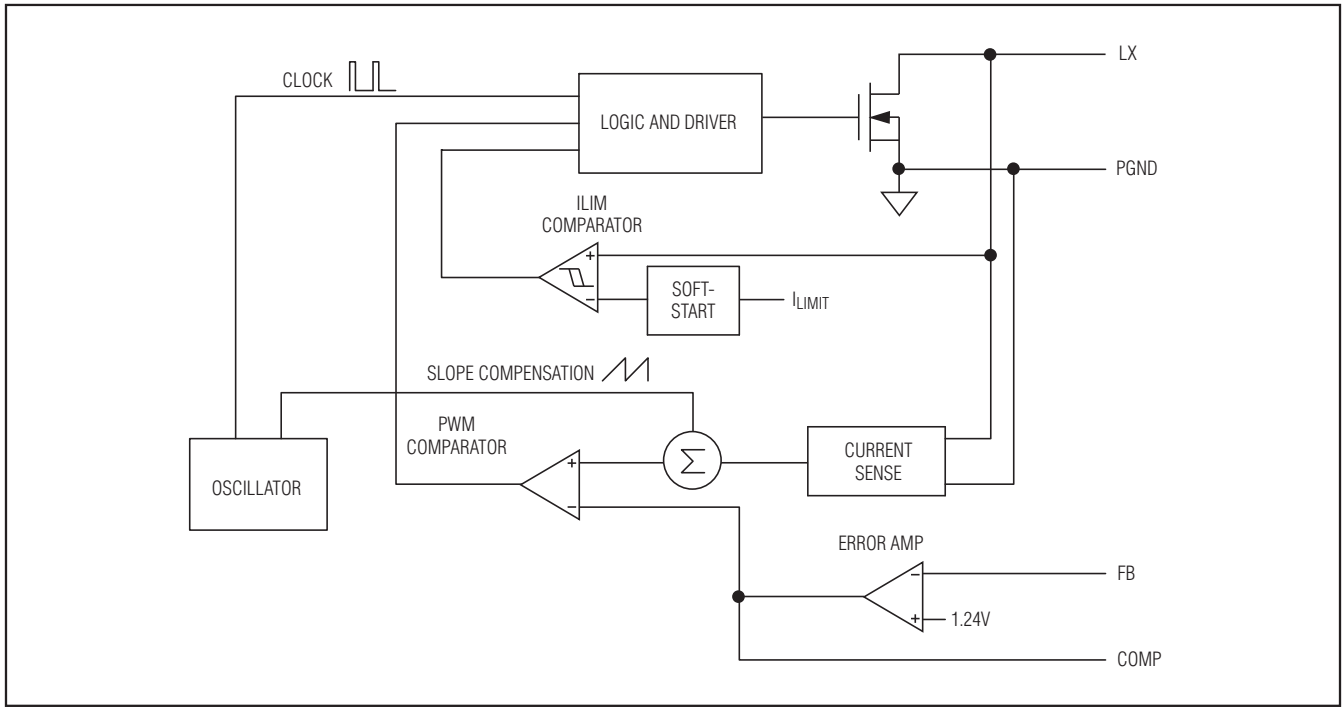


Figure 3. Step-Up Regulator Block Diagram

Undervoltage Lockout (UVLO)

The UVLO circuit compares the input voltage at IN with the UVLO threshold (2.0V typ) to ensure that the input voltage is high enough for reliable operation. The 150mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO rising threshold, startup begins. When the input voltage falls below the UVLO falling threshold, the controller turns off the main step-up regulator, the reference, the operational amplifier, and negative linear-regulator controller.

Overcurrent Protection

The step-up regulator features an adjustable cycle-by-cycle current limit. The inductor current is sensed through the LX switch during the LX switch on-time. If the peak inductor current rises above the current-limit threshold set by R_{ENA}, the LX switch immediately turns off until the next switching cycle, effectively limiting the peak inductor current each cycle.

Soft-Start

The soft-start feature effectively limits the inrush current during startup by linearly ramping up the step-up regulator's peak switch current limit. The soft-start period terminates when either the output voltage reaches regulation or full current limit is reached. The soft-start capacitor (C_{SS}) is charged with a 4mA (typ) current source such that a full current limit is reached when voltage across C_{SS} reaches 1.24V.

Fault Protection

The MAX17103 monitors OPAS for an overvoltage condition. If the OPAS voltage is above 17V (typ), the MAX17103 disables the gate driver of the step-up regulator and prevents the internal MOSFET from switching. The OPAS overvoltage condition does not set the fault latch.

Anytime after the boost soft-start period, if V_{FB} falls below 1.1V (typ) or if V_{FBN} rises above 420mV (typ) for more than 160ms (typ), the controller turns off all outputs, except LDOO and REF, until the input voltage is cycled off then on again.

DC-DC Converter with Integrated Scan Driver, VGL Controller, Op Amp, and LDO for TFT LCD

Operational Amplifier

The MAX17103 has an operational amplifier that is typically used to drive the LCD backplane (VCOM) or the gamma-correction-divider string. The operational amplifier features ±200mA output short-circuit current, 12V/µs (min) slew rate, and 12MHz (typ) bandwidth. While the op amp is a rail-to-rail input and output design, its accuracy is significantly degraded for input voltages within 1V of its supply rails (OPAS and AGND).

Short-Circuit Current Limit

The operational amplifier limits short-circuit current to approximately ±200mA if the output is directly shorted to OPAS or to AGND. If the short-circuit condition persists, the junction temperature of the IC rises until it reaches the thermal-shutdown threshold (+160°C typ). Once the junction temperature reaches the thermal-shutdown threshold, an internal thermal sensor immediately shuts down all outputs until the input voltage is cycled off then on again.

Driving Pure Capacitive Loads

The operational amplifier is typically used to drive the LCD backplane (VCOM) or the gamma-correction divider string. The LCD backplane consists of a distributed series capacitance and resistance, a load that can be easily driven by the operational amplifier. However, if the operational amplifier is used in an application with a pure capacitive load, steps must be taken to ensure stable operation. As the operational amplifier's capacitive load increases, the amplifier's bandwidth decreases and gain peaking increases. A 5Ω to 50Ω small resistor placed between VCOM and the capacitive load reduces peaking, but also reduces the gain. An alternative method of reducing peaking is to place a series RC network (snubber) in parallel with the capacitive load. The RC network does not continuously load the output or reduce the gain. Typical values of the resistor are between 100Ω and 200Ω and the typical value of the capacitor is 10pF.

High-Voltage Level-Shifting Scan Driver

The MAX17103 includes a high-voltage (40V) level-shifting scan driver that includes logic functions necessary to drive row driver functions on the panel glass (Figure 4). The driver outputs (XCK, CKH, and STH) swing between their power-supply rails (GHON and VGL) according to the input logic levels on the block's inputs (CK, XCK, CS, and ST) and by internal logic used during power-up and power-down. CKH and XCKH are normally complementary scan-clock outputs and STH is the output scan start signal.

The state of the CKH, XCKH, and STH scan-driver outputs and the internal charge-sharing switch (SW_{CS}) shown in Figure 4 are determined by the input logic levels CK, XCK, CS, and ST as shown in Tables 3 and 4.

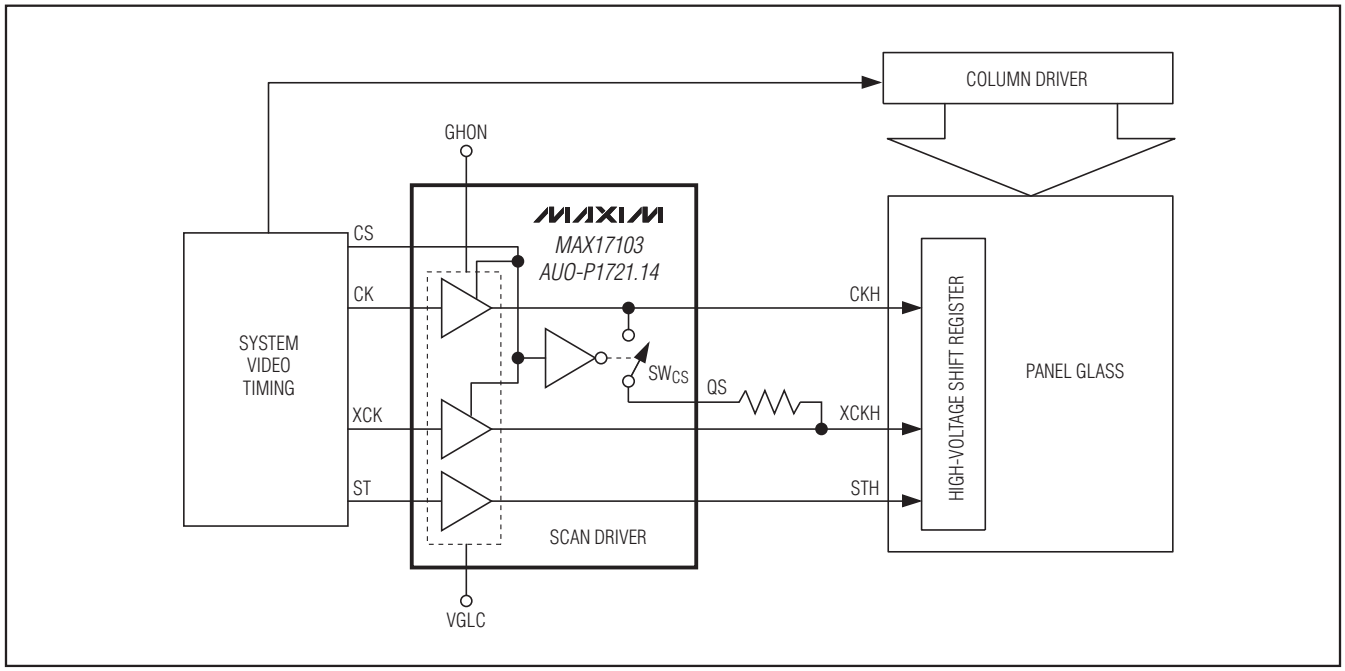


Figure 4. Scan Driver System Diagram

Except during power-up and power-down, the CKH and XCKH outputs are determined by the state of their corresponding inputs (CK and XCK) while the CS input is high. While the CS input is low, the CKH and XCKH driver outputs are high impedance regardless of the state of their corresponding inputs and the charge-sharing switch (SW_{CS}) is closed, connecting the CKH and XCKH outputs together to allow charge sharing between the capacitive loads connected to the two outputs.

During power-up, until V_{MAIN} has exceeded 90% of its regulation voltage for more than 64ms, the CKH and XCKH driver outputs are driven toward V_{VGL} if their corresponding inputs are driven low, or the CKH and XCKH driver outputs become high impedance if their corresponding inputs are driven high. Also, SWCS remains open regardless of the state of the CS input until V_{MAIN} has exceeded 90% of its regulation voltage for more than 64ms.

During power-down, V_{IN} or V_{LDO} is monitored at VDET by the voltage detector (see the *Voltage Detector* section). Once either V_{VDET} falls below 1.1V or V_{IN} falls below 2.0V (typ), the CKH and XCK outputs are driven to V_{GHON} regardless of the state of the CK and XCK inputs to discharge the panel.

The STH driver output is determined by the ST input except during power-down. During power-down, if V_{MAIN} has exceeded 90% of its regulation voltage for more than 64ms prior to the power-down, the STH output goes high impedance during the power-down once either V_{VDET} falls below 1.1V or V_{IN} falls below 2.0V (typ).

Table 3. STH Logic

CONDITIONS		INPUT	OUTPUT
V_{MAIN} has exceeded 90% of its regulation voltage for more than 64ms	V_{VDET} falls below 1.1V or V_{IN} falls below 2.0V	ST	STH
No	X	L	VGL
No	X	H	GHON
Yes	No	L	VGL
Yes	No	H	GHON
Yes	Yes	X	High-Z

H = High, L = Low, High-Z = High impedance, X = Don't care.

Table 4. CKH, XCKH, and SWCS Logic

CONDITIONS		INPUTS			OUTPUTS		
V_{MAIN} has exceeded 90% of its regulation voltage for more than 64ms	V_{VDET} falls below 1.1V or V_{IN} falls below 2.0V	CS	CK	XCK	SW_{CS}	CKH	XCKH
No	X	X	L	L	Open	VGL	VGL
No	X	X	L	H	Open	VGL	High-Z
No	X	X	H	L	Open	High-Z	VGL
No	X	X	H	H	Open	High-Z	High-Z
Yes	No	L	X	X	Closed	High-Z	High-Z
Yes	No	H	L	L	Open	VGL	VGL
Yes	No	H	L	H	Open	VGL	GHON
Yes	No	H	H	L	Open	GHON	VGL
Yes	No	H	H	H	Open	GHON	GHON
Yes	Yes	X	X	X	Open	GHON	GHON

H = High, L = Low, High-Z = High impedance, X = Don't care.

DC-DC Converter with Integrated Scan Driver, VGL Controller, Op Amp, and LDO for TFT LCD

The CK and XCK inputs are normally configured to drive the CKH and XCKH outputs complementary as shown in Figure 5. The CS input is normally configured to be driven low for a period of time that overlaps the CK and XCK input transitions. While CS is low, the CKH and XCKH outputs are high impedance and the internal charge-sharing switch (SW_{CS}) is closed such that charge is transferred from one load capacitance to the other load capacitance through an external resistor connected between QS and XCKH (see Figure 4). This transfer of charge allows CKH and XCKH to complete part of their transitions between the VGL and GHON power rails without drawing power from the power rails during this portion of the transition. This reduces the total power required from GHON and VGL to complete the remainder of the outputs' transitions.

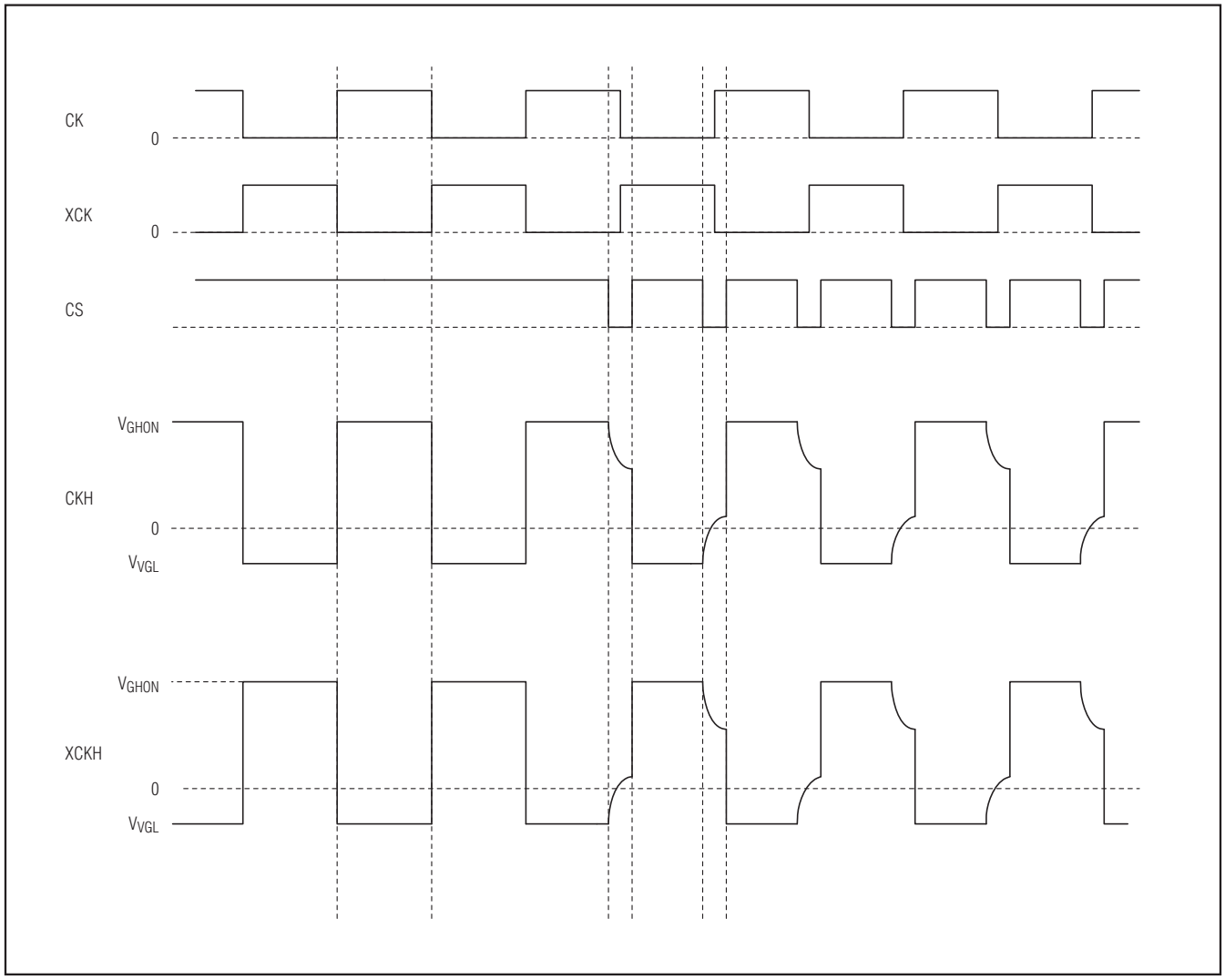


Figure 5. Scan Driver System Timing Utilizing Charge Sharing Between the CKH and XCKH Outputs

VGLC and GD

During power-up, the VGLC level-shifter output is high impedance until V_{MAIN} has exceeded 90% of its regulation voltage for more than 64ms, then is driven to VGL until power-down. During power-down, once either VDET falls below 1.1V (see the *Voltage Detector* section) or V_{IN} falls below 2.0V (typ), VGLC is driven to GHON and GD is pulled low to turn on an external p-channel MOSFET connected between GHON and the panel.

Table 5. VGLC and GD Logic

CONDITIONS		OUTPUTS	
V_{MAIN} has exceeded 90% of its regulation voltage for more than 64ms	V_{VDET} falls below 1.1V or V_{IN} falls below 2.0V	VGLC	GD
No	X	High-Z	GHON
Yes	No	VGL	GHON
Yes	Yes	GHON	GHON - 11V (typ)

X = Don't care, High-Z = High impedance.

Voltage Detector

The voltage detector monitors either V_{IN} or V_{LDOO} to generate a logic-low system reset signal ($\overline{RST}$) and to discharge the panel once the voltage being monitored falls below a desired threshold. The voltage being monitored is sensed through a resistor-divider whose midpoint is connected to VDET. Once V_{VDET} falls below 1.1V, $\overline{RST}$ is immediately pulled low and the panel is discharged by driving the level-shifter outputs CKH, XCKH, and VGLC to V_{GHON}, and by pulling GD low to turn on an external MOSFET connected between GHON and the panel. At power-up, $\overline{RST}$ is held low by the voltage detector such that $\overline{RST}$ is not released until a time delay set by C_{CD} passes after VDET has reached 1.15V (1.1V + 50mV hysteresis).

Figure 6 shows the voltage-detector configuration that is also used in the typical application circuit (Figure 1). Figure 7 shows the power-up and power-down voltage-detector timing of the configuration used in Figure 6.

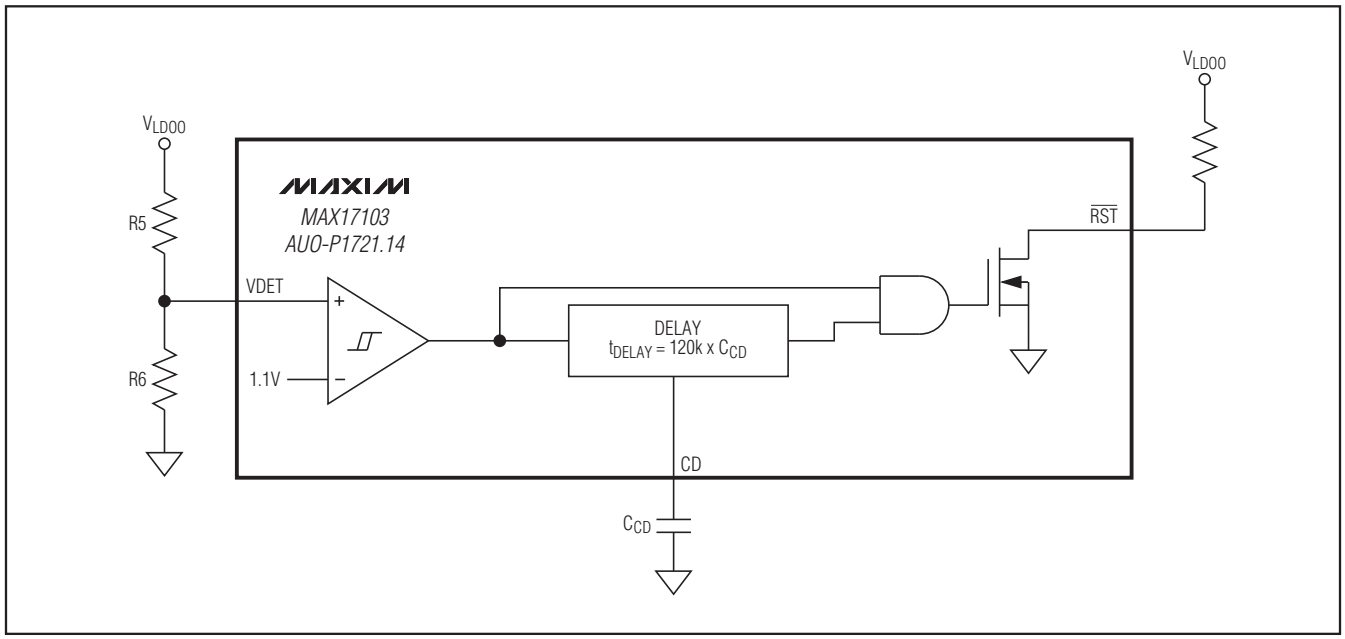


Figure 6. Typical Voltage-Detector Configuration

DC-DC Converter with Integrated Scan Driver, VGL Controller, Op Amp, and LDO for TFT LCD

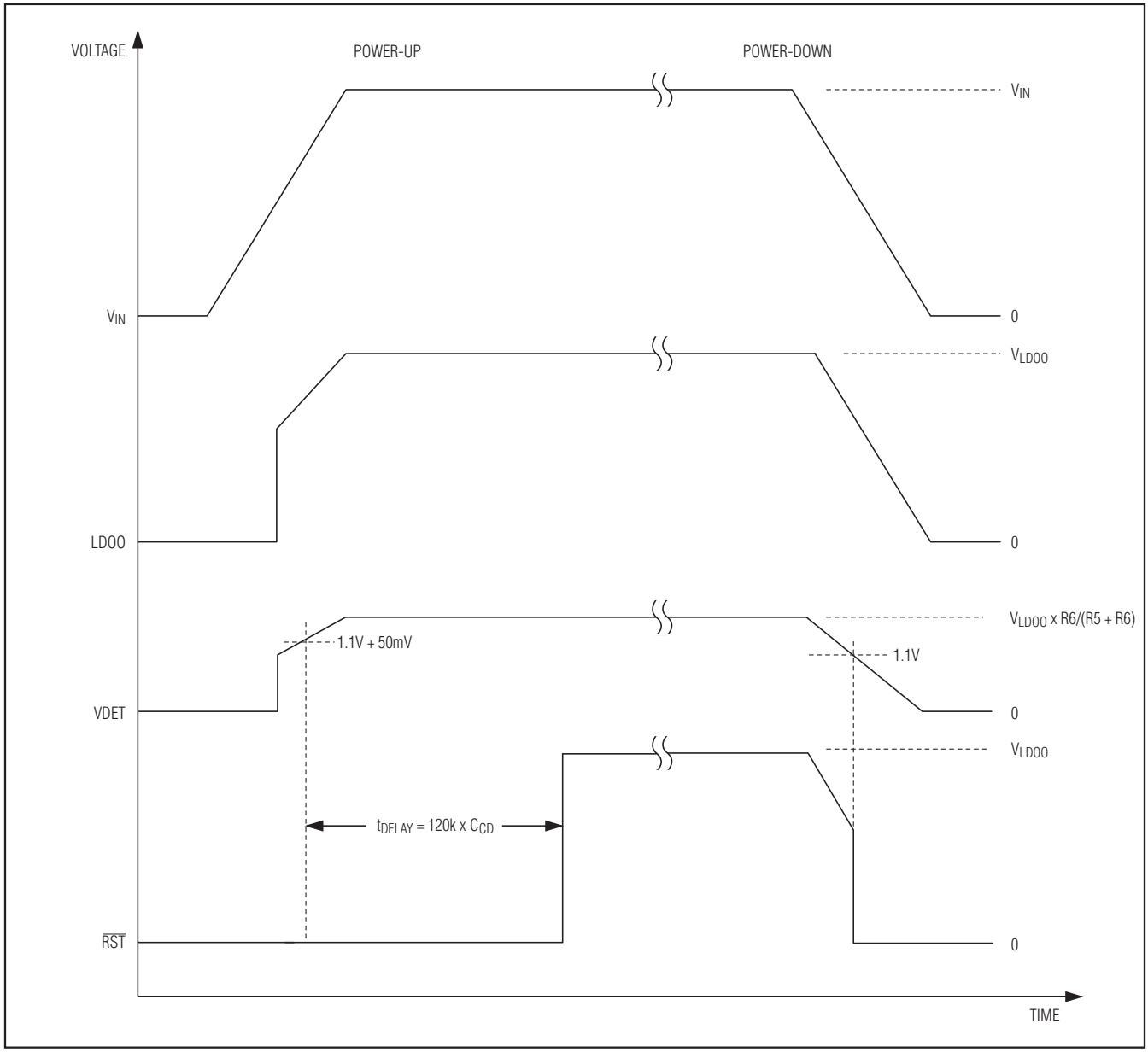


Figure 7. Voltage-Detector Power-Up and Power-Down Timing

Low-Dropout Linear Regulator (LDO)

The MAX17103 has an integrated 0.8Ω pass element and can provide at least 350mA. The output voltage is accurate within ±1%.

Gate-Off Linear-Regulator Controller

The negative linear controller provides a regulated gate-off voltage (VGL) for the TFT-LCD gate drivers by controlling the base drive current to an npn transistor typically connected to an unregulated negative charge pump as shown in Figure 1. The guaranteed base drive current that can be provided by DRVN is at least 1mA. During power-up, DRVN is prevented from providing base current to the npn transistor until 32ms after V_{MAIN} has reached 90% of its regulation voltage, keeping VGL off until this time.

Thermal-Overload Protection

When the junction temperature exceeds T_J = +160°C (typ), a thermal sensor activates a fault-protection latch, which shuts down all outputs, allowing the IC to cool down. All outputs remain off until the IC cools and the input voltage is cycled below, then back above the IN UVLO threshold.

The thermal-overload protection protects the IC in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

Design Procedure

Main Step-Up Regulator

Inductor Selection

The minimum inductance value, peak current rating, and series resistance are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output load capability, transient-response time, and output-voltage ripple. Physical size and cost are also important factors to be considered.

The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very high inductance values minimize the current ripple and therefore reduce the peak current, which decreases core losses in the inductor and I^2R losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increase physical size and can increase I^2R losses in the inductor. Low inductance values decrease the physical size, but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size, and cost.

The equations used here include a constant called LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full-load current. The best trade-off between inductor size and circuit efficiency for step-up regulators generally has an LIR between 0.3 and 0.5. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power-path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripple can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin high-resistance inductors are used, as is common for LCD panel applications, the best LIR can increase to between 0.5 and 1.0.

Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions.

In the typical operating circuit of Figure 1, the LCD's gate-on supply voltage is generated from an unregulated positive charge pump and the gate-off supply voltage is generated from a regulated negative charge pump controlled by the gate-off linear regulator. Both charge pumps are driven by the step-up regulator's LX node; therefore, the additional load on LX must be considered in the inductance and current calculations. The effective maximum output current, $I_{MAIN\ (EFF)}$ becomes the sum of the maximum load current of the step-up regulator's output plus the contributions from the positive and negative charge pumps:

$$I_{MAIN(EFF)} = I_{MAIN(MAX)} + n_{VN} \times I_{VN} + (n_{VP} + 1) \times I_{VP}$$

where $I_{MAIN(MAX)}$ is the maximum step-up output current, n_{VN} is the number of negative charge-pump stages, n_{VP} is the number of positive charge-pump stages, I_{VN} is the negative charge-pump output current, and I_{VP} is the positive charge-pump output current, assuming the initial pump source for I_{VP} is V_{MAIN}.

Calculate the approximate inductor value using the typical input voltage (V_{IN}), the maximum output current ($I_{MAIN(EFF)}$), the expected efficiency (η_{TYP}) taken from an appropriate curve in the *Typical Operating Characteristics*, the desired switching frequency (f_{OSC}), and an estimate of LIR based on the above discussion:

$$L = \left(\frac{V_{IN}}{V_{MAIN}}\right)^2 \left(\frac{V_{MAIN} - V_{IN}}{I_{MAIN(EFF)} \times f_{OSC}}\right)\left(\frac{\eta_{TYP}}{LIR}\right)$$

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage $V_{IN(MIN)}$ using conservation of energy and the expected efficiency at that operating point (η_{MIN}) taken from an appropriate curve in the *Typical Operating Characteristics*:

$$I_{IN(DC,MAX)} = \frac{I_{MAIN(EFF)} \times V_{MAIN}}{V_{IN(MIN)} \times \eta_{MIN}}$$

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{RIPPLE} = \frac{V_{IN(MIN)} \times \left(V_{MAIN} - V_{IN(MIN)}\right)}{L \times V_{MAIN} \times f_{OSC}}$$

$$I_{PEAK} = I_{IN(DC,MAX)} + \frac{I_{RIPPLE}}{2}$$

DC-DC Converter with Integrated Scan Driver, VGL Controller, Op Amp, and LDO for TFT LCD

The inductor's saturation current rating and the MAX17103 LX current limit should exceed I_{PEAK} and the inductor's DC current rating should exceed $I_{IN(DC,MAX)}$. For good efficiency, choose an inductor with less than 0.1Ω series resistance.

Considering the typical operating circuit, the maximum load current ($I_{MAIN(MAX)}$) is 250mA, with an 8.5V output and a typical input voltage of 3.3V. The effective full-load step-up current is:

$$I_{MAIN(EFF)} = 250mA + 1\times 10mA + (2+1)\times 10mA = 290mA$$

Choosing an LIR of 0.2 and estimating efficiency of 85% at this operating point:

$$L = \left(\frac{3.3V}{8.5V}\right)^2 \left(\frac{8.5V - 3.3V}{0.29A \times 1.2MHz}\right)\left(\frac{0.85}{0.2}\right) \approx 9.6\mu H$$

A 10µH inductor is chosen. Then, using the circuit's minimum input voltage (3.0V) and estimating efficiency of 80% at that operating point:

$$I_{IN(DC,MAX)} = \frac{0.29A \times 8.5V}{3V \times 0.8} \approx 1.03A$$

The ripple current and the peak current at that input voltage are:

$$I_{RIPPLE} = \frac{3V \times (8.5V - 3V)}{10\mu H \times 8.5V \times 1.2MHz} \approx 0.162A$$

$$I_{PEAK} = 1.03A + \frac{0.162A}{2} = 1.11A$$

Peak Inductor Current-Limit Setting

The inductor peak current limit can be adjusted up to 2A (max) by choosing the appropriate R_{ENA} resistor as configured in Figure 1 by the following:

$$R_{ENA} \approx \frac{(V_{LDOO} - 1.25V)(80000)}{I_{OCP}}$$

The above threshold set by R_{ENA} varies depending on the step-up converter's input voltage, output voltage, and duty cycle.

Output Capacitor Selection

The total output-voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$

$$V_{RIPPLE(C)} \approx \frac{I_{MAIN}}{C_{OUT}}\left(\frac{V_{MAIN} - V_{IN}}{V_{MAIN} f_{OSC}}\right)$$

and:

$$V_{RIPPLE(ESR)} \approx I_{PEAK} R_{ESR(COUT)}$$

where I_{PEAK} is the peak inductor current (see the *Main Step-Up Regulator Inductor Selection* section). For ceramic capacitors, the output-voltage ripple is typically dominated by $V_{RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Input Capacitor Selection

The input capacitor (C3) reduces the current peaks drawn from the input supply and reduces noise injection into the IC. A 10µF ceramic capacitor is used in the typical operating circuit (Figure 1) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply.

Rectifier Diode

The MAX17103 high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, a 1A Schottky diode complements the internal MOSFET well.

Output-Voltage Selection

The output voltage of the main step-up regulator is adjusted by connecting a resistive voltage-divider from the output (V_{MAIN}) to AGND with the center tap connected to FB (see Figure 1). Select R8 in the 10kΩ to 50kΩ range. Calculate R7 using the following equation:

$$R1 = R2 \times \left(\frac{V_{MAIN}}{1.24V} - 1\right)$$

Place R1 and R2 close to the IC.

Loop Compensation

Choose R_{COMP} to set the high-frequency integrator gain for fast-transient response. Choose C_{COMP} to set the integrator zero to maintain loop stability.

For low-ESR output capacitors, use the following equations to obtain stable performance and good transient response:

$$R_{COMP} \approx \frac{400 \times V_{IN} \times V_{MAIN} \times C_{OUT}}{L \times I_{MAIN(MAX)}}$$

$$C_{COMP} \approx \frac{40 \times V_{MAIN} \times L \times I_{MAIN(MAX)}}{(V_{IN})^2 \times R_{COMP}}$$

To further optimize transient response, vary R_{COMP} in 20% steps and C_{COMP} in 50% steps while observing transient-response waveforms.

LDO Output Voltage

The output voltage of the LDO is adjusted by connecting a resistive voltage-divider from the output (V_{LDOO}) to AGND with the center tap connected to LDOADJ (see Figure 1). Select R8 in the 10kΩ to 50kΩ range. Calculate R7 with the following equation:

$$R7 = R8 \times \left(\frac{V_{LDOO}}{1.24V} - 1 \right)$$

Place R7 and R8 close to the IC.

Connect a 1µF low equivalent-series-resistance (ESR) capacitor between LDOO and AGND to ensure stability and to provide good output-transient performance.

Input-Voltage Detector

Adjust the falling-edge threshold ($V_{DETECT(FALLING)}$) of the voltage being monitored (V_{DETECT}) by connecting a resistive voltage-divider from V_{DETECT} to AGND with the center tap connected to VDET. Select R6 in the 10kΩ to 1000kΩ range. Calculate R5 with the following equation:

$$R5 = R6 \times \left(\frac{V_{DETECT(FALLING)}}{1.1V} - 1 \right)$$

Place R5 and R6 close to the IC. Due to the 50mV hysteresis of the voltage-detector comparator, the rising-edge threshold ($V_{DETECT(RISING)}$) is related to the falling-edge threshold set above by:

$$V_{DETECT(RISING)} = V_{DETECT(FALLING)} + 50mV \times \left(1 + \frac{R5}{R6} \right)$$

Adjust the delay between the time V_{DETECT} has reached its rising threshold set by R5 and R6 above and the time $\overline{RST}$ goes high by connecting a capacitor between CD and AGND with the following equation:

$$C_{CD} = \frac{T_{DELAY}}{120k\Omega}$$

Gate-Off Linear-Regulator Controller

The output voltage of the negative linear regulator is adjusted by connecting a resistive voltage-divider from V_{VGL} to REF with the center tap connected to FBN (see Figure 1). Select R10 in the 10kΩ to 50kΩ range. Calculate R9 using the following equation:

$$R9 = \frac{|V_{VGL}|}{1.24V} \times R10$$

Place R9 and R10 close to the IC.

Applications Information

Power Dissipation

An IC's maximum power dissipation depends on the thermal resistance from the die to the ambient environment and the ambient temperature. The thermal resistance depends on the IC package, PCB copper area, other thermal mass, and airflow.

The MAX17103, with its exposed backside paddle soldered to 1in^2 of PCB copper, can dissipate approximately 1990mW into +70°C still air. More PCB copper, cooler ambient air, and more airflow increase the possible dissipation, while less copper or warmer air decreases the IC's dissipation capability. The major components of power dissipation are the power dissipated in the step-up regulator and the power dissipated by the operational amplifier.

The MAX17103's largest on-chip power dissipation occurs in the step-up switch, the VCOM amplifier, the LDO, and the high-voltage scan-driver outputs.

Step-Up Regulator

The largest portions of the power dissipated by the step-up regulator are the internal MOSFET, the inductor, and the output diode. If the step-up regulator with 3.3V input and 290mA output has approximately 85% efficiency, approximately 5% of the power is lost in the internal MOSFET, approximately 3% in the inductor, and approximately 5% in the output diode. The remaining few percent are distributed among the input and output capacitors and the PCB traces. If the input power is about 2.8W, the power lost in the internal MOSFET is approximately 140mW.

DC-DC Converter with Integrated Scan Driver, VGL Controller, Op Amp, and LDO for TFT LCD

Operational Amplifier

The power dissipated in the operational amplifier depends on the output current, the output voltage, and the supply voltage:

$$PD_{SOURCE} = I_{VCOM\_SOURCE} \times (V_{AVDD} - V_{VCOM})$$

$$PD_{SINK} = I_{VCOM\_SINK} \times V_{VCOM}$$

where I_{VCOM_SOURCE} is the output current sourced by the operational amplifier, and I_{VCOM_SINK} is the output current that the operational amplifier sinks. In a typical case where the supply voltage is 8.5V and the output voltage is 4.25V with an output source current of 30mA, the power dissipated is 128mW.

LDO

The power dissipated in the LDO depends on the LDO's output current, input voltage, and output voltage:

$$PD_{LDO} = I_{LDOO} \times (V_{LIN} - V_{LDOO})$$

Scan Driver Outputs

The power dissipated by the scan-driver outputs (CKH, XCKH, and STH) depends on the scan frequency, the capacitive load, and the difference between the GHON and VGL supply voltages:

$$PD_{SCAN} = 3 \times f_{SCAN} \times C_{PANEL} \times (V_{GHON} - V_{VGL})^2$$

If the scan frequency is 50kHz, the load of the three outputs is 3.4nF, and the supply voltage difference is 30V, then the power dissipated is 459mW.

PCB Layout and Grounding

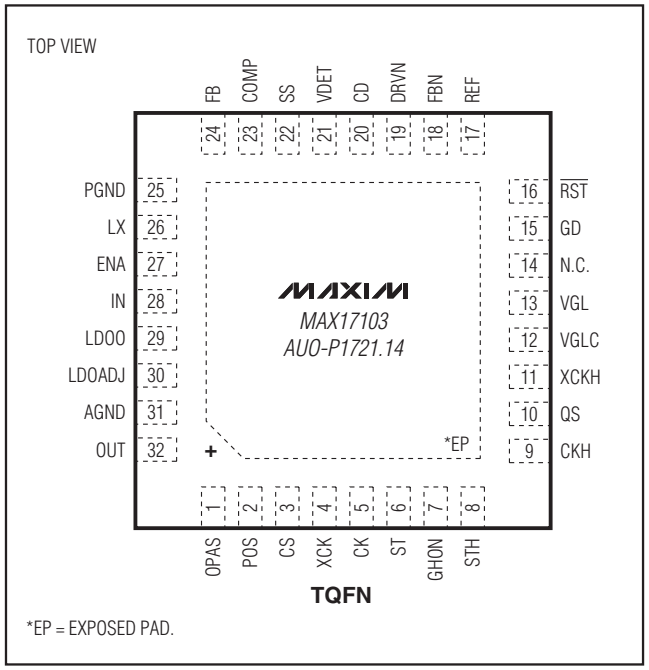
Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

1) Minimize the area of high-current loops by placing the inductor, output diode, and output capacitors near the input capacitors and near LX and PGND. The high-current input loop goes from the positive terminal of the input capacitor to the inductor, to the IC's LX pin, out of PGND, and to the input capacitor's negative terminal. The high-current output loop is from the positive terminal of the input capacitor to the inductor, to the output diode (D1), to the positive terminal of the output capacitors, reconnecting between the output capacitor and input capacitor ground terminals. Connect these loop components with short, wide connections. Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
2) Create a power ground island (PGND) consisting of the input and output capacitor grounds, PGND pin, and any charge-pump components. Connect all these together with short, wide traces or a small ground plane. Maximizing the width of the power ground traces improves efficiency and reduces output voltage ripple and noise spikes. Create an analog ground plane (AGND) consisting of the AGND pin, all the feedback-divider ground connections, the operational-amplifier-divider ground connections, the COMP capacitor ground connection, the AVDD capacitor ground connection, and the device's exposed backside pad. Connect the AGND and PGND islands by connecting the PGND pin directly to the exposed backside pad. Make no other connections between these separate ground planes.
3) Place the feedback-voltage-divider resistors as close as possible to the feedback pin. The divider's center trace should be kept short. Placing the resistors far away causes the FB trace to become an antenna that can pick up switching noise. Care should be taken to avoid running the feedback trace near LX or the switching nodes in the charge pumps.
4) Place IN pin bypass capacitors as close as possible to the device. The ground connections of the IN bypass capacitor should be connected directly to the AGND pin with a wide trace.
5) Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
6) Minimize the size of the LX node while keeping it wide and short. Keep the LX node away from the feedback node and analog ground. Use DC traces as shields, if necessary.

Refer to the MAX17103 evaluation kit for an example of proper board layout.

DC-DC Converter with Integrated Scan Driver, VGL Controller, Op Amp, and LDO for TFT LCD

Pin Configuration



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
32 TQFN-EP	T3255N-1	**21-0140**