

## General Description

AOZ18101DI-01/02 is a current-limiting over-voltage protection eFuse targeting applications that require front end protection at the input line. Both VIN and VOUT terminals are rated at 22V absolute maximum. There is a programmable soft-start feature that controls the inrush current for highly capacitive loads. It also has Input Under-Voltage Lock Out (UVLO), Input Over-Voltage Output Clamp (OVC), and Thermal Shut Down Protection (TSD).

AOZ18101DI-01/02 has built-in blocking FET for True Reverse Current Blocking (TRCB). For application flexibility, an external blocking FET control pin is also available if standalone MOSFET is preferred. It also features an internal current-limiting circuit that protects the supply from large load current. The current limit threshold can be set externally with a resistor. It will auto-restart after the fault conditions are released.

AOZ18101DI-01 is auto-restart version after fault condition. AOZ18101DI-02 is latch-off version after fault is detected. Both are available in small 3mmx3mm 10-pin DFN package.

AOZ18101DI-01 is pin to pin compatible with TPS259241. AOZ18101DI-02 is pin to pin compatible with TPS259240.

## Features

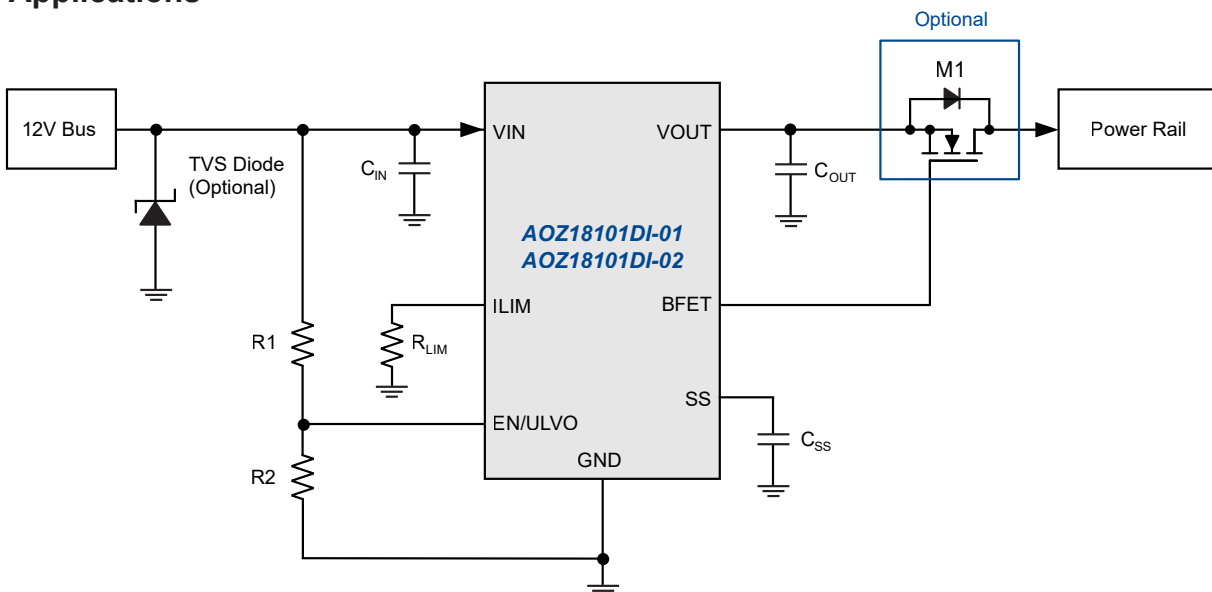
- 3.5V to 14V input voltage operating range
- 22V abs max voltage rating on VIN and VOUT pin
- Typical  $R_{ON}$ : 20mΩ
- 1A to 5A programmable current limit
- Built-in blocking FET for True Reverse Current Blocking (TRCB)
- Programmable output soft start time
- Fast Over Current Protection (OCP)
- Input Over-Voltage Output Clamp (OVC)
- Input Under-Voltage Lock Out (UVLO)
- Thermal Shut Down Protection (TSD)
- ±2kV HBM ESD rating
- ±1kV CDM ESD rating
- IEC 61000-4-2: ±8kV on VIN and VOUT
- IEC 61000-4-5: ± 40V on VIN, No cap
- IEC 62368-1: 2014 Certificate No US-40222-UL

## Applications

- Servers
- HDD and SSD drivers
- PCI cards
- Networking



## Typical Applications



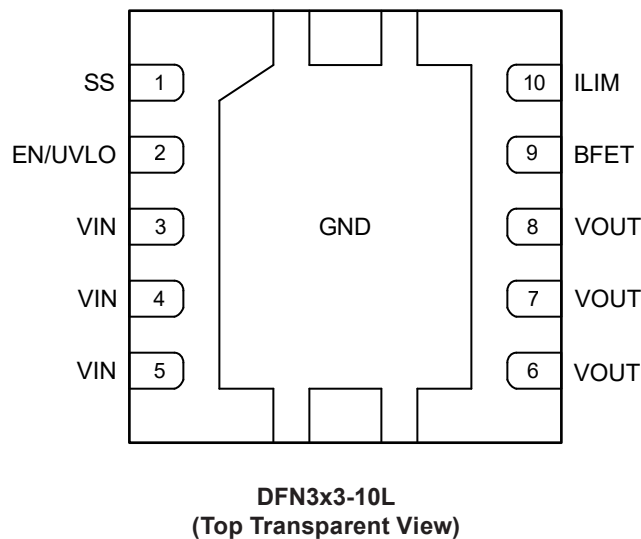
## Ordering Information

Part Number	Fault Recovery	Operating Voltage Range	Package	Environmental
AOZ18101DI-01	Auto-Restart	3.5V – 14V	DFN3x3-10L	RoHS
AOZ18101DI-02	Latch-Up	3.5V – 14V	DFN3x3-10L	RoHS



AOS products are offered in packages with Pb-free plating and compliant to RoHS standards. Please visit [www.aosmd.com/media/AOSGreenPolicy.pdf](http://www.aosmd.com/media/AOSGreenPolicy.pdf) for additional information.

## Pin Configuration



## Pin Description

Pin Number	Pin Name	Pin Function
1	SS	Soft-start control. Connect a capacitor $C_{SS}$ from SS to GND to set the soft-start time.
2	EN/UVLO	Enable input. Active high. It can be used as UVLO by connecting resistor divider from VIN.
3, 4, 5	VIN	Supply input. Connected to main power supply. They are internally connected together.
6, 7, 8	VOUT	Power output. They are internally connected together.
9	BFET	External blocking FET gate control. This pin can be left open when it is not used. When external blocking FET is used, connect this pin to the gate of the blocking FET.
10	ILIM	Current limit set pin. Connect a 1% resistor RLIM from ILIM to GND to set the current limit threshold.
EXP	GND	Ground. Connect to GND. For best thermal performance make the ground copper pads as large as possible and connect to EXP to the ground plane through multiple thermal VIAs.

## Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
V <sub>IN</sub> , V <sub>OUT</sub> to GND	-0.3V to 22V
V <sub>OUT</sub> to GND Transient < 1 μs	-1.2V
EN/UVLO, ILIM, SS to GND	-0.3V to 6V
BFET to GND	-0.3V to 22V
Junction Temperature (T <sub>J</sub> )	+150°C
Storage Temperature (T <sub>S</sub> )	-65°C to +150°C
ESD Rating HBM All Pins	±2kV
IEC 61000-4-2: V <sub>OUT</sub> and V <sub>IN</sub>	±8kV

## Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
Supply Voltage V <sub>IN</sub> , V <sub>OUT</sub> to GND	3.5V to 14V
BFET to GND	0V to V <sub>OUT</sub> +6V
EN/UVLO, ILIM, SS to GND	0V to 5.5V
Switch DC Current (I <sub>SW</sub> )	0 A to 5A
Junction Temperature (T <sub>J</sub> )	-40°C to +125°C
Package Thermal Resistance DFN3x3-10L (Θ <sub>JA</sub> )	65°C/W

## Electrical Characteristics<sup>(1)</sup>

T<sub>A</sub> = 25°C, V<sub>IN</sub> = 12V, EN = 5V, R<sub>LIM</sub> = 100kΩ, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>General</b>						
V <sub>VIN</sub>	Input Supply Voltage		3.5		14	V
V <sub>UVLO_R</sub>	Under-voltage Lockout Threshold	V <sub>IN</sub> rising	2.9		3.4	V
V <sub>UVLO_HYS</sub>	Under-voltage Lockout Hysteresis	V <sub>IN</sub> falling		250		mV
I <sub>VIN_ON</sub>	Input Quiescent Current	I <sub>OUT</sub> = 0A		500		μA
I <sub>VIN_OFF</sub>	Input Shutdown Current	EN/UVLO = 0V		125		μA
V <sub>OVC</sub>	Output Over Voltage Clamp	V <sub>IN</sub> = 17V, I <sub>OUT</sub> = 10mA	14.0	15.0	16.5	V
R <sub>ON</sub>	Switch ON-Resistance	V <sub>IN</sub> = 12V, I <sub>OUT</sub> = 1A		20		mΩ
		V <sub>IN</sub> = 5V, I <sub>OUT</sub> = 1A		21		
V <sub>EN_H</sub>	EN Input Logic High Threshold	EN/UVLO rising	1.3	1.40	1.45	V
V <sub>EN_L</sub>	EN Input Logic Low Threshold	EN/UVLO falling	1.2	1.35	1.4	V
I <sub>EN_BIAS</sub>	EN Input Bias Current	EN/UVLO = 1.8V	-100		100	nA
<b>Dynamic Timing Characteristics</b>						
t <sub>D_ON</sub>	Turn-On Delay Time	From EN/UVLO > V <sub>EN_H</sub> to V <sub>OUT</sub> = 0.1V. C <sub>SS</sub> = open		600		μs
t <sub>ON</sub>	Turn-On Time (V <sub>OUT</sub> from 0.1V to 11.7V)	C <sub>SS</sub> = open		900		μs
		C <sub>SS</sub> = 1nF		10		ms
t <sub>D_OFF</sub>	Turn-Off Delay Time	From EN/UVLO < V <sub>EN_H</sub> to BFET = falling down to 12V, C <sub>BFET</sub> = open		0.5		μs
t <sub>BFET_ON</sub>	BFET Turn-On Time	From EN/UVLO > V <sub>EN_H</sub> to BFET = rising above to 12V, C <sub>BFET</sub> = 1nF		1.3		ms
		From EN/UVLO > V <sub>EN_H</sub> to BFET = rising above to 12V, C <sub>BFET</sub> = 10nF		2.3		ms

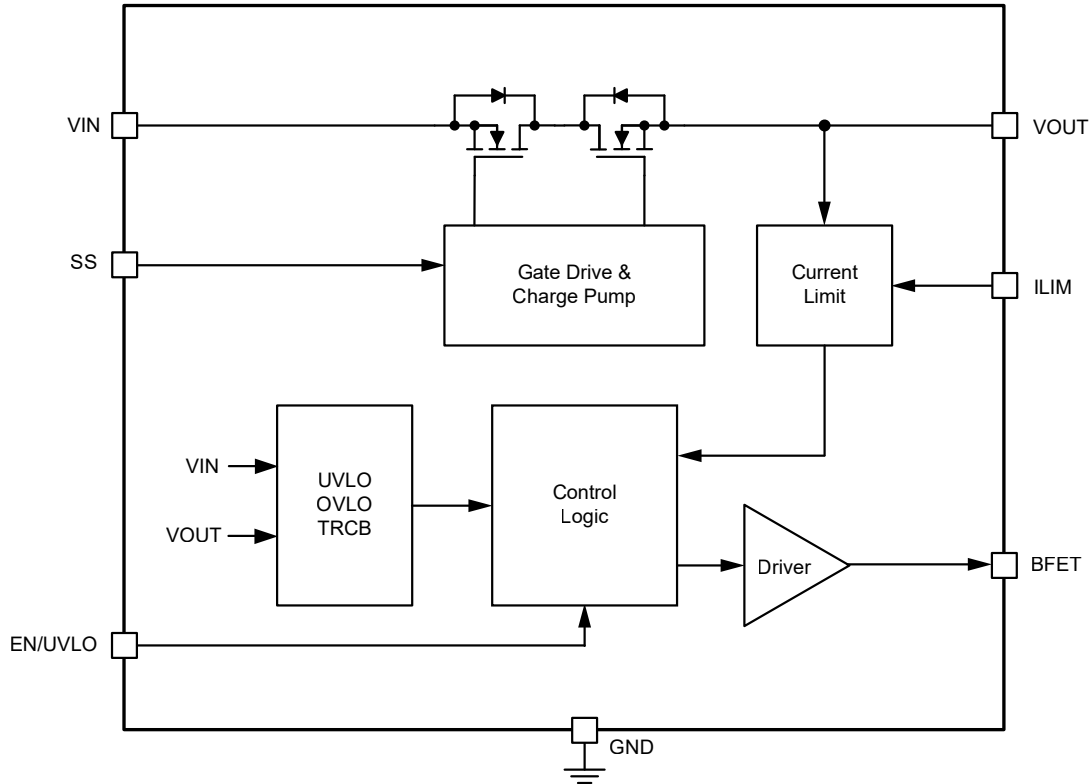
**Electrical Characteristics<sup>(1)</sup>**
 $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{V}$ ,  $V_{EN} = 5\text{V}$ ,  $R_{LIM} = 100\text{k}\Omega$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{BFET\_OFF}$	BFET Turn-Off Time	From EN/UVLO < $V_{EN\_L}$ to BFET = falling down to 12V, $C_{BFET} = 1\text{nF}$		6		$\mu\text{s}$
		From EN/UVLO < $V_{EN\_L}$ to BFET = falling down to 12V, $C_{BFET} = 10\text{nF}$		50		$\mu\text{s}$
<b>True Reverse-Current Blocking (TRCB)</b>						
$V_{T\_TRCB}$	TRCB Protection Trip Point	$V_{IN} - V_{OUT}$ , $V_{OUT}$ rising		18		mV
$t_{TRCB}$	TRCB Response Time	$V_{OUT} - V_{IN} > V_{T\_TRCB} + 500\text{mV}$		1		$\mu\text{s}$
<b>Over Current Protection (OCP)</b>						
$I_{LIM}$	Current Limit Threshold	$R_{LIM} = 150\text{k}\Omega$	4.50	5.10	5.70	A
		$R_{LIM} = 100\text{k}\Omega$	3.46	3.75	4.03	
		$R_{LIM} = 45.3\text{k}\Omega$	1.79	2.10	2.42	
		$R_{LIM} = 10\text{k}\Omega$		1.00		
		$R_{LIM} = 0$ or Open		0.75		
$I_{OCP\_FAST}$	Fast OCP Threshold for Current Spike	Based on $I_{LIM}$ value		160		%
$t_{OCP\_FAST}$	Fast OCP Response Time	From $I_{OUP} > (I_{LIM} \times 160\%)$		300		ns
<b>Blocking FET Driver</b>						
$I_{BFET}$	BFET Driving Current	BFET = $V_{OUT}$		10		$\mu\text{A}$
$R_{BFET\_DIS}$	BFET Discharge Resistance			29		$\text{k}\Omega$
<b>Thermal Shutdown (TSD)</b>						
$T_{SD}$	Thermal Shutdown Threshold	Temperature rising		140		$^\circ\text{C}$
$T_{SD\_HYS}$	Thermal Shutdown Hysteresis	Temperature falling		30		$^\circ\text{C}$

**Note:**

1. Guaranteed by characterization and design.

**Functional Block Diagram**



## Timing Diagrams

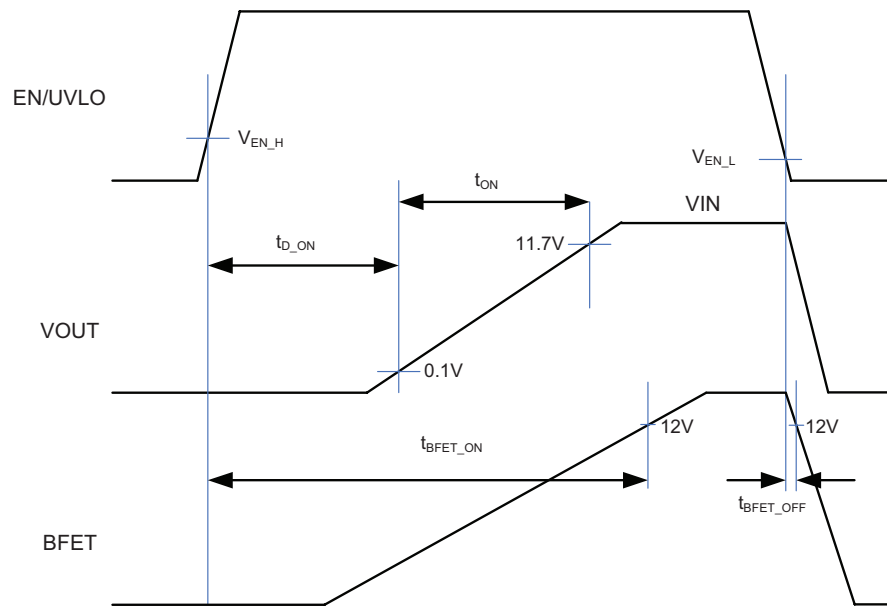


Figure 1. Turn-on Delay, Turn-on and Turn-off Time

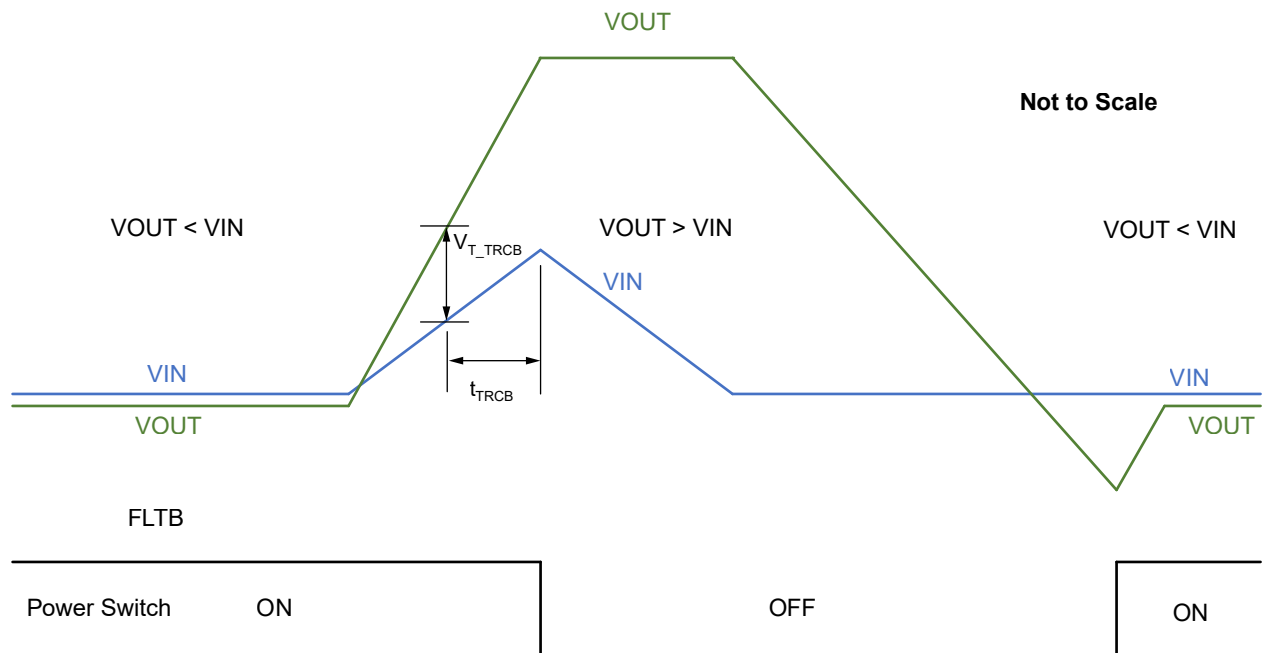


Figure 2. True Reverse Current Blocking (TRCB) Operation

Timing Diagrams (Continued)

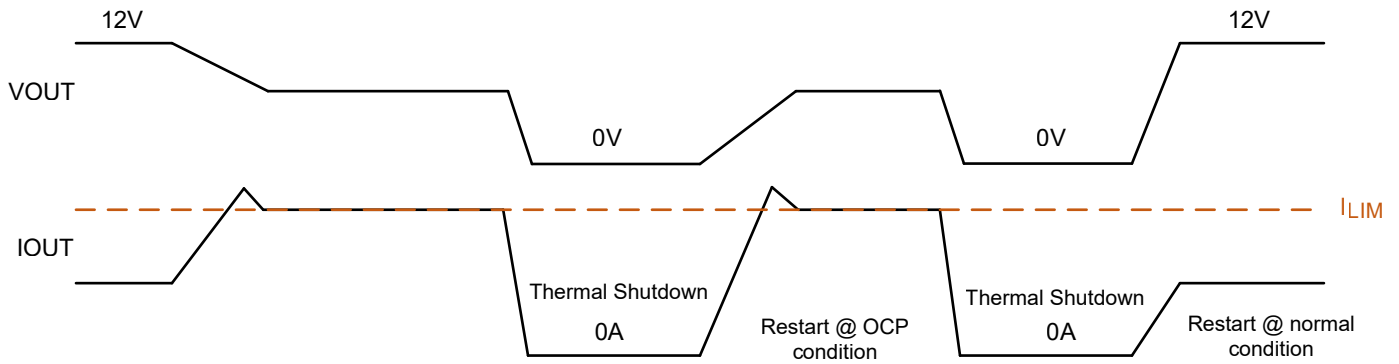


Figure 3. Current Limit Operation (AOZ18101-01 Auto-Restart)

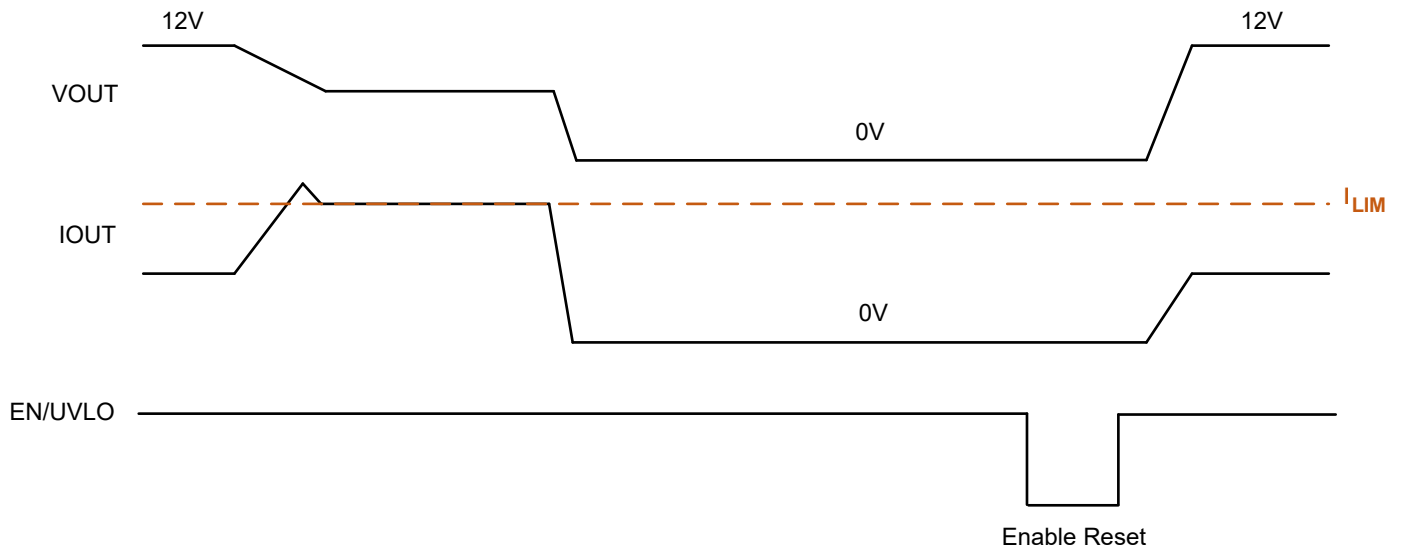
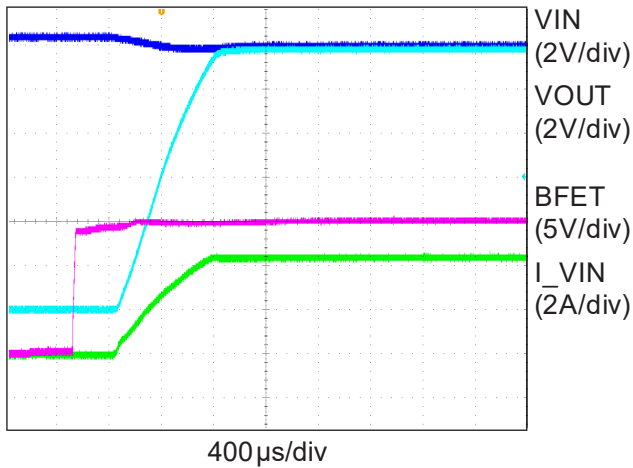


Figure 4. Current Limit Operation (AOZ18101-02 Latch-off)

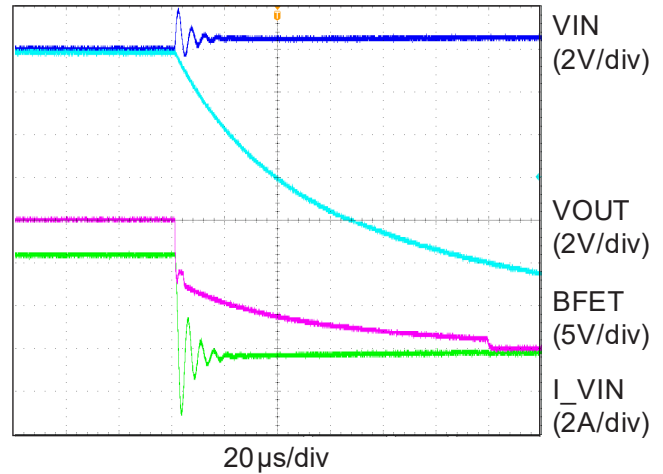
### Typical Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{V}$ ,  $EN = 5\text{V}$ ,  $C_{IN} = 10\mu\text{F}$ ,  $C_{OUT} = 10\mu\text{F}$ ,  $C_{SS} = 1\text{nF}$ ,  $R_{LIM} = 150\text{k}\Omega$ , unless otherwise specified.

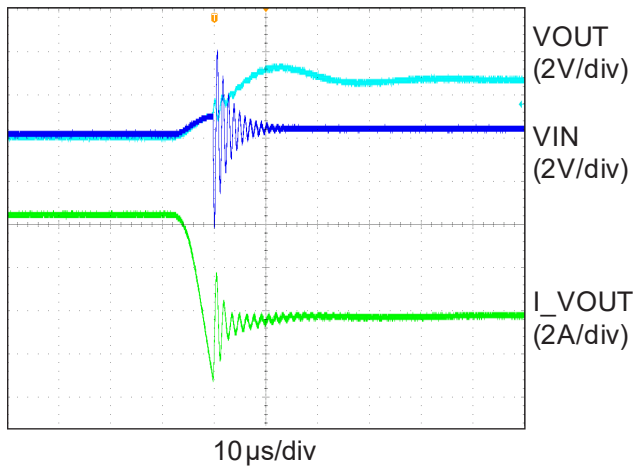
**Start Up (Load = 5A)**



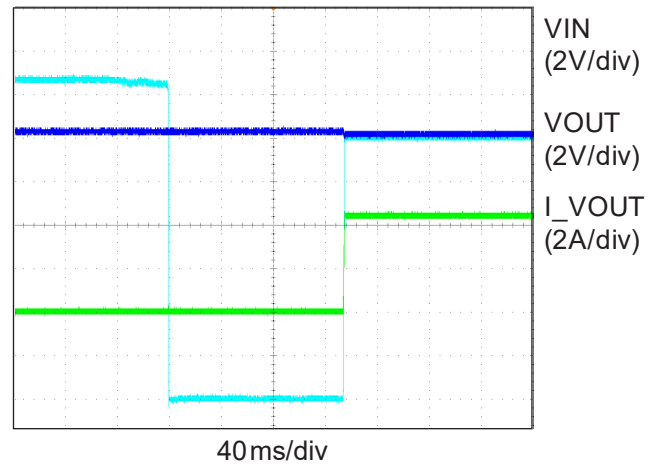
**Shutdown**



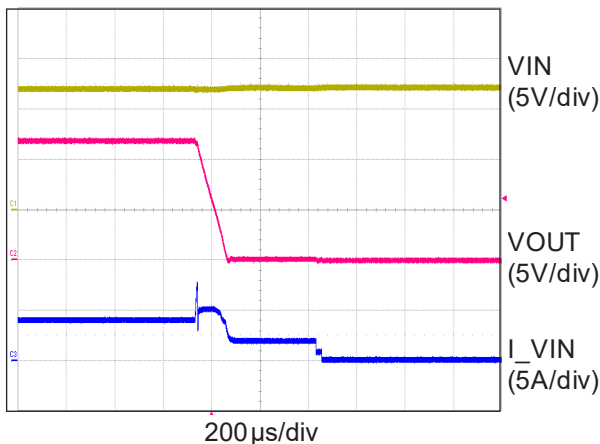
**True Reverse Current Blocking Trigger (not external FET)**



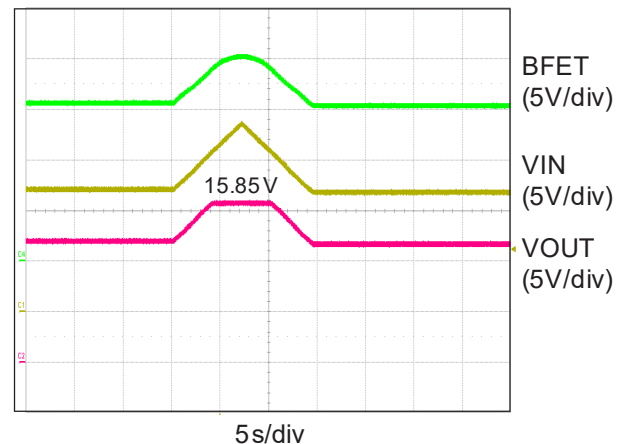
**True Reverse Current Blocking Release (no external FET)**



**Over-Current Protection**



**Output Over-Voltage Clamp**





## Typical Characteristics

$T_A = 25\text{ }^\circ\text{C}$ ,  $V_{IN} = 12\text{ V}$ ,  $EN = 5\text{ V}$ ,  $C_{IN} = 10\text{ }\mu\text{F}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$ ,  $C_{SS} = 1\text{ nF}$ ,  $R_{LIM} = 150\text{ k}\Omega$ , unless otherwise specified.

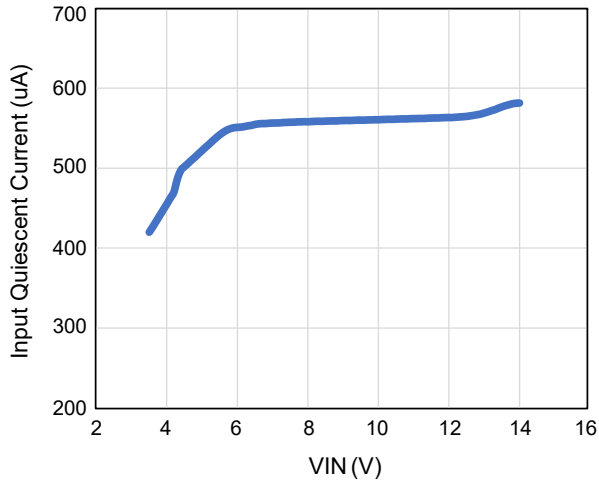


Figure 5. Input Quiescent Current vs. VIN

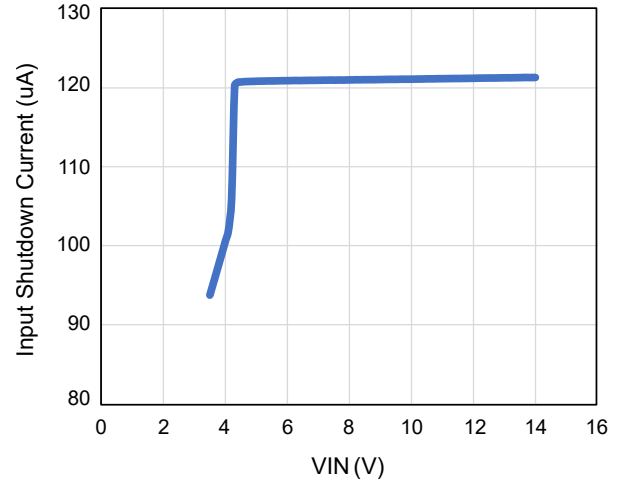


Figure 6. Input Shutdown Current vs. VIN

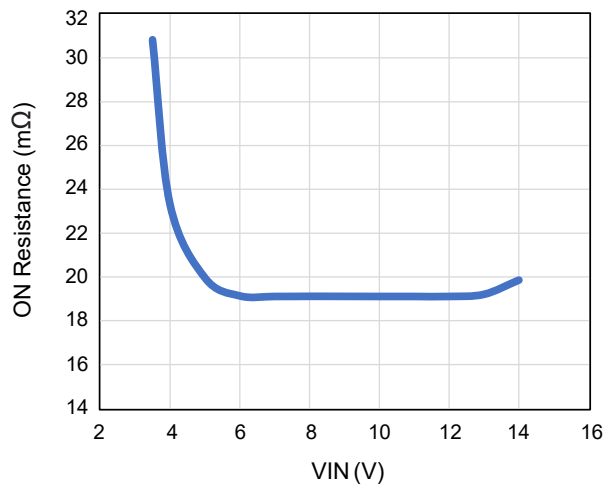


Figure 7. ON Resistance vs. VIN

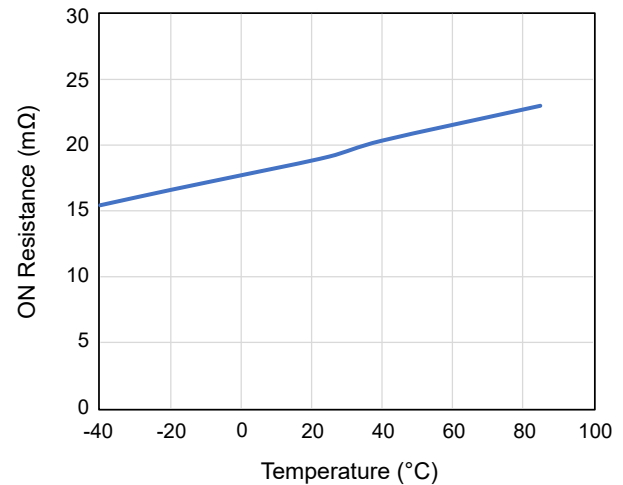


Figure 8. ON Resistance vs. Temperature (VIN = 12V)

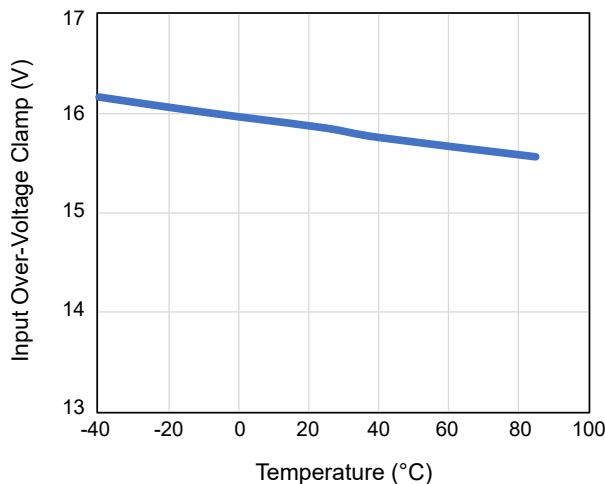


Figure 9. Input Over-Voltage Clamp vs. Temperature

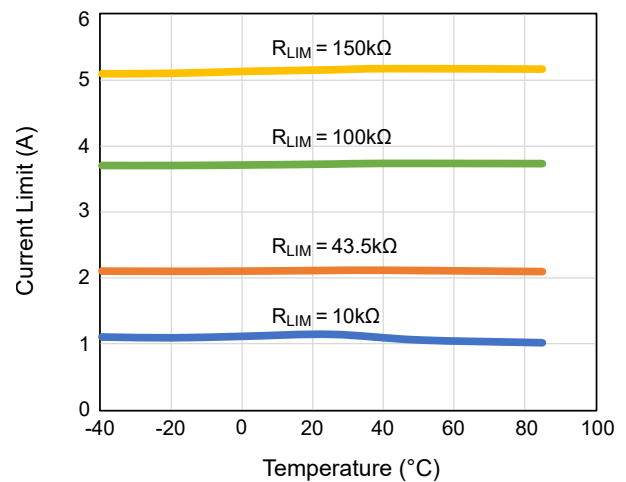


Figure 10. Current Limit vs. Temperature

## Detailed Description

AOZ18101DI-01/02 is a current-limiting power switch with under-voltage, over-voltage, over-current, reverse-current and thermal shutdown protections. The VIN and VOUT pins are rated 22V abs max.

The device has True Reverse-Current Blocking (TRCB) features that will prevent undesired current flow from output to its input in either enabled or disabled state.

### Enable and Under-Voltage Lockout

The EN/UVLO pin is the ON/OFF control for the power switch. The device is enabled when the voltage at EN/UVLO pin is higher than  $V_{EN\_H}$  and the input voltage is higher than the under-voltage lockout threshold,  $V_{IN} > V_{UVLO\_R}$ .

EN/UVLO pin can be biased with resistor divider network from VIN so that device enable will be tracking the input voltage. While disabled, the AOZ18101DI-01/02 draws 125µA from supply. EN/UVLO cannot be left floating.

### Input Under-Voltage Lockout (UVLO)

The under-voltage lockout (UVLO) circuit monitors the input voltage. The power switch and the BFET for charging the gate of the external FET are only allowed to turn on when input voltage is higher than UVLO threshold ( $V_{UVLO\_R}$ ). Otherwise the switch is off.

### Over-Voltage Clamp (OVC)

The voltage at VIN pin is constantly monitored once the device is enabled. In case input voltage exceeds the over-voltage protection threshold ( $V_{OVC}$ ), the output voltage will be clamped at the threshold voltage.

Under the over-voltage clamp (OVC) condition, the output voltage is clamped to the  $V_{OVC}$  level. The power dissipation in the internal FETs under this condition is  $P_{FET\_OVC} = (V_{IN} - V_{OVC}) \times I_{OUT}$ , which can heat up the device and causes thermal shutdown when the temperature reaches TSD.

### Programmable Current Limit and Over-Current Protection (OCP)

The AOZ18101DI-01/02 implemented current limit to ensure that the current through the switch does not exceed current limit threshold set by the external resistor RLIM.

The current limit threshold can be estimated using the equation below:

$$I_{LIM} = (0.7 + 3 \times 10^{-5} \times R_{LIM})$$

where  $R_{LIM}$  unit is in Ohm and  $I_{LIM}$  unit is in Ampere.

AOZ18101DI-01/02 continuously limits the output current when output is overloaded. Under this condition, the part is dissipating excessive power due to higher voltage drop across VIN to VOUT. If over current continues to exist, it will reach thermal shutdown threshold and the switch will be turned off.

For AOZ18101DI-01 Auto-Restart version, the power switch will be turn on again to restart after thermal shutdown is released.

For AOZ18101DI-02 Latch Off version, the power switch will only be turned on after toggling the EN/UVLO input logic to reset the device.

The AOZ18101DI-01/02 integrates a fast comparator which will trigger to turn off the switch at 160% of the current limit threshold set by ILIM pin. After the fast comparator turns off the switch, the switch will be turned on to regulate the current to the set current limit threshold.

### Programming Soft Start

The output soft-start time can be programmed externally through SS pin. The output soft-start time can be estimated using the equations below:

$$t_{ON} = \frac{(C_{SS} + 0.07) \times VIN}{1.067}$$

where  $C_{SS}$  unit is in nF and  $t_{ON}$  unit is in ms.

The SS pin can be left floating ( $C_{SS} = \text{Open}$ ) for the minimum soft-start time (0.75ms for  $V_{IN} = 12V$ ).

The device has internal SOA management to protect the internal FETs. Design Tool is available to select the appropriate  $C_{SS}$  based on load and input voltage.

### Blocking FET Driver (BFET)

When external blocking FET (N-Channel MOSFET) is used, connect the BFET pin to the gate of the blocking FET. The BFET pin charges the gate of the external FET when both the voltage at EN/UVLO pin is higher than  $V_{EN\_H}$  and the input voltage is higher than the under-voltage lockout threshold,  $V_{IN} > V_{UVLO\_R}$ . The BFET pin discharges current from the gate of the external FET via a 29kΩ internal discharge resistor, when either the voltage at EN/UVLO pin is lower than  $V_{EN\_L}$  or the input voltage is lower than the under-voltage lockout threshold,  $V_{IN} < (V_{UVLO\_R} - V_{UVLO\_HYS})$ .

AOZ18101DI-01/02 does not need external blocking FET to perform reverse current blocking as this function is integrated inside. This driver is available for application compatibility if external FET is already placed.

### True Reverse Current Blocking (TRCB)

True reverse-current blocking prevents undesired current flow from output to input when power switch is in either on or off state. When device is enabled, power switch is quickly turned off whenever output voltage is higher than input voltage by 18mV ( $V_{T\_TRCB}$ ). Once the device detects the TRCB condition it will quickly turn off the switch in 1  $\mu$ s ( $t_{TRCB}$ ). The power switch can be turned on again when  $V_{OUT} < V_{IN}$ .

### Thermal Shut Down Protection (TSD)

Thermal shutdown protects device from excessive temperature. The power switch is turned off when the die temperature reaches thermal shutdown threshold of 140°C. There is a 30°C hysteresis. The power switch is allowed to turn on again if die temperature drops below approximately 110°C.

### Input Capacitor Selection

The input capacitor prevents large voltage transients from appearing at the input, and provides the instantaneous current needed each time the switch turns on to charge output capacitors and to limit input voltage drop. It also prevents high-frequency noise on the power line from passing through to the output. The input capacitor should be located as close to the pin as possible. A minimum of 10  $\mu$ F ceramic capacitor should be used. A higher capacitor value is strongly recommended to further reduce the transient voltage drop at the input.

In some applications, a Transient Voltage Suppressor (TVS) can be added on the input side to ensure that the input voltage transients don't exceed the Absolute Maximum Ratings of the device.

### Output Capacitor Selection

The output capacitor acts in a similar way. Also, the output capacitor has to supply enough current for a large load that it may encounter during system transient. This bulk capacitor must be large enough to supply fast transient load in order to prevent the output from dropping.

A Schottky diode can be added between the output and ground to absorb negative voltage spikes

### Power Dissipation Calculation

Calculate the power dissipation for normal load condition using the following equation:

$$\text{Power Dissipation} = R_{ON} \times (I_{OUT})^2$$

### Layout Guidelines

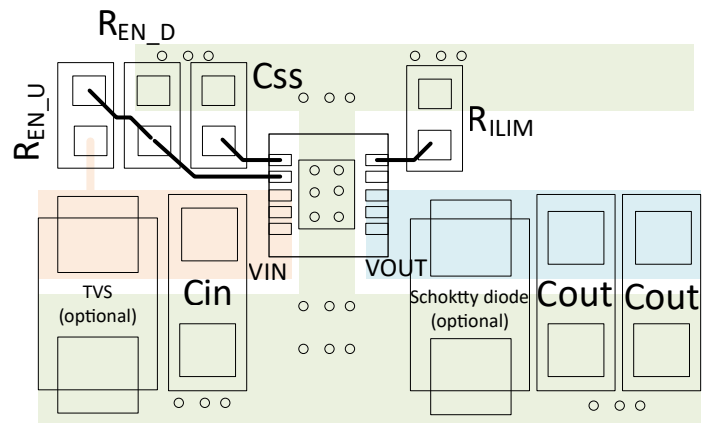
Good PCB layout is important for improving the thermal and overall performance of AOZ18101DI-01/02. To optimize the switch response time to output short-circuit conditions, keep all traces as short as possible to reduce the effect of unwanted parasitic inductance. Place the input and output bypass capacitors as close as possible to the VIN and VOUT pins. The input and output PCB traces should be as wide as possible. The input and output traces should be sized to carry at least twice the full-load current.

Place a decoupling capacitor as close as possible to the VIN and GND terminals of the device. Minimize the loop area formed by the bypass-capacitor connection, the VIN pins, and the GND pin (EXP) of the IC.

If protective devices such as TVS and Schottky diode are needed, place them physically close to the IC, and route with short traces to reduce inductance.

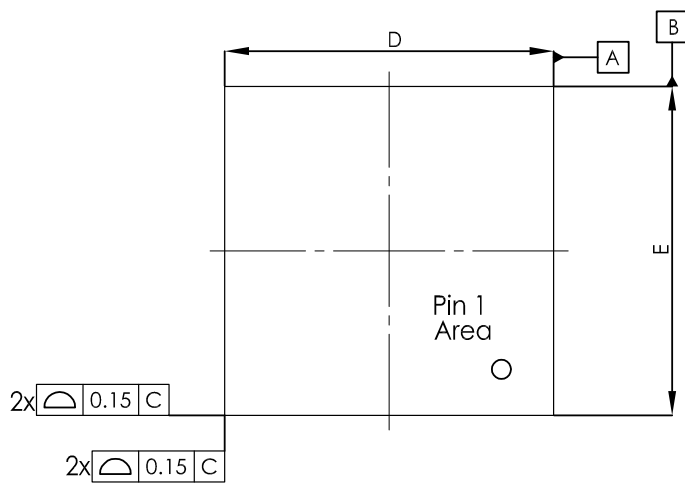
For the most efficient thermal dissipation, connect the exposed pad to the ground plane with thermal vias as many as possible.

Figure 11 shows example for the AOZ18101DI-01/02 layout. Note that the TVS and the Schottky diode are optional.

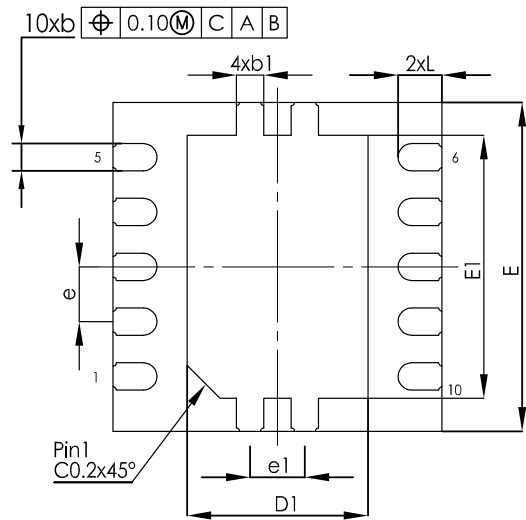


**Figure 11. PCB Layout Example**

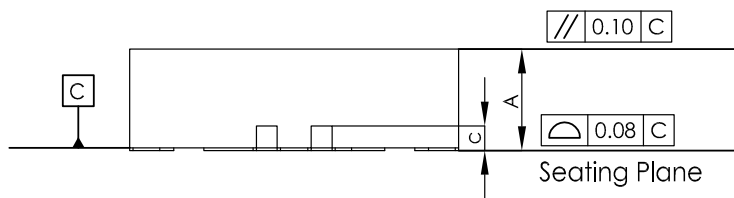
**Package Dimensions, DFN3x3-10L**



**TOP VIEW**

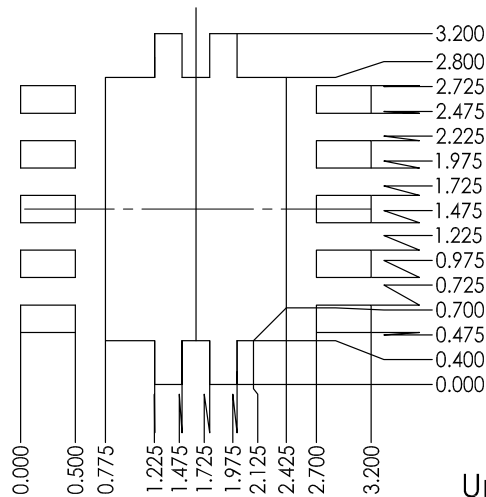


**BOTTOM VIEW**



**SIDE VIEW**

**RECOMMENDED LAND PATTERN**



Unit: mm

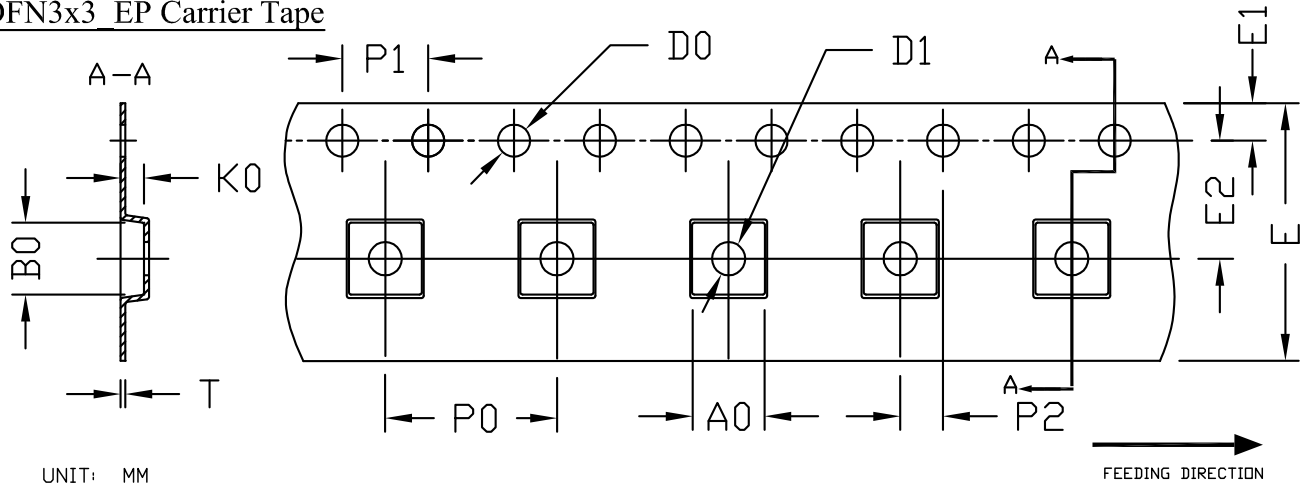
SYMBOLS	DIM. IN MM			DIM. IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	---	0.05	0.000	0.000	0.002
D	2.90	3.00	3.10	0.114	0.118	0.122
D1	1.55	1.65	1.75	0.061	0.065	0.069
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	2.30	2.40	2.50	0.091	0.094	0.098
L	0.30	0.40	0.50	0.012	0.016	0.020
b	0.18	0.25	0.30	0.007	0.010	0.012
b1	0.25REF			0.010REF		
c	0.20REF			0.008REF		
e	0.50BSC			0.020BSC		
e1	0.50REF			0.02REF		

**NOTE:**

1. Dimensioning and tolerancing comply with ASME Y14.5M 1994.
2. Controlled dimensions are in millimeters.
3. Coplanarity applies to the exposed pad(s) and all terminal leads having metallization.

**Tape and Reel Dimensions, DFN3x3-10L**

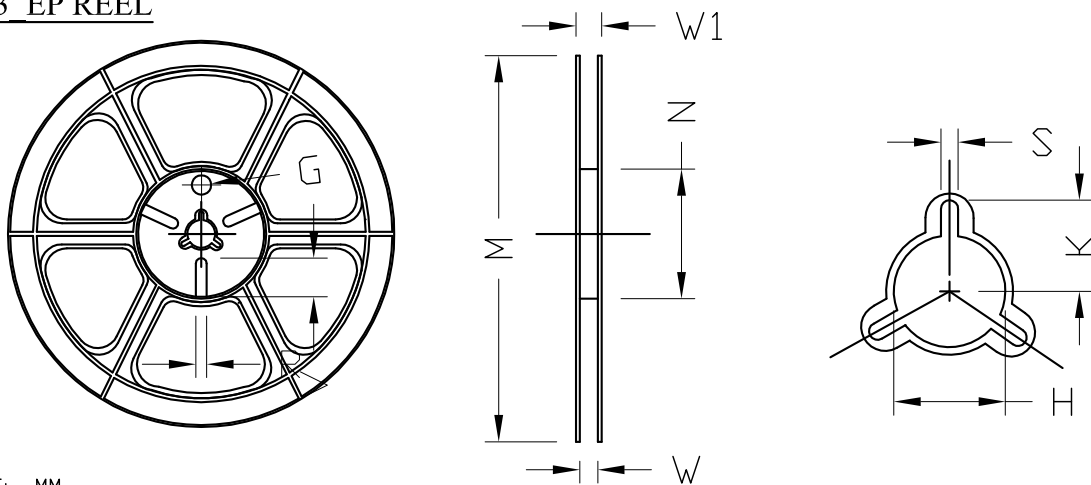
DFN3x3 EP Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN3x3_EP	3.40 ±0.10	3.35 ±0.10	1.10 ±0.10	1.50 +0.10 -0	1.50 +0.10 -0	12.00 ±0.30	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

DFN3x3 EP REEL

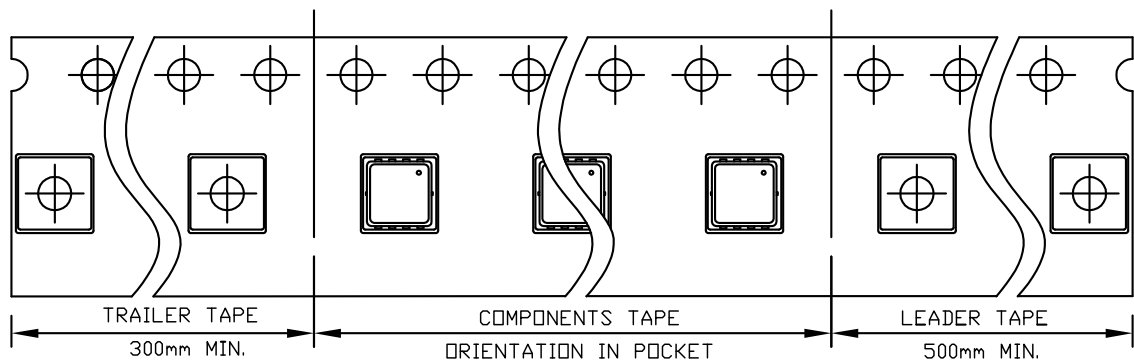


UNIT: MM

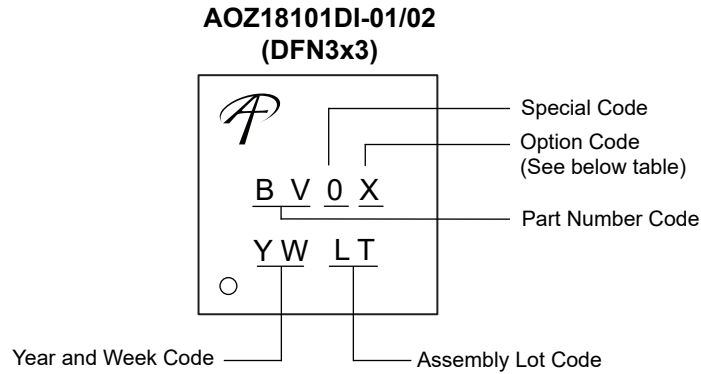
TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.00 ±0.50	ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	ø13.00 +0.50 -0.20	10.60	2.00 ±0.50	---	---	---

PIC

Unit Per Reel:  
5000pcs



**Part Marking**



Part Number	Description	Marking Code
AOZ18101DI-01	Auto-Restart	BV01
AOZ18101DI-02	Latch Off	BV02

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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.