Four-Channel LCD Backlight Driver with Integrated Bias Power

General Description

The RT4831A is an integrated four-channel backlight WLED driver with LCD bias supply for portable device. The backlight WLED driver supports up to 4P8S WLED configuration. Meanwhile, the driver maximum acceptable output voltage is 29V. Each channel current is controlled by the I^2C interface and/or the external PWM input to achieve 11 bit LED current steps from 60μA to 30mA in exponential or linear mapping curves. The LCD bias supply is implemented with a Boost, a LDO and an inverting charge pump to provide positive and negative voltage. The LCD bias provides up to 150mA output current and the output voltage can be programmed via I^2C interface from ±4V to ±6.5V with 50mV/step. The RT4831A is available in a WL-CSP-24B 1.84x2.68 (BSC) package.

Ordering Information

RT4831A□

Package Type
WSC : WL-CSP-24B 1.84x2.68 (BSC)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

Suitable for use in SnPb or Pb-free soldering processes.

Features

System

- **Hardware Enable Pin**
- **I^2C Controlled Interface**
- **Over-Temperature Protection**

Backlight WLED Driver

- **2.7V to 5V Input Voltage Range**
- **Drives Up to 4P8S WLED Configuration (29V Maximum Output Voltage)**
- **External PWM Input and I^2C Brightness Control**
- **11 Bit Exponential and Linear Dimming Control**
- **Programmable Over-Voltage Protection**
- **Programmable Over-Current Protection**
- **Auto Operating Frequency (250kHz, 500kHz, 1MHz)**
- **WLED Current Ramp Up / Ramp Down Smoothen**

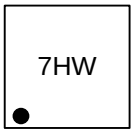
LCD Bias Supply

- **2.7V to 5V Input Voltage Range**
- **Programmable Positive / Negative Output Voltage from ±4V to ±6.5V with 50mV/Step**
- **Programmable Boost Output Voltage from 4V to 7.15V with 50mV/Step**
- **150mA Output Current Capability**
- **Output Short-Circuit Protection**

Applications

- LCD Panels with up to 32 LEDs
- Smartphone
- Tablet

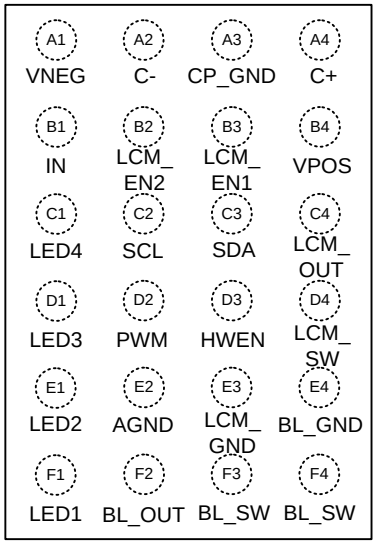
Marking Information



7H : Product Code
W : Date Code

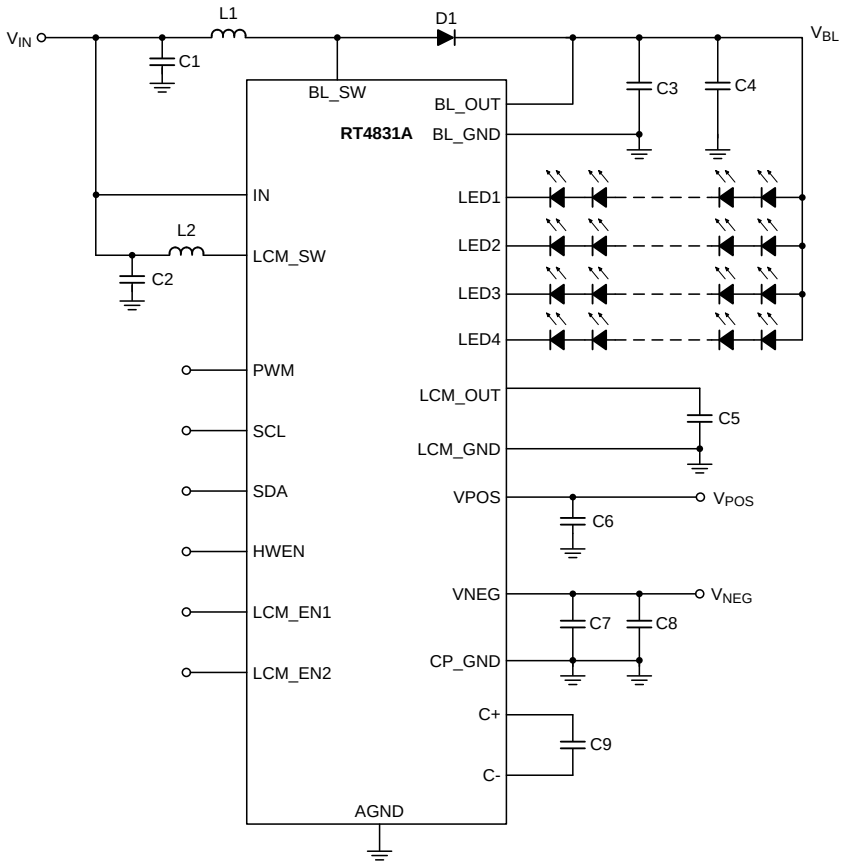
Pin Configuration

(TOP VIEW)



WL-CSP-24B 1.84x2.68 (BSC)

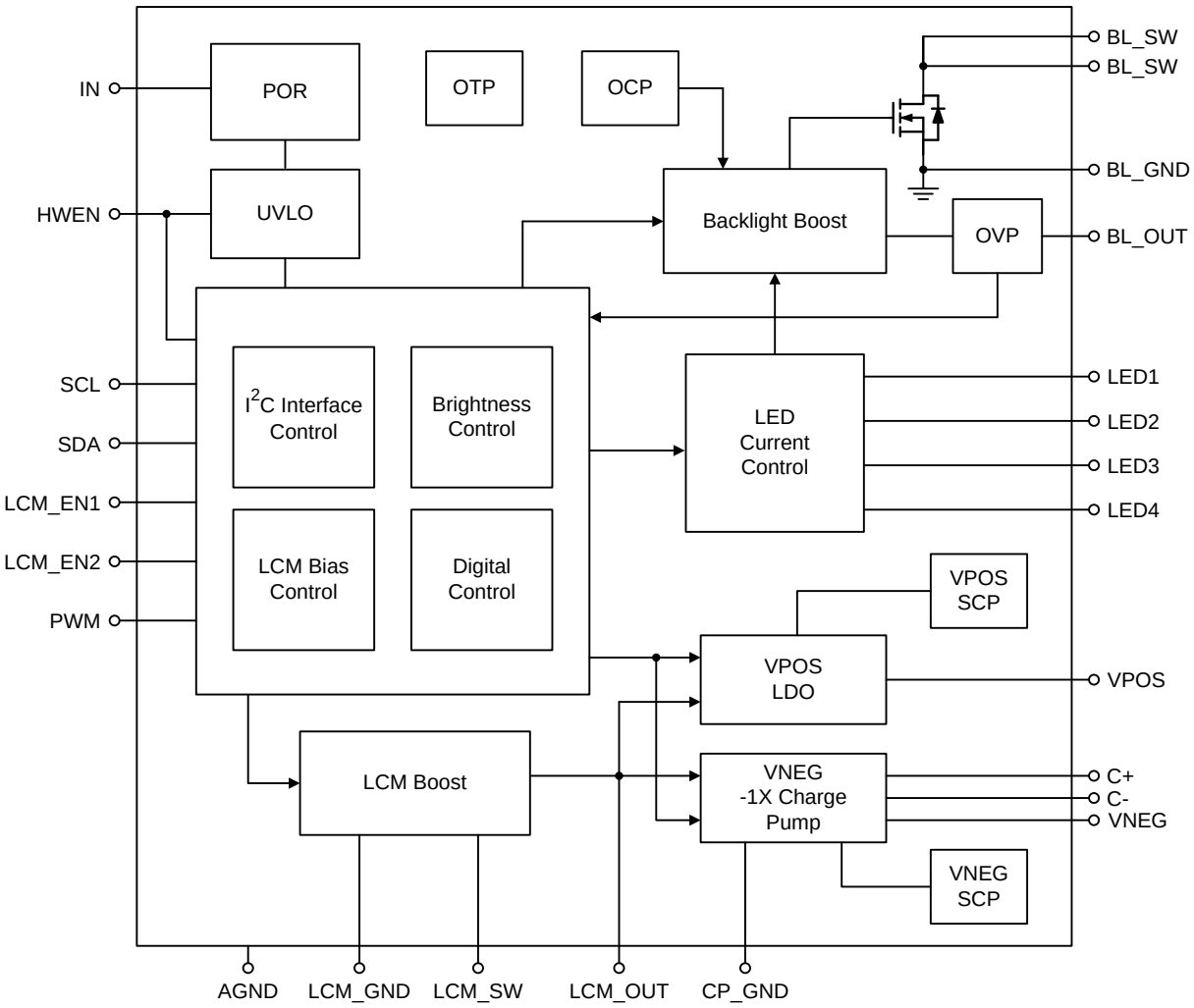
Simplified Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
A1	VNEG	Charge pump negative output. Connect a 10μF decouple ceramic capacitor between this pin and CP_GND pin.
A2	C-	Charge pump flying capacitor negative connection. Connect a 10μF ceramic capacitor between this pin and C+ pin.
A3	CP_GND	Charge pump ground.
A4	C+	Charge pump flying capacitor positive connection. Connect a 10μF ceramic capacitor between this pin and C- pin.
B1	IN	Input voltage connection. Connect a 10μF or larger decouple ceramic capacitor between this pin and ground.
B2	LCM_EN2	Enable input for LCD bias VNEG.
B3	LCM_EN1	Enable input for LCD bias VPOS.
B4	VPOS	LCD bias positive output. Connect a 10μF decouple ceramic capacitor between this pin and ground.
C1	LED4	Backlight LED current sink 4 input. Connect the cathode of LED string 4 to this pin.
C2	SCL	I^2C serial clock input. An external pull-up resistor is required.
C3	SDA	I^2C serial data input/output. An external pull-up resistor is required.
C4	LCM_OUT	LCD bias boost output. Connect a 10μF decouple ceramic capacitor between this pin and LCM_GND pin.
D1	LED3	Backlight LED current sink 3 input. Connect the cathode of LED string 3 to this pin.
D2	PWM	Backlight PWM dimming input.
D3	HWEN	Chip enable input.
D4	LCM_SW	LCD bias boost inductor connection.
E1	LED2	Backlight LED current sink 2 input. Connect the cathode of LED string 2 to this pin.
E2	AGND	Analog ground.
E3	LCM_GND	LCD bias boost ground.
E4	BL_GND	Backlight boost ground.
F1	LED1	Backlight LED current sink 1 input. Connect the cathode of LED string 1 to this pin.
F2	BL_OUT	Backlight boost output voltage sense connection.
F3, F4	BL_SW	Backlight boost inductor connection.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- IN, LCM_EN2, LCM_EN1, SCL, SDA, PWM, HWEN ---------- –0.3V to 6V
- C+, VPOS, LCM_OUT ---------- –0.3V to 8.5V
- LCM_SW ---------- –0.3V to 8.5V
  (<200ns) ---------- –2.7V to 18V
- VNEG, C- ---------- –7V to 0.3V
- BL_SW ---------- –0.3V to 33V
  (<200ns) ---------- –9V to 35V
- LED4, LED3, LED2, LED1, BL_OUT ---------- –0.3V to 30V
- Power Dissipation, P_D @ T_A = 25°C
  WL-CSP-24B 1.84x2.68 (BSC) ---------- 2.69W
- Package Thermal Resistance (Note 2)
  WL-CSP-24B 1.84x2.68 (BSC), θ_{JA} ---------- 37.1°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 2.7V to 5V
- LCM_EN1 and LCM_EN2 Voltage ---------- 0V to 1.8V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(T_A = 25°C, V_{IN} = 3.6V, C_1 = C_2 = 10µF, C_3 = C_4 = 1µF, C_5 = C_9 = 10µF, C_6 = C_7 = C_8 = 10µF, L1 = 4.7µH and L2 = 2.2µH, LCD Bias normal mode operation, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
System						
Quiescent Current	I_Q	HWEN = H, Backlight and LCD bias disabled	--	1	7	µA
	I_{Q_BL}	HWEN = H, Backlight enabled at non-switching state, LCD bias disabled	--	1	1.4	mA
	I_{Q_LCM}	HWEN = H, LCD bias enabled with no load in normal mode, Backlight disabled	--	0.5	1	mA
Leakage Current	I_{LEAK}	HWEN = L	--	0.2	0.8	µA
IN Under-Voltage Lockout Threshold	UVLO	Rising	2.15	2.3	2.45	V
UVLO Hysteresis	UVLO_H		--	260	--	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Backlight – Boost						
Output Over-Voltage Threshold	$V_{OUT\_OV\_BL}$	2.7V ≤ V_{IN} ≤ 5V, 0x02[7:5] = 011 to 111	28.5	29	29.5	V
		2.7V ≤ V_{IN} ≤ 5V, 0x02[7:5] = 010	24.5	25	25.5	
		2.7V ≤ V_{IN} ≤ 5V, 0x02[7:5] = 001	20.5	21	21.5	
		2.7V ≤ V_{IN} ≤ 5V, 0x02[7:5] = 000	16.3	17	17.7	
Current Sink Regulation Voltage	V_{HR}	I_{LED} = 5mA	--	120	--	mV
		I_{LED} = 30mA	--	310	--	
Current Sink Minimum Regulation Voltage	V_{HR_min}	I_{LED} = 95% of $I_{LED\_nominal\_5mA}$	--	30	50	mV
Low-Side MOSFET On Resistance	$R_{ON\_LG\_BL}$	From BL_SW pin to BL_GND pin	--	0.2	--	Ω
Inductor Peak Current Limit	$I_{CL\_PK\_BL}$	2.7V ≤ V_{IN} ≤ 5V, 0x11[1:0] = 11	1584	1800	2016	mA
		2.7V ≤ V_{IN} ≤ 5V, 0x11[1:0] = 10	1320	1500	1680	
		2.7V ≤ V_{IN} ≤ 5V, 0x11[1:0] = 01	1056	1200	1344	
		2.7V ≤ V_{IN} ≤ 5V, 0x11[1:0] = 00	792	900	1008	
Switching Frequency	f_{SW_BL}	2.7V ≤ V_{IN} ≤ 5V, 0x03[7] = 1	900	1000	1100	kHz
		2.7V ≤ V_{IN} ≤ 5V, 0x03[7] = 0	450	500	550	
Maximum Duty Cycle	D_{MAX_BL}	2.7V ≤ V_{IN} ≤ 5V	--	92	--	%
Backlight – Current Sink						
Minimum Output Current	I_{LED_MIN}	2.7V ≤ V_{IN} ≤ 5V, 0x04 = 01h, 0x05 = 00h, linear mode or exponential mode	--	60	--	μA
Maximum Output Current	I_{LED_MAX}	2.7V ≤ V_{IN} ≤ 5V, 0x04 = 07h, 0x05 = FFh, linear mode or exponential mode	--	30	--	mA
Current Accuracy	I_{LED_ACC}	2.7V ≤ V_{IN} ≤ 5V, 60μA ≤ ILED ≤ 30mA, linear mode or exponential mode	–3	--	3	%
Current Matching	I_{LED_MATCH1}	2.7V ≤ V_{IN} ≤ 5V, 60μA ≤ ILED ≤ 2mA, linear mode or exponential mode	–3	--	3	%
	I_{LED_MATCH2}	2.7V ≤ V_{IN} ≤ 5V, 2mA ≤ ILED ≤ 30mA, linear mode or exponential mode	–2	--	2	%
Current Step	$I_{LED\_STEP\_LIN}$	linear mode (code to code)	--	14.63	--	μA
	$I_{LED\_STEP\_EXP}$	Exponential mode (code to code)	--	0.3	--	%
LCD Bias – Boost						
Output Over-Voltage Threshold	V_{LCM_OV}	2.7V ≤ V_{IN} ≤ 5V	--	7.8	--	V
Output Voltage Range	V_{LCM}		4	--	7.15	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage Step			--	50	--	mV
Low-Side MOSFET On Resistance	$R_{ON\_LG\_LCM}$	From LCM_SW pin to LCM_GND pin	--	290	--	mΩ
High-Side MOSFET On Resistance	$R_{ON\_HG\_LCM}$	From LCM_SW pin to LCM_OUT pin	--	170	--	mΩ
Inductor Valley Current Limit	$I_{CL\_VALLEY\_LCM}$		--	1	--	A
Switching Frequency	f_{SW_LCM}	V_{LCM} = 6V, operating under CCM	2.1	2.5	2.9	MHz
LCD Bias – VPOS						
Output Voltage Range	V_{POS}		4	--	6.5	V
Output Voltage Step			--	50	--	mV
Output Voltage Accuracy	V_{POS_ACC}	V_{POS} = 5.4V	–1.5	--	1.5	%
Maximum Output Current	I_{POS_MAX}		150	--	--	mA
Output Current Limit	I_{POS_CL}		--	180	--	mA
Dropout Voltage	V_{DROP_POS}	V_{POS} = 5.7V, I_{POS} = 80mA (Note 5)	--	--	160	mV
Output Discharge Resistor	R_{DIS_POS}		30	80	270	Ω
LCD Bias – VNEG						
Output Voltage Range	V_{NEG}		–6.5	--	-4	V
Output Voltage Step			--	50	--	mV
Output Voltage Accuracy	V_{NEG_ACC}	V_{NEG} = –5.4V	–1.5	--	1.5	%
Maximum Output Current	I_{NEG_MAX}		150	--	--	mA
Output Current Limit	I_{NEG_CL}		--	200	--	mA
Charge-Pump MOSFET On Resistance	R_{ON_Q1}		--	469	--	mΩ
	R_{ON_Q2}		--	280	--	
	R_{ON_Q3}		--	100	--	
	R_{ON_Q4}		--	183	--	
Output Discharge Resistor	R_{DIS_NEG}		--	6	20	Ω

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Logic (HWEN, PWM, LCM_EN1 and LCM_EN2)						
HWEN Pull Down Resistor	R_{PD_HWEN}		--	300	--	kΩ
PWM Pull Down Resistor	R_{PD_PWM}		--	300	--	kΩ
LCM_EN1/ LCM_EN2 Pull Down Resistor	R_{PD_LCMEN}		--	300	--	kΩ
Input Logic Low	V_{IL}	2.7V ≤ V_{IN} ≤ 5V	0	--	0.4	V
Input Logic High	V_{IH}	2.7V ≤ V_{IN} ≤ 5V (Note 6)	1.2	--	V_{IN}	V

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.

Note 6. The maximum voltage applied on LCM_EN1 and LCM_EN2 should be less than V_{IN} - 1V.

System Characteristics

The following specifications are guaranteed by design and are not performed in production testing. (T_A = 25°C, V_{IN} = 3.6V, C_1 = C_2 = 10μF, C_3 = C_4 = 1μF, C_5 = C_9 = 10μF, C_6 = C_7 = C_8 = 10μF, L1 = 4.7μH and L2 = 2.2μH, LCD Bias normal mode operation, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
System						
Over-Temperature Protection	OTP		--	140	--	°C
Over-Temperature Protection Hysteresis	OTP_H		--	20	--	°C
HWEN, LCM_EN1 and LCM_EN2 Control						
HWEN Enable Deglitch	$t_{ON\_DEG\_HWEN}$	Slave address available	--	60	--	ns
HWEN Disable Deglitch	$t_{OFF\_DEG\_HWEN}$	Slave address unavailable	--	200	--	ns
LCM_EN1 / LCM_EN2 Enable Deglitch	$t_{ON\_DEG\_LCM\_EN}$	LCD bias VPOS/ VNEG enabled	--	30	--	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
LCM_EN1 / LCM_EN2 Disable Deglitch	$t_{OFF\_DEG\_LCM\_EN}$	LCD bias VPOS/ VNEG disabled	--	75	--	ns
Backlight – Boost						
Efficiency	Eff_{BL}	I_{LED} = 5mA per LED string, 4P6S	--	90	--	%
Backlight – PWM Dimming Control						
PWM Frequency Range	f_{PWM}		50	--	50000	Hz
PWM Minimum On Time	$t_{ON\_MIN\_PWM}$	PWM sample rate = 24MHz	183.3	--	--	ns
		PWM sample rate = 4MHz	1100	--	--	
		PWM sample rate = 1MHz	4400	--	--	
PWM Minimum Off Time	$t_{OFF\_MIN\_PWM}$	PWM sample rate = 24MHz	183.3	--	--	ns
		PWM sample rate = 4MHz	1100	--	--	
		PWM sample rate = 1MHz	4400	--	--	
PWM Resolution	PWM_{RES}	f_{PWM} = 2kHz to 11kHz, select PWM sample rate = 24MHz f_{PWM} = 200Hz to 2kHz, select PWM sample rate = 4MHz f_{PWM} = 50Hz to 500Hz, select PWM sample rate = 1MHz	--	11	--	bits
Turn On Delay Time	t_{START_UP}	PWM sample rate = 4MHz, PWM duty from 0% to 50%	--	3.5	--	ms
PWM Shutdown Period	t_{STBY}	PWM sample rate = 24MHz	0.54	0.6	0.66	ms
		PWM sample rate = 4MHz	0.27	3	3.3	
		PWM sample rate = 1MHz	22.5	25	27.5	
PWM Deglitch Time	t_{DEG_PWM}	2.7V ≤ V_{IN} ≤ 5V, 0x10[2:1] = 11	--	200	--	ns
		2.7V ≤ V_{IN} ≤ 5V, 0x10[2:1] = 10	--	160	--	
		2.7V ≤ V_{IN} ≤ 5V, 0x10[2:1] = 01	--	100	--	
		2.7V ≤ V_{IN} ≤ 5V, 0x10[2:1] = 00	--	0	--	
LCD Bias – Boost						
Start-Up Time	t_{ST_LCM}	Channel enabled command (I^2C or LCM_ENx) to V_{LCM} = 100% of setting	--	--	2.5	ms
Efficiency	Eff_{LCM}	V_{LCM} = 5.9V, 6mA ≤ I_{LCM} ≤ 160mA, L2 = 2.2µH (use DEF201610F-2R2M=P2)	--	92	--	%
Load Transient	$V_{LOAD\_TRAN\_LCM}$	V_{LCM} = 5.8V, I_{LCM} = 0mA to 150mA, t_r = t_f = 1.5µs	–150	--	150	mV
Line Transient	$V_{LINE\_TRAN\_LCM}$	I_{LCM} = 30mA, V_{IN} = 3.35V to 3.85V, V_{LCM} = 5.7V, SR_r = SR_f = 100mV/µs, 200Hz, 12.5% duty cycle	–50	25	50	mV
Output Ripple Voltage	$V_{RIPPLE1\_LCM}$	I_{LCM} = 5mA, C_5 = 20µF (nominal)	--	50	--	mV
	$V_{RIPPLE2\_LCM}$	I_{LCM} = 50mA, C_5 = 20µF (nominal)	--	50	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
LCD Bias – VPOS						
Start-Up Time	t_{ST_POS}	V_{POS} = 0% to 100% of setting, 0x0A[5:4] = 01, C_6 = 10μF	--	800	--	μs
Peak Start-Up Inrush Current	$I_{IN\_POS\_START\_UP}$	V_{LCM} = 6.3V, V_{POS} = 5.8V, C_6 = 10μF	--	--	250	mA
Load Transient	$V_{LOAD\_TRAN\_POS}$	I_{POS} = 0mA to 50mA, V_{LCM} = 5.8V, V_{POS} = 5.5V, t_r = t_f = 1μs, C_6 = 10μF (nominal)	--	50	--	mV
		I_{POS} = 0mA to 150mA, V_{LCM} = 6.15V, V_{POS} = 5.8V, t_r = t_f = 10μs, C_6 = 10μF (nominal)	--	50	--	
Line Transient	$V_{LINE\_TRAN\_POS}$	I_{POS} = 5mA, V_{LCM} = 5.8V, V_{POS} = 5.5V, V_{IN} = 3.35V to 3.85V, SR_r = SR_f = 100mV/μs, 200Hz, 12.5% duty cycle	–50	25	50	mV
Load Regulation	$V_{LOAD\_REG\_POS}$	0mA ≤ I_{POS} ≤ 150mA	--	--	20	mV
Output Ripple Voltage	V_{RIPPLE_POS}	0mA ≤ I_{POS} ≤ 150mA	--	--	10	mV
Power Supply Rejection Ratio	$PSRR_{\_POS}$	f = 10Hz to 500kHz, I_{POS} = 40mA, V_{LCM} – V_{POS} ≥ 300mV	25	--	--	dB
LCD Bias – VNEG						
Start-Up Time	t_{ST_NEG}	V_{NEG} = 0% to 100% of setting, 0x0A[3:0] = 0001, C_7 = 10μF	--	1.5	--	ms
Efficiency	$Eff1_{\_NEG}$	V_{LCM} = 5.7V, V_{NEG} = –5.4V, –15mA ≤ I_{NEG} ≤ –5mA	89	--	92	%
	$Eff2_{\_NEG}$	V_{LCM} = 5.7V, V_{NEG} = –5.4V, –80mA ≤ I_{NEG} ≤ –15mA	92	--	93	%
Load Transient	$V_{LOAD\_TRAN\_NEG}$	I_{NEG} = 0mA to –50mA, V_{LCM} = 5.7V, V_{NEG} = –5.4V, t_r = t_f = 1μs, C_7 = 10μF (nominal)	--	100	--	mV
		I_{NEG} = 0mA to –150mA, V_{LCM} = 6.15V, V_{NEG} = –5.8V, t_r = t_f = 10μs, C_7 = C_8 = 10μF (nominal)	--	150	--	
Line Transient	$V_{LINE\_TRAN\_NEG}$	I_{NEG} = –5mA, V_{LCM} = 5.7V, V_{NEG} = –5.4V, V_{IN} = 3.35V to 3.85V, SR_r = SR_f = 100mV/μs, 200Hz, 12.5% duty cycle	–50	25	50	mV
Output Ripple Voltage	V_{RIPPLE_NEG}	I_{NEG} = 0mA to –150mA, V_{LCM} = 6.15V, V_{NEG} = –5.8V, C_7 = C_8 = 10μF (nominal)	--	--	100	mV
I^2C Characteristics						
SCL, SDA High-Level Input Threshold Voltage	V_{IH_I2C}		1.26	--	2.3	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCL, SDA Low-Level Input Threshold Voltage	V_{IL_I2C}		–0.5	--	0.54	V
SDA Digital Output Low	V_{OL_I2C}		--	--	0.36	V
SCL Clock Frequency	f_{CLK}		--	--	1000	kHz
Bus Free Time between Stop and Start Condition	t_{BUF}		0.5	--	--	µs
(Repeated) Start Hold Time	$t_{HD;STA}$		0.26	--	--	µs
(Repeated) Start Setup Time	$t_{SU;STA}$		0.26	--	--	µs
STOP Condition Setup Time	$t_{SU;STO}$		0.26	--	--	µs
SDA Data Hold Time	$t_{HD;DAT}$		0.1	--	--	ns
SDA Valid Time	$t_{VD;DAT}$		--	--	0.45	µs
SDA Valid Acknowledge Time	$t_{VD;ACK}$		--	--	0.45	µs
SDA Setup Time	$t_{SU;DAT}$		50	--	--	ns
SCL Clock Low Time	t_{LOW}		0.5	--	--	µs
SCL Clock High Time	t_{HIGH}		0.26	--	--	µs

Typical Application Circuit

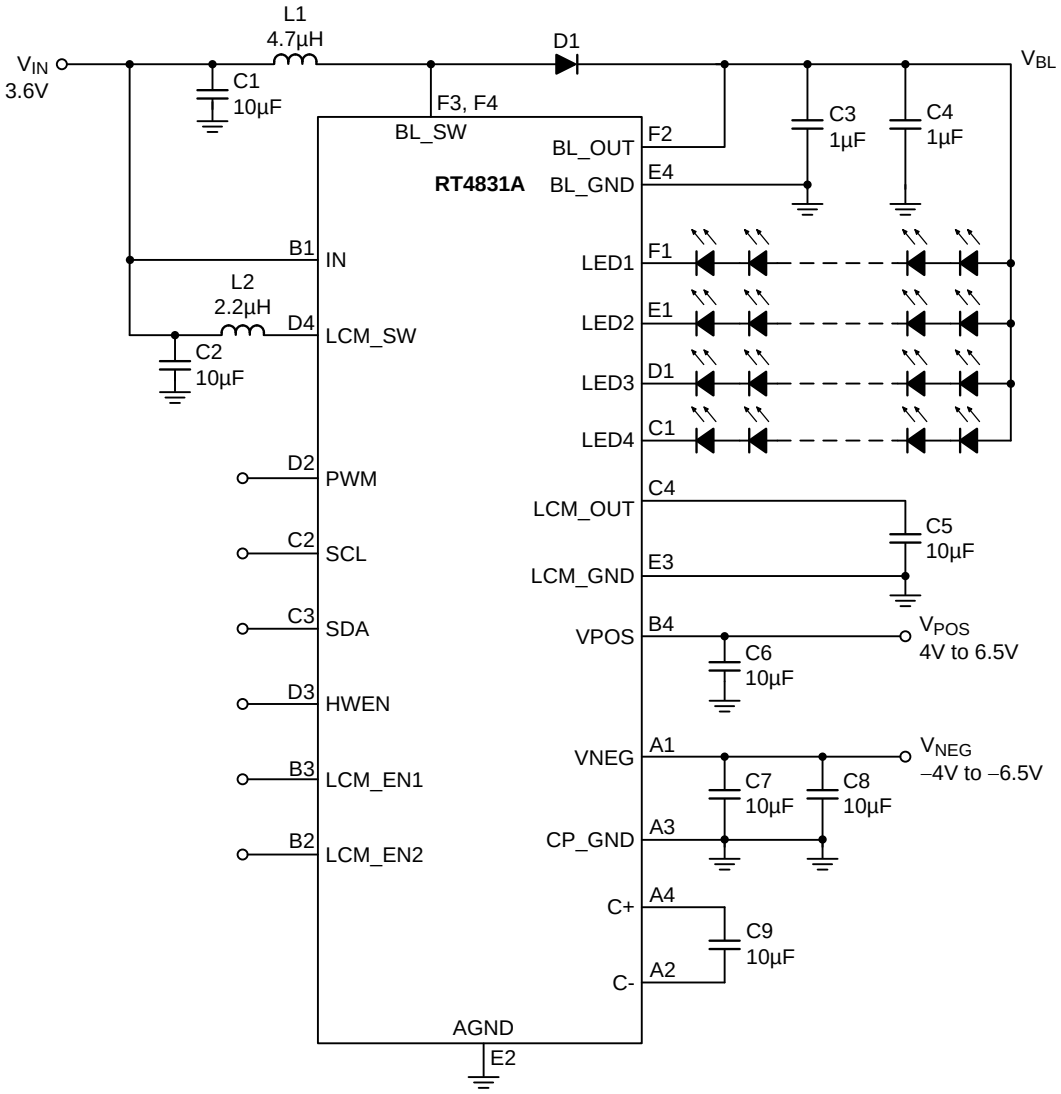
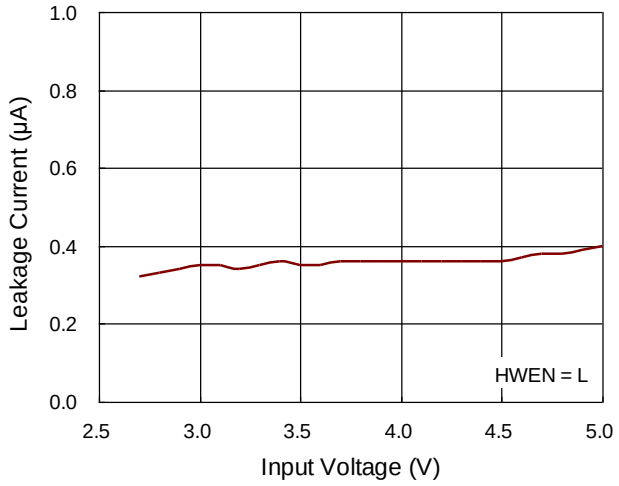


Table 1. Component List of Evaluation Board

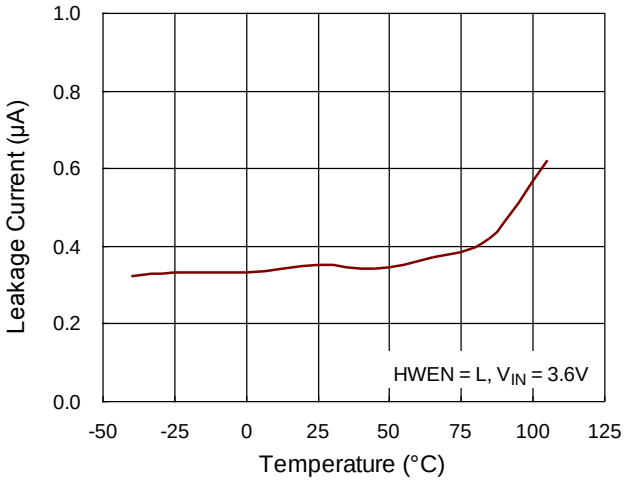
Reference	Qty	Part Number	Description	Package	Manufacturer
C1, C2	1	GRM155R60J106ME44D	10µF/6.3V/X5R	0402	MURATA
C3, C4	1	UMK212ABJ105KD-T	1µF/50V/X5R	0805	TAIYO
C5, C9	1	GRM188R61C106MA73D	10µF/16V/X5R	0603	MURATA
C6, C7, C8	1	GRM188R61A106MAAL	10µF/10V/X5R	0603	MURATA
D1	1	PMEG4010EPK	1A/40V	DFN1608D-2	NEXPERIA
L1	1	VLS252010HBU-4R7M	4.7µH/1.84A/329mΩ	252010	TDK
L2	1	SPH201610H2R2MT	2.2µH/1.45A/264mΩ	201610	SUNLORD

Typical Operating Characteristics

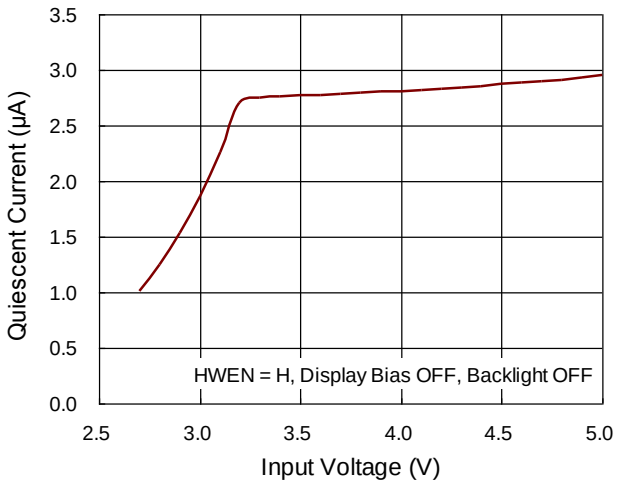
Leakage Current vs. Input Voltage



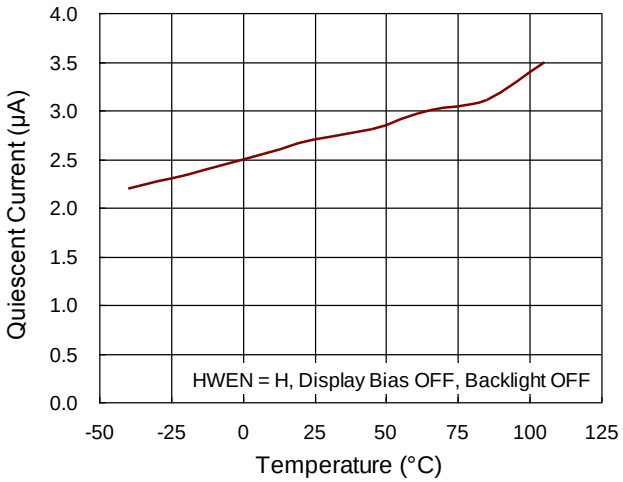
Leakage Current vs. Temperature



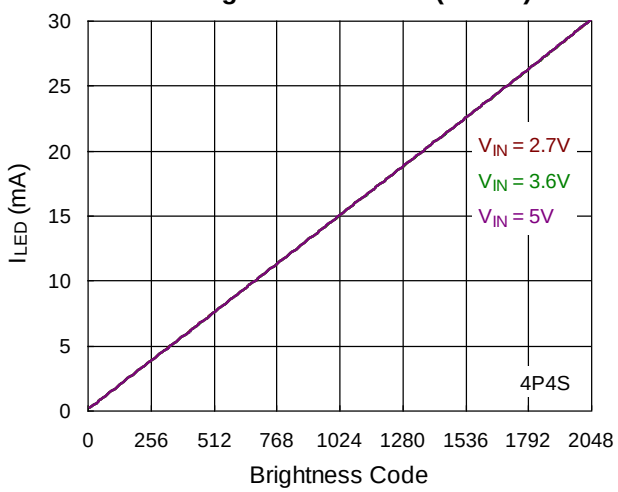
Quiescent Current vs. Input Voltage



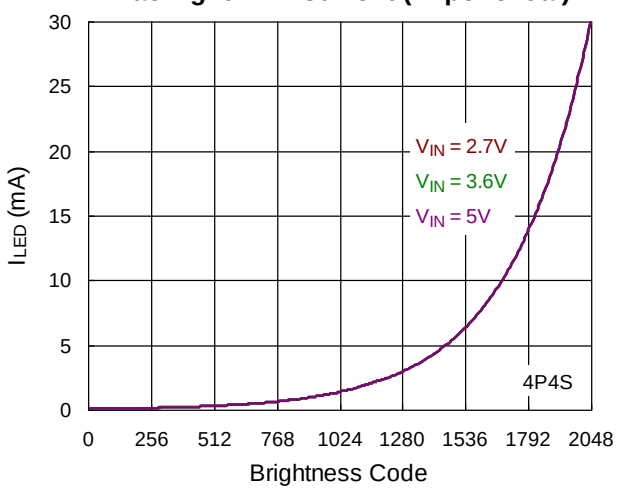
Quiescent Current vs. Temperature



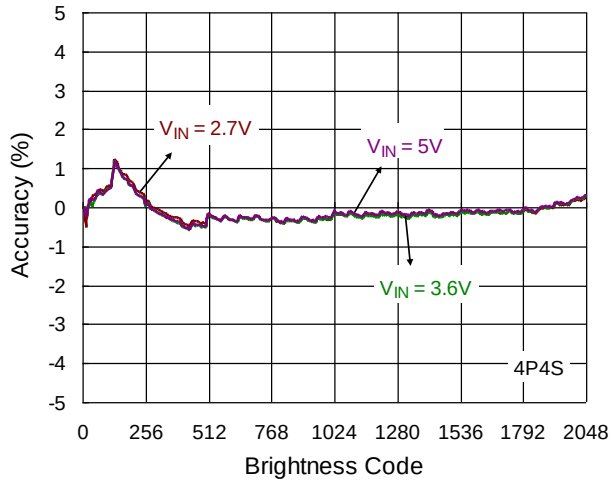
Backlight LED Current (Linear)



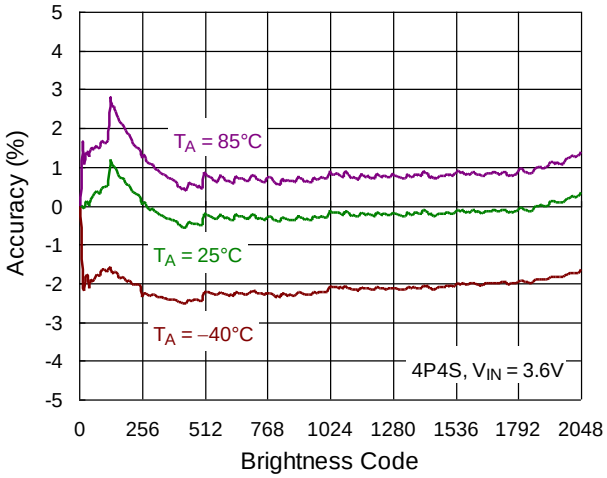
Backlight LED Current (Exponential)



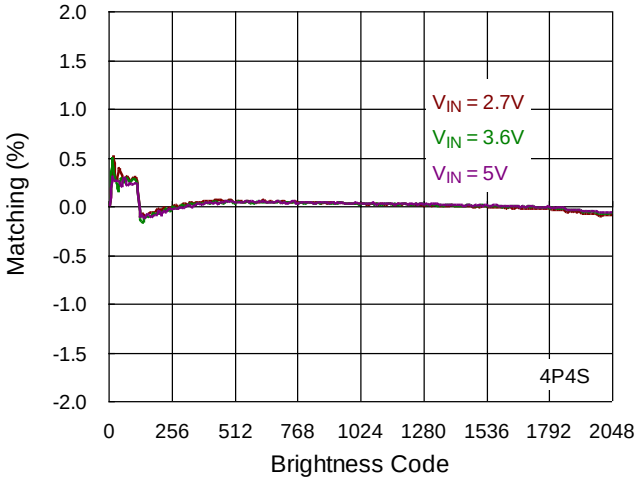
Backlight LED Current Accuracy



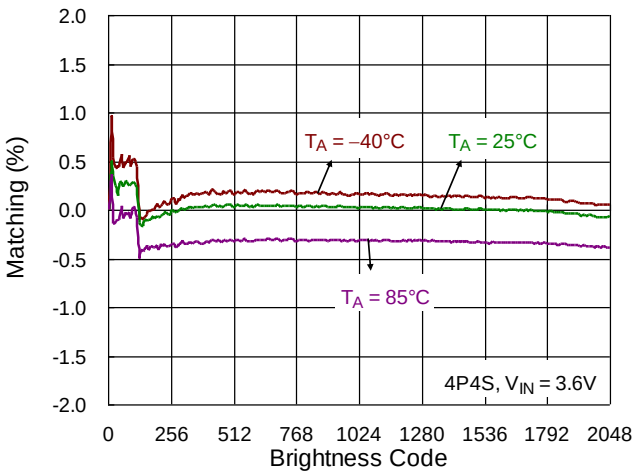
Backlight LED Current Accuracy (Temperature)



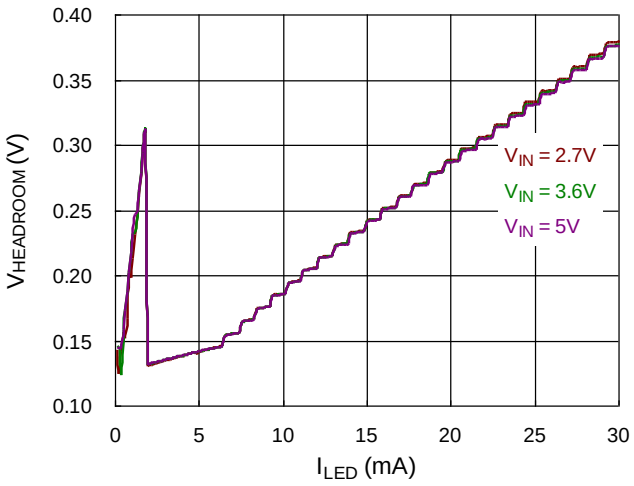
Backlight LED Current Matching



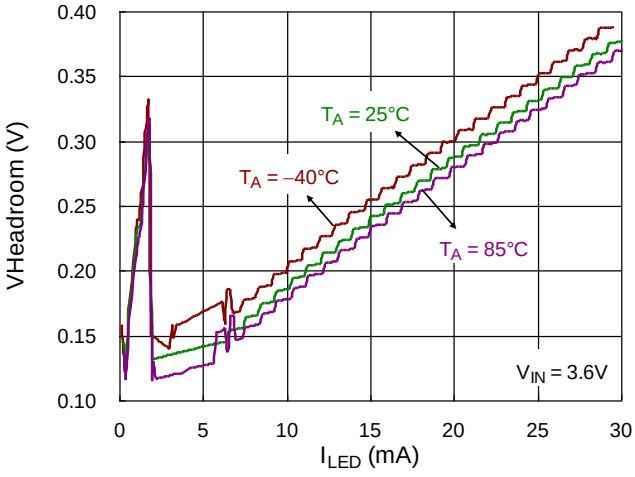
Backlight LED Current Matching (Temperature)



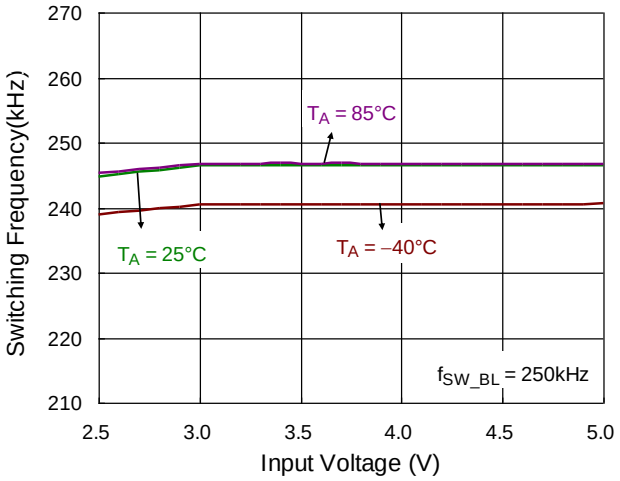
Backlight Regulated Headroom Voltage



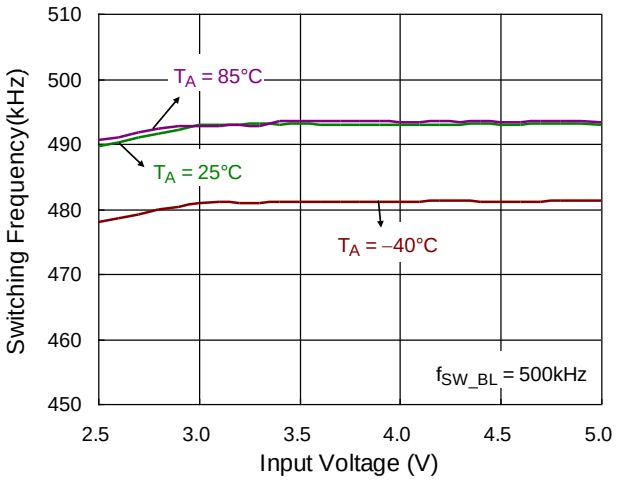
Backlight Regulated Headroom Voltage (Temperature)



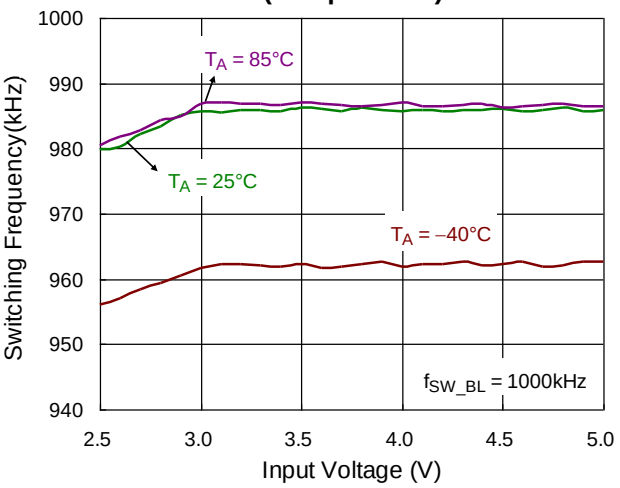
Backlight Boost Switching Frequency (Temperature)



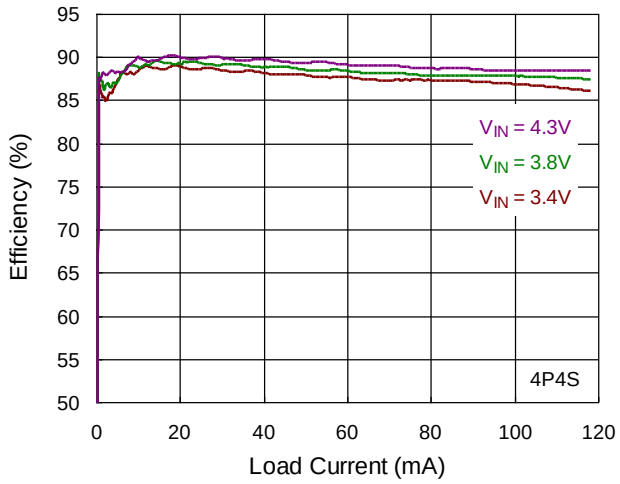
Backlight Boost Switching Frequency (Temperature)



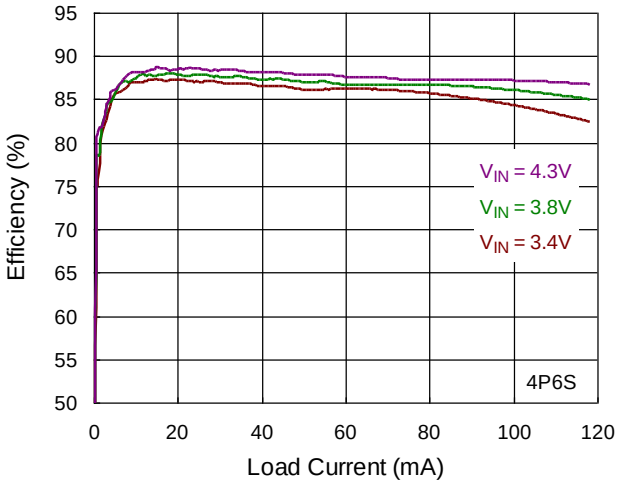
Backlight Boost Switching Frequency (Temperature)



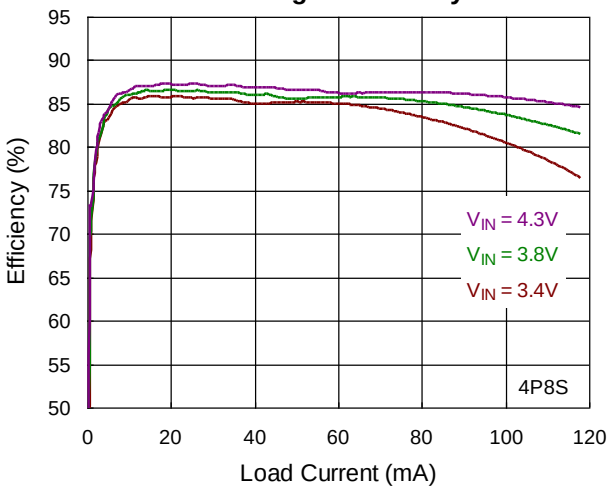
Backlight Efficiency

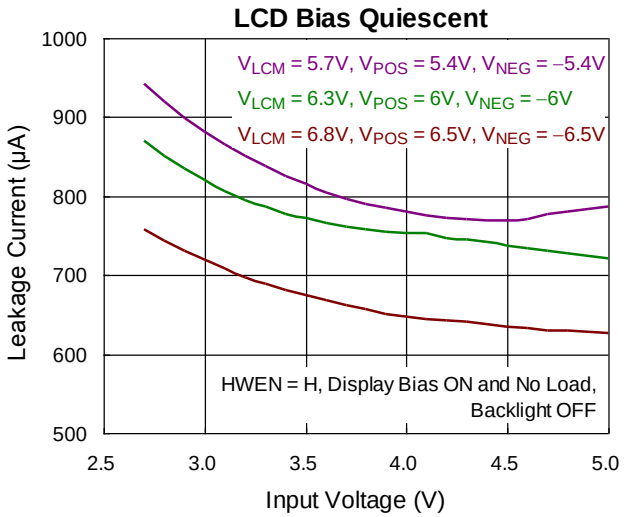


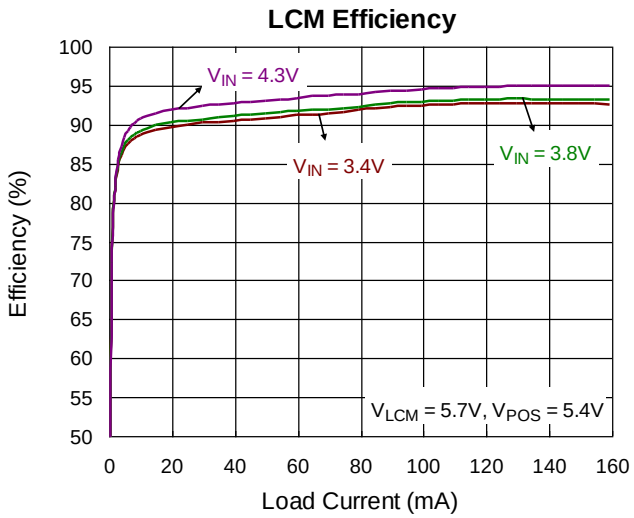
Backlight Efficiency

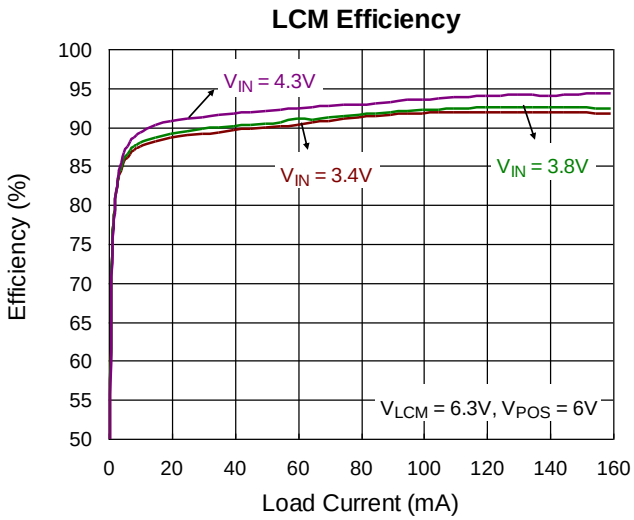


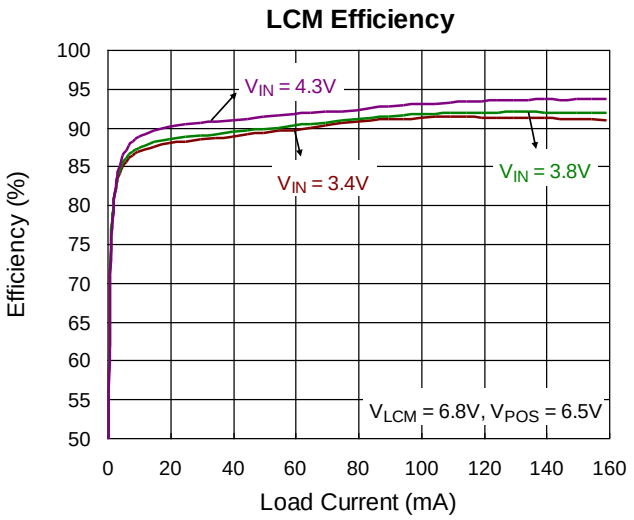
Backlight Efficiency

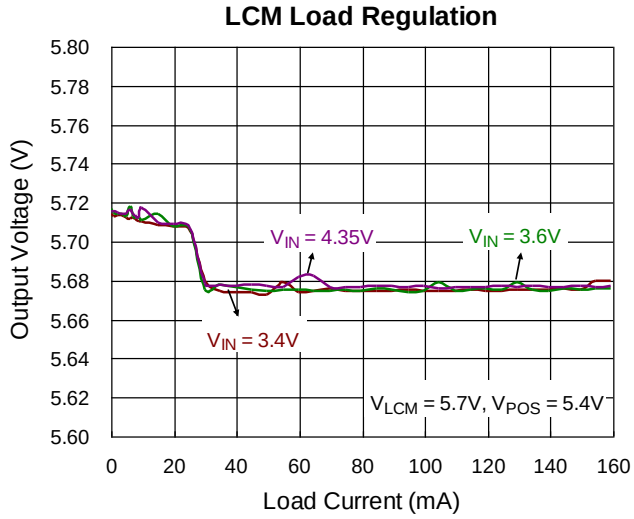


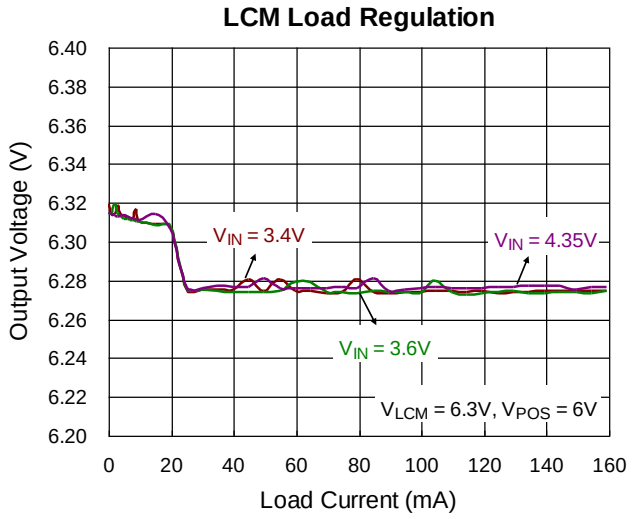




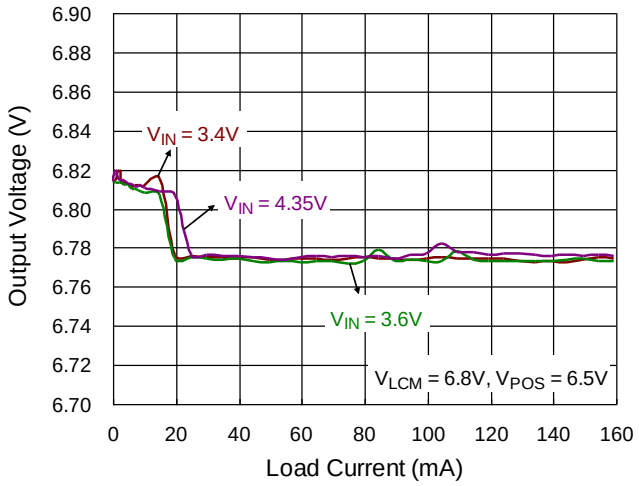




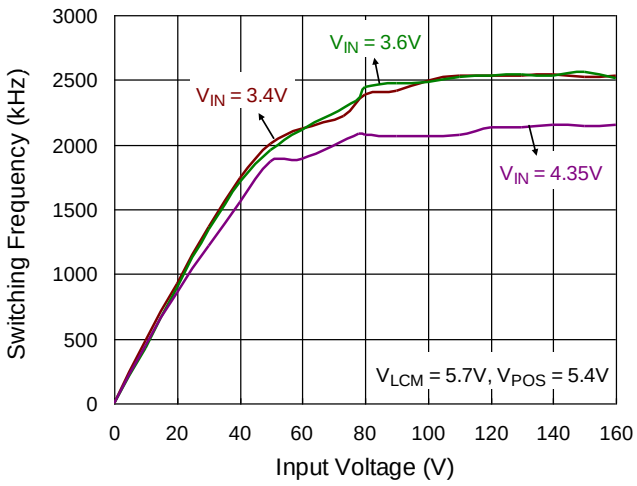




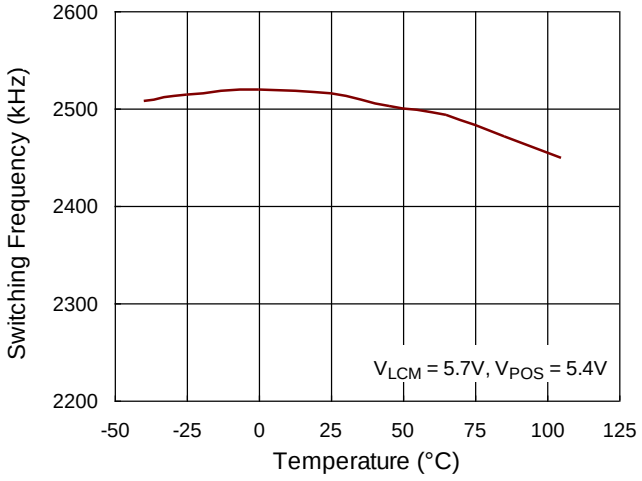
LCM Load Regulation



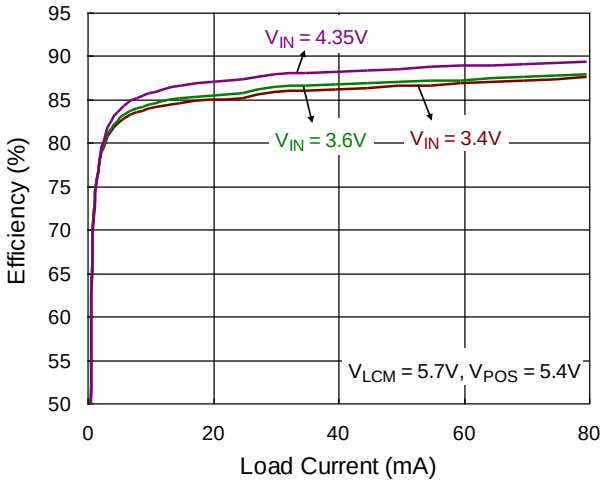
LCM Switching Frequency



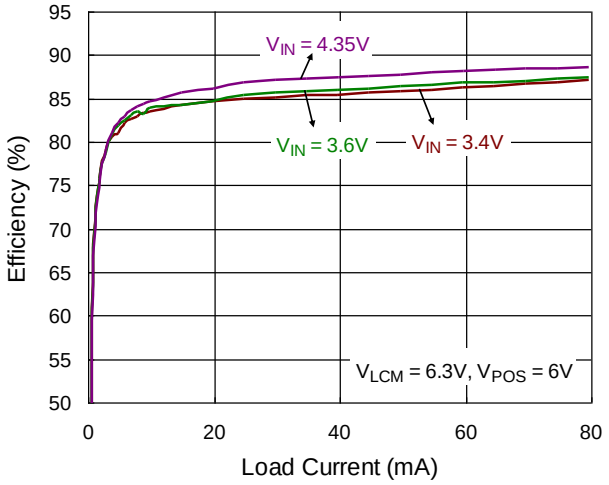
LCM Switching Frequency vs. Temperature



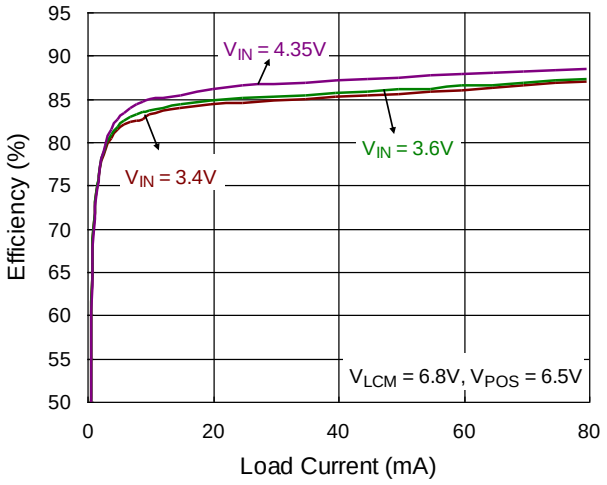
LCM+POS Efficiency



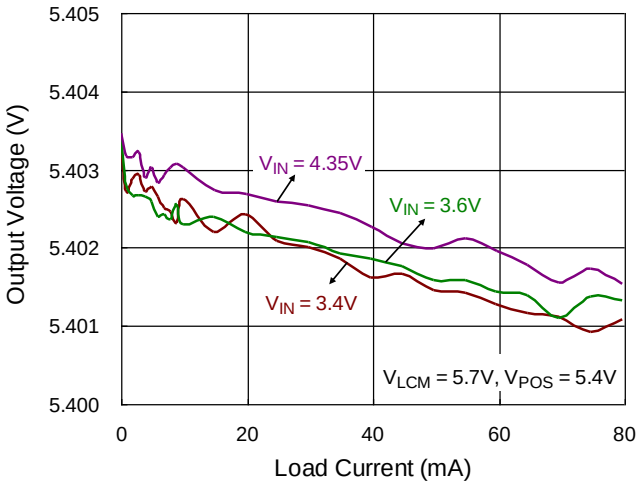
LCM+POS Efficiency



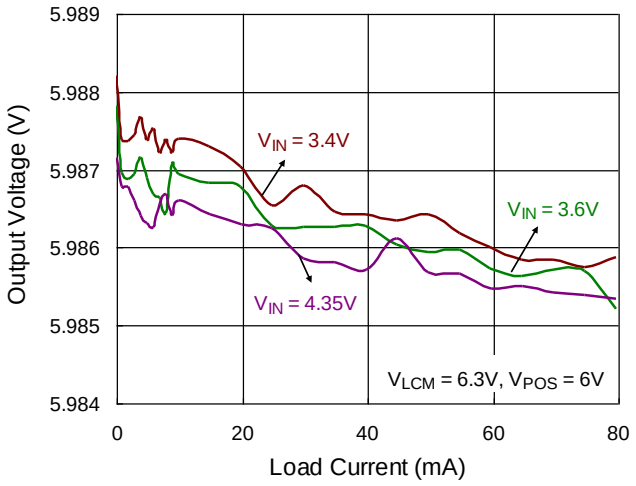
LCM+POS Efficiency



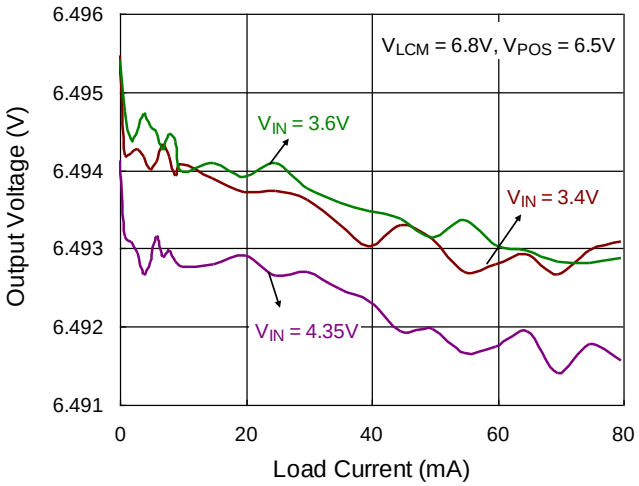
POS Load Regulation



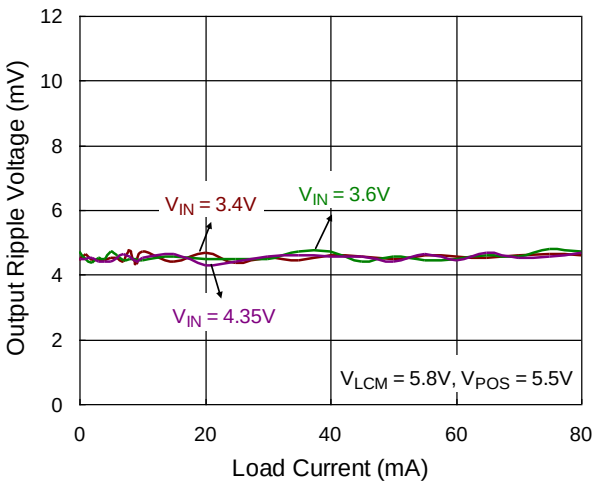
POS Load Regulation



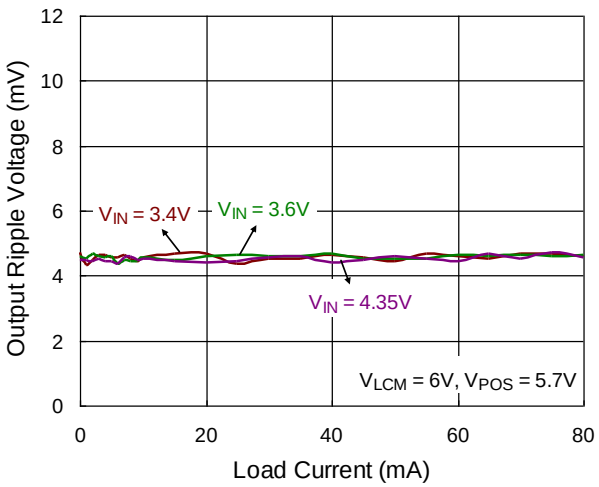
POS Load Regulation



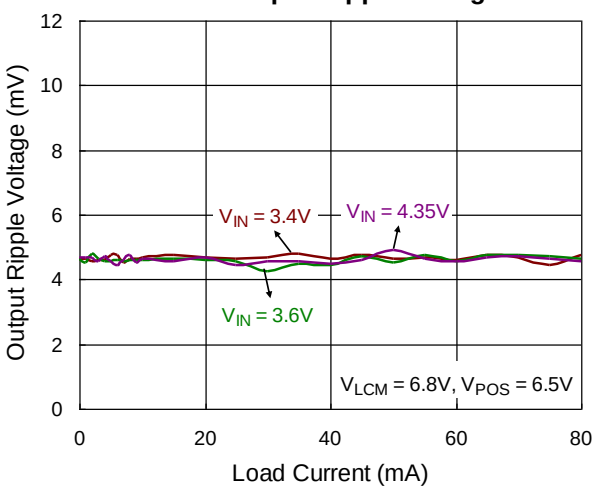
POS Output Ripple Voltage



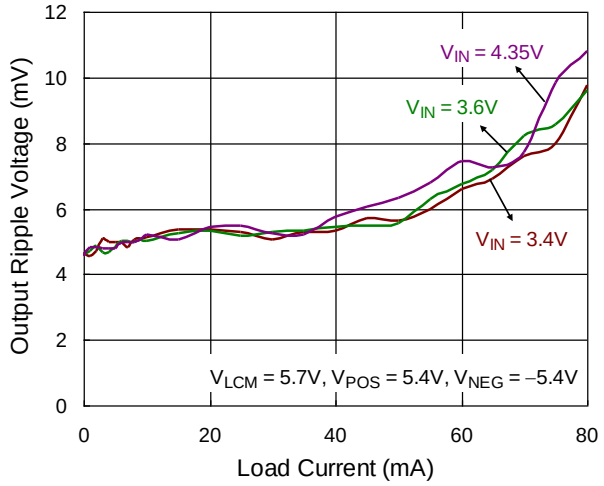
POS Output Ripple Voltage



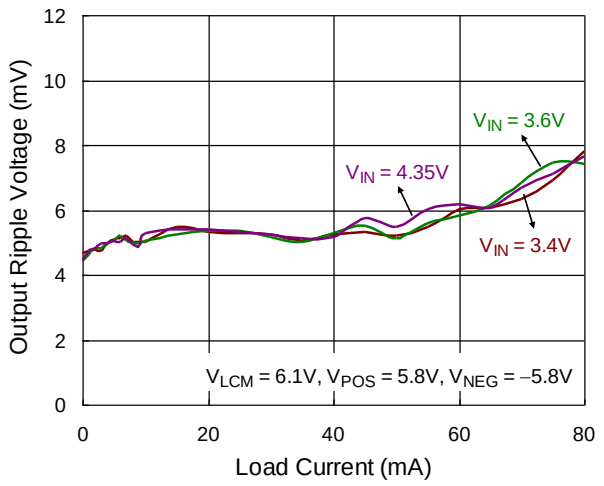
POS Output Ripple Voltage



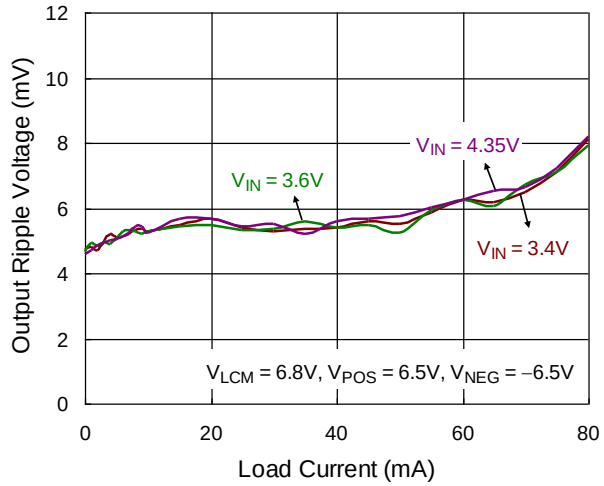
POS Output Ripple Voltage



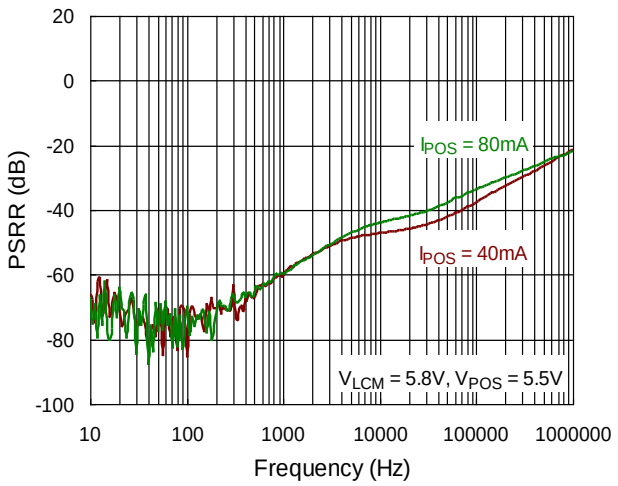
POS Output Ripple Voltage



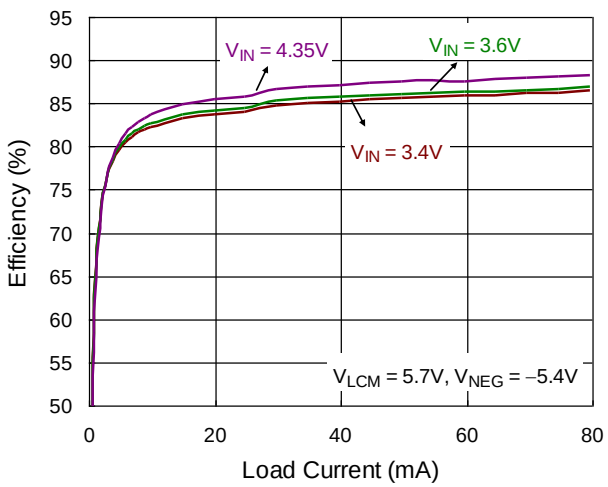
POS Output Ripple Voltage



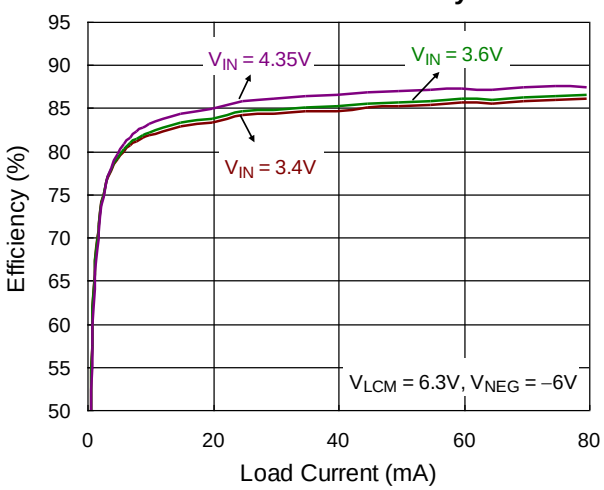
POS Output PSRR



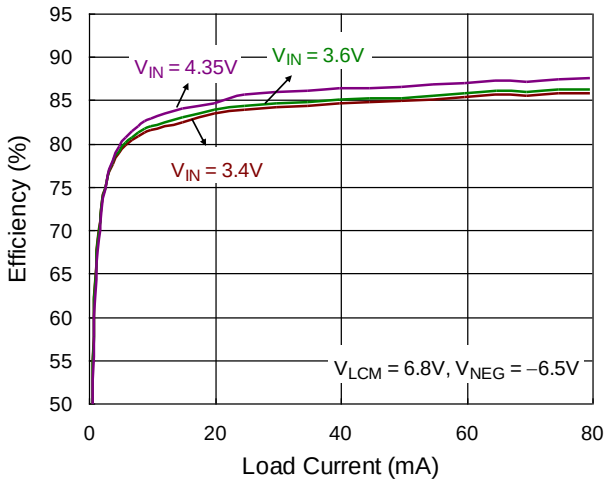
LCM+NEG Efficiency



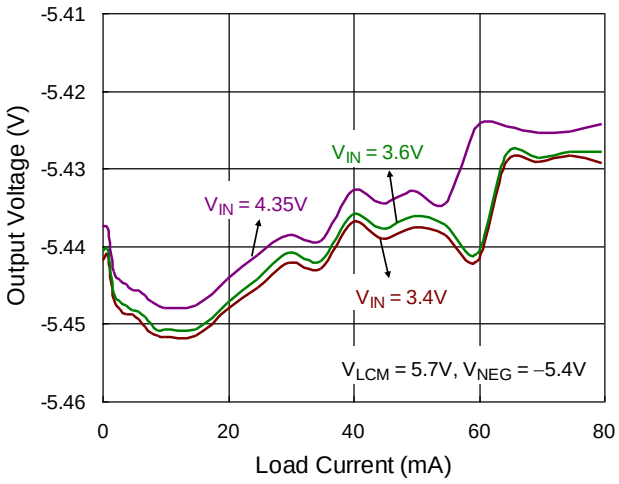
LCM+NEG Efficiency



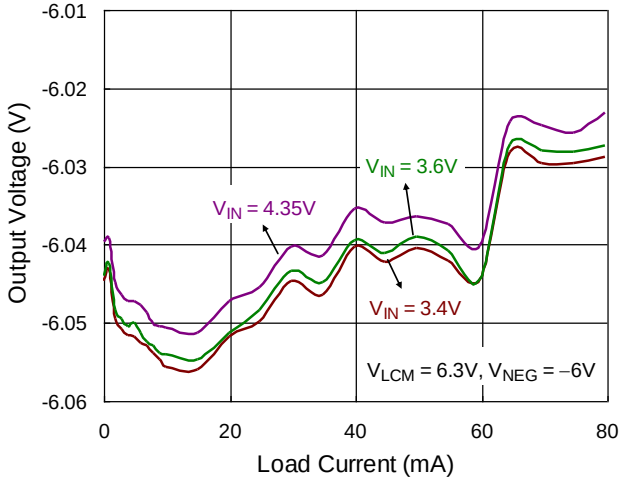
LCM+NEG Efficiency



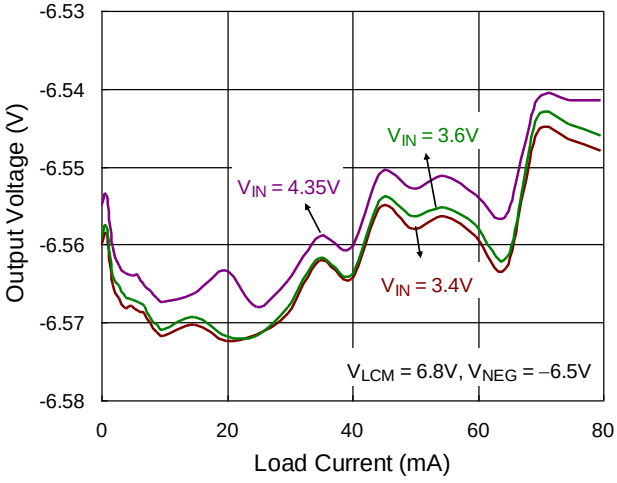
NEG Load Regulation



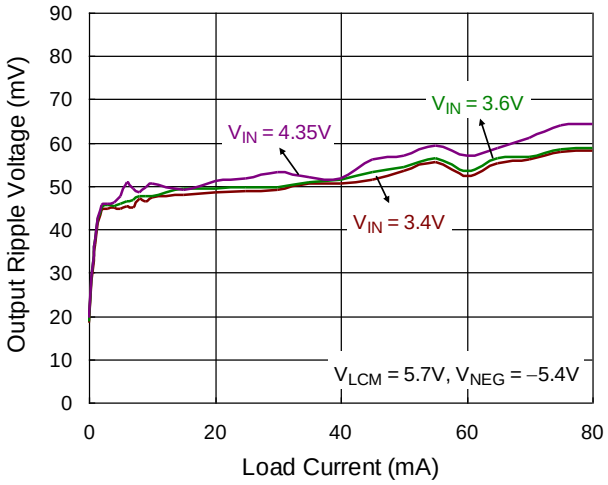
NEG Load Regulation



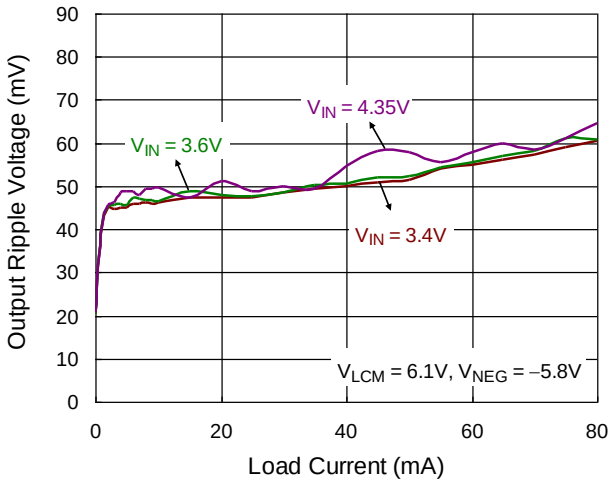
NEG Load Regulation



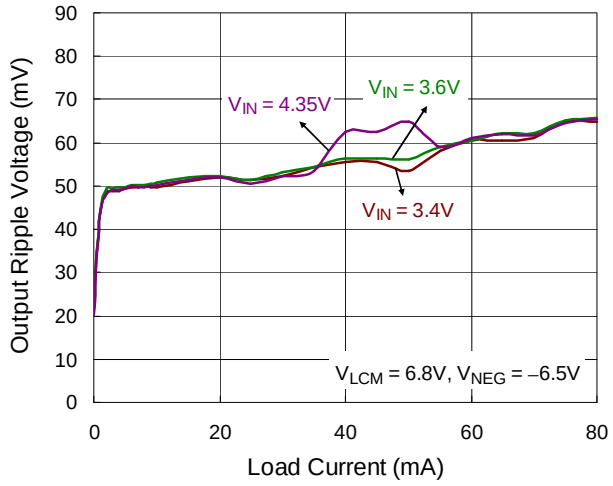
NEG Output Ripple Voltage



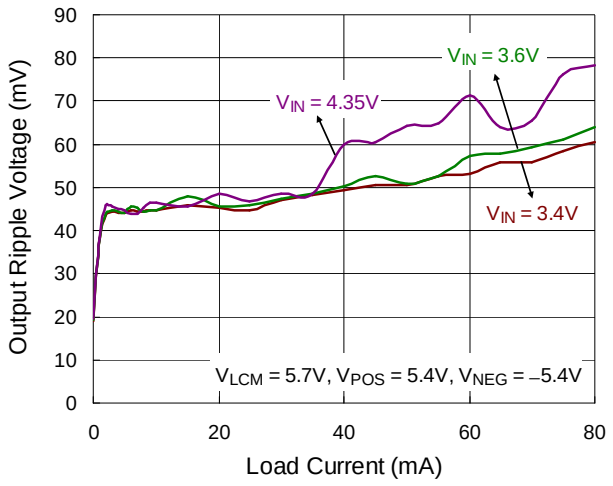
NEG Output Ripple Voltage



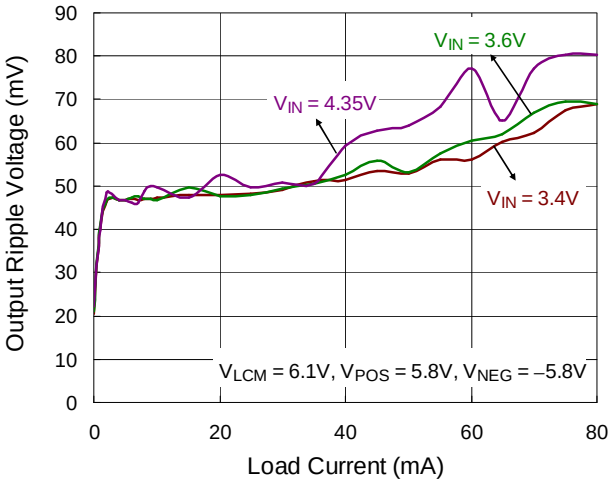
NEG Output Ripple Voltage



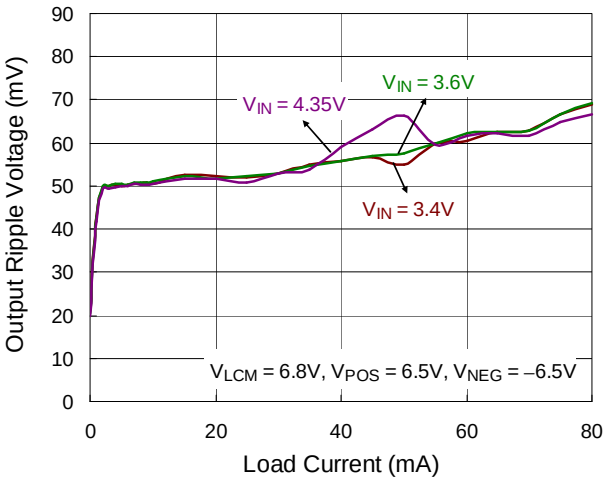
NEG Output Ripple Voltage



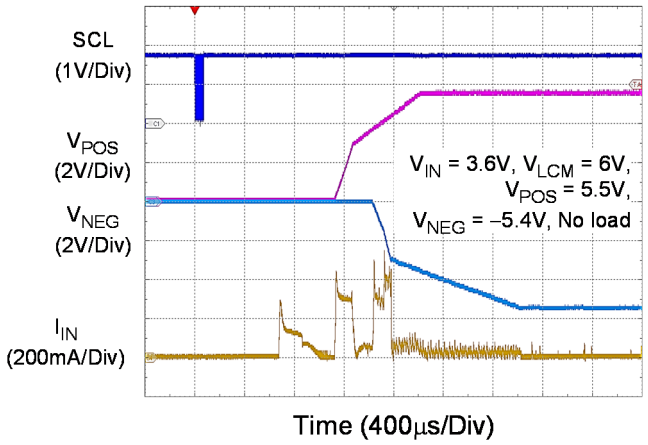
NEG Output Ripple Voltage



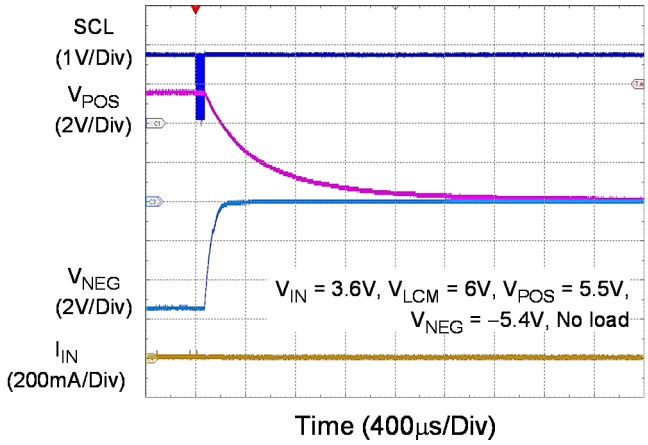
NEG Output Ripple Voltage



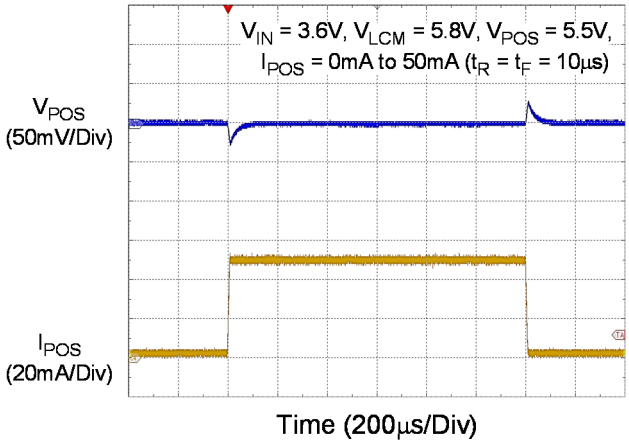
LCD Bias Power On



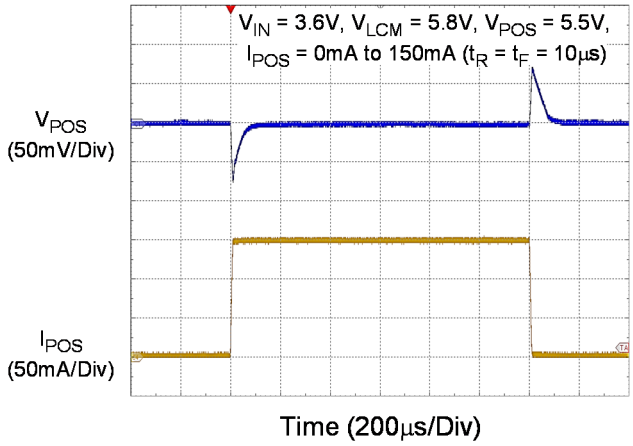
LCD Bias Power Off



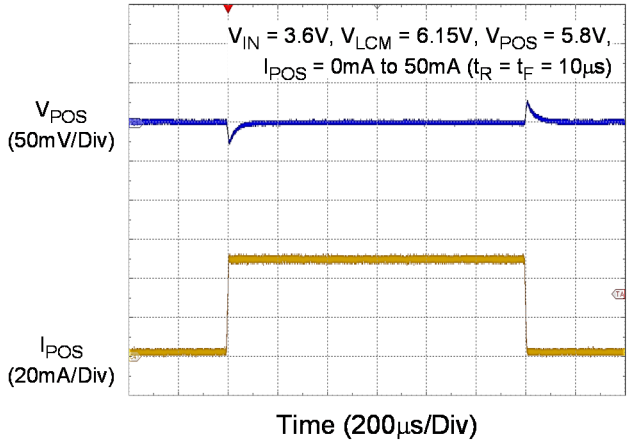
POS Load Transient



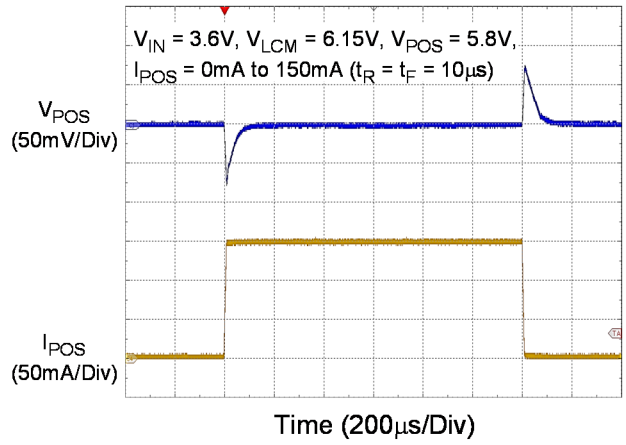
POS Load Transient



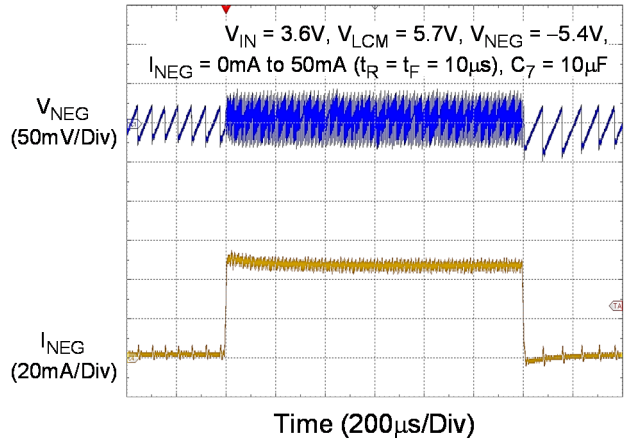
POS Load Transient



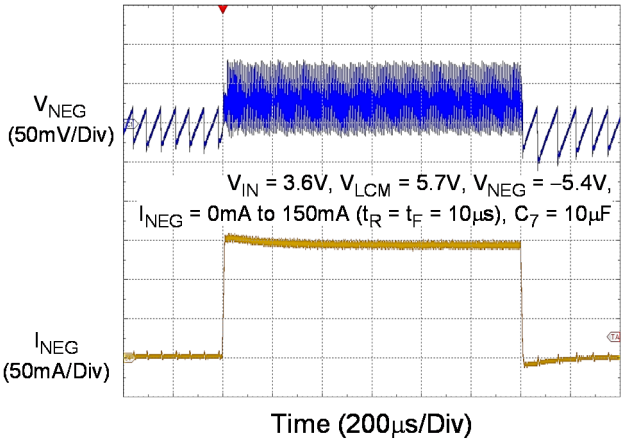
POS Load Transient



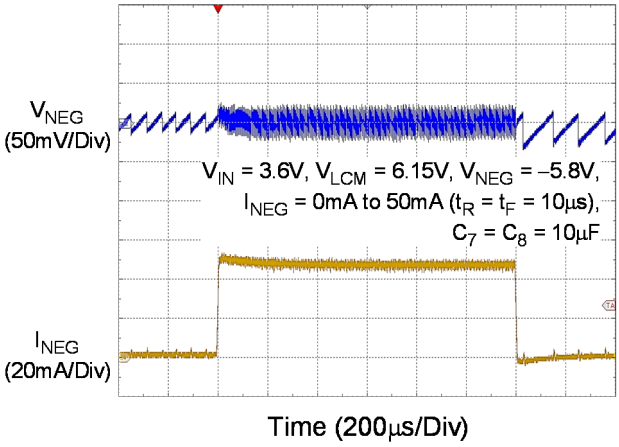
NEG Load Transient



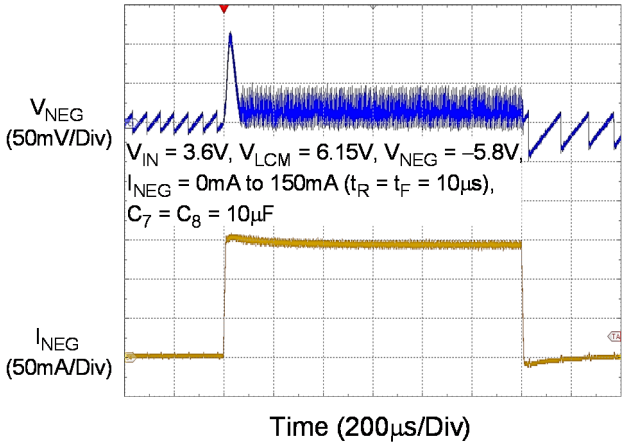
NEG Load Transient



NEG Load Transient



NEG Load Transient



Application Information

The RT4831A is a single chip which includes a four-channel backlight WLED driver and a LCD bias supply.

System Under-Voltage Protection

The RT4831A does not operate with V_{IN} voltage below the Under-Voltage Lock Out (UVLO) level. There is a typical 260mV hysteresis implemented to avoid unstable on/ off behavior. The device is initialized in its default state after V_{IN} voltage recovers from UVLO.

Thermal Protection

The RT4831A features an over-temperature protection (OTP). When the junction temperature exceeds typical 140°C, OTP will be triggered to shut down the device and the OTP flag bit 0x0F[6] is set 1 for notification. When the RT4831A recovers from OTP, it can re-start only with resetting channel enable registers (0x08 for Backlight and 0x09 for LCD bias).

Chip Enable and Disable Control

The HWEN pin controls the RT4831A start up without enabling channels. If HWEN pin is at low state, the RT4831A is in shutdown down mode and I^2C will return NACK to any request. When HWEN pin is at high state, the device is in standby mode and all channels are controllable via I^2C with corresponding ENABLE commands. There are built-in resistors on HWEN, LCM_EN1, LCM_EN2 and PWM pins to keep at low state if pins are left unconnected.

Backlight and LCD Bias Control

- **Backlight**
  - **Operation Control**

    The RT4831A backlight can be controlled by different parameters. Table 1 describes the different backlight operating states.

Table 1. Backlight Control

HWEN	BLED_EN 0x08[4]	BLED_CHx_EN 0x08[3:0]	Brightness Code 0x04[2:0] & 0x05[7:0]	BLED_PWM_EN 0x02[0]	PWM Pin	BLED_CHx_FB_DISABLE 0x10[6:3]	Status
0	X	X	X	X	X	X	Shutdown
1	0	X	X	X	X	X	Standby
1	1	0000	X	X	X	0000	Standby
1	1	1111	= 0	X	X	0000	Standby
1	1	1111	> 0	0	X	0000	ILEDx = BLED Brightness
1	1	1111	> 0	1	Duty = 0	0000	Standby
1	1	1111	> 0	1	Duty > 0	0000	ILEDx = (BLED Brightness x PWM Duty)
1	1	1111	> 0	1	Duty > 0	1111	Standby

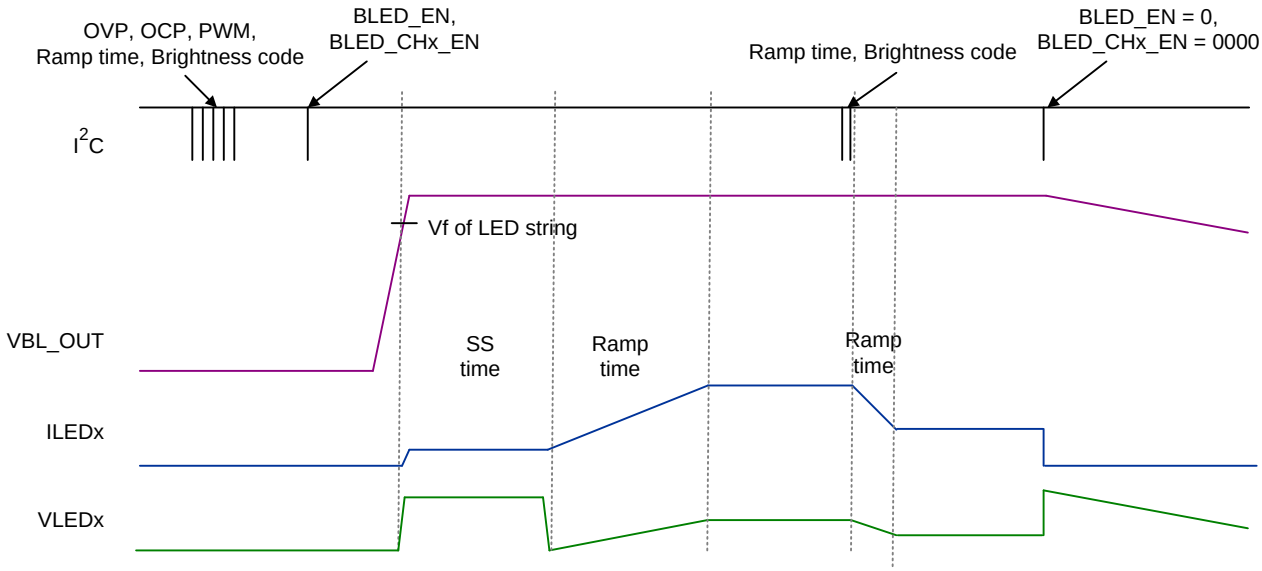


Figure 1. Power Sequence with I^{2}C

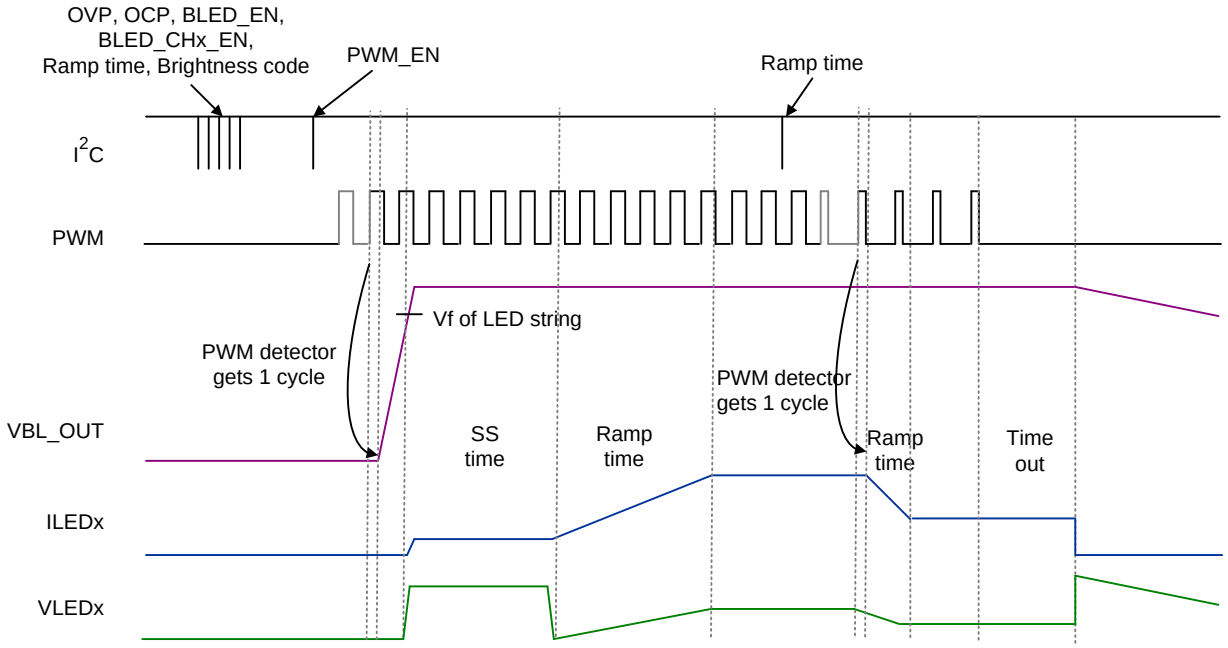


Figure 2. Power Sequence with PWM

Register Programming

The following registers or bits must be programmed while the register bit 0x08[4] = 0 (BLED_EN) and register bit 0x08[3:0] = 0 (BLED_CHx_EN).

- **Register 0x02[0] (BLED_PWM_EN)**
- **Register 0x02[1] (BLED_PWM_RAMP_EN)**
- **Register 0x02[2] (BLED_CONFIG)**
- **Register 0x02[3] (BLED_CODE)**
- **Register 0x03[1:0] (BLED_PWM_HYS)**
- **Register 0x03[2] (BLED_PWM_ SAMPLE)**
- **Register 0x03[6:3] (BLED_RAMPTIME)**
- **Register 0x06 (BLED_AFLT)**
- **Register 0x07 (BLED_AFHT)**
- **Register 0x10[0] (BLED_PWM_24MHz_SAMPLE)**
- **Register 0x10[2:1] (BLED_PWM_DEGLITCH)**
- **Register 0x10[6:3] (BLED_CHx_FB_DISABLE)**
- **Register 0x14[1:0] (BLED_SMOOTH_EN)**

LED Brightness Current Control and PWM Brightness Dimming

The LED brightness current level is controlled via the register only (I^2C) or the register together with PWM duty cycle (I^2C + PWM). The brightness maps to the LED current can be set either linear mapping or exponential mapping.

When register 0x02[0] = 0 (BLED_PWM_EN), the LED current is set via the register and each channel output current for the 11 bits brightness code can be approximate by below equation.

- **Linear Mode**

  ILED = 45.37μA + 14.63μA x brightness code

- **Exponential Mode**

  ILED = 60μA x $1.003040572^{\text{brightness code}}$

When register 0x02[0] = 1 (BLED_PWM_EN), the IC built-in PWM dimming function is activated to participate in controlling the LED brightness current. Each channel output current for the 11 bits brightness code can be approximate by below equation.

- **Linear Mode (PWM)**

  ILED = 45.37μA + 14.63μA x brightness code x PWM Duty

- **Exponential Mode (PWM)**

  ILED = 60μA x $1.003040572^{\text{brightness code x PWM Duty}}$

PWM Resolution and Input Frequency Range

The PWM input frequency must be operated at range from 50Hz to 50kHz. To achieve the full 11-bit maximum resolution of PWM duty cycle to the LED brightness code, the input PWM duty cycle must be ≥ 11-bits, and the PWM sample period ($1/f_{SAMPLE}$) must be smaller than the minimum PWM input pulse width. Figure 3 shows the ideal maximum resolutions based on the input PWM frequency. The minimum PWM frequency for each PWM sample rate is based on PWM timeout. Note to set register 0x08[4] = 0 (BLED_EN) before changing the different PWM sampling rate.

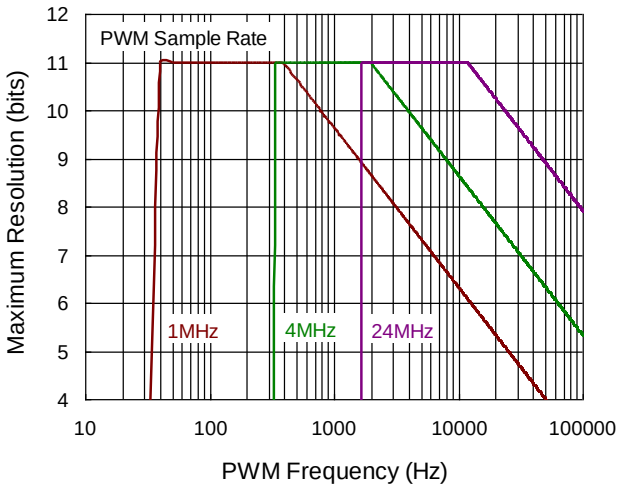


Figure 3. PWM Sample Rate, Resolution, and PWM Input Frequency

Table 2. Input Quiescent with Different Dimming Mode

Dimming Mode	Typical Input Quiescent Current I_{LED} = 30mA/string, 4P4S
I^2C mode	1.75mA
PWM mode, Sample rate = 1MHz	2.18mA
PWM mode, Sample rate = 4MHz	2.21mA
PWM mode, Sample rate = 24MHz	2.37mA

▸ PWM Ramper

The PWM ramper smooths the transition from one brightness value to another. If register 0x02[1] = 0, the PWM duty cycle is multiplied with the I^2C brightness code at the output of the ramper and there is no current ramping between PWM duty cycle change. When 0x02[1] = 1, ramper is activated and ramping is achieved between I^2C x PWM currents. Register 0x03[6:3] is used to set up the up and down ramp time. Ramp time is always same regardless the amount of change in brightness.

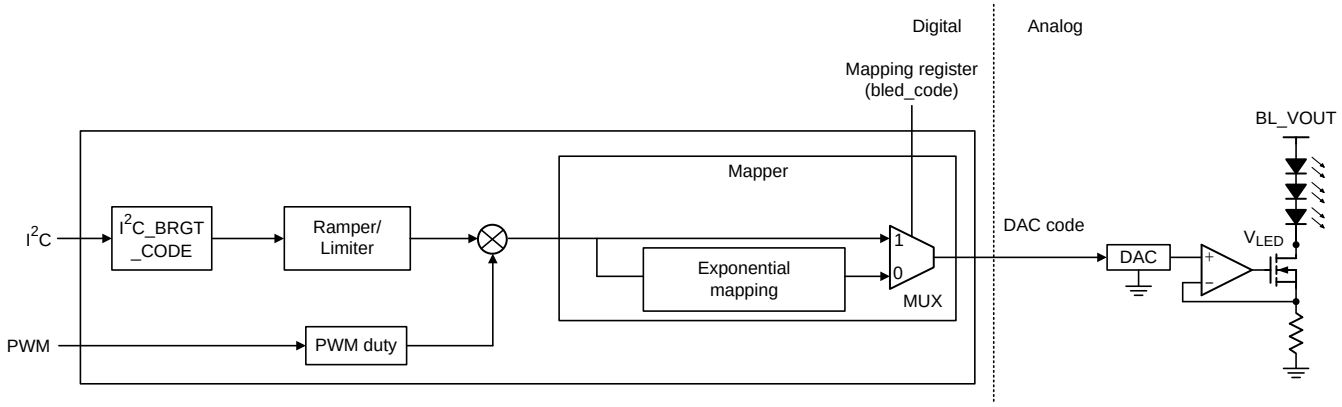


Figure 4. I^2C + PWM Brightness Control, 0x02[1] = 0, PWM Ramper Disabled

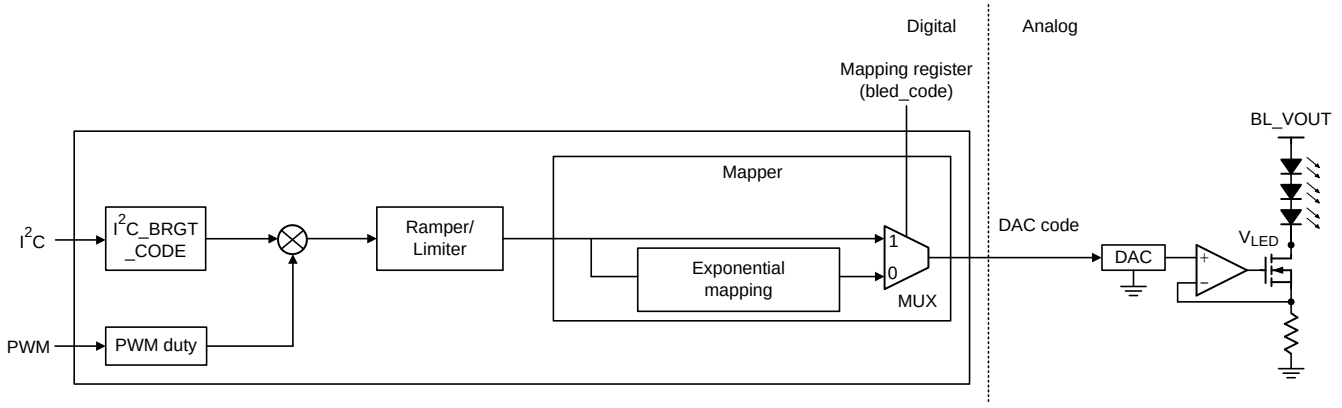


Figure 5. I^2C + PWM Brightness Control, 0x02[1] = 1, PWM Ramper Enabled

PWM Hysteresis

The RT4831A provides unidirectional hysteresis design to prevent jitter at the input PWM signal without reducing the resolution. There are 4 selectable hysteresis settings with register 0x03[1:0]. The hysteresis options for the 1MHz and 4MHz PWM sample rate settings are 1, 2, 4, and 6 bits and for the 24MHz PWM sample rate setting are 0, 1, 2, and 3 bits. Note to set register 0x08[4] = 0 (BLED_EN) before changing the different PWM hysteresis. Refer to below figure for explanations.

(a) PWM duty changes with the same direction. (increase or decrease) LED current changes following the new PWM duty even it does not overcome the PWM hysteresis.

(b) PWM duty changes with reverse direction of the previous duty.

(b-1) If the new PWM duty does not overcome the hysteresis, the LED current keeps the original value without any change.

(b-2) If the new PWM duty overcomes the hysteresis, the LED current changes following the changed PWM duty.

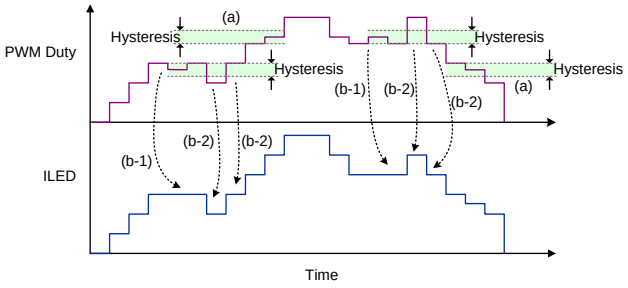


Figure 6. PWM Hysteresis

PWM Timeout

The RT4831A features PWM timeout function to turn off boost output if no PWM pulse detected when the PWM dimming is enabled. The timeout duration changes based on the PWM sample rate selected which results in a minimum supported PWM input frequency.

Table 3. PWM Timeout & Minimum Supported PWM Frequency

Sample Rate	Time Out	Minimum PWM Frequency
1MHz	25ms	48Hz
4MHz	3ms	400Hz
24MHz	0.6ms	2000Hz

PWM-to-Digital Code Readback

In PWM mode, the register 0x12[7:0] and 0x13[2:0] can read back the 11 bits PWM duty detector result. With example of readback value 0x3FF (decimal 1023), the PWM duty is calculated approximately 50%. (1023/2047)

Minimum Regulated Headroom Voltage

To optimize the system efficiency, the RT4831A integrates a minimum regulated headroom voltage function with good ILED accuracy and matching performance. Following graph is the VLED tracking target for the minimum one of the VLED strings that is enable.

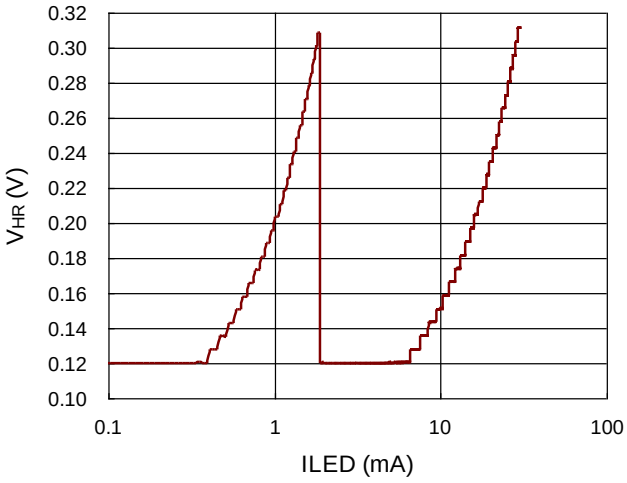


Figure 7. Linear Regulated Headroom Voltage vs. Programmed LED Current

▸ Boost Switching Frequency

The RT4831A serves 2 fixed switching frequency (1MHz and 0.5MHz) and auto-frequency function (1MHz, 0.5MHz and 0.25MHz) to optimize the boost efficiency. When both registers 0x06 (AFLT) and 0x07 (AFHT) are zero code, the boost switching frequency is fixed and the value is set via the register 0x03[7].

Auto-frequency mode is enabled whenever there is non-zero code in either register 0x06 or register 0x07. With comparison of registers 0x05[7:0] (Brightness MSB), 0x06[7:0] and 0x07[7:0], the RT4831A auto switchovers different switching frequency. Table 4 gives an example of boost switching frequency setting. Note the inductor selection and OCP level need to be taken into consideration with different applications.

Table 4. Boost Switching Frequency Setting Example

Brightness MSB 0x05[7:0]	BLED_BST_FREQUENCY 0x03[7]	BLED_AFLT 0x06[7:0]	BLED_AFHT 0x07[7:0]	Switching Frequency
X	0	0x00	0x00	0.5MHz (Fixed)
X	1	0x00	0x00	1MHz (Fixed)
< 0x40	X	0x40	0x80	0.25MHz (Auto)
0x40 ≤ & < 0x80	X	0x40	0x80	0.5MHz (Auto)
≥ 0x80	X	0x40	0x80	1MHz (Auto)

• LCD Bias

▸ Operation Control

The RT4831 LCD bias provides four different operating modes (Normal, Auto, Wake1 and Wake2) for flexible application. Registers 0x09[7:5] are used to control the operating mode.

Table 5. LCD Bias Control

HWEN	DSV_MODE_EN 0x09[7:5]	DSV_VPOS_EN 0x09[2]	DSV_VNEG_EN 0x09[1]	DSV_EXTERNAL_EN 0x09[0]	LCM_EN1	LCM_EN2	Status
Low	XXX	X	X	X	X	X	Shutdown
High	000	X	X	X	X	X	Standby
High	100	0	0	0	X	X	Normal Mode Standby
High	100	X	X	1	0	0	Normal Mode Standby
High	100	1	0	0	X	X	Normal Mode Channel enabled via I^2C VPOS = 0x0D setting target VNEG is off state
High	100	0	1	0	X	X	Normal mode Channel enabled via I^2C VPOS is off state VNEG = 0x0E setting target

HWEN	DSV_MODE_EN 0x09[7:5]	DSV_VPOS_EN 0x09[2]	DSV_VNEG_EN 0x09[1]	DSV_EXTERNAL_EN 0x09[0]	LCM_EN1	LCM_EN2	Status
High	100	1	1	0	X	X	Normal mode Channel enabled via I^{2}C VPOS = 0x0D setting target VNEG = 0x0E setting target
High	100	X	X	1	1	0	Normal mode Channel enabled via external pin VPOS = 0x0D setting target VNEG is off state
High	100	X	X	1	0	1	Normal mode Channel enabled via external pin VPOS is off state VNEG = 0x0E setting target
High	100	X	X	1	1	1	Normal mode Channel enabled via external pin VPOS = 0x0D setting target VNEG = 0x0E setting target
High	101	1	1	0	X	X	Auto sequence mode Channel enabled via I^{2}C VPOS = 0x0D setting target VNEG = 0x0E setting target
High	101	X	X	1	X	1	Auto sequence mode Channel enabled via LCM_EN2 VPOS = 0x0D setting target VNEG = 0x0E setting target
High	110	1	1	X	X	0	Wake1 Mode Standby
High	110	0	0	X	X	1	Wake1 Mode Standby
High	110	1	0	X	X	1	Wake1 Mode VPOS = VIN VNEG is off state
High	110	0	1	X	X	1	Wake1 Mode VPOS is off state VNEG = –VIN
High	110	1	1	X	X	1	Wake1 Mode VPOS = VIN VNEG = –VIN
High	111	1	1	X	X	0	Wake2 Mode Standby
High	111	0	0	X	X	1	Wake2 Mode Standby
High	111	1	0	X	X	1	Wake2 Mode VPOS = 0x0D setting target VNEG is off state

HWEN	DSV_MODE_EN 0x09[7:5]	DSV_VPOS_EN 0x09[2]	DSV_VNEG_EN 0x09[1]	DSV_EXTERNAL_EN 0x09[0]	LCM_EN1	LCM_EN2	Status
High	111	0	1	X	X	1	Wake2 Mode VPOS is off state VNEG = 0x0E setting target
High	111	1	1	X	X	1	Wake2 Mode VPOS = 0x0D setting target VNEG = 0x0E setting target

▸ Normal Mode Control Setting

POS and NEG outputs are regulated to programmed values with normal mode operation. The channel on-off setting of POS and NEG can be programmed via I^{2}C with dedicated registers or external pins.

- Registers 0x09[2]/ 0x09[1] are able to software control POS/ NEG on-off.
- With register 0x09[0]=1, LCM_EN1/ LCM_EN2 are used to hardware control POS/ NEG on-off.

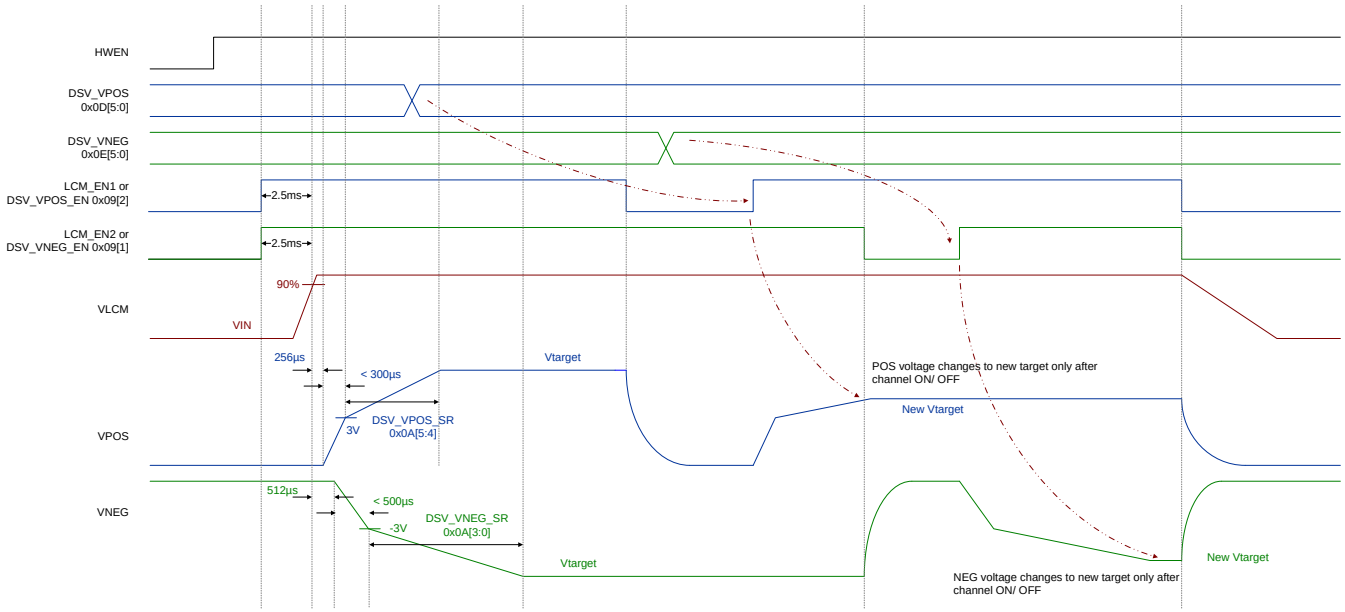


Figure 8. Example for Normal Mode with I^{2}C Software Control or External Pins Control

▸ Auto Mode Control Setting

In auto mode, POS and NEG are on or off in sequence. Within power on sequence, V_{POS} voltage ramp up to the programmed value, then V_{NEG} voltage starts to ramp down to its programmed value after 1.2ms (typ.). Within power-off sequence, V_{NEG} voltage drops to 0V then V_{POS} starts to turn off after 1.2ms (typ.). Channels on-off setting can be programmed via I^{2}C with dedicated registers or external pin.

- Registers 0x09[2] and 0x09[1] are able to software control POS and NEG on-off. Note only both above register bits are written 1, there will be output voltage VPOS and VNEG.
- With register 0x09[0] = 1, LCM_EN2 is used to hardware control POS and NEG on-off.

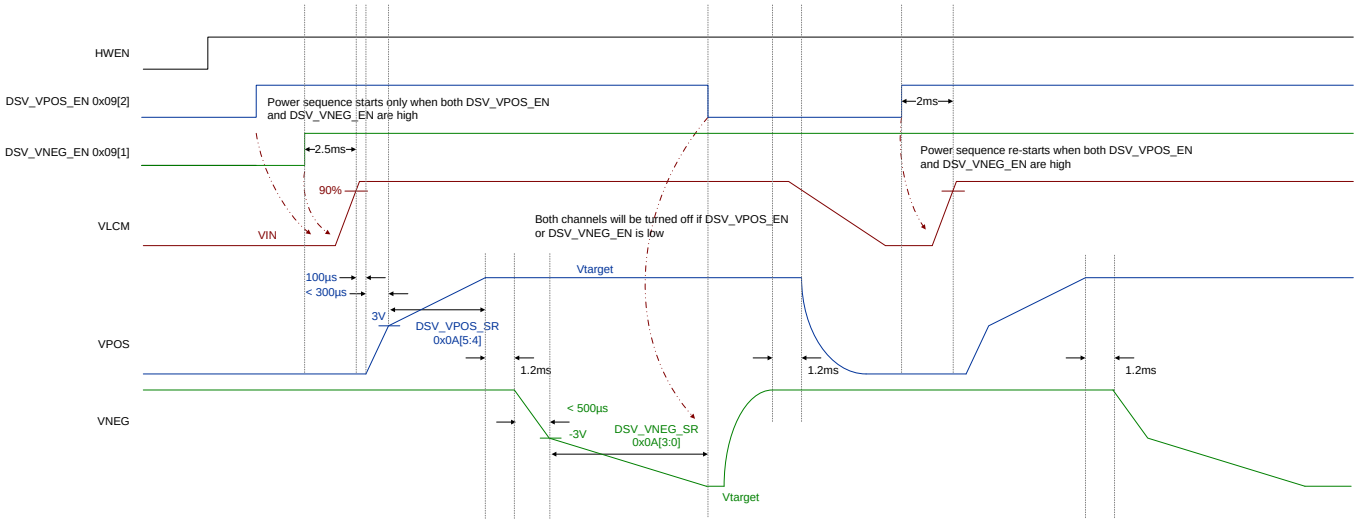


Figure 9. Example for Auto Mode with I^{2}C Software Control

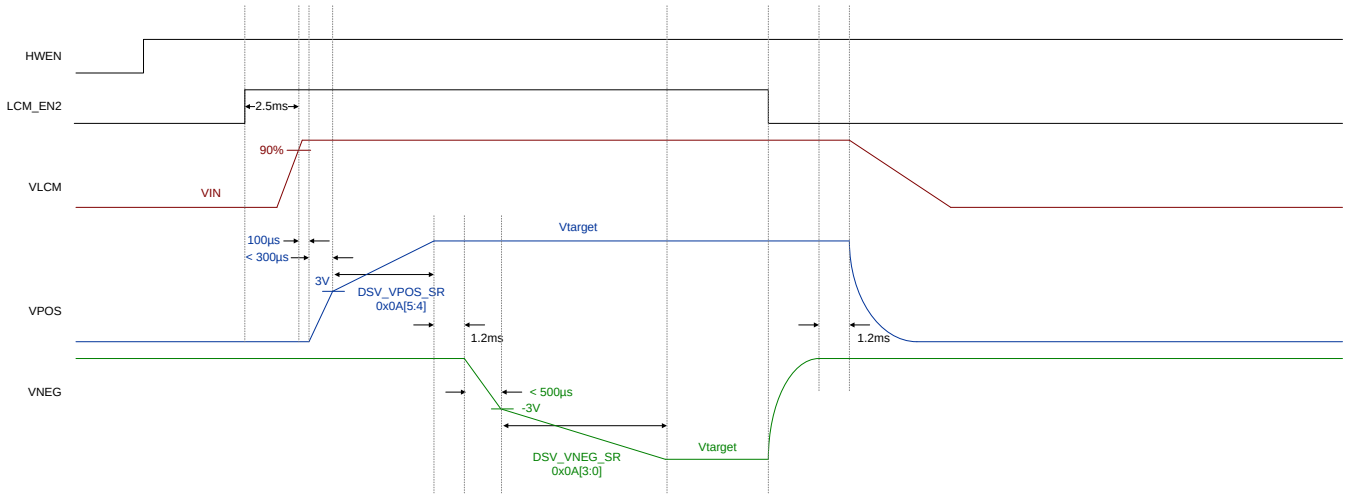


Figure 10. Example for Auto Mode with External Pin Control

▸ Wake1 Mode Control Setting

In wake1 mode, the RT4831A passes V_{IN} through to the LCM boost output, the enabled POS and NEG outputs. Due to the impedance of the LCM boost, the POS LDO and the NEG charge pump, the respective outputs are regulated close to V_{IN} only at very light load current and drops as the load increases. POS and NEG on-off setting can be controlled only by external pin.

- Registers 0x09[2]/ 0x09[1] with external pin LCM_EN2 are used to control POS/ NEG on-off.

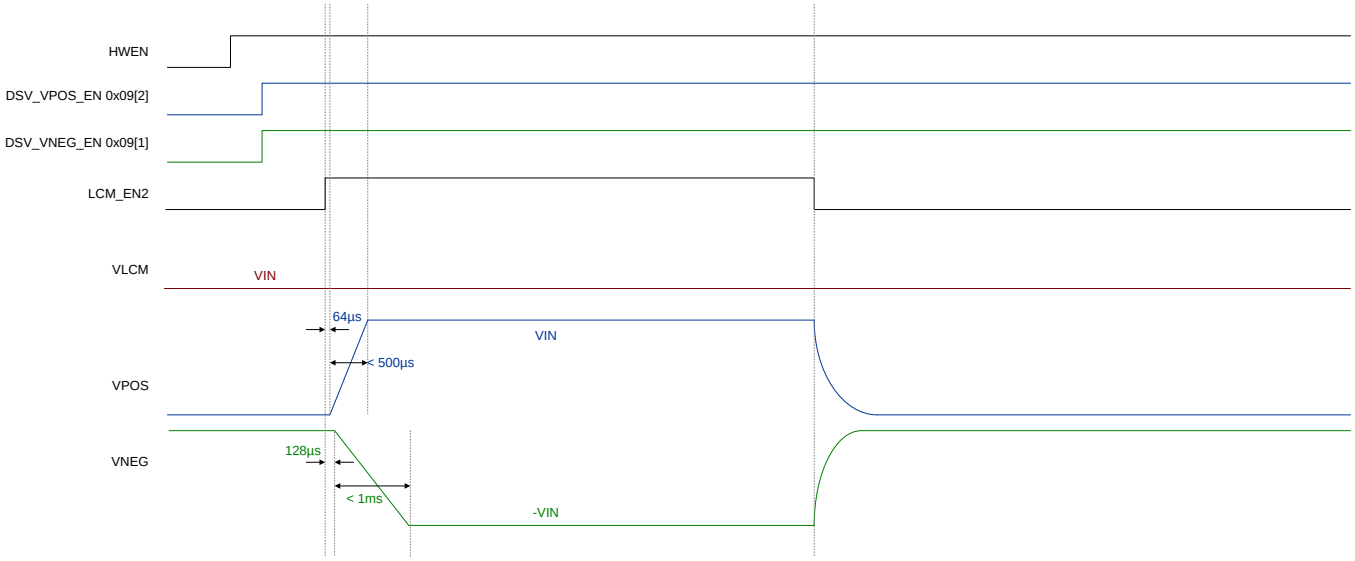


Figure 11. Example for Wake1 Mode with External Pin Control

▸ Wake2 Mode Control Setting

In wake2 mode, the V_{POS} and V_{NEG} are regulated to programmed values. POS and NEG on-off setting can be controlled only by external pin.

- Registers 0x09[2]/ 0x09[1] with external pin LCM_EN2 are used to control POS/ NEG on-off.

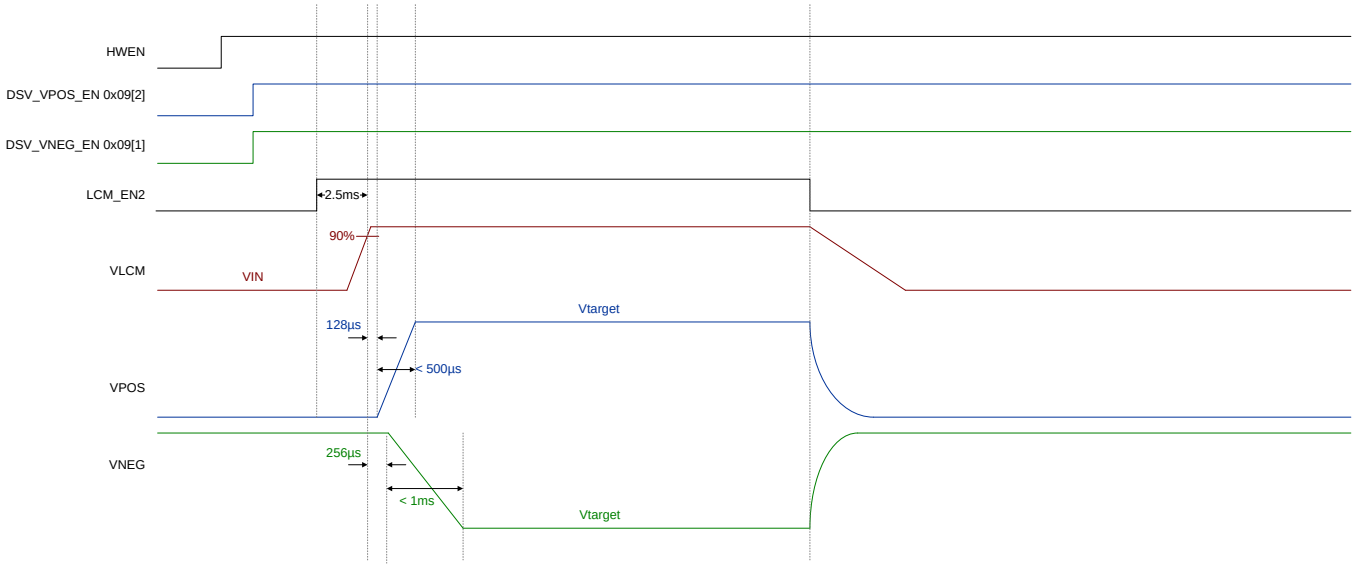


Figure 12. Example for Wake2 Mode with External Pin Control

Output Voltage Setting

The RT4831A LCD bias output voltage V_{LCM}, V_{POS} and V_{NEG} can be programmed via I^2C with dedicated registers.

- **LCM**

  Register 0x0C[5:0] is used to control LCM output voltage ranges from 4V to 7.15V with 50mV step. It is recommended to select V_{LCM} with the estimation : V_{LCM} = max (V_{POS}, |V_{NEG}|)+V_{HR}, where V_{HR} ≥ 200mV for lower currents and V_{HR} ≥ 300mV for higher currents.

- **POS**

  Register 0x0D[5:0] is used to control POS output voltage ranges from 4V to 6.5V with 50mV step. Note the new programmed voltage is not output when channel is at on state. It takes effect only after the channel is disabled and re-enabled.

- **NEG**

  Register 0x0E[5:0] is used to control NEG output voltage ranges from −4V to −6.5V with 50mV step. Note the new programmed voltage is not output when channel is at on state. It takes effect only after the channel is disabled and re-enabled.

Output Active Discharge Setting

The RT4831A integrates internal switch resistors to actively discharge the output voltage when the channel is off.

The POS active discharge function is controlled by register 0x09[4].

The NEG active discharge function is controlled by register 0x09[3].

Channel Protection Features

The RT4831A equips boost output Over-Voltage Protection and LED Over-Current Protection for backlight; LCM output Over-Voltage Protection, and POS/ NEG output Short-Circuit Protection for LCD bias, to prevent the device from damages causing by abnormal operation or fault conditions. (over-load, short-circuit, soldering issue…etc.)

Backlight

Boost Output Over-Voltage Protection

The OVP function prevents the RT4831A from being damaged when LED with no connection or any open circuit conditions. Via the registers 0x02[7:5] and 0x02[4], the RT4831A sets the BLED OVP flag, register 0x0F[1] = 1 for notification or OVP flag with backlight shutdown when over-voltage found on the output terminal. Disabling the OVP shutdown (0x02[4] = 0) function when the quick dimming (>10mA/500μs) application such as CABC to avoid triggering the OVP shutdown.

Over-Current Protection

There are four selectable OCP thresholds with the register 0x11[1:0]. When the inductor current reaches the low-side MOSFET peak current limit threshold, the low-side MOSFET will be turned-off. Meanwhile, the register 0x0F[0] is set 1 for notification. The maximum inductor current is decided by the inductor current rising rate and the response delay time of the internal network.

Below tables are the OCP level setting recommendations for different applications without triggering OCP. Note the inductor saturation current selected should be higher than OCP level.

L = 4.7μH	30mA	25mA	20mA
4P4S	1.5A	1.2A	0.9A
4P5S	1.8A	1.5A	1.2A
4P6S	1.8A	1.5A	1.5A
4P7S	1.8A	1.8A	1.5A
4P8S	1.8A	1.8A	1.5A

L = 10μH	30mA	25mA	20mA
4P4S	1.2A	0.9A	0.9A
4P5S	1.5A	1.2A	0.9A
4P6S	1.8A	1.5A	1.2A
4P7S	1.8A	1.5A	1.2A
4P8S	1.8A	1.8A	1.5A

For different LED applications, the following tables show the V_{IN} operating range due to the maximum duty and OCP limitation.

L = 4.7μH	30mA	25mA	20mA
4P4S	2.5 to 5V	2.5 to 5V	2.5 to 5V
4P5S	2.5 to 5V	2.5 to 5V	2.5 to 5V
4P6S	2.5 to 5V	2.5 to 5V	2.5 to 5V
4P7S	2.7 to 5V	2.5 to 5V	2.5 to 5V
4P8S	3.1 to 5V	2.7 to 5V	2.5 to 5V

L = 10μH	30mA	25mA	20mA
4P4S	2.5 to 5V	2.5 to 5V	2.5 to 5V
4P5S	2.5 to 5V	2.5 to 5V	2.5 to 5V
4P6S	2.7 to 5V	2.5 to 5V	2.5 to 5V
4P7S	2.9 to 5V	2.7 to 5V	2.5 to 5V
4P8S	3.1 to 5V	2.9 to 5V	2.7 to 5V

- **LCD Bias**
  - **LCM Output Over-Voltage Protection**

    The RT4831A monitors the LCM output voltage to protect LCM_OUT and LCM_SW from exceeding safe operating voltages. If output voltage V_{LCM} reaches the over-voltage threshold 7.8V (typ.), the RT4831A sets the LCM OVP flag, register 0x0F[5] for notification. Once the OVP condition is removed, the flag can be cleared with an I^2C read back of the register. The RT4831A only reports LCM OVP condition and does not shutdown the LCM bias.

  - **LCM Inductor Over-Current Protection**

    When the loading current is increased such that the inductor current is above the high-side MOSFET valley current limit threshold, the off-time is increased until the inductor current is decreased to valley current threshold. The maximum inductor current is decided by the high-side MOSFET valley current limit level and internal designed inductor current ripple.

  - **POS Output Short-Circuit Protection**

    If the output current at POS exceeds 180mA (typ.), the RT4831A sets the POS SCP flag, register 0x0F[3]. Register 0x0A[7:6] configures the IC behavior for the POS SCP. Three options are report flag, report flag with shutdown POS/ NEG, and report flag with shutdown POS/ NEG/ Backlight. Once the output over current condition is removed, the flag can be cleared with an I^2C read back of the register. To avoid falsely triggering a short-circuit condition, the register 0x0B[3:2] provides four programmable POS short-circuit filter options : 100μs, 500μs, 1ms, and 2ms.

  - **NEG Output Short-Circuit Protection**

    Once the VNEG output voltage rise above 79% (typ.) of its programmed value, the RT4831A sets the NEG SCP flag, register 0x0F[2]. Register 0x0A[7:6] configures the IC behavior for the NEG SCP. Three options are report flag, report flag with shutdown POS/ NEG, and report flag with shutdown POS/ NEG/ Backlight. Once the output voltage goes back to 82% (typ.) of its programmed value, the flag can be cleared with an I^2C read back of the register. To avoid falsely triggering a short-circuit condition, the register 0x0B[1:0] provides four programmable NEG short-circuit filter options : 100μs, 500μs, 1ms, and 2ms.

Table 6. Protection

Channel	Type	Threshold (typ.)	Deglitch Time (typ.)	Protection	Reset and Threshold (typ.)
System	UVLO	V_{IN} ≤ 2.04V	NA	IC Shutdown	V_{IN} ≥ 2.3V
	OTP	Temperature ≥ 140°C	NA	Flag with shutdown display bias and backlight	Temperature ≤ 120°C
Backlight	BLED OVP	V_{OUT} ≥ $V_{OUT\_OV\_BL}$	Occur 32μs every 500μs cycling time	0x02[4] 0 : Flag only (default) 1 : Flag with shutdown backlight	V_{OUT} ≤ $V_{OUT\_OV\_BL}$
	BLED OCP	I_{BL_SW} ≥ $I_{CL\_PK\_BL}$	Occur 32μs every 500μs cycling time	Flag only	I_{BL_SW} ≤ $I_{CL\_PK\_BL}$
LCD bias	LCM OVP	V_{LCM} ≥ 7.8V	Occur 128μs every 1000μs cycling time	Flag only	V_{LCM} ≤ 7.8V
	POS SCP	I_{POS} ≥ I_{POS_CL}	0x0B[3:2] 00 : 2ms (default) 01 : 1ms 10 : 500μs 11 : 100μs	0x0A[7:6] 00 : Flag only (default) 01 : Flag only 10 : Flag with shutdown display bias 11 : Flag with shutdown display bias and backlight	I_{POS} ≤ I_{POS_CL}
	NEG SCP	V_{NEG} ≥ V_{NEG_target} x 79%	0x0B[1:0] 00 : 2ms (default) 01 : 1ms 10 : 500μs 11 : 100μs	0x0A[7:6] 00 : Flag only (default) 01 : Flag only 10 : Flag with shutdown display bias 11 : Flag with shutdown display bias and backlight	V_{NEG} ≤ V_{NEG_target} x 82%

Unused Channel Pin Connection

If the RT4831A backlight or LCD bias function is unused, the related pins need to be connected as below table.

Table 7. Unused Channel Pin Connection

Unused Part	Unused Function	Unused Pin Name	Pin Connection (Short to ground / Floating / Others)
Backlight	All functions	BL_OUT	Floating
		BL_SW	Floating
		BL_GND	Short to ground
		PWM	Floating
		LED1	Floating
		LED2	Floating
		LED3	Floating
		LED4	Floating
	Channel 1 only	LED1	Floating
	Channel 2 only	LED2	Floating
	Channel 3 only	LED3	Floating
	Channel 4 only	LED4	Floating
LCD Bias	All functions	LCM_OUT	Floating
		LCM_SW	Floating
		LCM_GND	Short to ground
		VPOS	Floating
		VNEG	Floating
		C+	Floating
		C-	Floating
		CP_GND	Short to ground
		LCM_EN1	Floating
		LCM_EN2	Floating

Component Selection

- **Inductor Selection**

  Inductance in the range from 4.7μH to 15μH is required for backlight boost converter. To ensure the boost stability, register 0x011[7:6] is used to adjust with corresponding selected inductance. The 2.2μH inductance is recommend for LCD bias boost converter. There are two main considerations when choosing an inductor :

  (1) The inductor saturation current must be chosen higher than the RT4831A peak current limit level for the application with consideration of ambient temperature.

  (2) To select an inductor with the low DCR to provide good performance and efficiency for application.

- **Input Capacitor Selection**

  For the RT4831A, it is recommended at least a 10μF input capacitor for backlight and a 10μF input capacitor for LCD bias. Input capacitor should be located as close to the RT4831A as impossible to reduce the PCB series resistance and inductance that can inject noise into the chip.

- **Boost Output Capacitor Selection**

  Two 1μF output capacitor in parallel for backlight and 10μF output capacitor for LCD bias are sufficient for most applications. Note the capacitor tolerance, operating voltage and ambient temperature all needs to be taken into considerations for the effective capacitance. The ripple voltage is an important index for choosing output capacitor. This portion consists of two parts. One is the product of ripple current with the ESR of the output capacitor, while the other part is formed by the charging and discharging process of the output capacitor. The output ripple can be calculated as below.

$$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_{OUT1} = \Delta V_{ESR} + \frac{I_{OUT} \times D}{f_{SW} \times C_{OUT}}$$

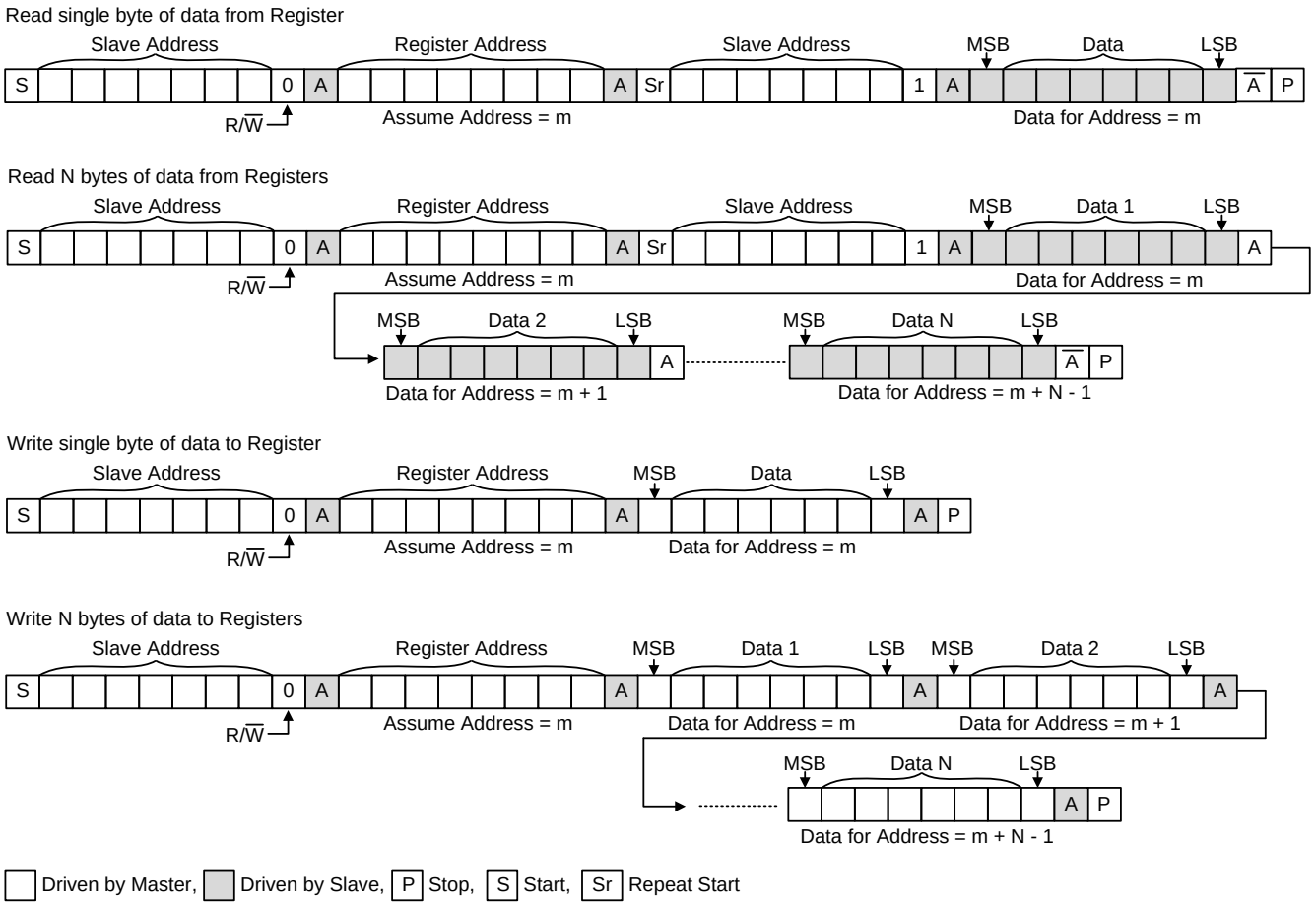
  where $\Delta V_{ESR} = I_{Crms} \times R_{CESR}$

I²C Interface

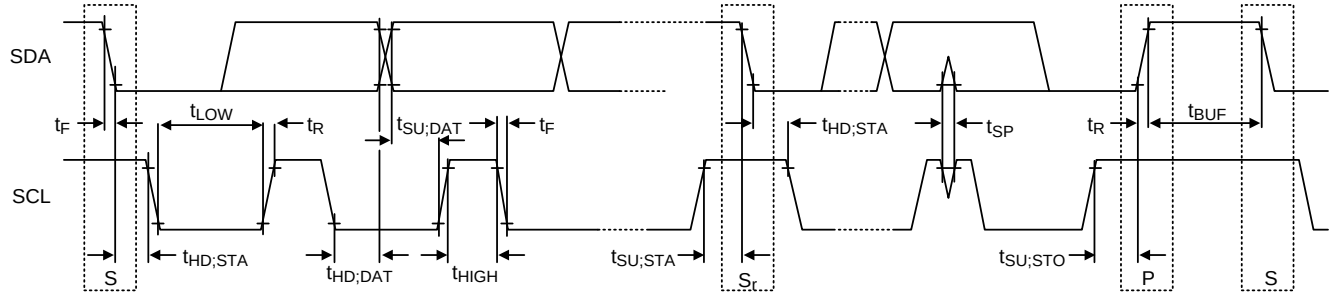
The following table shows the RT4831A slave address 0x11(7bit).

RT4831A I²C Slave Address			
MSB	**LSB**	**R/W bit**	**R/W**
001000	1	1/0	23/22

The I²C interface bus must be connect a resistor 2.2kΩ to power node and independent connection to processor, individually. The I²C timing diagrams are listed below.



I²C Waveform Information



I²C Register Table

R : Read Only

RC : Read then Clear

RW : Read and Write

RWC : Read and Write Clear (Write "1" then automatic clears to "0" after procedure finish)

Addr	RegName	Bit	BitName	Default	Type	Description
0x01	Revision	7:2	Version_ID	000000	R	Chip Version
		1:0	Vendor_ID	11	R	11 : RICHTEK
0x02	Backlight Configuration 1	7:5	BLED_OVP	001	RW	Backlight OVP 000 : 17V 001 : 21V (default) 010 : 25V 011 : 29V 100 to 111 : 29V
		4	BLED_OVP_SHUTDOWN	0	RW	Shutdown Enable for Backlight OVP 0 : OVP is report only (default) 1 : OVP shutdown
		3	BLED_CODE	1	RW	Backlight Mapping Code 0 : Exponential 1 : Linear (default)
		2	BLED_CONFIG	0	RW	Backlight PWM Configuration 0 : Active High (default) 1 : Active Low
		1	BLED_PWM_RAMP_EN	0	RW	PWM Ramp Mode Enable 0 : w/o Ramp (default) 1 : w/ Ramp
		0	BLED_PWM_EN	0	RW	PWM Enable 0 : PWM disable (default) 1 : PWM enable

Addr	RegName	Bit	BitName	Default	Type	Description
0x03	Backlight Configuration 2	7	BLED_BST_ FREQUENCY	1	RW	Backlight Boost Switching Frequency (Please also see registers 0x06 and 0x07) 0 : 500kHz 1 : 1MHz (default)
		6:3	BLED_RAMPTIME	0001	RW	Backlight Ramp Up/Down Time 0000 : 0 0001 : 500μs (default) 0010 : 750μs 0011 : 1ms 0100 : 2ms 0101 : 5ms 0110 : 10ms 0111 : 20ms 1000 : 50ms 1001 : 100ms 1010 : 250ms 1011 : 800ms 1100 : 1s 1101 : 2s 1110 : 4s 1111 : 8s
		2	BLED_PWM_ SAMPLE	1	RW	PWM Sampling Frequency 0 : 1MHz 1 : 4MHz (default) (Please see also register 0x10)
		1:0	BLED_PWM_HYS	01	RW	PWM Input Hysteresis PWM Sample Frequency (1MHz or 4MHz) 00 : 1 bit 01 : 2 bit (default) 10 : 4 bit 11 : 6 bit PWM Sample Frequency (24MHz) 00 : 0 01 : 1 bit (default) 10 : 2 bits 11 : 3 bits
0x04	Backlight Brightness LSB	7:3	Reserved	00000	RW	Reserved
		2:0	BLED_DIM_L	111	RW	LSBs of 11 bit Backlight Brightness control, BLED_DIM[2:0], update after write register 0x05.
0x05	Backlight Brightness MSB	7:0	BLED_DIM_H	11111111	RW	MSBs of 11 bit Backlight Brightness control, BLED_DIM[10:3].

Addr	RegName	Bit	BitName	Default	Type	Description
0x06	Backlight Auto-Frequency Low	7:0	BLED_AFLT	00000000	RW	If 0x05 code is smaller than 0x06, Backlight Boost switching frequency will be set to 250kHz. (Please also see register 0x03 and 0x07)
0x07	Backlight Auto-Frequency High	7:0	BLED_AFHT	00000000	RW	If 0x05 code is greater than 0x06 but NOT greater than 0x07, Backlight Boost switching frequency will be set to 500kHz. If 0x05 code is greater than 0x07, switching frequency will be set 1MHz. (Please also see register 0x03 and 0x06)
0x08	Backlight Enable	7	SF_RESET	0	RWC	Software Reset 0 : Not Reset (default) 1 : Reset (Automatic returns to 0 after reset)
		6:5	Reserved	00	RW	Reserved
		4	BLED_EN	0	RW	Blacklight Enable 0 : Disable (default) 1 : Enable
		3	BLED_CH4_EN	0	RW	LED4 Channel Enable 0 : Disable (default) 1 : Enable
		2	BLED_CH3_EN	0	RW	LED3 Channel Enable 0 : Disable (default) 1 : Enable
		1	BLED_CH2_EN	0	RW	LED2 Channel Enable 0 : Disable (default) 1 : Enable
		0	BLED_CH1_EN	0	RW	LED1 Channel Enable 0 : Disable (default) 1 : Enable

Addr	RegName	Bit	BitName	Default	Type	Description
0x09	Display Bias Configuration 1	7:5	DSV_MODE_EN	000	RW	Display Bias Mode 000 : Display Bias Off (I^2C and External) (default) 100 : Normal Mode 101 : Auto Seqence 110 : Wake Up 1 111 : Wake Up 2 Others : Reserved
		4	DSV_VPOS_DISC	1	RW	VPOS Discharge Enable 0 : Not Discharge 1 : Active Discharge (default)
		3	DSV_VNEG_DISC	1	RW	VNEG Discharge Enable 0 : Not Discharge 1 : Active Discharge (default)
		2	DSV_VPOS_EN	0	RW	VPOS Channel Enable 0 : Disable (default) 1 : Enable
		1	DSV_VNEG_EN	0	RW	VNEG Channel Enable 0 : Disable (default) 1 : Enable
		0	DSV_EXTERNAL_EN	0	RW	Display Bias External Control 0 : Disable (default) 1 : Enable
0x0A	Display Bias Configuration 2	7:6	DSV_SHORT_MODE	00	RW	Display Bias Short Mode 00 : Flag Only (default) 01 : Flag Only 10 : Flag with Shutdown Display Bias 11 : Flag with Shutdown Display Bias and Backlight
		5:4	DSV_VPOS_SR	01	RW	VPOS Ramp Up Time (refer to Figure 8) 00 : 256µs 01 : 512µs (default) 10 : 768µs 11 : 1024µs
		3:0	DSV_VNEG_SR	0001	RW	VNEG Ramp Up Time (refer to Figure 8) 0000 : 500µs 0001 : 1024µs (default) 0010 : 1536µs 0011 : 2048µs 0100 : 2560µs 0101 : 3072µs 0110 : 3584µs 0111 : 4096µs 1000 : 4608µs 1001 : 5120µs 1010 : 5632µs 1011 : 6144µs 1100 : 6656µs 1101 : 7168µs 1110 : 7680µs 1111 : 8192µs

Addr	RegName	Bit	BitName	Default	Type	Description
0x0B	Display Bias Configuration 3	7:4	Reserved	0000	RW	Reserved
		3:2	DSV_VPOS_SHORT_TIMER	00	RW	VPOS Short Timer 00 : 2ms (default) 01 : 1ms 10 : 500μs 11 : 100μs
		1:0	DSV_VNEG_SHORT_TIMER	00	RW	VNEG Short Timer 00 : 2ms (default) 01 : 1ms 10 : 500μs 11 : 100μs
0x0C	LCM Bias	7:6	Reserved	00	RW	Reserved
		5:0	DSV_VLCM	101000	RW	VLCM Voltage 000000 : 4V 000001 : 4.05V : 101000 : 6V (default) : 111111 : 7.15V
0x0D	VPOS Bias	7:6	Reserved	00	RW	Reserved
		5:0	DSV_VPOS	011110	RW	VPOS Voltage 000000 : 4V 000001 : 4.05V : 011110 : 5.5V (default) : 110010 : 6.5V 110011 to 111111 map to 6.5V
0x0E	VNEG Bias	7:6	Reserved	00	RW	Reserved
		5:0	DSV_VNEG	011100	RW	VNEG Voltage 000000 : −4V 000001 : −4.05V : 011100 : −5.4V (default) : 110010 : −6.5V 110011 to 111111 map to −6.5V

Addr	RegName	Bit	BitName	Default	Type	Description
0x0F	Flags	7	Reserved	0	RC	Reserved
		6	OTP_FLAG	0	RC	Chip Over-Temperature Flag 0 : Normal operation (default) 1 : Thermal shutdown
		5	DSV_LCM_OVP_FLAG	0	RC	Display Bias LCM Output Over-Voltage Flag 0 : Normal operation (default) 1 : VLCM > 7.8V
		4	Reserved	0	RC	Reserved
		3	DSV_VPOS_SCP_FLAG	0	RC	Display Bias VPOS Output Short Circuit Flag 0 : Normal operation (default) 1 : VPOS output has hit the over-current threshold
		2	DSV_VNEG_SCP_FLAG	0	RC	Display Bias VNEG Output Short Circuit Flag 0 : Normal operation (default) 1 : VNEG > 0.84 × VNEG_target
		1	BLED_OVP_FLAG	0	RC	Bcaklight Output Over-Voltage Flag 0 : Normal operation (default) 1 : Backlight Boost output > OVP threshold
		0	BLED_OCP_FLAG	0	RC	Bcaklight Boost Over-Current Flag 0 : Normal operation (default) 1 : Backlight Boost switch current > OCP threshold

Addr	RegName	Bit	BitName	Default	Type	Description
0x10	Backlight Option 1	7	Reserved	0	RW	Reserved
		6	BLED_CH4_FB_DISABLE	0	RW	LED4 Feedback Setting 0 : Enable (default) 1 : Disable
		5	BLED_CH3_FB_DISABLE	0	RW	LED3 Feedback Setting 0 : Enable (default) 1 : Disable
		4	BLED_CH2_FB_DISABLE	0	RW	LED2 Feedback Setting 0 : Enable (default) 1 : Disable
		3	BLED_CH1_FB_DISABLE	0	RW	LED1 Feedback Setting 0 : Enable (default) 1 : Disable
		2:1	BLED_PWM_DEGLITCH	11	RW	PWM Dglitch Filter Time 00 : 0ns 01 : 100ns 10 : 160ns 11 : 200ns (default)
		0	BLED_PWM_24MHz_SAMPLE	0	RW	PWM Sampling Frequency 24MHz Enable 0 : Disable (default) 1 : Enable (Please also see register 0x03)
0x11	Backlight Option 2	7:6	BLED_L_SELECT	00	RW	Backlight Boost L Select 00 : 4.7μH (default) 01 : 10μH 10 : 15μH 11 : 15μH
		5:4	BLED_SEL_P	11	RW	Reserved
		3:2	BLED_SEL_I	01	RW	Reserved
		1:0	BLED_OC	01	RW	Backlight Over-Current Limit 00 : 900mA 01 : 1200mA (default) 10 : 1500mA 11 : 1800mA
0x12	PWM-to-Digital Code LSB Readback	7:0	BLED_PWM_TO_DIG_L	00000000	R	11 bit PWM-to-Digital Conversion Code LSBs

Addr	RegName	Bit	BitName	Default	Type	Description
0x13	PWM-to-Digital Code MSB Readback	7:3	Reserved	00000	R	Reserved
		2:0	BLED_PWM_TO_DIG_H	000	R	11 bit PWM-to-Digital Conversion Code MSBs
0x14	Backlight Smooth	7:2	Reserved	000000	R	Reserved
		1	BLED_RAMP_DN_SMOOTH_EN	0	RW	Backlight Smooth Enable for Ramp Down 0 : Disable (default) 1 : Enable
		0	BLED_RAMP_UP_SMOOTH_EN	0	RW	Backlight Smooth Enable for Ramp Up 0 : Disable (default) 1 : Enable
0x15	I2C Protect	7:1	Reserved	0000000	R	Reserved
		0	I2C_SAFE_TIMER_EN	0	RW	I^2C safe timer to reset the I^2C slave when SDAO stays low longer than 1 second. 0 : Disable (default) 1 : Enable

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-24B 1.84x2.68 (BSC) package, the thermal resistance, θ_{JA}, is 37.1°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C - 25°C) / (37.1°C/W) = 2.69W for a WL-CSP-24B 1.84x2.68 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 13 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

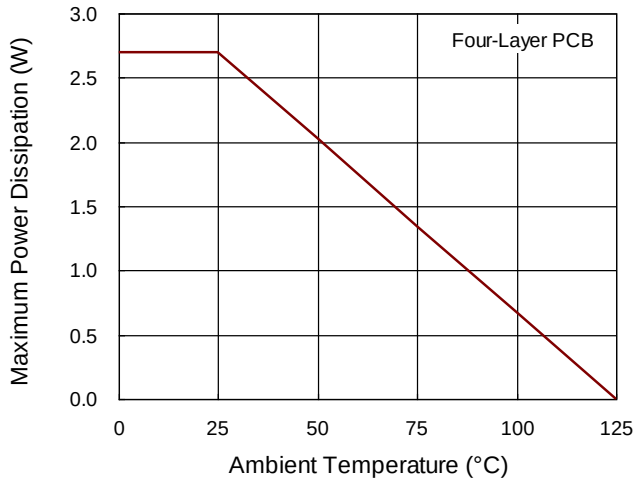


Figure 13. Derating Curve of Maximum Power Dissipation

Layout Considerations

The PCB layout is an important step to maintain the high performance of the RT4831A. Both the high current and the fast switching nodes demand full attention to the PCB layout to keep the robustness of the RT4831A through the PCB layout. Improper layout might lead to the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. For the best performance of the RT4831A, the following PCB layout guidelines must be strictly followed.

- The trace from switching node to inductor should be as short as possible to minimized the switching loop for better EMI.
- Place the input and output capacitors close to the input and output pins respectively for good filtering. Both Backlight and LCD bias inputs must have an independent capacitor to filter switching noise. The suggested capacitor value is 10μF.
- To guarantee IC normal operation, there must have a dedicated power trace connected from the IN pin to the input capacitor of Backlight or LCD bias.
- Keep the main power traces as wide and short as possible.
- Separate the CP_GND, AGND, LCM_GND and BL_GND. Each connects to a strong ground plane for maximum thermal dissipation and noise protection.

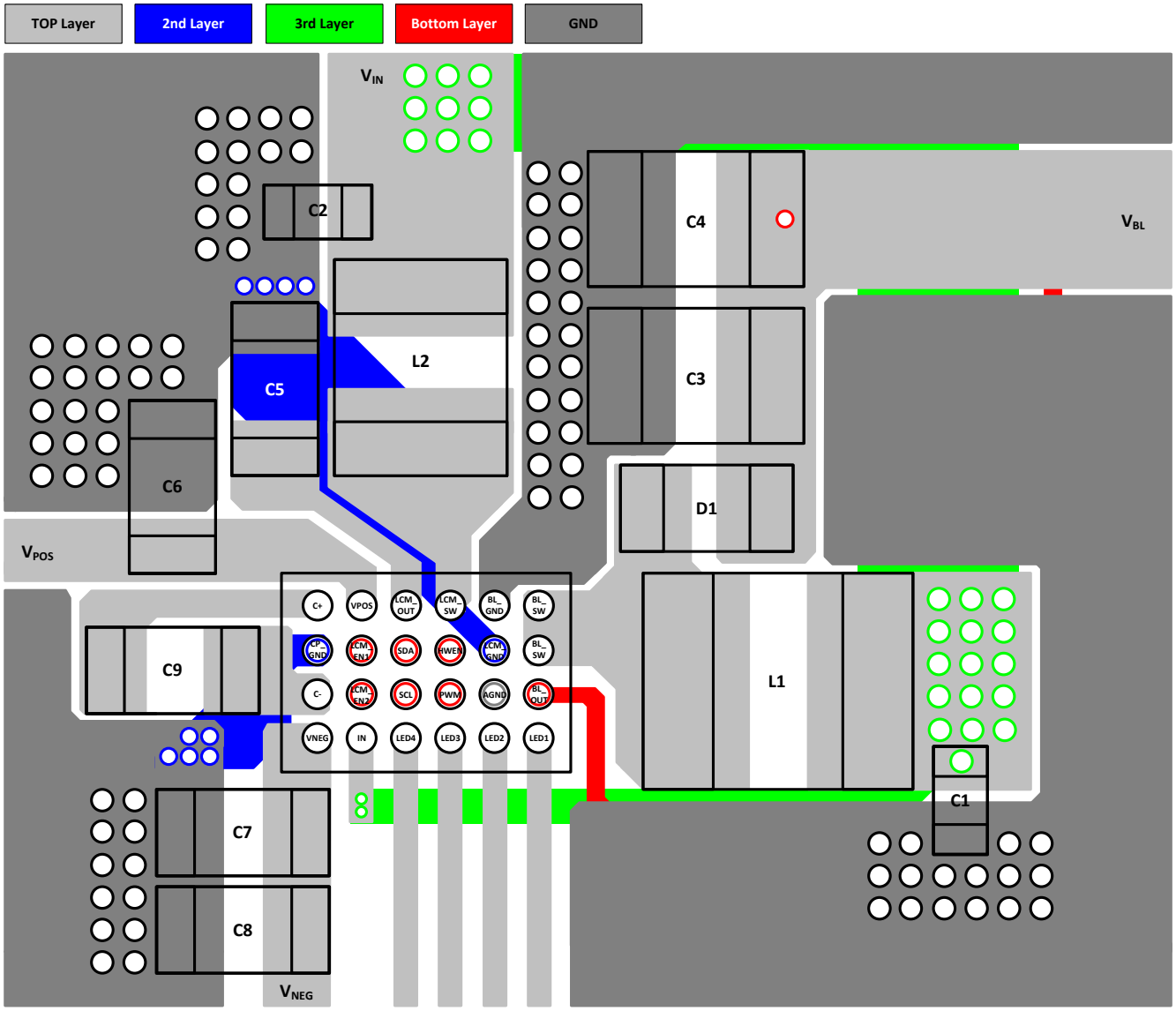
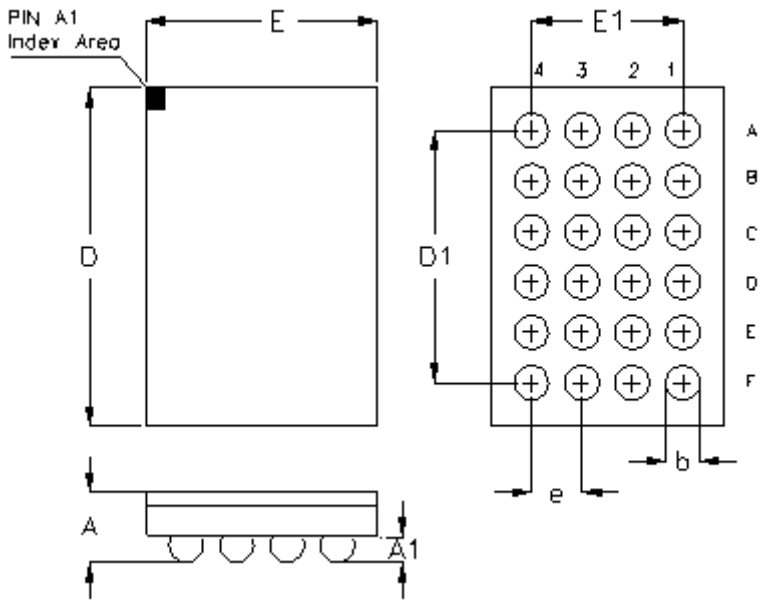


Figure 14. PCB Layout Guide

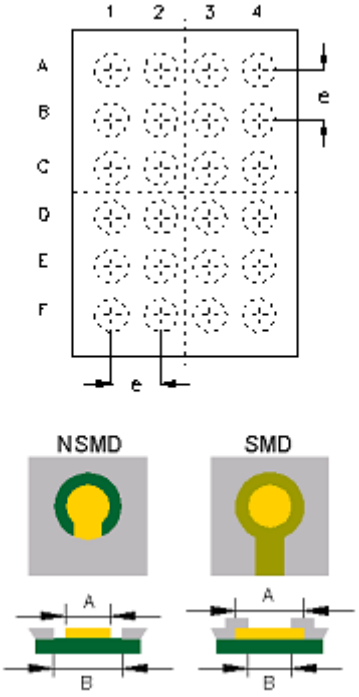
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	2.640	2.720	0.104	0.107
D1	2.000		0.079	
E	1.800	1.880	0.071	0.074
E1	1.200		0.047	
e	0.400		0.016	

24B WL-CSP 1.84x2.68 Package (BSC)

Footprint Information



Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP1.84X2.68-24(BSC)	24	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

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