TEXAS INSTRUMENTS

TPS54380EVM-001 3-Amp SWIFT™ Regulator Evaluation Module

User's Guide

June 2003 *PMP Systems Power*

SLVU087

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It is important to operate this EVM within the input voltage range of 3 V to 5 V and the output voltage range of 0.9 V to 3.3 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 55°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

About This Manual

This user's guide describes the characteristics, operation and use of the TPS54380EVM evaluation module (EVM). The user's guide includes a schematic diagram, printout-circuit board (PCB) layouts, and bill of materials.

How to Use This Manual

- ❏ Chapter 1—Introduction
- ❏ Chapter 2—Test Setup and Results
- ❏ Chapter 3—Board Layout
- ❏ Chapter 4—Schematic and Bill of MAterials

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

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Related Documentation From Texas Instruments

- ❏ TPS54380 data sheet (literature number SLVS454)

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Chapter 1

Introduction

This chapter contains background information for the TPS54380 as well as support documentation for the TPS54380EVM-001 evaluation module (HPA001). The TPS54380EVM-001 performance specifications are given, with the schematic and bill of material for the TPS54380EVM-001.

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1.1 Background

The TPS54380 tracking dc/dc converter provides accurate power sequencing in applications where two or more voltages are required for a load. These types of applications include core and I/O power supplies for microprosessors, DSPs, and FPGAs. Typically, some specific relation between the core and I/O supply voltages has to be provided during the power-up and power-down sequences. The TPS54380 tracking dc/dc converter is capable of direct tracking, ratiometric tracking, and voltage sequencing with a second power source. The TPS54380EVM-001 is a two-channel EVM demonstrating the flexibility inherent in the TPS54380 design for tracking and sequencing core and I/O voltages. The TPS54380 generates the core voltage and is nominally set at 1.8 V. The nominal 3.3-V I/O voltage is provided by a TPS2013 distribution switch. Rated input voltage and output current range is given in Table 1–1. This evaluation module demonstrates the small PCB areas that are achieved when designing with the TPS54380 regulator. The switching frequency is set at a nominal 700 kHz, allowing the use of a small footprint 1.0-μH output inductor. The MOSFETs of the TPS54380 are incorporated inside the TPS54380 package. This eliminates the need for external MOSFETs and their associated drivers. The low drain-to-source on resistance of the MOSFETs gives the TPS54380 high efficiency and helps to keep the junction temperature low at high output currents. The compensation components are provided external to the IC, and allow for an adjustable output voltage and a customizable loop response. The TPS54380 device uses the TRACKIN pin to access the tracking and sequencing capabilities. An internal multiplexer circuit compares the voltage at this pin with the internal reference voltage and uses the lesser of the two as the reference for the output voltage regulation. When the output of another power supply or distribution switch is connected to the TRACKIN pin of TPS54380, the output of the TPS54380 tracks the output of this other channel during power up or down, until the voltage at TRACKIN pin becomes higher then the internal reference voltage. By applying the other power supply output to the TRACKIN pin through an appropriate resistor divider network, any required power up and power down relation between two output voltages of regulators can be set by changing the ratio of the divider network.

Table 1–1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Current Range
TPS54380EVM–001	3.0 to 5.5 V	Core, –3 A to 3 A I/O, 0–1.5 A

Input voltage range is limited by the TPS2013 distribution switch.

1.2 Performance Specification Summary

A summary of the TPS54380EVM-225 performance specifications is provided in Table 1–2. Specifications are given for an input voltage of 3.3 V and an output voltage of 1.8 V unless otherwise specified. The ambient temperature is 25°C for all measurements, unless otherwise noted. The data presented in Table 1–2 compiled with no load on the I/O output. The input voltage range is limited to 5.5 V by the distribution switch. The maximum input voltage for the TPS54380 is 6 V.

Table 1–2. TPS54380EVM-001 Performance Specification Summary

Specification		Test Conditions	Min	Typ	Max	Units
Input voltage range			3.0	3.3 or 5.0	5.5	V
Output voltage set point			0.9	1.8	3.3	V
Output current range		V_I = 3 V to 5.5 V	–3		3	A
Line regulation		I_O = 0–3 A, V_I = 3 V to 5.5 V		± 0.1%		
Load regulation		V_I = 3.3 V, I_O = 0 to 3 A		±0.2%		
Load transient response	Voltage change	I_O =0.75 A to 2.25 A		–24		mV_{PK}
	Recovery time			120		µs
	Voltage change	I_O = 2.25 A to 075 A		20		mV_{PK}
	Recovery time			120		µs
Loop bandwidth		V_I = 3 V		50		kHz
Phase margin		V_I = 3 V		62°		
Loop bandwidth		V_I = 5.5 V		80		kHz
Phase margin		V_I = 5.5 V		46°		
Input ripple voltage				50	200	mV_{PP}
Output ripple voltage				6	10	mV_{PP}
Output rise time				N/A		ms
Operating frequency			280	700	700	kHz
Maximum efficiency		V_I = 5.0 V, Vo = 1.8 V, I_O = 1.0 A		89%		–

1.3 Modifications

The TPS54380EVM–001 is designed to demonstrate the small size that can be attained when designing with the TPS54380, so many of the features, which allow for extensive modifications have been omitted from this EVM. Changing the value of R2 can change the output voltage in the range of 0.9 V to 3.3 V. The value of R2 for a specific output voltage can be calculated by using Equation 1–1. Table 1–3 list the values for R2 for some common output voltages.

Equation 1–1.

$$R2 = 10\ k\Omega \times \frac{0.891\ V}{V_O - 0.891\ V}$$

Table 1–3. Output Voltage Programming

Output Voltage (V)	R2 Value (kΩ)
0.9	1000
1.2	28.7
1.5	14.7
1.8	9.76
2.5	5.49
3.3	3.74

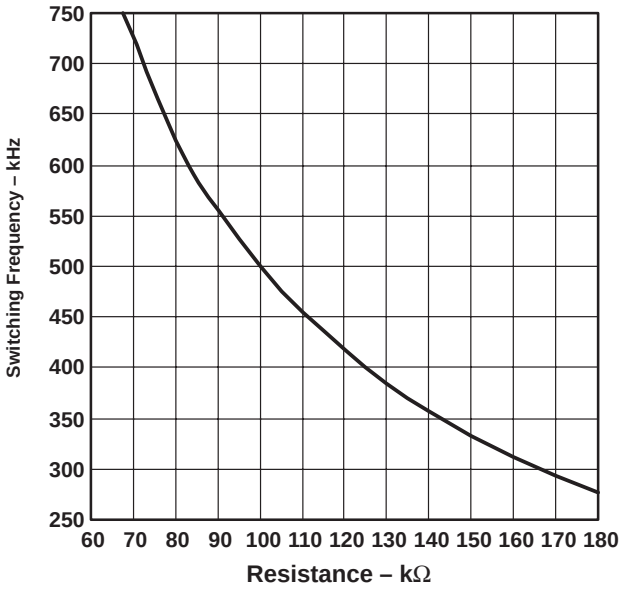
The minimum output voltage is limited by the minimum controllable on time of the device, 200 ns, and is dependent upon the duty cycle and operating frequency. The approximate minimum output voltage can be calculated using Equation 1–2.

Equation 1–2.

$$V_{OUTMIN} = 200n\ sec \times f_s \times V_{INMAX}$$

The switching frequency may be trimmed to any value between 280 kHz and 700 kHz by changing the value of R4. Decreasing the switching frequency results in increased output ripple unless the value of L1 is increased. A plot of the value of RT versus the switching frequency is given in Figure 1–1.

Figure 1–1. Frequency Trimming Resistor Selection Graph



An onboard electrolytic input capacitor may be added at C1.

1.3.1 Power Sequencing

By selecting different R6–R7 resistor divider ratios, different power sequencing scenarios can be set. The equations 1–3, 1–4 and 1–5 below show how to select the different ways of power sequencing.

Equation 1–3.

$$\frac{R6}{R7} = \frac{R1}{R2}$$ –core voltage tracks I/O voltage;

Equation 1–4.

$$\frac{R6}{R7} = \frac{\left(V_{I/O} - 0.891\right)}{8.891}$$ – ratiometric relation between core and I/O voltage;

Equation 1–5.

$$\frac{R6}{R7} < \frac{R1}{R2}$$ –core voltage rises first at power up and falls seconde at power down.

Chapter 2

Test Setup and Results

This chapter describes how to properly connect, set up, and use the TPS54380EVM-001 evaluation module. The chapter also includes test results typical for the TPS54380EVM-001 and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start up.

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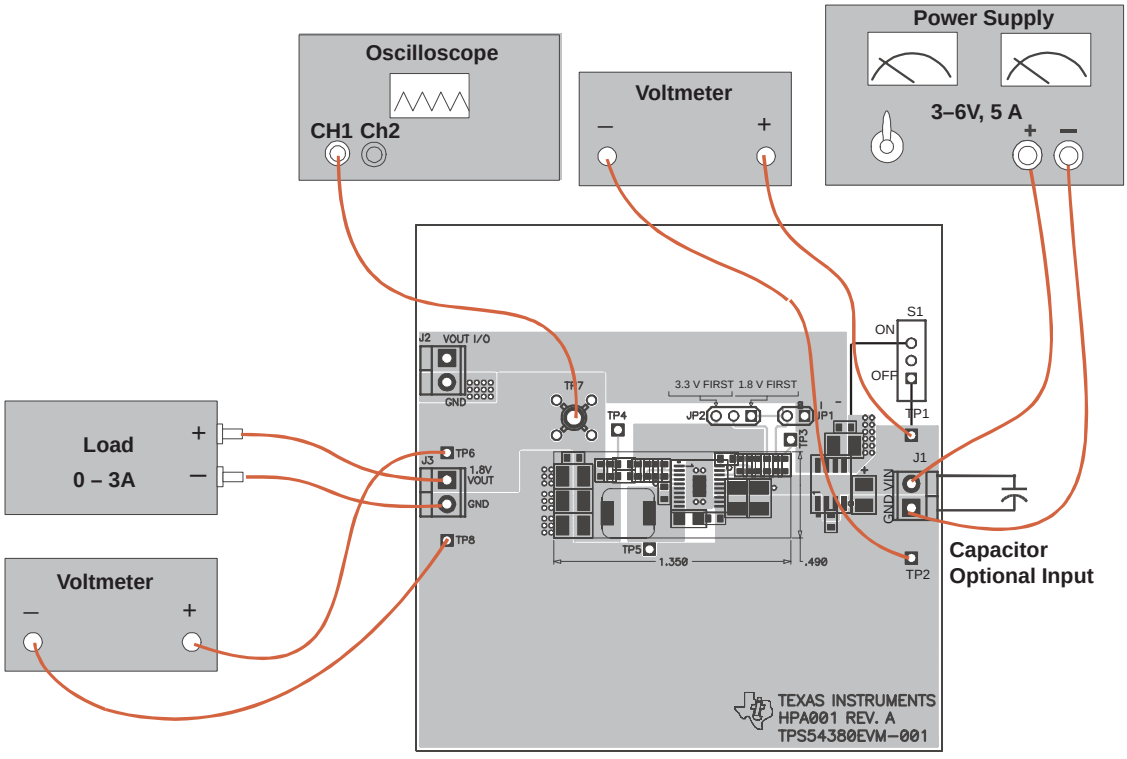
2.1 Input/Output Connections

The TPS54380EVM-001 has the following three input/output connectors: V_I J1, V_O I/O J2 and V_O Core J3. A diagram showing the connection points is shown in Figure 2–1. A power supply capable of supplying 5 A is connected to J1 through a pair of 20 AWG wires. The load is connected to J2 through a pair of 16 AWG wires. The maximum load current capability should be 3 A. Wire lengths are minimized to reduce losses in the wires. Test point TP6 provides a place to easily connect an oscilloscope voltage probe to monitor the output voltage. The TPS54380 is intended to be used as a point of load regulator. In typical applications it is usually located close to the input voltage source. When using the TPS54380EVM–001 with an external power supply as the source for V_I, an additional bulk capacitor may be required, depending upon the output impedance of the source and length of the hook-up wires. The test results presented were obtained using a 470 µF, 16-V additional input capacitor. Alternately, C1 may be populated with an input filter capacitor. Connection is shown for no load on the I/O voltage output. The I/O voltage may be supply up to 1.5 A into an external load.

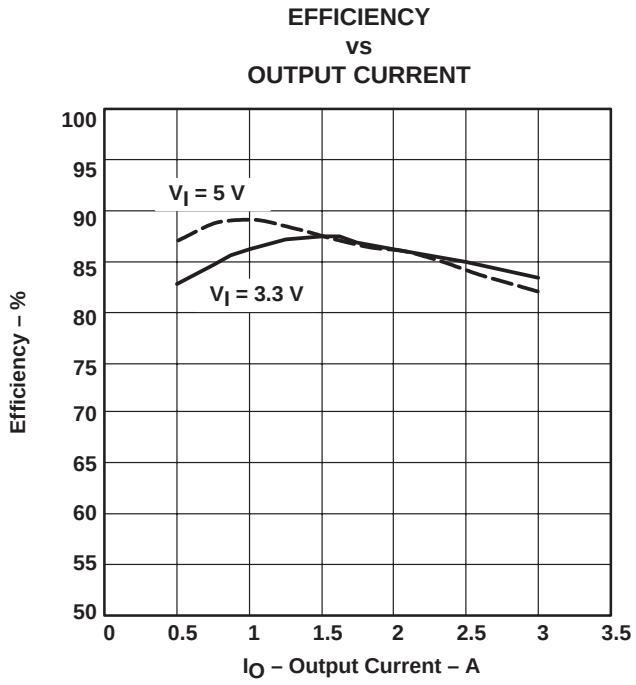
Figure 2–1. Connection Diagram



2.2 Efficiency

The TPS54380EVM–001 efficiency peaks at load current of about 1 A to 2 A, and then decreases as the load current increases towards full load. Figure 2–2 shows the efficiency for the TPS54380 at an ambient temperature of 25°C. The efficiency is lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the MOSFETs. The efficiency is slightly lower at 700 kHz than at lower switching frequencies, due to the gate and switching losses in the MOSFETs.

Figure 2–2. Measured Efficiency, TPS54380

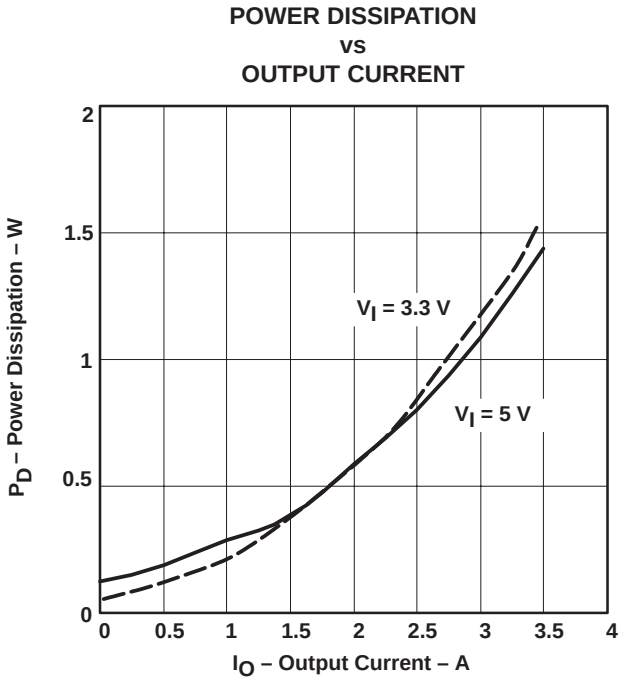


2.3 Power Dissipation

The low junction-to-case thermal resistance of the PWP package, along with a good board layout, allows the TPS54380EVM-001 EVMs to output full rated load current while maintaining safe junction temperatures. With a 3.3-V input source and a 3-A load, the junction temperature is approximately 60°C, while the case temperature is approximately 55°C. The total circuit losses at 25°C are shown in Figure 2–3. Power dissipation is shown for input voltages of 3.3 V and 5.0 V.

For additional information on the dissipation ratings of the devices, see the individual product data sheets.

Figure 2–3. Measured Circuit Losses



2.4 Output Voltage Regulation

The output voltage load regulation of the TPS54380EVM–001 is shown in Figure 2–4, while the output voltage line regulation is shown in Figure 2–5. Measurements are given for an ambient temperature of 25°C.

Figure 2–4. Load Regulation

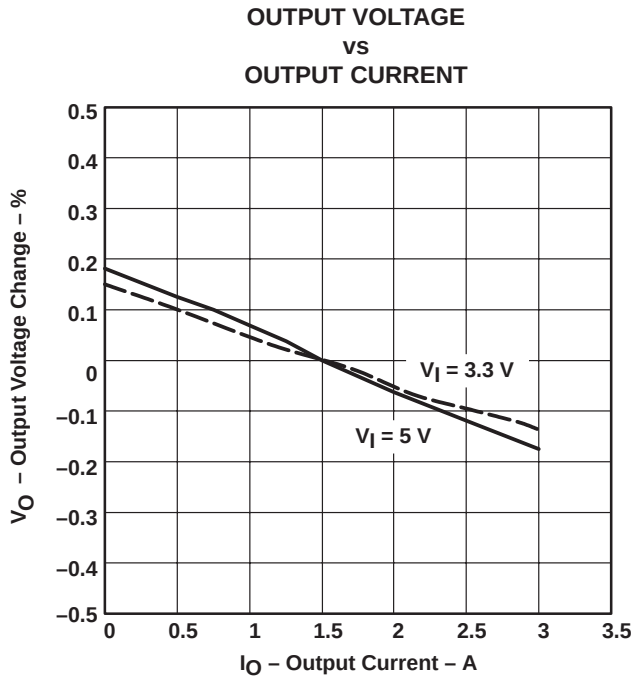
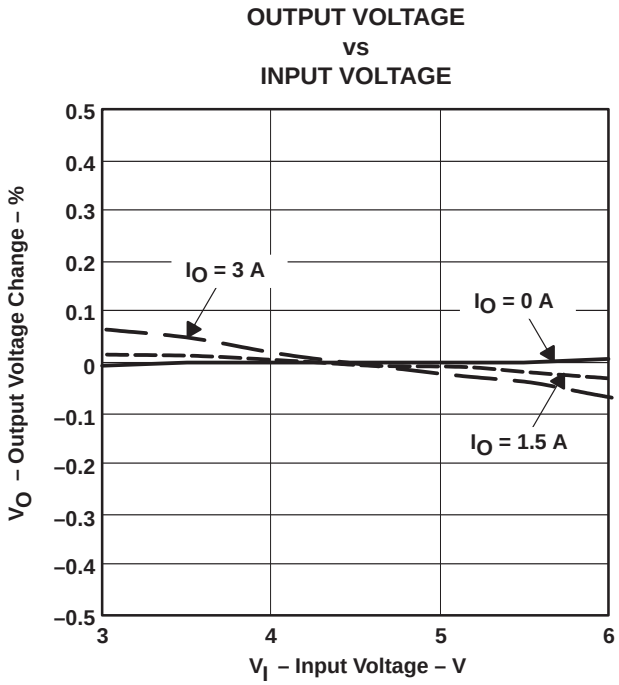


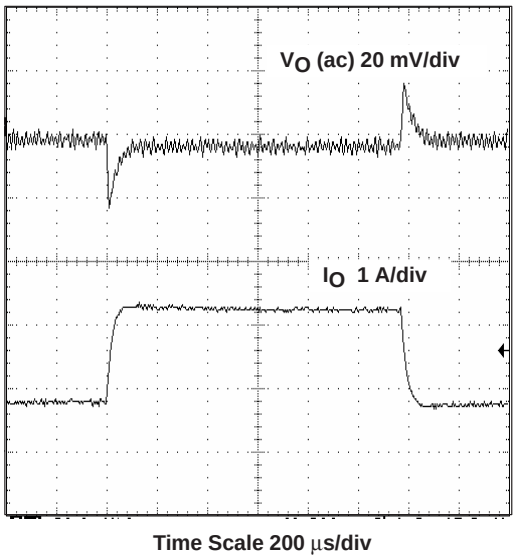
Figure 2–5. Line Regulation



2.5 Load Transients

The TPS54380EVM–001 response to load transients is shown in Figure 2–6. The current step is from 25% to 75% of maximum rated load. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

Figure 2–6. Load Transient Response, TPS54380



2.6 Loop Characteristics

The TPS54380EVM–001 loop response characteristics are shown in Figure 2–7 and Figure 2–8. Gain and phase plots are shown for each device at minimum and maximum operating voltage.

Figure 2–7. Measured Loop Response, TPS54380, V_I = 3 V

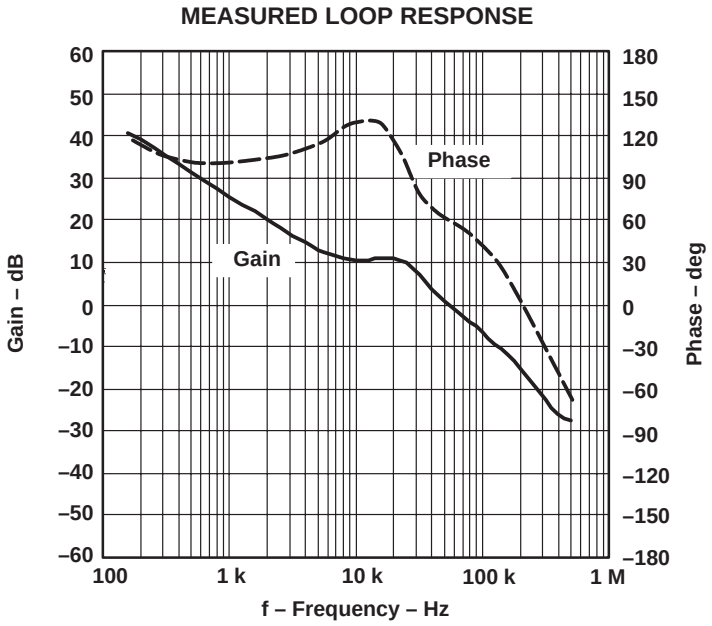
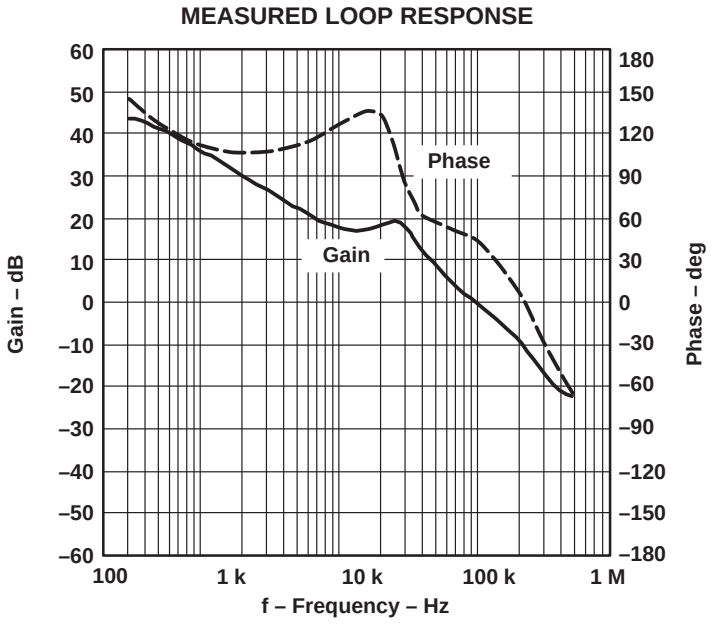


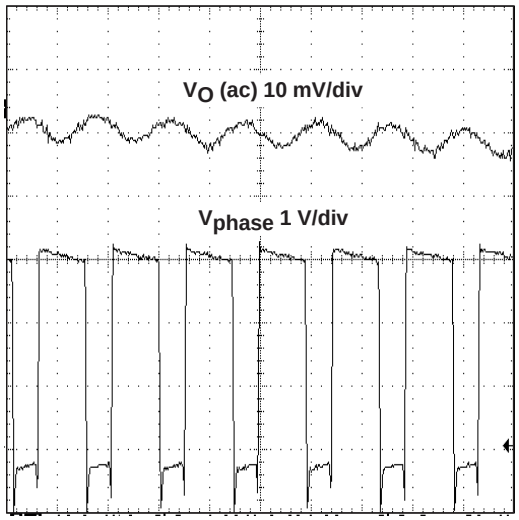
Figure 2–8. Measured Loop Response, TPS54380, V_I = 5.5 V



2.7 Output Voltage Ripple

The TPS54X73EVM–225 output voltage ripple is shown in Figure 2–9. The input voltage is 3.3 V for the TPS54380. Output current is the rated full load of 3 A. Voltage is measured directly across output capacitors.

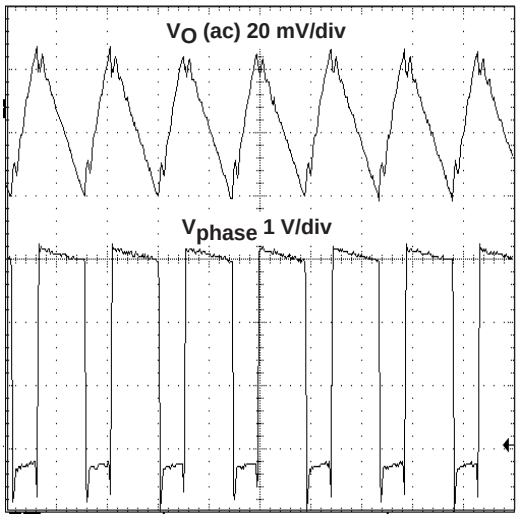
Figure 2–9. Measured Output Voltage Ripple, TPS54380



2.8 Input Voltage Ripple

The TPS54X73EVM–225 output voltage ripple is shown in Figure 2–10. The input voltage is 3.3 V for the TPS54380. Output current for each device is rated full load of 3 A.

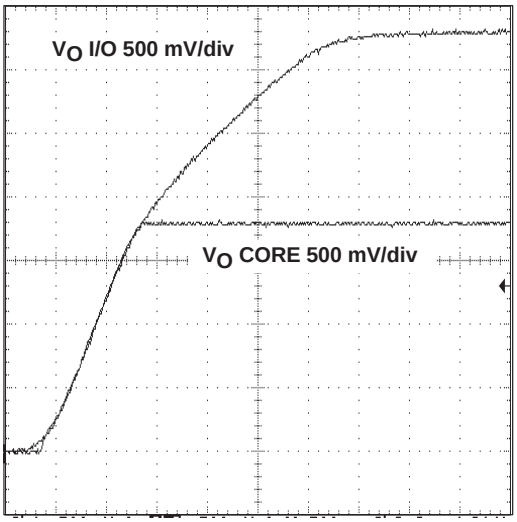
Figure 2–10. Input Voltage Ripple, TPS54380



2.9 Powering Up and Down

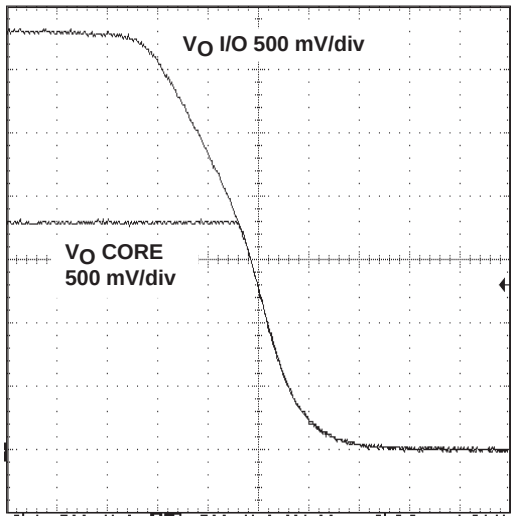
The TPS54380 regulator provides different modes for power up and power down sequencing of the core and I/O voltages. By selecting the different ratios for the resistor divider R6/R7 (Figure 4–1), the slope of core voltage during powering up and down can be set equal to, higher than, or lower than the slope of I/O voltage. If the resistors R6 = R1 and R7 = R2, then the core voltage tracks the I/O voltage. The start-up voltage waveform of the TPS54380EVM-001 for this condition is shown in Figure 2–11. The waveform shows that the core voltage regulator tracks the output of I/O regulator until the core regulator reaches its nominal 1.8-V level. After that, the core regulator starts to regulate its output at the preset 1.8-V level. The I/O regulator continues its ramp up until the voltage reaches the nominal 3.3-V level. The output voltage waveforms during powering up do not depend on load currents. The output voltage waveforms are powered up by asserting the ENABLE signal, while the input voltage is already applied.

Figure 2–11. Power Up With Tracking



The power-down waveform is shown in Figure 2–12. During power down, the output voltage fall time is defined by the output capacitance and load resistance. In this case the I/O output load resistance has been set to 20 Ω and the core output load resistance set to 1 Ω. With the I/O output voltage falling with a slew rate of about 1.25 V/ms, there is essentially no difference between the core voltage and I/O voltage.

Figure 2–12. Powering Down With Tracking



The TPS54380EVM–001 EVM provides the ability to change the slew rate of output voltage of core regulator by using jumper JP2 (see schematic in Figure 4–1). If jumper JP2 is set so that R8 is connected in parallel to R7, ratiometric power sequencing is implemented. For ratiometric sequencing the following condition needs to be met:

if R6 = 10 kΩ then R8 II R7 = $(R7 \times 0.891)/(V_{I/O} - 0.891)$.

In this case the I/O and core voltages reach their nominal values at the same time. The waveforms for ratiometric powering up and down are shown in Figure 2–13 and Figure 2–14.

Figure 2–13. Powering Up With Ratiometric Sequencing

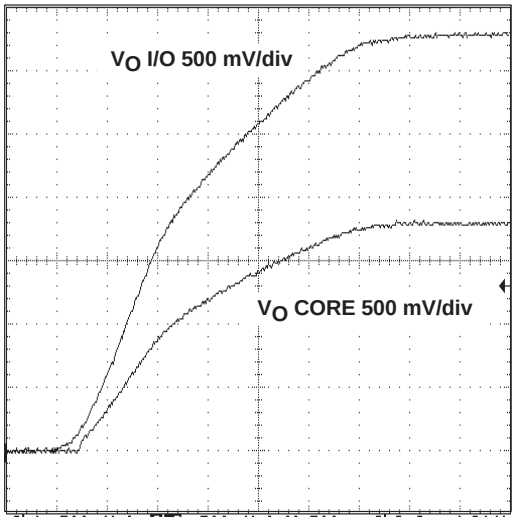
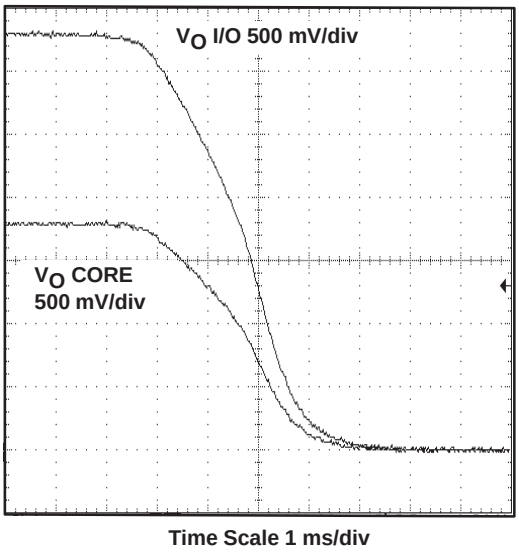


Figure 2–14. Powering Down With Ratiometric Sequencing



If jumper JP2 is set so that R8 is connected in parallel to R6, the core voltage rises first during powering up and falls second during power down. The waveforms with this type of sequencing are shown in Figure 2–15 and Figure 2–16.

Figure 2–15. Powering Up With Core Voltage Rising First

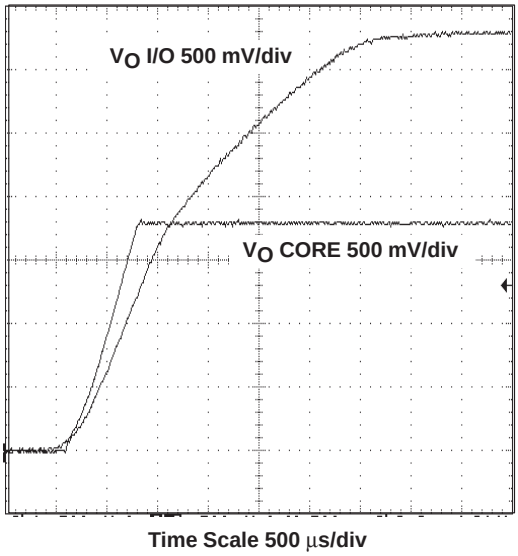
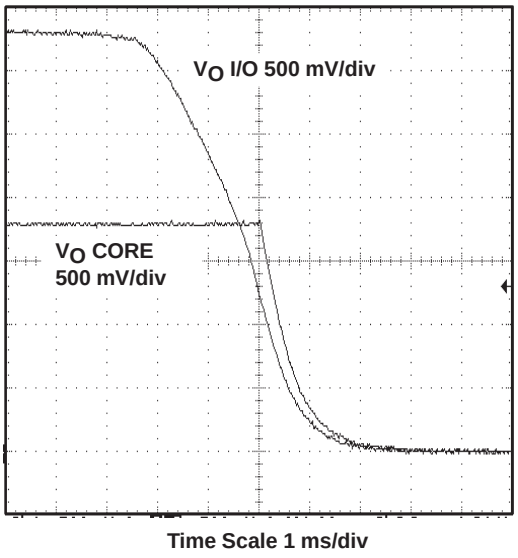


Figure 2–16. Powering Up With Core Voltage Falling Second



Chapter 3

Board Layout

This chapter provides a description of the TPS54380EVM–001 board layout and layer illustrations.

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3.1 Layout

The board layout for the TPS54380EVM-001 is shown in Figure 3–1 through Figure 3–3. The top-side layer of the TPS54380EVM–001 is laid out in a manner typical of a user application. The top and bottom layers are 1.5 oz. copper.

The top layer contains the main power traces for V_I, V_O, and $V_{(phase)}$. Also on the top layer are connections for the remaining pins of the TPS54380 and a large area filled with ground. The bottom layer contains ground and V_O copper areas, and some signal routing. The top and bottom ground traces are connected with multiple vias placed around the board including 10 directly under the TPS54380 device to provide a thermal path from the PowerPAD™ land to ground.

The input decoupling capacitors (C5 and C9), bias decoupling capacitor (C4), and bootstrap capacitor (C3) are all located as close to the IC as possible. In addition, the compensation components are kept close to the IC. The compensation circuit ties to the output voltage at the point of regulation, adjacent to the high frequency bypass output capacitor.

Figure 3–1. Top-Side Layout

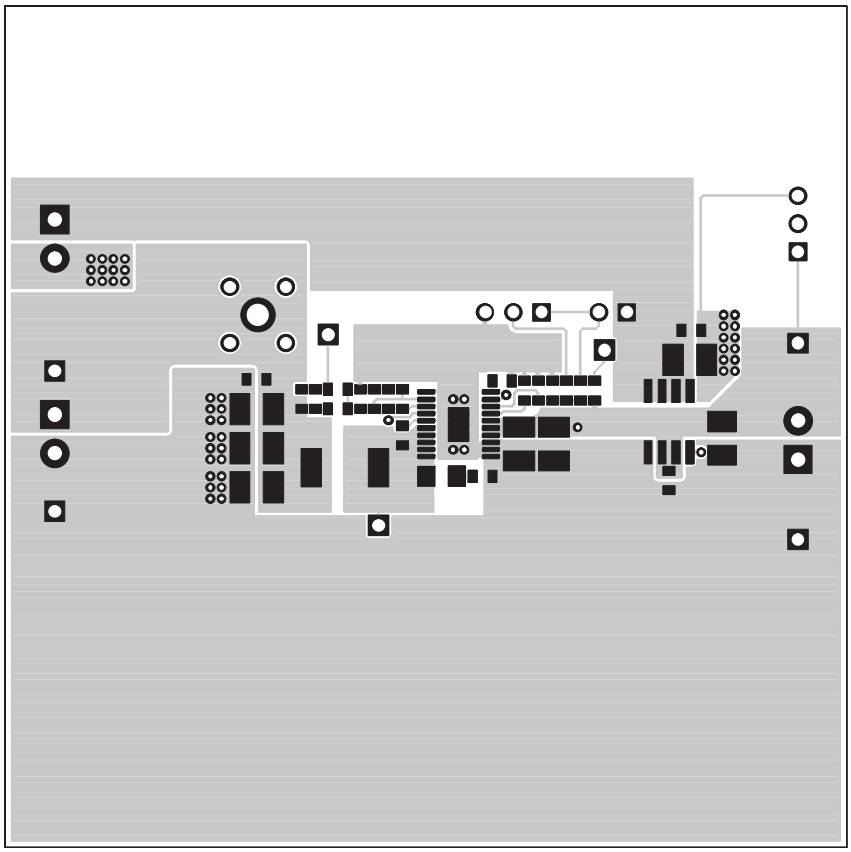


Figure 3–2. Bottom Side Layout (looking from top side)

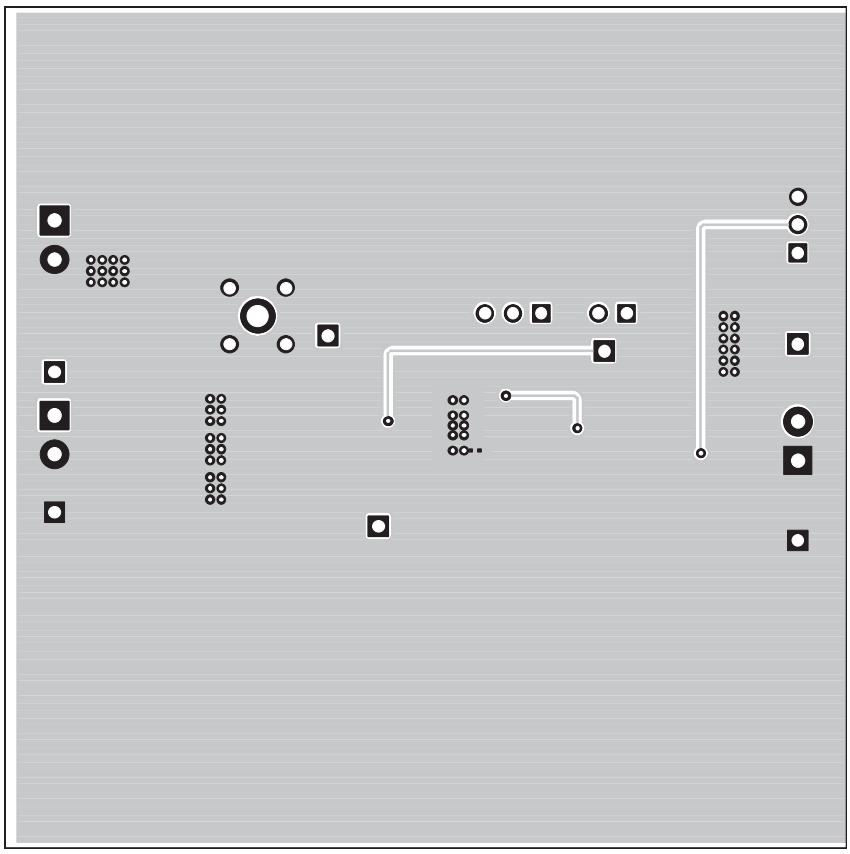
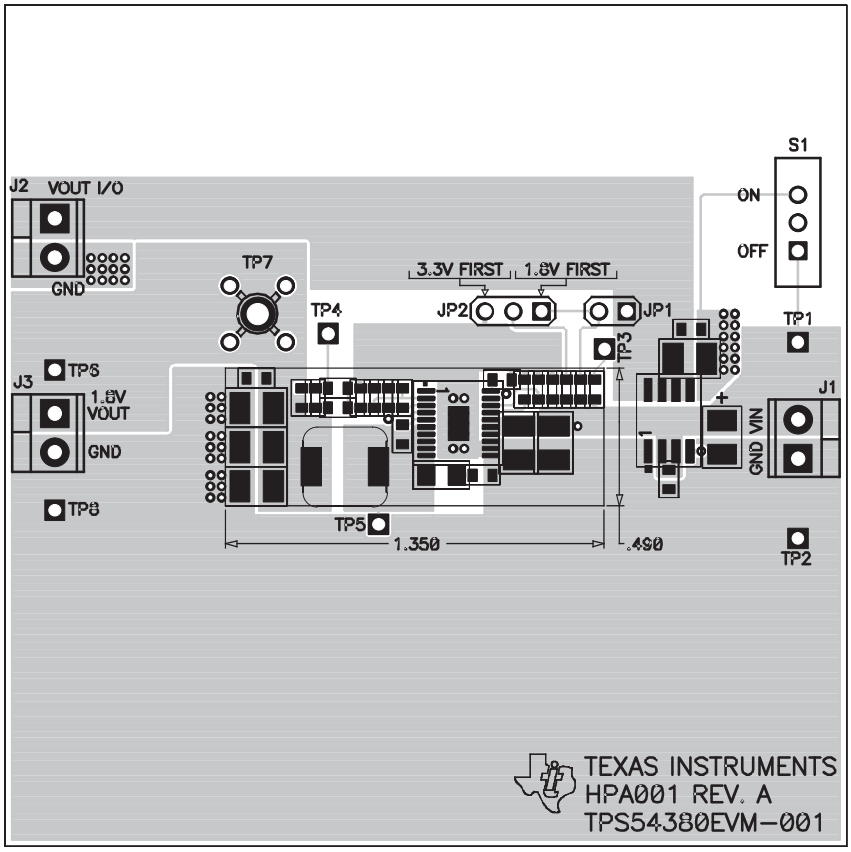


Figure 3–3. Top Side Assembly



Chapter 4

Schematic and Bill of Materials

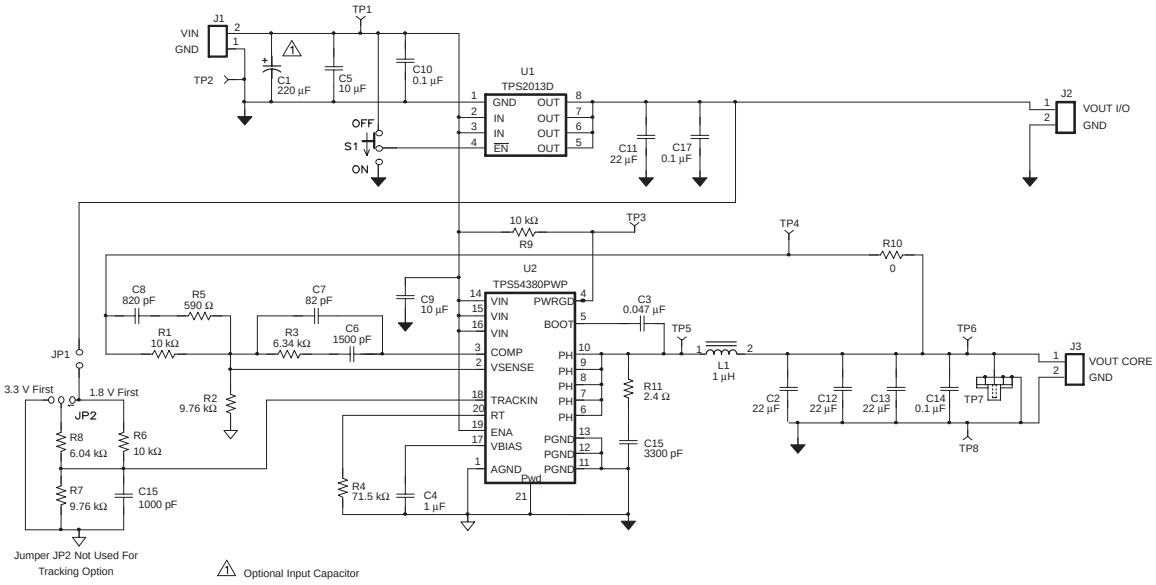
The TPS54380EVM–001 schematic and bill of materials are presented in this chapter.

Topic **Page**

4.1 Schematic

The schematic for the TPS54380EVM–001 is shown in Figure 4–1.

Figure 4–1. TPS54380EVM–001 Schematic



4.2 Bill of Materials

Table 4–1 contains the bill of materials for the TPS54380EVM–001.

Table 4–1. TPS54380EVM-001 Bill of Materials

Count	RefDes	Description	Size	MFR	Part Number
–	C1	Capacitor, POSCAP, 220 μF, 10 V, 40-mΩ, 20%	D4	Sanyo	10TPB220M
4	C2, C11, C12, C13	Capacitor, ceramic, 22 μF, 6.3 V, X5R, 20%	1210	Taiyo Yuden	JMK325BJ226MN
1	C3	Capacitor, ceramic, 0.047 μF, 25 V, X7R, 10%	603	Std	Std
1	C4	Capacitor, ceramic, 1.0 μF, 10 V, X5R, 20%	603	Std	Std
2	C5, C9	Capacitor, ceramic, 10 μF, 10 V, X5R, 20%	1210	Taiyo Yuden	LMK325BJ106MN
1	C6	Capacitor, ceramic, 1500 pF, 50 V, X7R, 10%	603	Std	Std
1	C7	Capacitor, ceramic, 82 pF, 50 V, NPO, 5%	603	Std	Std
1	C8	Capacitor, ceramic, 820 pF, 50 V, X7R, 10%	603	Std	Std
2	C10, C17	Capacitor, ceramic, 0.1 μF, 25 V, X7R, 10%	603	Std	Std
1	C14	Capacitor, ceramic, 0.1 μF, 25 V, X7R, 10%	603	Std	Std
1	C15	Capacitor, ceramic, 3300 pF, 50 V, X7R, 10%	603	Std	Std
1	C16	Capacitor, ceramic, 1000 pF, 25 V, X7R, 10%	603	Std	Std
3	J1, J2, J3	Terminal block, 2 pin, 6 A, 3,5 mm	75525	OST	ED1514
1	JP1	Header, 2 pin, 100 mil spacing, (36-pin strip)	0.100 × 2”	Sullins	PTC36SAAN
1	JP2	Header, 3 pin, 100 mil spacing, (36-pin strip)	0.100 × 3”	Sullins	PTC36SAAN
1	L1	Inductor, SMT, 1.0 μH, 8.5 A, 10 mΩ	0.270 sq	Vishay	IHLP–2525CZ–01
1	R1	Resistor, chip, 10.0 kΩ, 1/16 W, 1%	603	Std	Std
1	R2	Resistor, chip, 9.7 kΩ, 1/16 W, 1%	603	Std	Std
1	R3	Resistor, chip, 6.34 kΩ, 1/16 W, 1%	603	Std	Std
1	R4	Resistor, chip, 71.5 kΩ, 1/16 W, 1%	603	Std	Std
1	R5	Resistor, chip, 590 Ω, 1/16 W, 1%	603	Std	Std
1	R6	Resistor, chip, 10.0 kΩ, 1/16 W, 1%	603	Std	Std
1	R7	Resistor, chip, 9.76 kΩ, 1/16 W, 1%	603	Std	Std
1	R8	Resistor, chip, 6.04 kΩ, 1/16 W, 1%	603	Std	Std
1	R9	Resistor, chip, 768 Ω, 1/16 W, 1%	603	Std	Std
1	R10	Resistor, chip, 0 Ω, 1/16 W, 1%	603	Std	Std
1	R11	Resistor, chip, 2.4 Ω, 1/8 W, 1%	1206	Std	Std
1	S1	Switch, 1P2T, slide, PC mount, 200 mA	0.46 × 0.16	E_Switch	EG1218
1	SH1	Short jumper			
5	TP1, TP3, TP4, TP5, TP6	Test point, red, 1 mm	0.038”, 6400”	Farnell	240–345
2	TP2, TP8	Test point, black, 1 mm	0.038”, 6400”	Farnell	240–333
1	TP7	Adaptor, 3.5-mm probe clip (or 131–5031–00)	72900	Tektronix	131–4244–00
1	U1	IC, High-side power distribution SW with current limit	SO8	TI	TPS2013D
1	U2	IC, dc/dc tracking converter	PWP20	TI	TPS54380PWP
1	—	PCB, 3 In × 3 In × 0.062 In		Any	HPA001

Notes: 1) These assemblies are ESD sensitive, ESD precautions must be observed.
2) These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3) These assemblies must comply with workmanship standards IPC–A–610 Class 2.
4) Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.