MOP-AL404C

Parallel Display Specifications

Revision 1.1

Revision History

Revision	Description	Author
1.1	Corrected Pinout	Divino
1.0	Initial Release	Clark

Contents

Features

The Matrix Orbital Parallel display series offers a low cost display solution utilizing an industry standard communication interface for simple integration into a wide variety of new and existing applications. The Light Emitting Diode backlight with configurable brightness and voltage controlled contrast allows the MOP Liquid Crystal Display line to offer a professional display solution with low power impact for any project. The standard alphanumeric font set also allows up to eight custom characters to be saved in display Random Access Memory for a custom design touch.

Hardware

Drawing

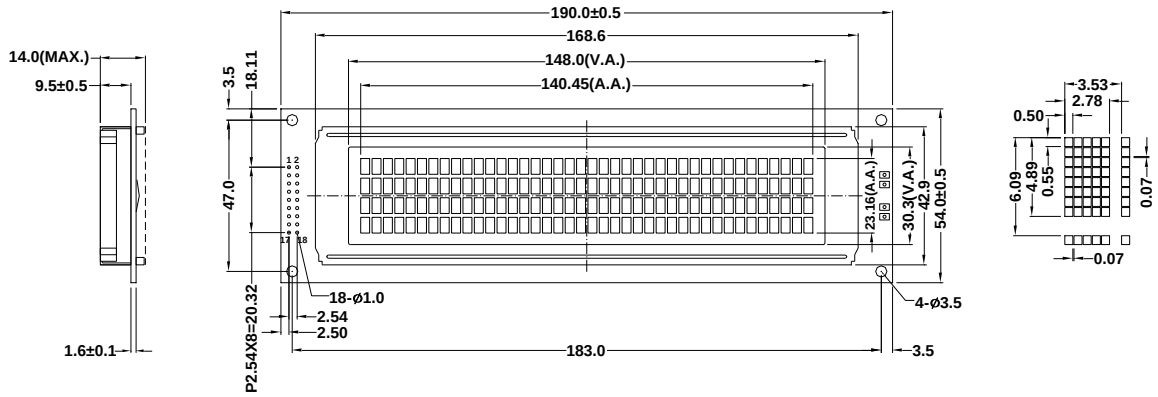

Figure 1: MOP-AL404C Mechanical Drawing

Interface

Table 1: Parallel Data

Pin	Symbol	Description
1	DB7	Data bit 7
2	DB6	Data bit 6
3	DB5	Data bit 5
4	DB4	Data bit 4
5	DB3	*Data bit 3
6	DB2	*Data bit 2
7	DB1	*Data bit 1
8	DB0	*Data bit 0

***Note:** Not used in 4-bit mode

Table 2: Display Control

Pin	Symbol	Description
9	CE	Chip Enable
10	R/W	Read/Write
11	RS	Register Select
12	V_0	Supply Voltage for LCD (Contrast)
13	V_{SS}	Ground
14	V_{DD}	Supply Voltage for Logic
15	CE	Chip Enable
16	NC	No Connect
17	LED(+)	Anode of LED Backlight
18	LED(-)	Cathode of LED Backlight

Instructions

Outline

The MOP line is controlled using a standard HD44780 compliant controller. The display is enabled by pulling the Chip Enable (CE) pin high, communication to and from the device is controlled using the Read/Write (R/W) input, and one of two available 8-bit registers are selected via the Register Select (RS) line. Using Register Select, either the Instruction Register (IR) or Data Register (DR) is selected by toggling RS low or high respectively.

While executing from the IR, the display will pull the Most Significant Bit of the data bus, DB7, high. While this Busy Flag (BF) is set, any instructions sent to the unit will be ignored. The status of this flag and the current position of the Address Counter (AC) can be obtained by performing a read operation on the instruction register at any time.

Table 3: Register Selection

RS	R/W	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 to DB6)
1	0	Write data to DDRAM or CGRAM (DR to DDRAM or CGRAM)
1	1	Read data from DDRAM or CGRAM (DDRAM or CGRAM to DR)

When writing for the DR, one of two locations can be chosen using the AC. The value provided to the AC when executing a set address command differentiates these locations. The AC is automatically decremented or incremented after a read or a write.

DDRAM provides eighty bytes of display memory to all displays. Memory outside the bounds of the display area can be used as general RAM. DDRAM addressing begins at the top left of the display with a value of 0, addresses then increment from left to right then down once a row is filled.

Table 4: One Line Addressing

Position	1	2	...	80
DDRAM Address	00	01	...	4F

Table 5: Two Line Addressing

Position	1	2	...	40
DDRAM Address	00	01	...	27
	40	41	...	67

Table 6: Four Line Addressing

Position	1	2	...	20
DDRAM Address	00	01	...	13
	40	41	...	53
	14	15	...	27
	54	55	...	67

CGRAM provides eight custom characters that can be created by writing to CGRAM locations then displayed using the first eight CGROM character codes, as seen in the character ROM table below.

Characters are sent to the display by performing a write operation on the DR using the correct character address within CGROM. Instructions are issued by writing to the IR; a complete list is available below.

Instruction Table

Table 7: Parallel Instruction Table

Instruction	Instruction Code										Description
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Clear Display	0	0	0	0	0	0	0	0	0	1	Write “20H” to all DDRAM locations, set DDRAM address to “00H”, return cursor to its original position, and set I/D to “1”.
Return Home	0	0	0	0	0	0	0	0	1	—	Set DDRAM address to “00H” and return cursor to its original position if shifted. The contents of DDRAM are not changed.
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display. DDRAM and CRAM addresses are incremented and cursor moves right when I/D is set to “1”, the opposite is true when reset to “0”. Setting SH to “1” causes the entire display to shift affecting only DDRAM.
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and blinking of cursor (B) on/off control bit. Setting D, C, or B to “1” will cause the display, underline cursor, or blinking cursor to turn on, the opposite is true for reset.
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	—	—	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data. Setting S/L to “1” will shift the screen horizontally while the opposite will move the cursor through all screen positions. Setting R/L to “1” will shift right immediately. AC and DDRAM are not altered.
Function Set	0	0	0	0	1	DL	N	F	—	—	Set interface data length, numbers of display line and, display font type. Setting DL to “1” specifies 8-bit mode, “0” 4-bit. Setting N to “1” permits a multi-line display, “0” a single. Resetting F to “0” indicates a 5x8 dot character.
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Read the status of the display controller through the BF Bit. The contents of address counter can also be read.
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM), location is determined by the AC. AC and display shift are adjusted as specified.
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM), location is determined by the AC, set command is recommended previous to this. Only AC is adjusted.

Character ROM

The character generator ROM stores up to two hundred fifty-six 5×8 dot character patterns from 8-bit character codes. The first eight characters are reserved for custom characters saved in CGRAM.

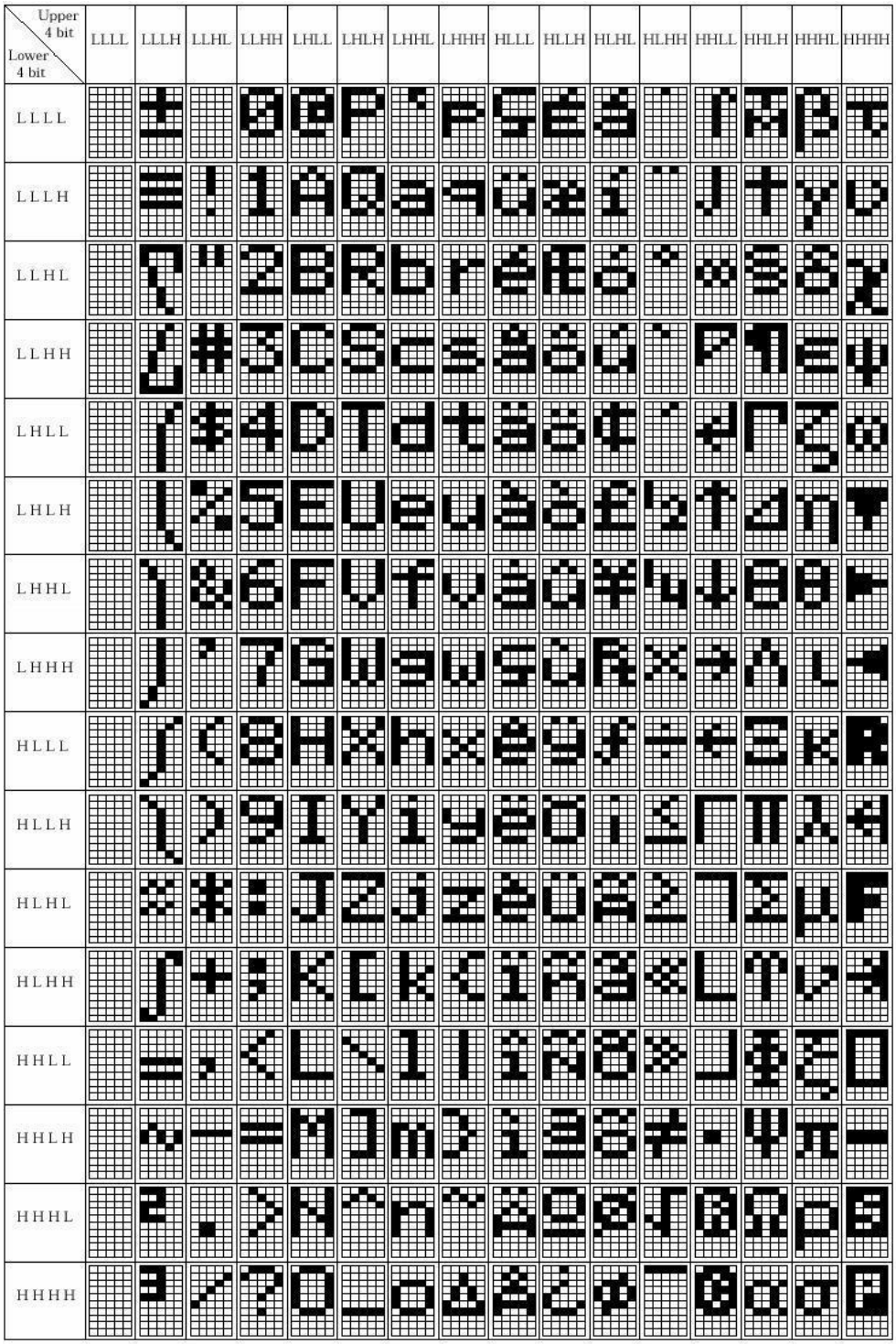

Figure 2: European Character Set

Character RAM

CGRAM allows the creation of up to eight 5x8 character patterns. Eight bytes are assigned to each character address, the least significant five bits of which represent the five pixel columns. Pixels are activated by setting the bit in their position in CGRAM to "1".

Each character has eight addresses in CGRAM corresponding to each of its eight pixel rows. The highest three bits represent the character address in DDRAM. The lowest three bits of this address represent the row positions beginning with 0 at the top. The last row will be logically OR'd with the cursor when it is active.

Finally, each character can be referenced in DDRAM and written to the screen using its eight bit address.

Table 8:Relationship between CGRAM Addresses, Character Codes (DDRAM Data) and Character Patterns (CGRAM Data)

Character Codes (DDRAM data)	CGRAM Address	Character Patterns (CGRAM data)
7 6 5 4 3 2 1 0	5 4 3 2 1 0	7 6 5 4 3 2 1 0
High Low	High Low	High Low
0 0 0 0 * 0 0 0	0 0 0	* * * 1 1 1 1 0
	0 0 1	1 0 0 0 1
	0 1 0	1 0 0 0 1
	0 1 1	1 1 1 1 0
	1 0 0	1 0 1 0 0
	1 0 1	1 0 0 1 0
	1 1 0	1 0 0 0 1
	1 1 1	* * * 0 0 0 0 0 — Cursor position
0 0 0 0 * 0 0 1	0 0 1	* * * 1 0 0 0 1 — Character pattern (1)
	0 0 0	0 1 0 1 0
	0 0 1	1 1 1 1 1
	0 1 0	0 0 1 0 0
	0 1 1	1 1 1 1 1
	1 0 0	0 0 1 0 0
	1 0 1	0 0 1 0 0
	1 1 0	0 0 0 0 0 — Cursor position
	1 1 1	* * * — Character pattern (2)
	0 0 0	* * *
	0 0 1	
0 0 0 0 * 1 1 1	1 1 1	1 0 0
		1 0 1
		1 1 0
		* * *

Note: * Indicates no effect.

Timing Characteristics

Table 9: Read and Write Operation Specifications

		Write			Read			
Item	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Enable cycle time	t_{cycE}	1200	—	—	1200	—	—	ns
Enable pulse width (high level)	PW_{EH}	140	—	—	140	—	—	ns
Enable rise/fall time	t_{Er},t_{Ef}	—	—	25	—	—	25	ns
Address set-up time (RS, R/W to E)	t_{AS}	0	—	—	0	—	—	ns
Address hold time	t_{AH}	10	—	—	10	—	—	ns
Data set-up time	t_{DS}	40	—	—	—	—	100	ns
Data hold time	t_H	10	—	—	10	—	—	ns

Conditions: Ta=25°C, VDD=5.0± 0.5V

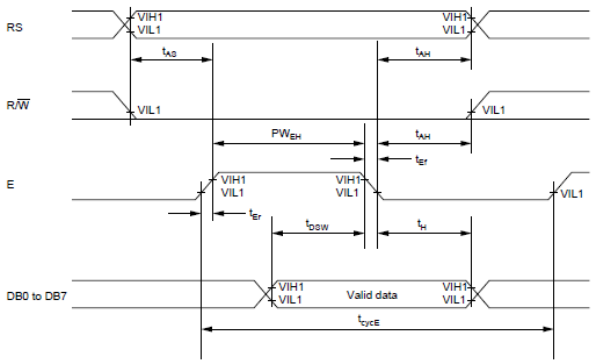

Figure 3: Write Timing Waveform

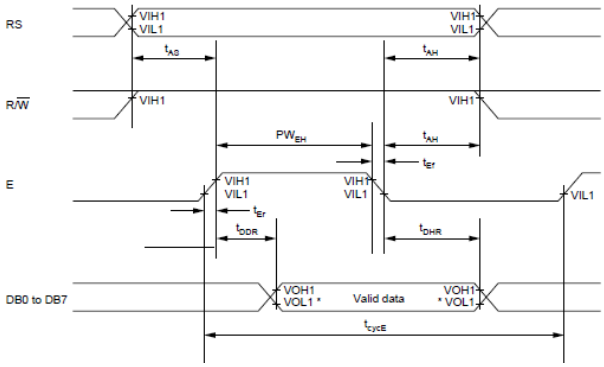

Figure 4: Read Timing Waveform

Initialization

Before beginning any application, it is recommended that all display settings be initialized. Below are algorithms for initializing the display in both 8-bit and 4-bit communication modes.

Before the first wait condition, please allow Vcc to rise to 4.5V then wait 40ms. During the three function set commands that follow, note that the busy flag cannot be checked; it becomes available in the last block. The unit will always expect a total of 8 bits to be sent, so note the structure used in four bit mode. The last initialization block will set the number of lines and character font as specified, turn the display off, issue the display clear command, and finally set the entry mode as desired.

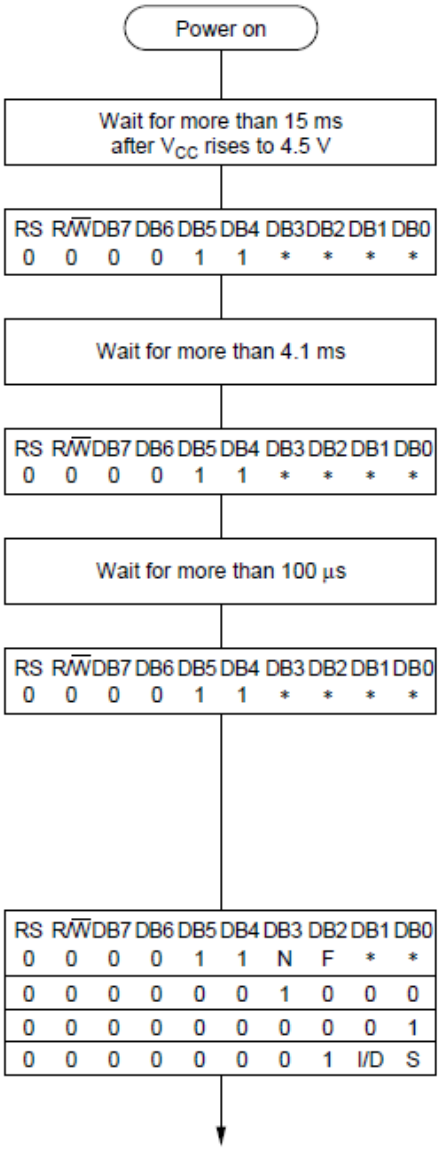

Figure 5: 8-bit Initialization

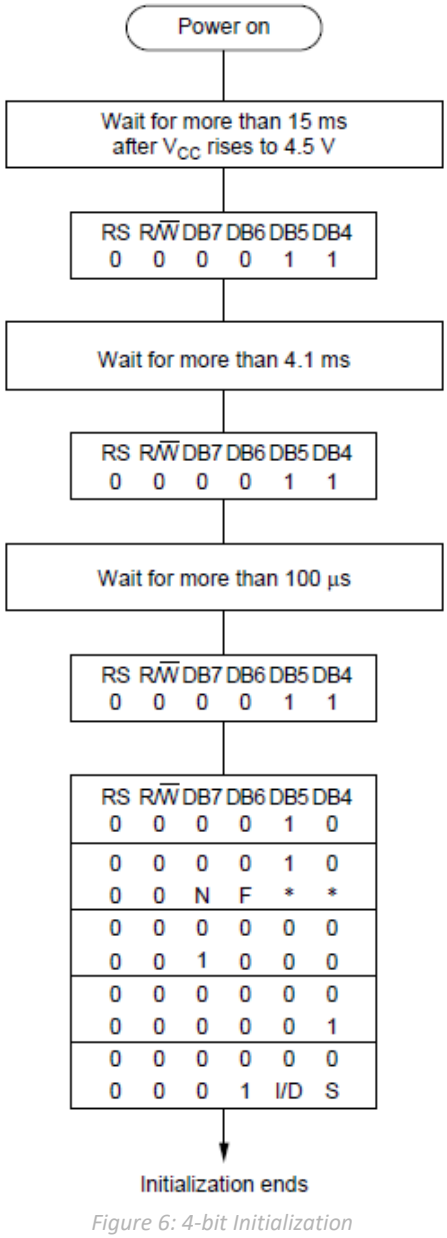

Figure 6: 4-bit Initialization

Note: * Indicates do not care condition.

Specifications

Electrical

Table 10: Electrical Characteristics

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage For Logic	V_{DD}	4.5	5.0	5.5	V
Supply Voltage For LCD (Contrast)	V_0	-13.5	—	V_{DD}	V
Input High Voltage	V_{IH}	0.7 V_{DD}	—	V_{DD}	V
Input Low Voltage	V_{IL}	V_{SS}	—	0.3 V_{DD}	V
Supply Current (V_{DD}=5V)	I_{DD}	1.5	2.0	3.5	mA
Supply Voltage of Yellow-Green Backlight (100 Die)	V_{LED}	3.8	4.1	4.3	V
Supply Current of Yellow-Green Backlight (100 Die)	I_{LED}	0	—	500	mA

Optical

Table 11: Display Characteristics

Item	Dimension	Unit
Number of Characters	40 Characters x 4 Lines	—
Module dimension	190.0 x 54.0 x 14.0	mm
View area	148.0 x 30.3	mm
Active area	140.45 x 23.16	mm
Character size	2.78 x 4.89	mm
Character pitch	3.53 x 6.09	mm
Dot size	0.50 x 0.55	mm
Dot pitch	0.57 x 0.62	mm
LCD type	STN	
Duty	1/16	
View direction	12 o'clock	

Table 12: Viewing Characteristics

Item	Symbol	Min	Typ	Max	Unit
View Angle	(V)θ	-20	—	35	deg
	(H)ϕ	-30	—	30	deg
Contrast Ratio	CR	—	3	—	—
Response Time	T rise	—	—	250	ms
	T fall	—	—	250	ms

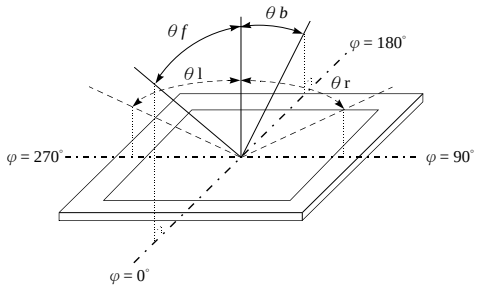

Figure 7: Viewing Angle Definition

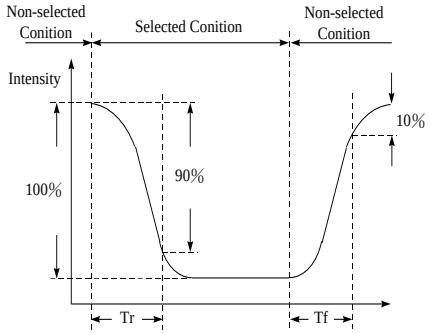

Figure 8: Display Response Time

Environmental

Table 13: Environmental Specifications

Item	Symbol	Min	Max	Unit
Operating Temp.	Top	-20	70	℃
Storage Temp.	Tstr	-30	80	℃

Note: Maximum 90% non-condensing humidity.

Troubleshooting

Power

For your MOP Display to function correctly, appropriate power must be applied, often as indicated by the backlight illuminating or a darkening of the character spaces. Please refer to the power diagram below and reference all voltages to the specifications provided.

Table 14

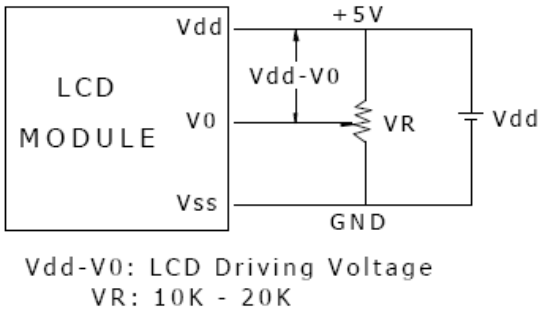

Figure 9: Single Supply Configuration

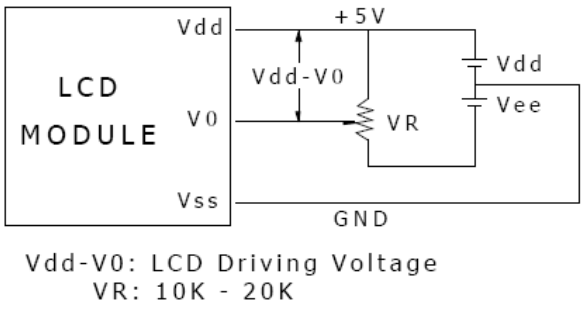

Figure 10: Dual Supply Configuration

Display

If your display is powered successfully, the backlight or contrast should be evident. A lack of text could be the result of a high contrast voltage, lower V_0. Also, ensure the expected DDRAM addresses are shown by moving the display to the home position.

Communication

When communication of either text or commands is interrupted, check all data and control pins for continuity. Ensure the display has been initialized correctly before sending information using the appropriate initialization algorithm. For 4-bit mode ensure D4-D7 are used. Finally, slow down communication and refer to timing diagrams and specifications for proper control flow.

Precautions

- Do not make extra holes on the display, modify its shape, or change the components.
- Avoid applying excessive electrical shock to the module.
- Do not drop, bend, twist, or disassemble the display.
- Avoid operation outside absolute maximum ratings.
- Solder only to the I/O terminals provided.
- Store in an anti-static container within a clean environment.

Ordering

Part Numbering Scheme

Table 15: Parallel Part Numbering Scheme

MOP	-	A	L	40	4	C	-	B	Y	F	Y	-	2	5	E	-	3	I	N
1		2	3	4	5	6		7	8	9	10		11	12	13		14	15	16

Options

Table 16: Parallel Part Options

#	Designator	Options
1	Product Line	MOP: Matrix Orbital Parallel Display
2	Display Type	A: Alphanumeric
3	Screen Type	L: Liquid Crystal Display
4	Display Columns	8: Eight Character Columns 16: Sixteen Character Columns 20: Twenty Character Columns 24: Twenty-Four Character Columns 40: Forty Character Columns
5	Display Rows	2: Two Character Rows 4: Four Character Rows
6	Display Form Factor	A: A Form Factor B: B Form Factor C: C Form Factor F: F Form Factor
7	IC Package	B: Chip on Board
8	LCD Glass Type	B: STN Positive Blue F: FFSTN Negative G: STN Positive Grey T: FSTN Negative W: FSTN Positive Y: STN Positive Yellow
9	Polarizer Style	F: Transflective T: Transmissive
10	Backlight Colour	R: Red Y: Yellow-Green W: White
11	Viewing Angle	1: 6:00 2: 12:00
12	Controller	5: S6A0069 Compatible
13	Character Set	E: European J: Japanese
14	Input Voltage	3: 5.0V
15	Temperature Range	I: Industrial
16	Negative Voltage Generation	N: None Provided

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