Contents

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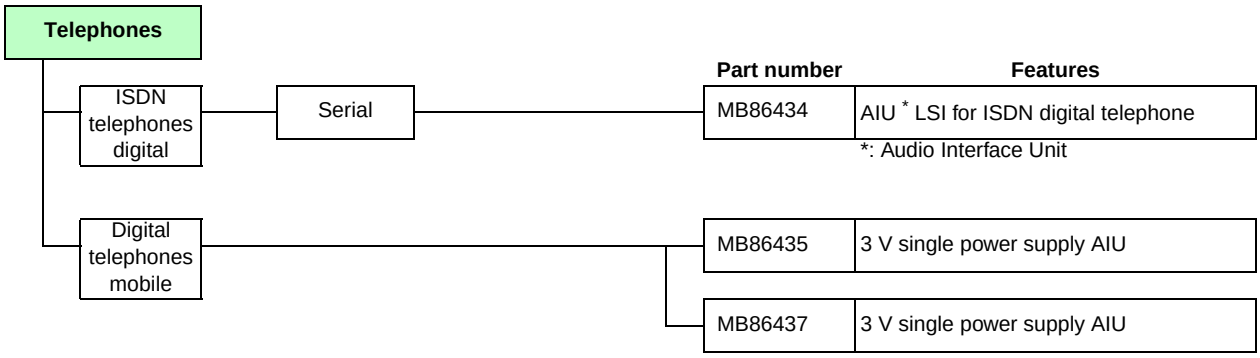
ASSP Product Line-up

Telephone Products



Part number	Features
MB86434	AIU * LSI for ISDN digital telephone
MB86435	3 V single power supply AIU
MB86437	3 V single power supply AIU

*: Audio Interface Unit

Telephone Products

ISDN Digital Telephone LSIs

Part number	Functions	CODEC	Power supply voltage (V)	Package
				QFP
MB86434	AIU for ISDN digital telephones CODEC, DTMF tones, service tone Internal ringer tone	A-laW μ-laW 14-bit linear	+5±5%	64P

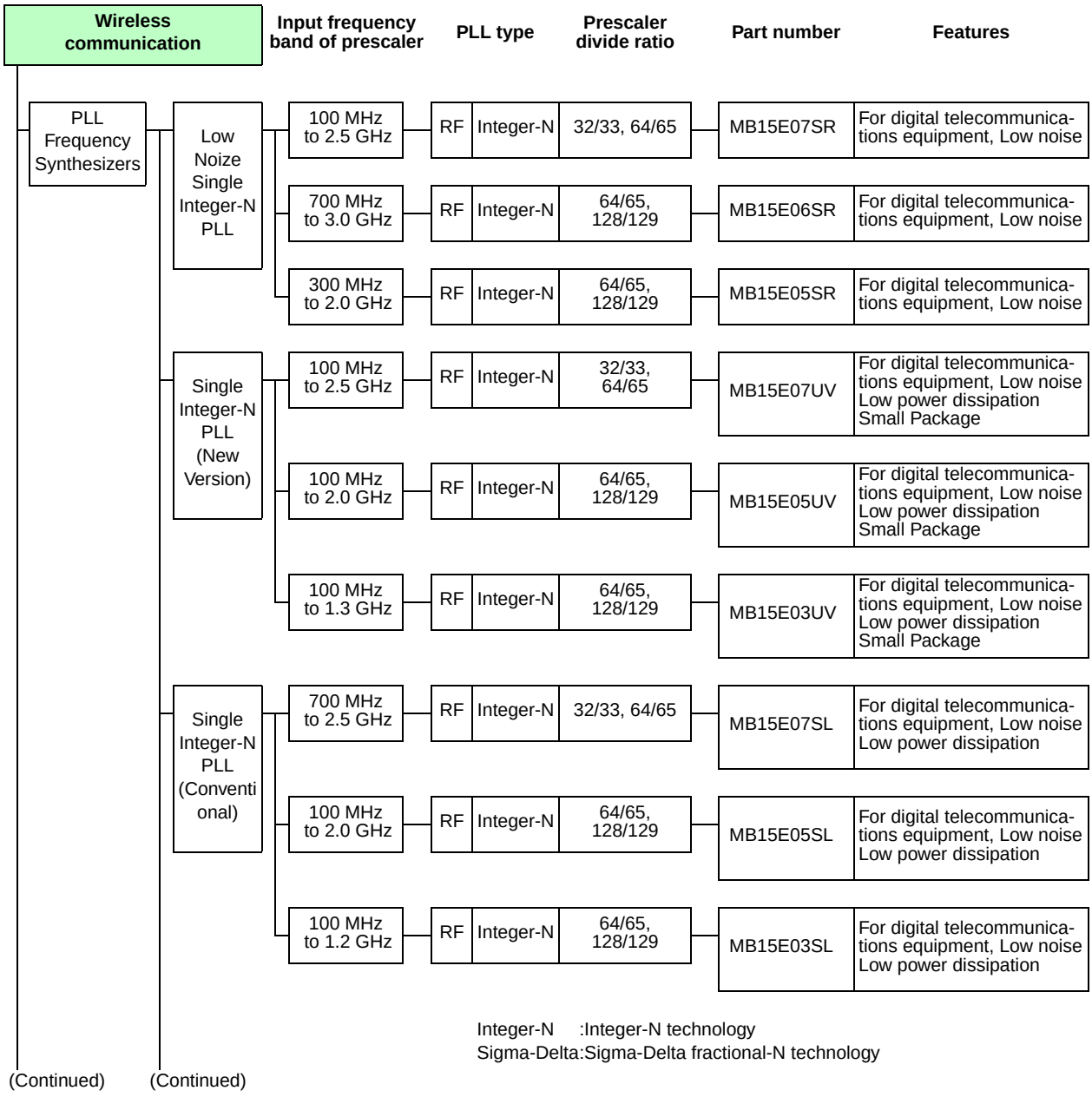
Package: P - Plastic

LSIs for Digital Mobile Telephones

Part number	Functions	Compression law	Power supply voltage (V)	Package
				LQFP
MB86435	3 V single power supply AIU	A-laW μ-laW linear	2.7 to 3.6	64P
MB86437				48P

Package: P - Plastic

Wireless Communication Products



Wireless communication		Input frequency band of prescaler	PLL type		Prescaler divide ratio	Part number	Features
PLL Frequency Synthesizers	Low Noize Single Integer-N PLL	100 MHz to 2.5 GHz	RF	Integer-N	32/33, 64/65	MB15E07SR	For digital telecommunications equipment, Low noise
		700 MHz to 3.0 GHz	RF	Integer-N	64/65, 128/129	MB15E06SR	For digital telecommunications equipment, Low noise
		300 MHz to 2.0 GHz	RF	Integer-N	64/65, 128/129	MB15E05SR	For digital telecommunications equipment, Low noise
	Single Integer-N PLL (New Version)	100 MHz to 2.5 GHz	RF	Integer-N	32/33, 64/65	MB15E07UV	For digital telecommunications equipment, Low noise Low power dissipation Small Package
		100 MHz to 2.0 GHz	RF	Integer-N	64/65, 128/129	MB15E05UV	For digital telecommunications equipment, Low noise Low power dissipation Small Package
		100 MHz to 1.3 GHz	RF	Integer-N	64/65, 128/129	MB15E03UV	For digital telecommunications equipment, Low noise Low power dissipation Small Package
	Single Integer-N PLL (Conventional)	700 MHz to 2.5 GHz	RF	Integer-N	32/33, 64/65	MB15E07SL	For digital telecommunications equipment, Low noise Low power dissipation
		100 MHz to 2.0 GHz	RF	Integer-N	64/65, 128/129	MB15E05SL	For digital telecommunications equipment, Low noise Low power dissipation
		100 MHz to 1.2 GHz	RF	Integer-N	64/65, 128/129	MB15E03SL	For digital telecommunications equipment, Low noise Low power dissipation

Integer-N :Integer-N technology
Sigma-Delta:Sigma-Delta fractional-N technology

(Continued) (Continued)

Wireless Communication Products

PLL Frequency Synthesizers

• Low Noize Single Integer-N PLL

Part number	Input frequency band (Hz)		PLL Type	Divide ratio				Power supply current typ (mA)	Power save current typ (µA)	Power supply voltage (V)			Package	
	min	max		Prescaler	Program counter	Swallow counter	Reference counter			min	typ	max	BCC	TSSOP
MB15E07SR	100M	2.5G	Integer-N	32/33, 64/65	Binary 11bit 3 to 2047	Binary 7bit 0 to 127	Binary 14bit 3 to 16383	8.0	0.1	2.7	3.75	5.0	16P	16P
								7.0	0.1	2.7	3.0	5.0		
MB15E06SR	700M	3.0G		64/65, 128/129				8.0	0.1	2.7	3.0	4.0	16P	16P
MB15E05SR	300M	2.0G		64/65, 128/129				7.0	0.1	2.7	3.75	5.0	16P	16P
								6.0	0.1	2.7	3.0	5.0		

Package: P - Plastic

• Single Integer-N PLL (New Version)

Part number	Input frequency band (Hz)		PLL Type	Divide ratio				Power supply current typ (mA)	Power save current typ (µA)	Power supply voltage (V)			Package	
	min	max		Prescaler	Program counter	Swallow counter	Reference counter			min	typ	max	TSSOP	BCC
◎MB15E07UV	100M	2.5G	Integer-N	32/33, 64/65	Binary 11bit 3 to 2047	Binary 7bit 0 to 127	Binary 14bit 3 to 16383	3.5	0.1	2.4	3.0	3.6	16P	18P
◎MB15E05UV		2.0G		64/65, 128/129				2.9	0.1	2.4	3.0	3.6	16P	18P
◎MB15E03UV		1.3G		64/65, 128/129				2.1	0.1	2.4	3.0	3.6	16P	18P

◎ : Now planning

Package: P - Plastic

• Single Integer-N PLL (Conventional)

Part number	Input frequency band (Hz)		PLL Type	Divide ratio				Power supply current typ (mA)	Power save current typ (µA)	Power supply voltage (V)			Package	
	min	max		Prescaler	Program counter	Swallow counter	Reference counter			min	typ	max	SSOP	BCC
MB15E07SL	700M	2.5G	Integer-N	32/33, 64/65	Binary 11bit 3 to 2047	Binary 7bit 0 to 127	Binary 14bit 3 to 16383	4.5	0.1	2.4	3.0	3.6	16P	16P
MB15E05SL	100M	2.0G		64/65, 128/129	Binary 11bit 3 to 2047	Binary 7bit 0 to 127	Binary 14bit 3 to 16383	3.5	0.1	2.4	3.0	3.6	16P	16P
MB15E03SL		1.2G		64/65, 128/129	Binary 11bit 3 to 2047	Binary 7bit 0 to 127	Binary 14bit 3 to 16383	2.5	0.1	2.4	3.0	3.6	16P	16P

Package: P - Plastic

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	Input frequency band of prescaler	PLL type		Prescaler divide ratio	Part number	Features
Dual Integer-N PLL	400 MHz to 2.6 GHz	RF	Integer-N	32/33, 64/65	MB15F78UL	For digital telecommunications equipment Low noise Low power dissipation
	100 MHz to 1.2 GHz	IF	Integer-N	16/17, 32/33		
	2.0 GHz to 6.0 GHz	RF	Integer-N	6.0G : 16/17, 32/33	MB15F76UL	For digital high-speed telecommunications equipment
	100 MHz to 1.5 GHz	IF	Integer-N	1.5G : 4/5, 8/9		
		(Fixed part 4 division)				
	2.0 GHz to 4.0 GHz	RF	Integer-N	4.0G : 64/65, 128/129	MB15F74UV	Small Package For digital high-speed telecommunications equipment
	200 MHz to 2.0 GHz	IF	Integer-N	2.0G : 32/33, 64/65		
					MB15F74UL	For digital high-speed telecommunications equipment
	200 MHz to 2.25 GHz	RF	Integer-N	2.25G : 64/65, 128/129	MB15F73UV	Small Package For digital high-speed telecommunications equipment
	50 MHz to 600 MHz	IF	Integer-N	600M : 8/9, 16/17		
					MB15F73UL	For digital high-speed telecommunications equipment
	100 MHz to 1.3GHz	RF	Integer-N	1.3G : 64/65, 128/129	MB15F72UV	Small Package For digital high-speed telecommunications equipment
	50 MHz to 350 MHz	IF	Integer-N	350M : 8/9, 16/17		
					MB15F72UL	For digital high-speed telecommunications equipment
	500 MHz to 2.6 GHz	RF	Integer-N	32/33, 64/65	MB15F30UV	Small Package For digital high-speed telecommunications equipment Low power dissipation
	45 MHz to 510 MHz	IF	Integer-N	8/9, 16/17		
	100 MHz to 1.1GHz	RF	Integer-N	1.1G : 64/65, 128/129	MB15F07SL	For digital high-speed telecommunications equipment Low noise
	100 MHz to 1.1GHz	IF	Integer-N	1.1G : 64/65, 128/129		

Integer-N :Integer-N technology
Sigma-Delta:Sigma-Delta fractional-N technology

(Continued) (Continued)

• Dual Integer-N PLL

Part number	Input frequency band (Hz)		PLL Type	Divide ratio				Power supply current typ (mA)	Power save current typ (μA)	Power supply voltage (V)			Package	
	min	max		Prescaler	Program counter	Swallow counter	Reference counter			min	typ	max	BCC	TSSOP
MB15F74UV	2.0G 200M	4.0G 2.0G	Integer-N	RF : 64/65, 128/129 IF : 32/33, 64/65	Binary 11 bit 3 to 2047	Binary 7bit 0 to 127	Binary 14bit 3 to 16383	6.5 2.5	0.1 0.1	2.7	3.0	3.6	18P	–
MB15F73UV	200M 50M	2.25G 600M		RF : 64/65, 128/129 IF : 8/9, 16/17				2.0 1.2	0.1 0.1	2.4	2.7	3.6	18P	–
MB15F72UV	100M 50M	1.3G 350M		RF : 64/65, 128/129 IF : 8/9, 16/17				1.5 1.0	0.1 0.1	2.4	2.7	3.6	18P	–
MB15F30UV	500M 45M	2.6G 510M		RF : 32/33, 64/65 IF : 8/9, 16/17	Binary 11 bit 3 to 2047	Binary 7bit 0 to 63	Binary 15bit 3 to 32768	2.8 1.2	0.1 0.1	2.4	2.7	3.6	18P	–
MB15F78UL	400M 100M	2.6G 1.2G		RX : 32/33, 64/65 TX : 16/17, 32/33	Binary 11 bit 3 to 2047	Binary 7bit 0 to 127	Binary 14bit 3 to 16383	2.8 1.7	0.1 0.1	2.4	2.7	3.6	20P	20P
MB15F76UL	2.0G 100M	6.0G 1.5G		RF : 16/17, 32/33 (Fixed part 4 division) IF : 4/5, 8/9 (Fixed part 4 division)	Binary 13bit 3 to 8191	Binary 5bit 0 to 31	Binary 14bit 3 to 16383	6.2 2.3	0.1 0.1	2.5	3.0	3.6	20P	–
MB15F74UL	2.0G 200M	4.0G 2.0G		RF : 64/65,128/129 IF : 32/33,64/65	Binary 11bit 3 to 2047	Binary 7bit 0 to 127	Binary 14bit 3 to 16383	6.5 2.5	0.1 0.1	2.7	3.0	3.6	20P	–
MB15F73UL	200M 50M	2.25G 600M		RF : 64/65,128/129 IF : 8/9,16/17				2.0 1.2	0.1 0.1	2.4	2.7	3.6	20P	20P
MB15F72UL	100M 50M	1.3G 350M		RF : 64/65,128/129 IF : 350M: 8/9,16/17				1.5 1.0	0.1 0.1	2.4	2.7	3.6	20P	20P
MB15F07SL	100M 100M	1.1G 1.1G		64/65,128/129 64/65,128/129	Binary 11bit 3 to 2047	Binary 7bit 0 to 127	Binary 14bit 3 to 16383	5.5 5.5	0.1 0.1	2.5	3.0	3.6	16P	16P

Package: P - Plastic

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	Input frequency band of prescaler	PLL type		Prescaler divide ratio	Part number	Features
Single Sigma-Delta Fractional-N PLL	500 MHz to 2.0 GHz	RF	Sigma-Delta	16/17/18	MB15E65UV	High-speed lock-up/Low noize Modulo : 2^{18}/ 2^{15}
	1.0 GHz to 3.5 GHz	RF	Sigma-Delta	16/17/18	MB15E64UV	High-speed lock-up/Low noize Modulo : 2^{18}/ 2^{15}
Single Sigma-Delta Fractional-N PLL (RF) & Integer-N PLL (IF)	500MHz to 2.0 GHz	RF	Sigma-Delta	16/17, 20/21	MB15F63UL	High-speed lock-up Modulo : 2^{20} LPF switch
	100 MHz to 600MHz	IF	Integer-N	8/9, 16/17		
IF Band Integer-N PLL	233.15/ 259.20MHz	IF	Integer-N	16/17	MB15C101	IF PLL for PHS With no external setting of a divide ratio
	10 to 330MHz (1.2 V to 1.5 V)	IF	Integer-N	64/65	MB15C02	Low voltage Low power dissipation With setting of a divide ratio
IF Band Integer-N PLL With 68 bit Flash memory	100 to 500 MHz	IF	Integer-N	8/9 16/17	MB15C51	68 bit Flash memory (Internal) With setting of 2 divide ratio

Integer-N :Integer-N technology
Sigma-Delta:Sigma-Delta fractional-N technology

(Continued) (Continued)

• Single Sigma-Delta Fractional-N PLL

Part number	Input frequency band (Hz)		PLL Type	Divide ratio				Power supply current typ (mA)	Power save current typ (μA)	Power supply voltage (V)			Package
	min	max		Prescaler	Program counter	Swallow counter	Reference counter			min	typ	max	BCC
MB15E65UV	500 M	2.0 G	Sigma-Delta	16/17/18	Binary 8 bit 9 to 255	Binary 4 bit 0 to 15	Binary 6 bit 1 to 63	4.6	0.1	2.7	3.0	3.3	18P
MB15E64UV	1.0 G	3.5 G		16/17/18	Binary 8 bit 9 to 255	Binary 4 bit 0 to 15	Binary 6 bit 1 to 63	4.6	0.1	2.7	3.0	3.3	18P

Package: P - Plastic

• Single Sigma-Delta Fractional-N PLL (RF) & Integer-N PLL (IF)

Part number	Input frequency band (Hz)		PLL Type	Divide ratio				Power supply current typ (mA)	Power save current typ (μA)	Power supply voltage (V)			Package
	min	max		Prescaler	Program counter	Swallow counter	Reference counter			min	typ	max	BCC
MB15F63UL	500M 100M	2.0G 600M	Sigma-Delta, Integer-N	RF : 16/17, 20/21, IF : 8/9,16/17	Binary 7bit 5 to 127(RF) Binary 11bit 3 to 2047(IF)	Binary 4bit 0 to 15(RF) Binary 7bit 0 to 127(IF)	Binary 6bit 1 to 63(RF) Binary 14 bit 3 to 16383(IF)	6.1 1.4	0.1 0.1	2.7	3.0	3.3	20P

Package: P - Plastic

• IF Band Integer-N PLL

Part number	Input frequency band (Hz)		PLL Type	Divide ratio				Power supply current typ (mA)	Power save current typ (μA)	Power supply voltage (V)			Package	
	min	max		Prescaler	Program counter	Swallow counter	Reference counter			min	typ	max	SSOP	BCC
MB15C101	233.15 259.20		Integer-N	16/17	291 33	7 12	384 40	1.0	–	2.4	3.0	3.6	8P	16P
MB15C02	10 M	330M	Integer-N	64/65	12bit, 5 to 4095	6bit, 0 to 63	14bit, 16 to 16383	1.0	70	1.0	1.2	1.5	16P 20P	–

Package: P - Plastic

• IF Band Integer-N PLL (with 68 bit Flash memory)

Part number	Input frequency band (Hz)		PLL Type	Divide ratio				Power supply current typ (mA)	Power save current typ (μA)	Power supply voltage (V)			Package	
	min	max		Prescaler	Program counter	Swallow counter	Reference counter			min	typ	max	SSOP	BCC
○MB15C51	100 M	500 M	Integer-N	8/9 16/17	11 bit 3 to 2047	6 bit 0 to 63	10 bit 3 to 1023	3.0	0.1	2.7 4.9	3.0 5.0 *	3.5 5.1	16P	16P

* : When memory writing

○ : New product

Package: P - Plastic

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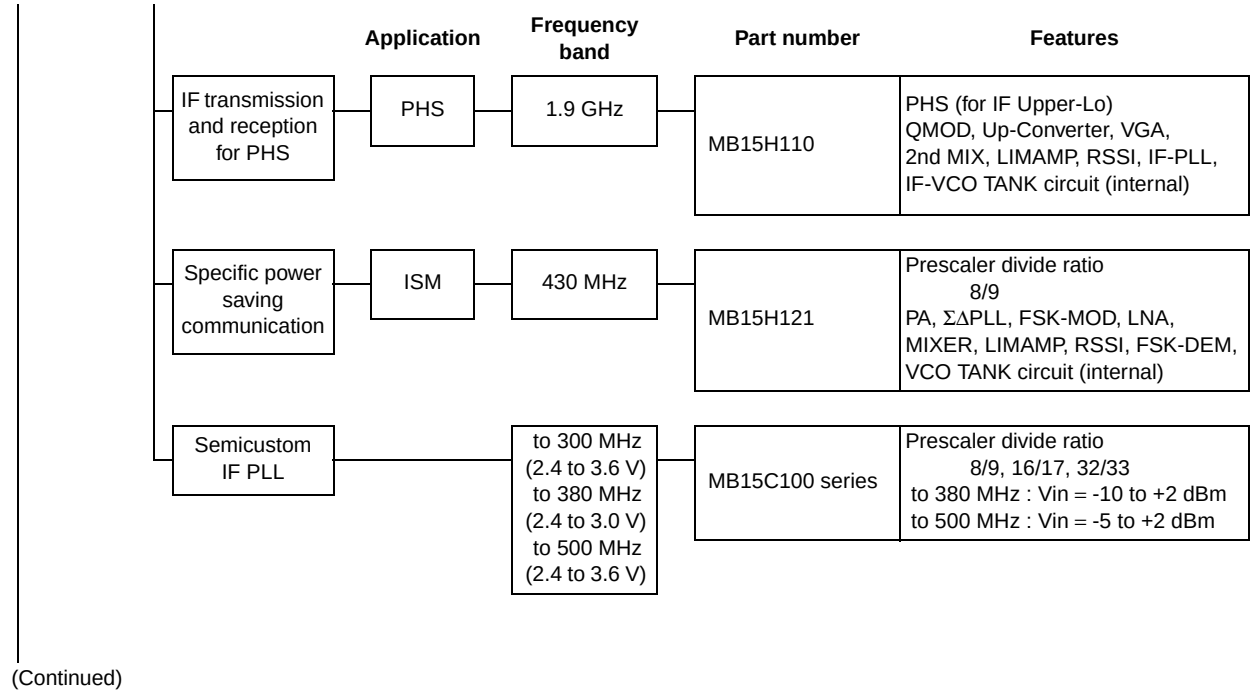

	Application	Frequency band	Part number	Features
IF transmission and reception for PHS	PHS	1.9 GHz	MB15H110	PHS (for IF Upper-Lo) QMOD, Up-Converter, VGA, 2nd MIX, LIMAMP, RSSI, IF-PLL, IF-VCO TANK circuit (internal)
Specific power saving communication	ISM	430 MHz	MB15H121	Prescaler divide ratio 8/9 PA, ΣΔPLL, FSK-MOD, LNA, MIXER, LIMAMP, RSSI, FSK-DEM, VCO TANK circuit (internal)
Semicustom IF PLL		to 300 MHz (2.4 to 3.6 V) to 380 MHz (2.4 to 3.0 V) to 500 MHz (2.4 to 3.6 V)	MB15C100 series	Prescaler divide ratio 8/9, 16/17, 32/33 to 380 MHz : Vin = -10 to +2 dBm to 500 MHz : Vin = -5 to +2 dBm

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• IF transmission and reception for PHS

Part number	Application	Frequency band (GHz)	Functions	Power supply current typ (mA)	Power save current typ (μA)	Power supply voltage (V)			Package
						min	typ	max	BCC
MB15H110	PHS	1.9	PHS (for IF Upper-Lo) QMOD, Up-Converter, VGA, 2ndMIX, LIMAMP, RSSI, IF-PLL, IF-VCO TANK circuit (internal)	29.7 : TX 10.5 : RX	0.3	2.7	2.9	3.1	40P (0.75 mm thickness)

Package: P - Plastic

• Specific power saving communication

Part number	Application	Frequency band (MHz)	Functions	Power supply current typ (mA)	Power save current typ (μA)	Power supply voltage (V)			Package
						min	typ	max	LQFP
○MB15H121	ISM	430	Prescaler divide ratio 8/9 PA, ΣΔPLL, FSK-MOD, LNA, MIXER, LIMAMP, RSSI, FSK-DEM, VCO TANK circuit (internal)	6.7 (PLL) 23.0 (TX) 5.0 (RX)	0.3	2.2	2.5	2.8	48P

○: New product

Package: P - Plastic

• Semicustom IF PLL

Part number (Series name)	Frequency band (MHz)	Prescaler divide ratio	Power supply current (mA)	Power supply voltage (V)	Package	
					SSOP	BCC
MB15C100 series	to 300 *1 (2.4 to 3.6 V) to 380 *1 (2.4 to 3.0 V) to 500 *2 (2.4 to 3.6 V)	8/9, 16/17, 32/33	1.2 (300 MHz, V_{CC} = 3 V)	+2.4 to +3.6	8P	16P (S type)

*1: Input sensitivity –10 to +2 dBm *2: Input sensitivity –5 to +2 dBm

Package: P - Plastic

Wireless Communication Products

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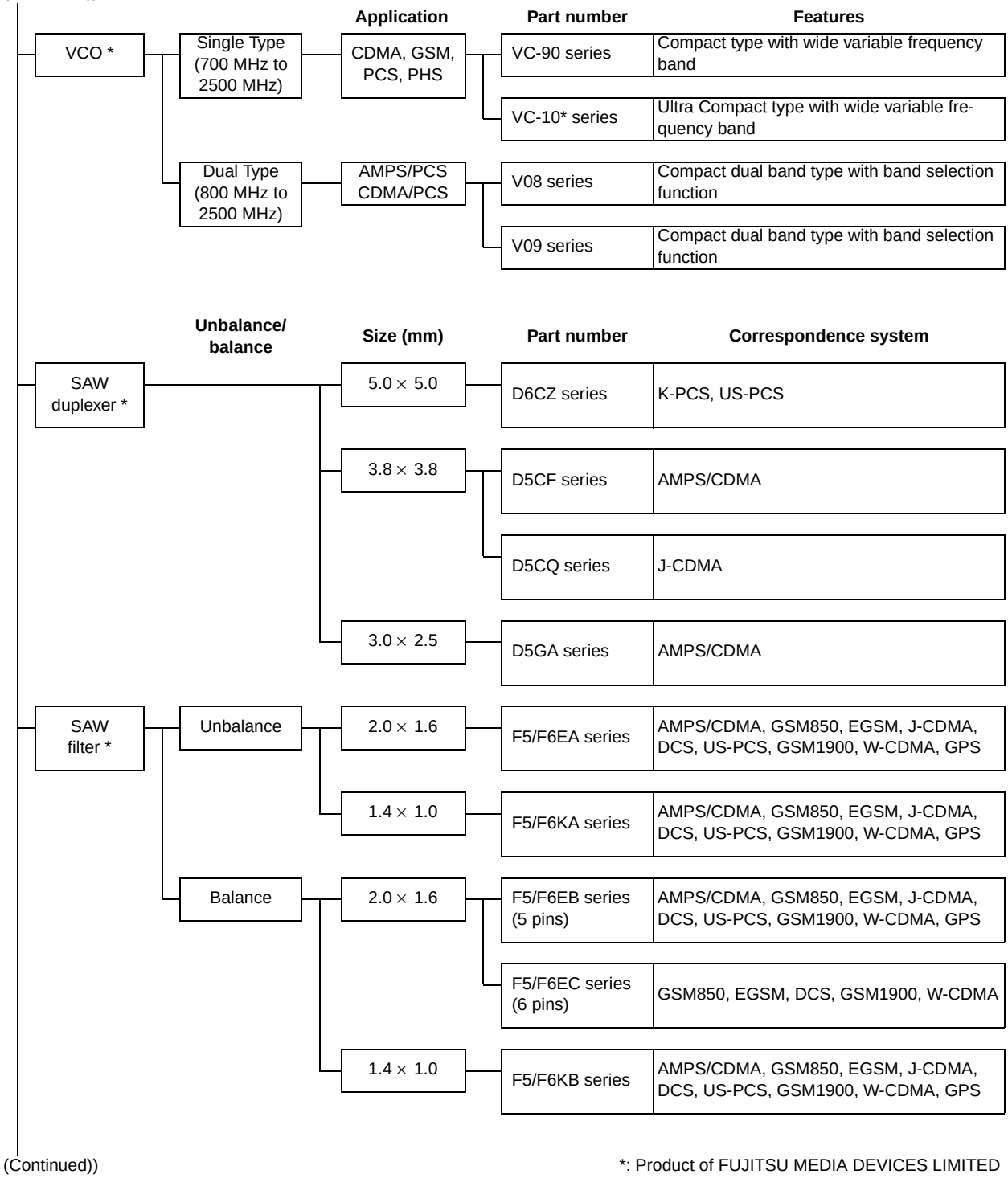

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VCO

Part number	Functions	Application	Frequency (MHz)	Power supply voltage (V)	Package Typ. (mm)
VC-90 series	Voltege Controlled Oscillator	CDMA,GSM,PCS,PHS	700 to 2500	2.5 to 3.3	5.0 × 4.0 × 1.55
VC-10* series					4.5 × 3.2 × 1.5
V08 series		AMPS•CDMA/PCS	800 to 2500	2.8	5.5 × 4.8 × 1.8
V09 series					5.0 × 4.0 × 1.4

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SAW Duplexer for Mobile Communication System

Correspondence system	Size (mm)	Part Number	Remarks
AMPS/CDMA	3.8 × 3.8	FAR-D5CF-881M50-D1F1	Two types of package are available
	3.0 × 2.5	FAR-D5GA-881M50-D1AA	Two types of package are available
J-CDMA	3.8 × 3.8	FAR-D5CQ-906M00-D1Q1	Two types of package are available
K-PCS	5.0 × 5.0	FAR-D6CZ-1G8550-D1T1	Two types of package are available
US-PCS	5.0 × 5.0	FAR-D6CZ-1G9600-D1XC	Two types of package are available

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SAW Filter for Mobile Communication System

Correspondence system	Transmission/ Reception	Size (mm)	Part number	Remarks
AMPS/CDMA, GSM850	Transmission	2.0 × 1.6	FAR-F5EA-836M50-D27A	Unbalanced
		1.4 × 1.0	FAR-F5KA-836M50-D4CM	Unbalanced
	Reception	2.0 × 1.6	FAR-F5EA-881M50-D27B	Unbalanced
			FAR-F5EB-881M50-B2JJ	5 pins, Balanced 100ohm output
			FAR-F5EB-881M50-B28W	5 pins, Balanced 150ohm output
			FAR-F5EC-881M50-B29W	6 pins, Balanced 150ohm output
		1.4 × 1.0	FAR-F5KA-881M50-D4CH	Unbalanced
			FAR-F5KB-881M50-B4ED	Balanced 100ohm output
			FAR-F5KB-881M50-B4EA	Balanced 150ohm output
EGSM	Transmission	2.0 × 1.6	FAR-F5EA-897M50-D27C	Unbalanced
		1.4 × 1.0	FAR-F5KA-897M50-D4CN	Unbalanced
	Reception	2.0 × 1.6	FAR-F5EA-942M50-D27F	Unbalanced
			FAR-F5EB-942M50-B28E	5 pins, Balanced 150ohm output
			FAR-F5EC-942M50-B29C	6 pins, Balanced 150ohm output
		1.4 × 1.0	FAR-F5KA-942M50-D4CJA	Unbalanced
			FAR-F5KB-942M50-B4EB	Balanced 150ohm output
J-CDMA	Transmission	2.0 × 1.6	FAR-F5EA-906M00-D27E	Unbalanced
		1.4 × 1.0	FAR-F5KA-911M50-D4CC	Unbalanced
	Reception	2.0 × 1.6	FAR-F5EA-851M00-L27P	Unbalanced
			FAR-F5EB-851M00-B28Y	5 pins, Balanced 100ohm output
		1.4 × 1.0	FAR-F5KA-856M50-D4CE	Unbalanced
			FAR-F5KB-856M50-B4EC	Balanced 100ohm output
GPS	-	2.0 × 1.6	FAR-F6EA-1G5754-L2AZ	Unbalanced
			FAR-F6EB-1G5754-B2BS	5 pins, Balanced 100ohm output
		1.4 × 1.0	FAR-F6KA-1G5754-L4AA	Unbalanced
			FAR-F6KB-1G5754-B4GE	Balanced 100ohm output
DCS	Reception	2.0 × 1.6	FAR-F6EA-1G8425-D2ABA	Unbalanced
			FAR-F6EB-1G8425-B2BG	5 pins, Balanced 150ohm output
			FAR-F6EC-1G8425-B2CE	6 pins, Balanced 150ohm output
		1.4 × 1.0	FAR-F6KA-1G8425-D4CK	Unbalanced
			FAR-F6KB-1G8425-B4GA	Balanced 150ohm output
US-PCS, GSM1900	Transmission	2.0 × 1.6	FAR-F6EA-1G8800-L2AN	For Full Band
		1.4 × 1.0	FAR-F6KA-1G8800-L4AF	For Full Band
	Reception	2.0 × 1.6	FAR-F6EA-1G9600-D2AC	Unbalanced
			FAR-F6EB-1G9600-B2BK	5 pins, Balanced 100ohm output
			FAR-F6EB-1G9600-B2BW	5 pins, Balanced 150ohm output
			FAR-F6EC-1G9600-B2CW	6 pins, Balanced 150ohm output
		1.4 × 1.0	FAR-F6KA-1G9600-D4CR	Unbalanced
			FAR-F6KB-1G9600-B4GP	Balanced 100ohm output
			FAR-F6KB-1G9600-B4GB	Balanced 150ohm output
W-CDMA	Transmission	2.0 × 1.6	FAR-F6EA-1G9500-D2AL	Unbalanced
			FAR-F6EB-1G9500-B2BQ	5 pins, Balanced 100ohm output
		1.4 × 1.0	FAR-F6KA-1G9500-D4CD	Unbalanced
			FAR-F6KB-1G9500-B4GJ	Balanced 100ohm output
	Reception	2.0 × 1.6	FAR-F6EA-2G1400-L2HL	Unbalanced
			FAR-F6EB-2G1400-B2BN	5 pins, Balanced 100ohm output
			FAR-F6EB-2G1400-B2BP	5 pins, Balanced 200ohm output
			FAR-F6EC-2G1400-B2CP	6 pins, Balanced 200ohm output
		1.4 × 1.0	FAR-F6KA-2G1400-D4CG	Unbalanced
			FAR-F6KB-2G1400-B4GC	Balanced 100ohm output
			FAR-F6KB-2G1400-B4GD	Balanced 200ohm output

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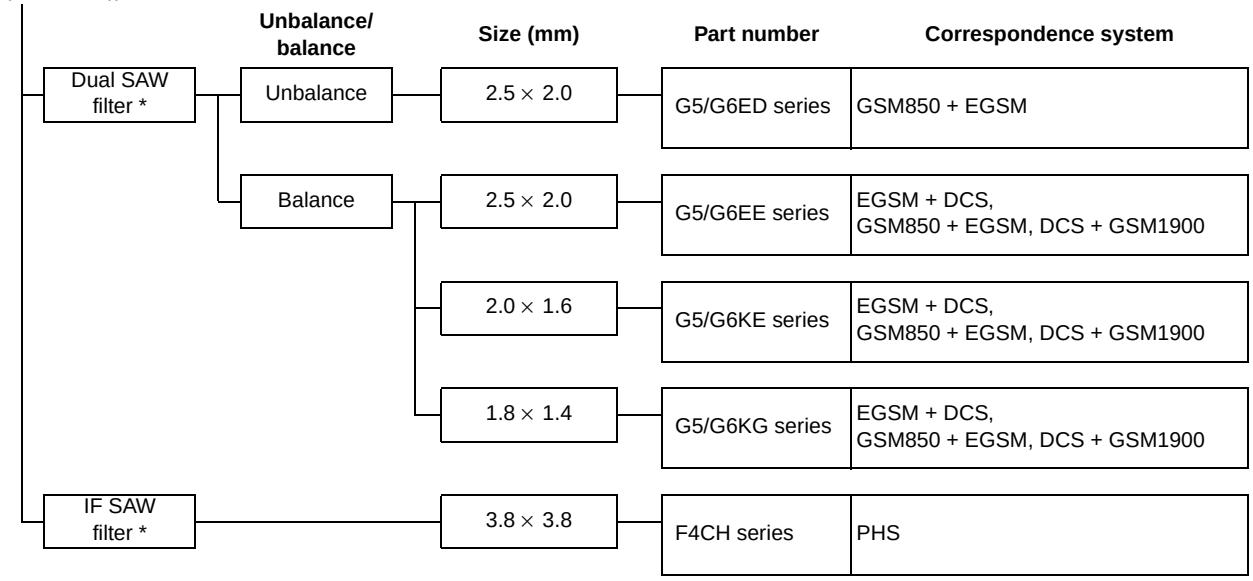

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SAW Dual Filter for Mobile Communication System

Correspondence system	Transmission/ Reception	Size (mm)	Part number	Remarks
EGSM + DCS	Reception	2.5 × 2.0	FAR-G6EE-1G8425-Y2PN	Balanced 150ohm output, Opposite type of Filter position is available.
		2.0 × 1.6	FAR-G6KE-1G8425-Y4QG	Balanced 150ohm output
		1.8 × 1.4	FAR-G6KG-1G8425-Y4SA	Balanced 150ohm output, Opposite type of Filter position is available.
GSM850 + EGSM	Transmission	2.5 × 2.0	FAR-G5ED-897M50-D2DE	Unbalanced
	Reception	2.5 × 2.0	FAR-G5EE-942M50-Y2PB	Balanced 150ohm output, Opposite type of filter position is available.
		2.0 × 1.6	FAR-G5KE-942M50-Y4QA	Balanced 150ohm output, Opposite type of filter position is available.
		1.8 × 1.4	FAR-G5KG-942M50-Y4SD	Balanced 150ohm output, Opposite type of filter position is available.
DCS + GSM1900	Reception	2.5 × 2.0	FAR-G6EE-1G9600-Y2PR	Balanced 150ohm output, Opposite type of filter position is available.
		2.0 × 1.6	FAR-G6KE-1G9600-Y4QB	Balanced 150ohm output, Opposite type of filter position is available.
		1.8 × 1.4	FAR-G6KG-1G9600-Y4SC	Balanced 150ohm output, Opposite type of filter position is available.
W-CDMA 800MHz + 2GHz	Transmission	1.8 × 1.4	FAR-G6KG-1G9500-Y4PF	Balanced 200ohm intput, Opposite type of filter position is available.
	Reception	1.8 × 1.4	FAR-G6KG-2G1400-Y4SE	Balanced 200ohm output, Opposite type of filter position is available.

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IF SAW filter for Mobile Communication System

Correspondence system	Size (mm)	Part number	Remarks
PHS	3.8 × 3.8	FAR-F4CH-243M95-T101D	Low Insertion loss

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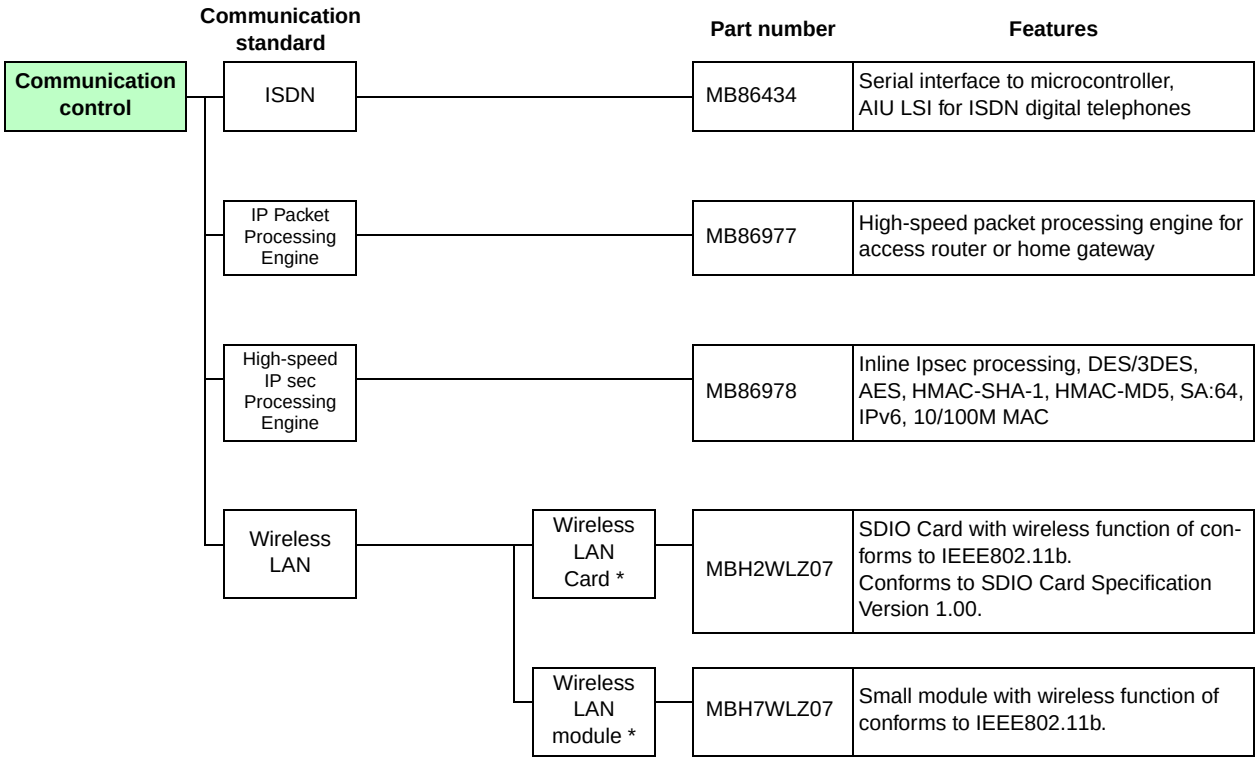
Communication Control/Communication Network



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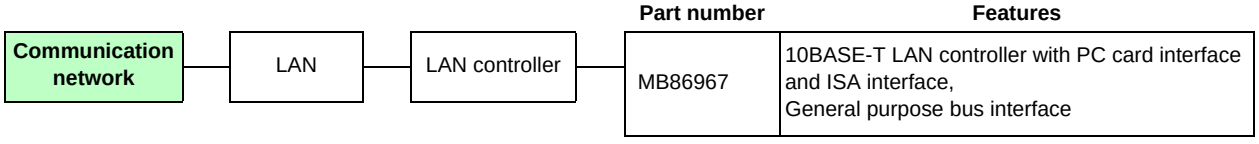


Communication Control

ISDN

Part number	Functions	Communication standard	Power supply voltage (V)	Package
				QFP
MB86434	AIU LSI for ISDN digital telephones, Internal CODEC, DTMF tones, service tone, and ringer tone	—	+5 ±5%	64P

Package: P - Plastic

IP Packet Processing Engine

Part number	Functions	Power supply voltage (V)	Package
			LQFP
MB86977	Enable to process following functions with hardware. IP Packet Forwarding Packet Filtering NAT PPPoE and more. Supports QoS, DMZ, IPv6 and more. 10/100M MAC (Conforms to IEEE802.3)	3.3 ±0.3 1.8 ±0.15	208P

Package: P - Plastic

High Speed IP sec Processing Engine

Part number	Functions	Power supply voltage (V)	Package
			FBGA
MB86978	Inline Ipsec processing, DES / 3DES,AES,HMAC - SHA-1,HMAC-MD5,SA:64,IPv6,10 / 100M MAC	3.3 ±0.3 1.8 ±0.15	337P 288P

Package: P - Plastic

Wireless LAN Card

Part number	Functions	Communication standard	Transfer speed (bps)	Power supply voltage (V)	Package (mm)
MBH2WLZ07	SDIO Card with wireless function of conforms to IEEE802.11b. Supports CF host slot and simultaneous operation of Wireless LAN, a PHS communication card, etc.	IEEE802.11b	11M/5.5M/ 2M/1M *	+3.3 ±5%	24 × 40

*: It is the maximum of a theoretical price increase of a WirelessLAN standard. (Product of FUJITSU MEDIA DEVICES LIMITED)

Wireless LAN Mini PCI module

Part number	Functions	Communication standard	Transfer speed (bps)	Power supply voltage (V)	Package (mm)
MBH7WLZ07	Small module with wireless function of conforms to IEEE802.11b.	IEEE802.11b	11M/5.5M/2M/1M *	+3.3 ±5%	14 × 12

*: It is the maximum of a theoretical price increase of a WirelessLAN standard. (Product of FUJITSU MEDIA DEVICES LIMITED)

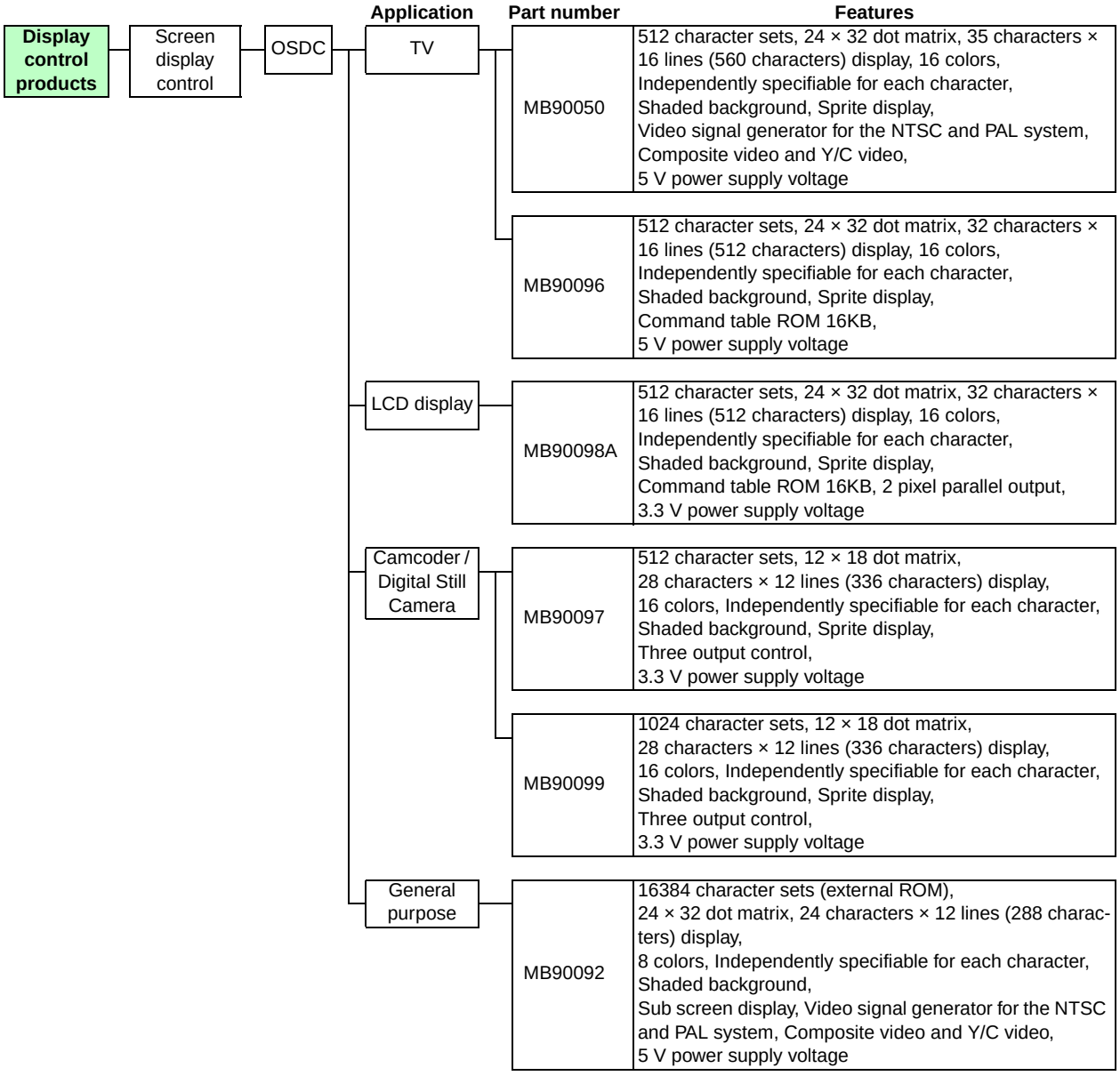
Communication Network

LAN

Part number	Functions	Communication standard	Power supply voltage (V)	Package
				LQFP
MB86967	10BASE-T Ethernet controller with PC card interface, ISA bus interface and General purpose bus interface	Conforms to IEEE 802.3	+5 ±5%	100P

Note: Ethernet is a registered trademark of XEROX Corporation of the USA. Package: P - Plastic

Display Control Products



Display Control Products

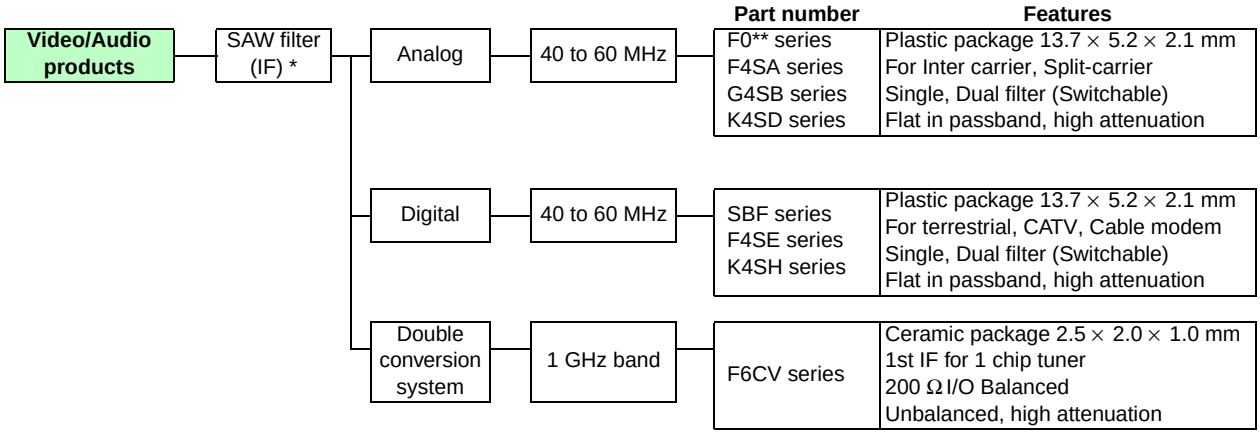
Screen Display Control

OSDC (On-Screen Display Controller)

Part number	Character generator	Number of character set	Character dot structure	Screen size	RGB digital output	Analog (video) output	Sync signal generation	Power supply voltage (V)	Package				
									SH-DIP	SOP	QFP	SSOP	FLGA
MB90050	Internal ROM	512	24 × 32	35 characters × 16 lines	6bit (16 color selection in 64 colors)	Composite Video and Y/C video	NTSC PAL	+5 ±10%	—	—	48P	—	—
MB90096	Internal ROM	512	24 × 32	32 characters × 16 lines	4bit (16 colors)	Unavailable	Unavailable	+5 ±10%	28P	28P	—	—	—
MB90098A	Internal ROM	512	24 × 32	32 characters × 16 lines	4bit (16 colors)	Unavailable	Unavailable	+3.3 ±0.3	—	28P	—	—	—
MB90097	Internal ROM	512	12 × 18	28 characters × 12 lines	4bit (16 colors)	Unavailable	Unavailable	+3.3 ±0.3	—	—	—	20P	—
MB90099	Internal ROM	1024	12 × 18	28 characters × 12 lines	4bit (16 colors)	Unavailable	Unavailable	+2.4 to +3.6	—	—	—	20P	20P
MB90092	External ROM	16384 (Max.)	24 × 32	24 characters × 12 lines	3bit (8 colors)	Composite Video and Y/C video	NTSC PAL	+5 ±10%	—	—	80P	—	—

Package: P - Plastic

Video/Audio Products



Part number	Features
F0** series F4SA series G4SB series K4SD series	Plastic package 13.7 × 5.2 × 2.1 mm For Inter carrier, Split-carrier Single, Dual filter (Switchable) Flat in passband, high attenuation
SBF series F4SE series K4SH series	Plastic package 13.7 × 5.2 × 2.1 mm For terrestrial, CATV, Cable modem Single, Dual filter (Switchable) Flat in passband, high attenuation
F6CV series	Ceramic package 2.5 × 2.0 × 1.0 mm 1st IF for 1 chip tuner 200 Ω I/O Balanced Unbalanced, high attenuation

*: Product of FUJITSU MEDIA DEVICES LIMITED

Video/Audio Products

IF SAW Filter for Analog

Applicable types	System	Video/Audio	Picuture carrier frequency (MHz)	Part number
NTSC Japan	Split-Carrier (single)	Video	58.75	FAR-F4SA-58M750-A008
	Split-Carrier (single)	Audio	58.75	FAR-F4SA-54M250-B011
	Split-Carrier (dual)	Video + Audio	58.75	FAR-G4SB-58M750-D011
NTSC USA	Inter-Carrier (single)	Video	45.75	F072TPL-A
	Split-Carrier (single)	Video	45.75	FAR-F4SA-45M750-A024
	Split-Carrier (single)	Audio	45.75	FAR-F4SA-41M250-B021
	Split-Carrier (dual)	Video + Audio	45.75	FAR-G4SB-45M750-D001
PAL, PAL Multi	Inter-Carrier (single)	Video	38.00	FAR-F4SA-38M000-A009
	Inter-Carrier (single)	Video	38.90	FAR-F4SA-38M900-A041
	Split-Carrier (single)	Video	38.90	FAR-F4SA-38M900-A072
	Split-Carrier (single)	Audio	38.90	FAR-F4SA-40M400-B071
	Split-Carrier (Switchable)	Video + Video	38.00	FAR-K4SD-38M000-F002
	Split-Carrier (Switchable)	Video + Video	38.00	FAR-K4SD-38M000-F011
	Split-Carrier (Switchable)	Audio + Audio	33.90/38.90	FAR-K4SD-40M400-G002

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IF SAW Filter for Digital

Applicable types	Center frequency (MHz)	3 dB Bandwidth (MHz)	Part number
DTV & CATV (QAM)	36.000	8.10	FAR-F4SE-36M000-A005
	36.000	8.20	FAR-F4SE-36M000-A002
	36.125	6.10	FAR-F4SE-36M125-A001
	36.125	7.00	SBF0407BPL
	36.125	8.00	FAR-F4SE-36M125-A004
	43.750	6.00	FAR-F4SE-43M750-A006
	44.000	5.49	FAR-F4SE-44M000-H0A1
	44.000	6.12	FAR-F4SE-44M000-H0A2
	44.000	4.00	FAR-F4SE-44M000-H0A3
	44.000	5.37	FAR-F4SE-44M000-H0A4
	44.000	6.00	FAR-F4SE-44M000-A007
	44.000	6.00	FAR-F4SE-44M000-H0A9
	44.000	6.20	FAR-F4SE-44M000-A008
	44.000	8.00	SBF0408LPL
	36.170	7.0/7.9 (Switchable)	FAR-K4SH-36M170-F003
	57.000	6.00	FAR-F4SE-57M000-H0J1
	57.000	5.60	FAR-F4SE-57M000-H0J3
	44.000	2.60	FAR-F4SE-44M000-H0A6

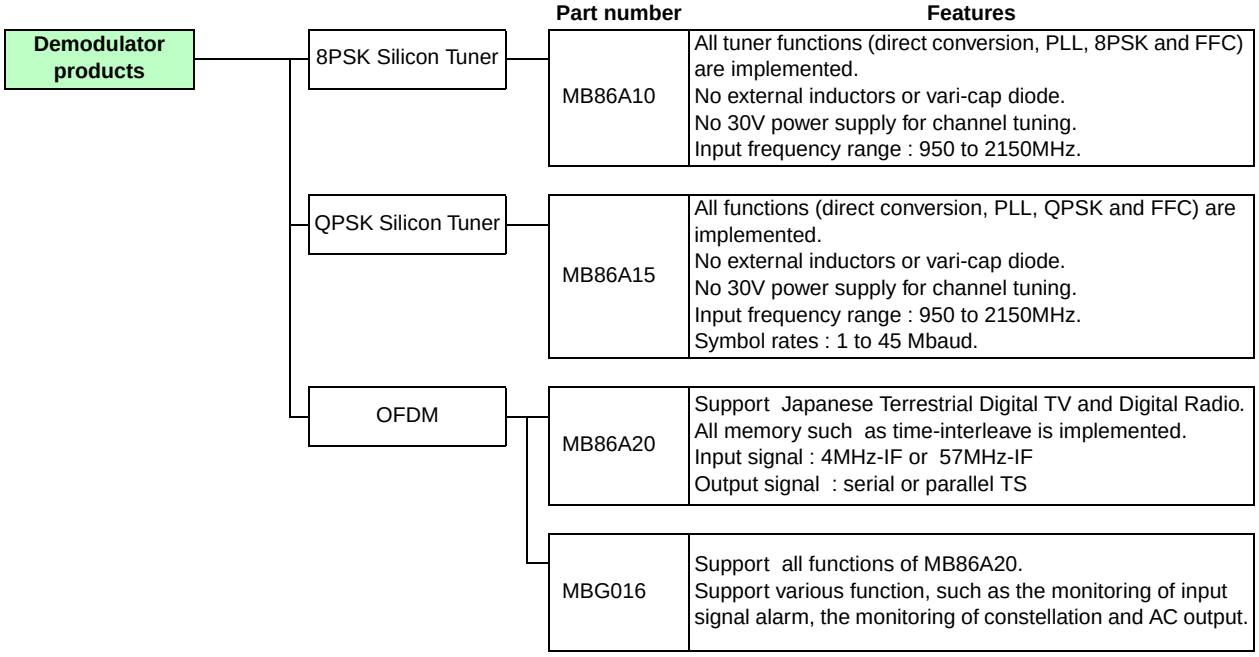
(Product of FUJITSU MEDIA DEVICES LIMITED)

IF SAW Filter for Double Conversion System

Applicable types	Center frequency (MHz)	Bandwidth (MHz)	Part number
1st IF	1086	10	FAR-F6CV-1G0860-C27B
	1220	8	FAR-F6CV-1G2200-C27A

(Product of FUJITSU MEDIA DEVICES LIMITED)

Demodulator products



	Part number	Features
8PSK Silicon Tuner	MB86A10	All tuner functions (direct conversion, PLL, 8PSK and FFC) are implemented. No external inductors or vari-cap diode. No 30V power supply for channel tuning. Input frequency range : 950 to 2150MHz.
QPSK Silicon Tuner	MB86A15	All functions (direct conversion, PLL, QPSK and FFC) are implemented. No external inductors or vari-cap diode. No 30V power supply for channel tuning. Input frequency range : 950 to 2150MHz. Symbol rates : 1 to 45 Mbaud.
OFDM	MB86A20	Support Japanese Terrestrial Digital TV and Digital Radio. All memory such as time-interleave is implemented. Input signal : 4MHz-IF or 57MHz-IF Output signal : serial or parallel TS
	MBG016	Support all functions of MB86A20. Support various function, such as the monitoring of input signal alarm, the monitoring of constellation and AC output.

Demodulator products

8PSK Silicon Tuner

Part number	Function	Power supply voltage (V)	Package
			QFP
MB86A10	RF tuner + 8PSK demodulator Digital BS support	2.3 to 2.7 3.0 to 3.6 4.75 to 5.25	120P

Package: P - Plastic

QPSK Silicon Tuner

Part number	Function	Power supply voltage (V)	Package
			QFP
MB86A15	RF tuner + QPSK demodulator DVB-S and DSS support	2.3 to 2.7 3.0 to 3.6 4.75 to 5.25	120P

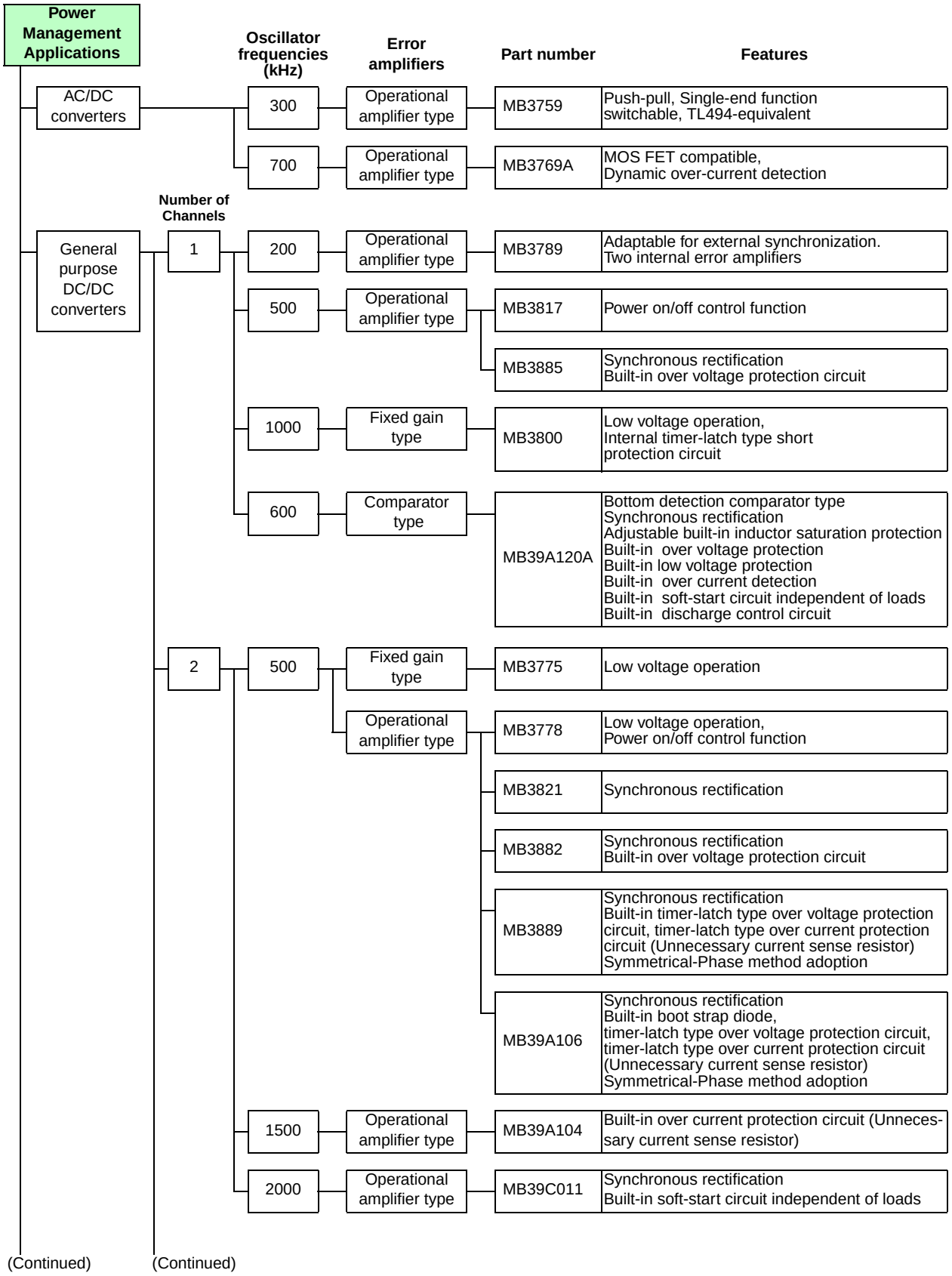
Package: P - Plastic

OFDM

Part number	Function	Power supply voltage (V)	Package	
			FBGA	QFP
MB86A20	OFDM demodulator ISDB-T support	1.4 to 1.6 1.65 to 1.95 3.0 to 3.6	144P	-
MBG016	OFDM demodulator of the high grade type ISDB-T support	1.4 to 1.6 1.65 to 1.95 3.0 to 3.6	-	208P

Package: P - Plastic

Power Management Applications



Power Management Applications

AC/DC Converters

Part number	Function	Power supply voltage (V)	No. of channels	Operating oscillator frequency (kHz) (Max.)	Reference voltage (V) (Typ.)	Reference voltage Precision (%)	Package SOP
MB3759	PWM-type controllers for AC/DC converters	+7 to +32	1	300	5	5.0	16P
MB3769A		+12 to +18		700		2.0	16P

Packages: P - Plastic

General purpose DC/DC Converters

Part number	Function	Power supply voltage (V)	No. of channels	Operating oscillator frequency (kHz) (Max.)	Reference voltage (V) (Typ.)	Reference voltage Precision (%)	Solutions	Package SOP	Package SSOP	Package TSSOP	Package QFN
MB3789	PWM-type controllers for DC/DC converters	+3.0 to +18	1	200	2.5	4.0	Up conversion	–	16P	–	–
MB3817		+2.5 to +18		500	1.5	2.0	Down conversion Up/Down conversion	–	16P	–	–
MB3885		+5.5 to +18			2.5	1.0	Down conversion	–	20P	–	–
MB3800		+1.8 to +15		1000	(0.5)	4.0	Up conversion	8P	8P	16P	–
○MB39A120A	Bottom detection comparator type controlers for DC/DC converters	+4.5 to +25	1	600	2.5	1.5	Down conversion	–	24P	–	24P
MB3775	PWM-type controllers for DC/DC converters	+3.6 to +18	2	500	1.28	1.5	Up conversion Down conversion Invert	16P	16P	–	–
MB3778					2.46	2.0		16P	16P	–	–
MB3821		+4.5 to +30			2.5		Down conversion	–	24P	–	–
MB3882		+5.5 to +18				1.0		–	24P	–	–
MB3889					3.5			–	–	30P	–
MB39A106		+6.5 to +18						–	–	30P	–
MB39A104		+7 to +19		1500	5.0			–	24P	–	–
○MB39C011		+4.5 to +17		2000	1.0			–	–	16P	24P

○ : New product

Packages: P - Plastic

Power Management Applications

(Continued)

(Continued)

	Number of Channels	Oscillator frequencies (kHz)	Error amplifiers	Part number	Features
DC/DC converters with switching FET	3	500	Operational amplifier type	MB3782	High generality
		2600	Operational amplifier type	MB39A112	Supports for control and soft-start of each channel High-precision reference voltage
	1	2000/ 3000	Fixed gain type	MB39C014	Current mode type Built-in LDO mode Low consumption current Synchronous rectification Built-in POWER GOOD function
	2	2000	Fixed gain type	MB39C015	Current mode type Built-in LDO mode Low consumption current Synchronous rectification Built-in voltage detection function

(Continued)

General purpose DC/DC Converters

Part number	Function	Power supply voltage (V)	No. of channels	Operating oscillator frequency (kHz) (Max.)	Reference voltage (V)		Solutions	Package	
					(Typ.)	Precision (%)		SOP	TSSOP
MB3782	PWM-type controllers for DC/DC converters	+3.6 to +18	3	500	2.5	2.0	Up conversion Down conversion Invert	20P	–
MB39A112		+7 to +25		2600	(1.0/ 1.23)	1.0	Down conversion	–	20P

Packages: P - Plastic

DC/DC converters with switching FET

Part number	Function	Power supply voltage (V)	No. of channels	Operating oscillator frequency (kHz) (Max.)	Reference voltage		Output current		Switching FET ON resistance			Solutions	Package			
					(V) (Typ.)	Precision (%)	DC/DC (mA) (Max)	Bypass FET (mA) (Max)	Pch MOS (Ω) (Typ)	Nch MOS (Ω) (Typ)	Bypass FET (Ω) (Typ)		BCC	SSOP	QFN	SON
○MB39C014	PWM type controllers for DC/DC converters	+2.5 to +5.5	1	2000/3000 (Fix)	2.5 (Output voltage)	2.0	800	–	0.3	0.2	–	Down conversion	10P	–	–	10P
○MB39C015			2	2000 (Fix)				–			–		20P	20P	24P	–

○ : New product

Packages: P - Plastic

Power Management Applications

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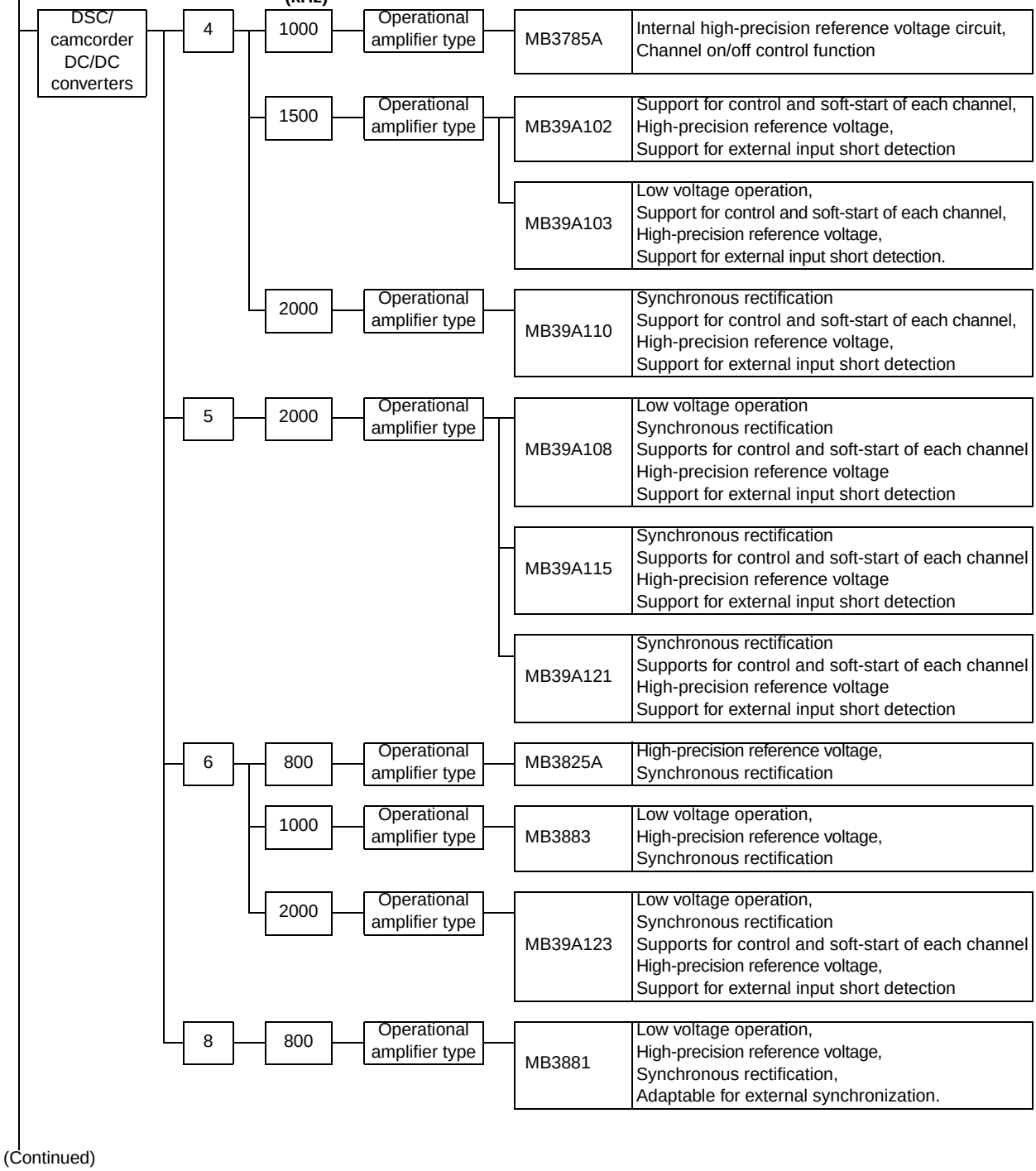

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DSC/Camcorder DC/DC Converters

Part number	Function	Power supply voltage (V)	No. of channels	Operating oscillator frequency (kHz) (Max.)	Reference voltage (V) (Typ.)	Reference voltage Precision (%)	Solutions	Drive circuit	Package LQFP	Package BCC	Package TSSOP
MB3785A	PWM-type controllers for DC/DC converters	+4.5 to +18	4	1000	2.5	1.0	Down conversion	PNP :4	48P	—	—
MB39A102		+2.5 to +11		1500	2.0		Up conversion Down conversion Up/Down conversion	Pch : 3, Nch : 1	—	32P	30P
MB39A103		+1.7 to +11						Pch : 1, Nch : 3	—	32P	30P
MB39A110		+2.5 to +11		2000				Pch : 3, Nch : 1	—	—	38P
MB39A108		+1.7 to +11	5					Pch : 3, Nch : 2	—	40P	38P
MB39A115								Pch : 4, Nch : 1	—	40P	38P
MB39A121		+2.5 to +11						Pch : 4, Nch : 1	48P	40P	—
MB3825A		+2.5 to +12	6	800	1.5		Down conversion	PNP : 6	64P**	—	—
MB3883		+1.7 to +9		1000	2.5		Up conversion Down conversion Up/Down conversion	Pch : 2, Nch : 4	48P	48P	—
MB39A123		+1.7 to +11		2000	2.0		Up conversion Down conversion Up/Down conversion Invert	Pch : 4, Nch : 2	48P	48P	—
MB3881		+1.8 to +13	8	800	2.5		Down conversion Up/Down conversion	Pch : 7, Nch : 1	64P*	—	—

* : 0.4 mm pitch
** : 0.4 mm pitch, 0.5 mm pitch

Packages: P - Plastic

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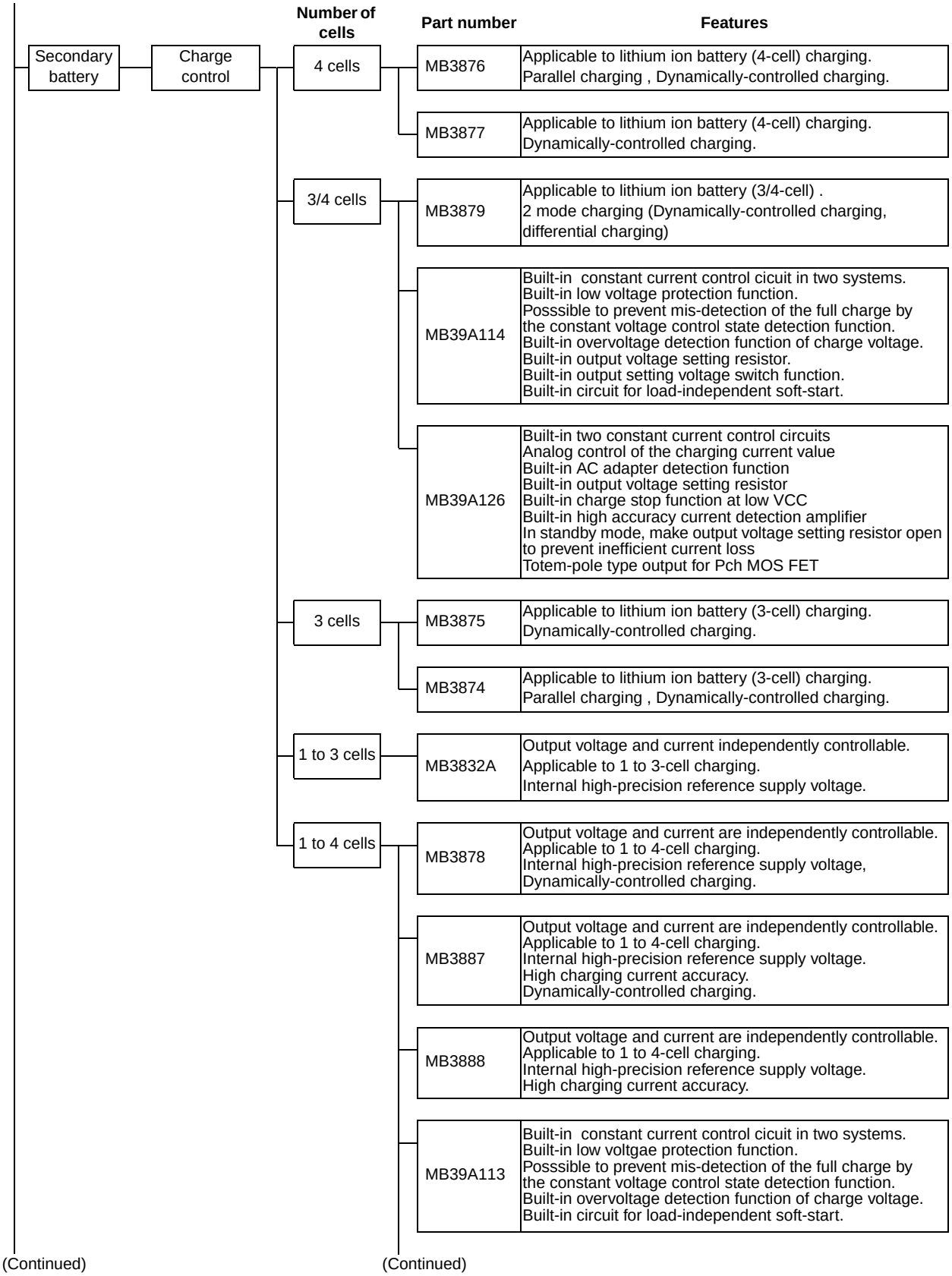

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Secondary Battery (Charge Control)

Part number	Function	Power supply voltage (V)	Output voltage (V)	Precision (%)		Number of cells	Operating oscillator frequency (kHz) (Max.)	Solutions	Package		
				Ta = +25 °C	Ta = -30 to +85 °C				SSOP	LQFP	QFN
MB3876	Charge control DC/DC converters	+7 to +25	16.8	±0.8	±1.0	4	500	Down conversion	24P	–	–
MB3877									24P	–	–
MB3879		+8 to +25	12.6/16.8	±0.8	±1.0	3/4			—	48P	—
			12.3/16.4	±0.9	±1.1						
MB39A114			12.6/16.8	±0.5	±0.74 *				24P	–	–
MB39A126									24P	–	28P
MB3875		+7 to +25	12.6	±0.8	±1.0	3			24P	–	–
MB3874									24P	–	–
MB3832A		+3.6 to +18	Any voltage level	±0.5	±1.0*	1 to 3			20P	–	–
MB3878		+7 to +25	4.2 V/cell	±0.8	±1.0	1 to 4			24P	–	–
MB3887		+8 to +25		±0.5	±0.74 *				24P	–	–
MB3888			Any voltage level						20P	–	–
MB39A113		+8 to +25	4.2 V/cell						24P	–	–

* : Ta = -10 to +85 °C

Package: P-plastic

Power Management Applications

(Continued)

(Continued)

	Part number	Features
Supply voltage monitoring applications	MB39A118	Built-in off time control function Built-in constant current control circuit in two systems Possible to control of the constant current by analog value Built-in for Nch MOS FET synchronous rectification type output stage Built-in battery select function Possible to set any output voltage by external resistor In IC standby mode, leave output voltage setting resistor open to prevent inefficient current loss
	MB39A119	Built-in off time control function Built-in voltage detection function of AC adapter Possible to prevent mis-detection of the full charge by the constant voltage control state detection function Built-in constant current control circuit in two systems Possible to control of the constant current by analog value Built-in for Nch MOS FET synchronous rectification type output stage Built-in charge stop function at low VCC Possible to set any output voltage by external resistor In IC standby mode, leave output voltage setting resistor open to prevent inefficient current loss
	MB39A125	Built-in two constant current control circuits Analog control of the charging current value Built-in AC adapter detection function External output voltage setting resistor Built-in charge stop function at low VCC Built-in high accuracy current detection amplifier In standby mode, make output voltage setting resistor open to prevent inefficient current loss Totem-pole type output for Pch MOS FET
Voltage detectors	MB3761	Wide operating voltage range, Easy addition of hysteresis characteristics
Supply voltage monitoring applications — Watchdog timer	MB3771	Accurate supply voltage drop detection, External add-on allows detection of any desired voltage drop
Single system	MB3773	Watchdog timer Accurate supply voltage drop detection
Double systems	MB3793-27A MB3793-28A MB3793-30A MB3793-34A MB3793-37A MB3793-42 MB3793-45	Watchdog timer Accurate supply voltage drop detection
Power management switches	MB3841	Low on-resistance switch
	MB3842 MB3845	Low on-resistance switch

Secondary Battery (Charge Control)

Part number	Function	Power supply voltage (V)	Output voltage (V)	Precision (%)		Number of cells	Operating oscillator frequency (kHz) (Max.)	Solutions	Package	
				Ta = +25 °C	Ta = -30 to +85 °C				SSOP	QFN
MB39A118	Charge control DC/DC converters	+8 to +25	4.2 V/cell	±0.5	±0.74 *	1 to 4	1000	Down conversion	–	28P
MB39A119									–	28P
MB39A125							500		24P	28P

* : Ta = -10 to +85 °C

Package: P-plastic

Voltage Detectors

Part number	Function	Power supply voltage (V)	Reference voltage (V) (Typ.)	Package
				SOP
MB3761	Voltage detector	+2.5 to +40	1.2	8P

Package: P - Plastic

Supply Voltage Monitoring Applications

Part number	Function	Power supply voltage (V)	Detection voltage (V)	Reset certified voltage (V) (Typ.)	Package	
					SOP	SSOP
MB3771	Supply voltage monitoring applications	+3.5 to +18	Any voltage level in addition to 4.2 V	0.8	8P	–
MB3773	Supply voltage monitoring applications with watchdog timer	+3.5 to +16			8P	–
MB3793-27A *1	Supply voltage monitoring applications with dual watchdog timer systems	+4 (Max.)	2.7±0.07		8P	8P
MB3793-28A *1			2.8±0.07		8P	8P
MB3793-30A *1		+6 (Max.)	3.0±0.07		8P	8P
MB3793-34A *1			3.4±0.08		8P	(8P)*2
MB3793-37A *1			3.7±0.1		8P	(8P)*2
MB3793-42 *1			4.2±0.1		8P	(8P)*2
MB3793-45 *1			4.5±0.1		8P	8P

*1:Detection voltages of the MB3793 series are available in the range from 2.4 V to 4.9 V in 0.1 V increments. Consult with supplier.

Package: P - Plastic

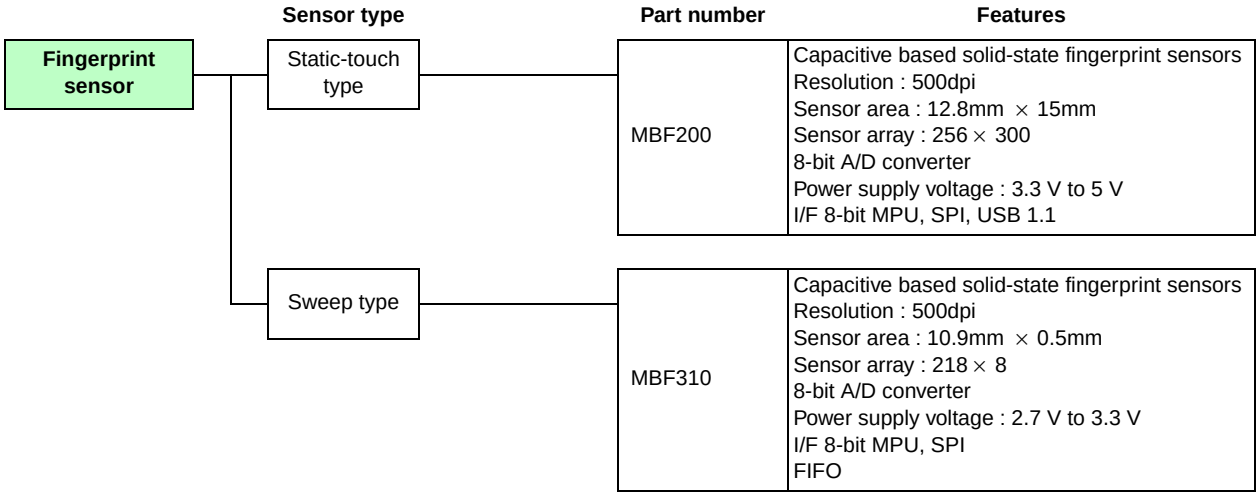
*2:( ) option

Switching Applications

Part number	Function	Power supply voltage (V) (Max.)	Number of channels	On-resistance (Ω)	Drive current (A) (Max.)	Package	
						SOP	SSOP
MB3841	Power management switch	5.5	1	0.045	2.0	8P	–
MB3842			2	0.1	0.6	–	20P
MB3845							

Package: P - Plastic

Fingerprint sensor

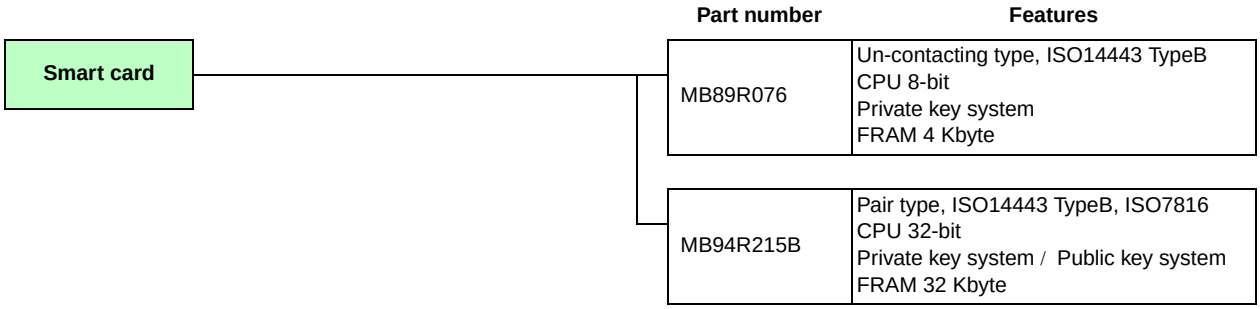


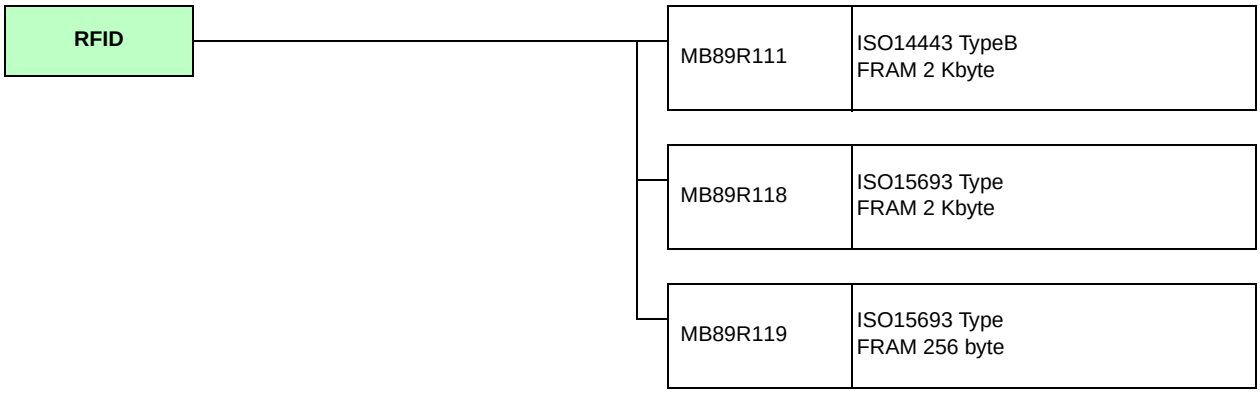
Fingerprint sensor

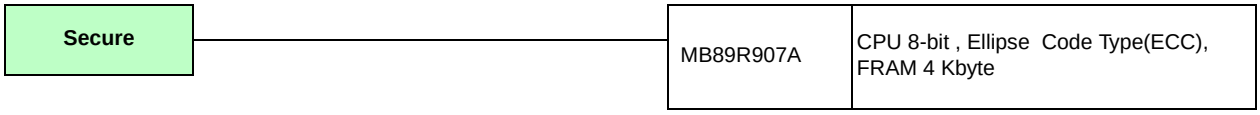
Part number	Resolution (dpi)	Sensor area (mm)	Sensor array (pixel)	Power supply voltage (V)	Interface	Others	Package	
							TSOP	FBGA
MBF200	500	12.8 × 15.0	256 × 300	3.3 to 5.0	8bit MPU SPI USB 1.1	-	80P	-
MBF310		10.9 × 0.5	218 × 8	2.7 to 3.3	8bit MPU SPI	FIFO	-	43P

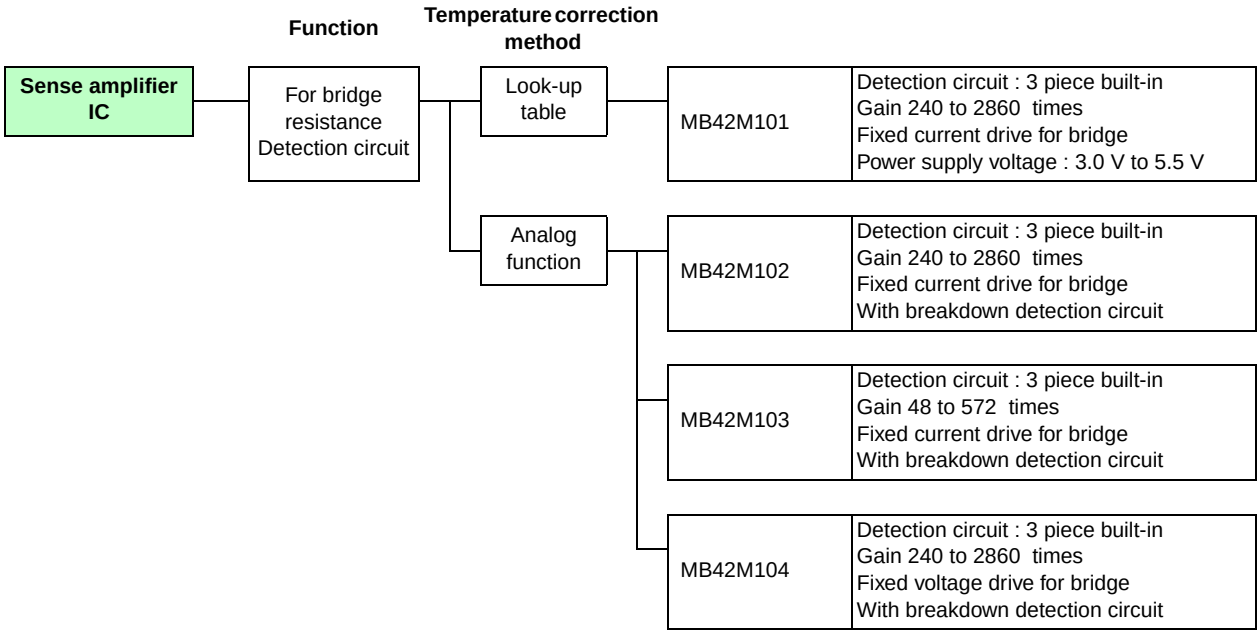
Package: P - Plastic

Smart card/RFID/Secure/Sense amplifier IC









Smart card/RFID/Secure/Sense amplifier IC

Smart card

Part number	Interface	CPU (bit)	FRAM (byte)	ROM (byte)	SRAM (byte)	Code Type	Shipment form
MB89R076	ISO14443 TypeB	8	4K	32K	512	DES	An exclusive package
MB94R215B	ISO14443 TypeB, ISO7816	32	32K	128K	8K	DES/RSA	An exclusive package

RFID

Part number	Interface	Transmission speed	FRAM (byte)	Shipment form
MB89R111	ISO14443 TypeB	106 Kbps, 212 Kbps	2K	Wafer
MB89R118	ISO15693	26.48 Kbps (52.97 Kbps)	2K	Wafer (With a golden Bump)
MB89R119	ISO15693	26.48 Kbps (52.97 Kbps)	256	Wafer (With a golden Bump)

Secure

Part number	CPU (bit)	FRAM (byte)	ROM (byte)	SRAM (byte)	Code Type	Power supply voltage (V)	Package
							QFP
MB89R907A	8	4K	32K	1K	Ellipse Code Type (ECC)	+5 ±5%	48P

Package: P - Plastic

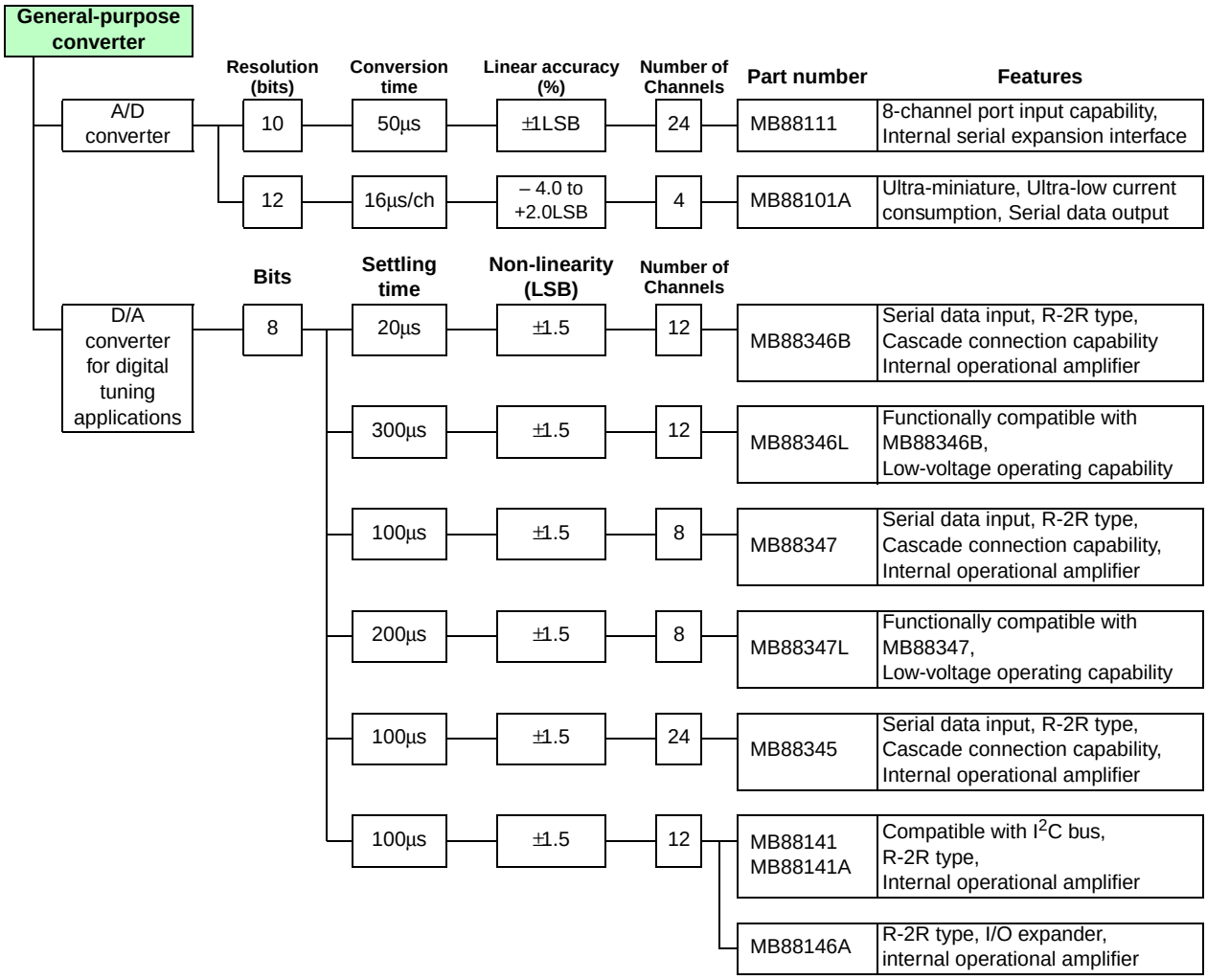
Sense amplifier IC

Part number	Function	Temperature correction method	Number of detection circuits	Gain (times)	Power supply voltage (V)	Others	Package
							BCC
MB42M101	For bridge resistance Detection circuit	Look-up table	3	240 to 2860	3.0 to 5.5	Digital compensation Fixed current drive Built-in memory 1280 bits	32P
◎MB42M102	For bridge resistance Detection circuit	Analog function	3	240 to 2860	4.5 to 5.5	Digital compensation Fixed current drive Built-in memory 1280 bits Breakdown detection circuit	40P
◎MB42M103	For bridge resistance Detection circuit	Analog function	3	48 to 572	4.5 to 5.5	Digital compensation Fixed current drive Built-in memory 1280 bits Breakdown detection circuit	40P
◎MB42M104	For bridge resistance Detection circuit	Analog function	3	240 to 2860	4.5 to 5.5	Digital compensation Fixed voltage drive Built-in memory 1280 bits Breakdown detection circuit	40P

◎: Now planning

Package: P - Plastic

General-Purpose Converter



General-Purpose Converter

A/D Converter

Part number	Function	Conversion method	Conversion time (µs/ch) (Max.)	Linearity error (%) (Max.)	Power supply voltage (V)	Package				
						DIP	SOP	SSOP	QFP	SH-DIP
MB88111	24-ch 10-bit A/D converter	Successive approximation	50	±1 LSB	+3.5 to +5.5	–	–	–	44P	48P
MB88101A	4-ch 12-bit A/D converter		16 (at 5 V±10%)	-4.0 to +2.0 LSB	+3.3 to +5.5	16P	16P	16P	–	–

Packages: P - Plastic

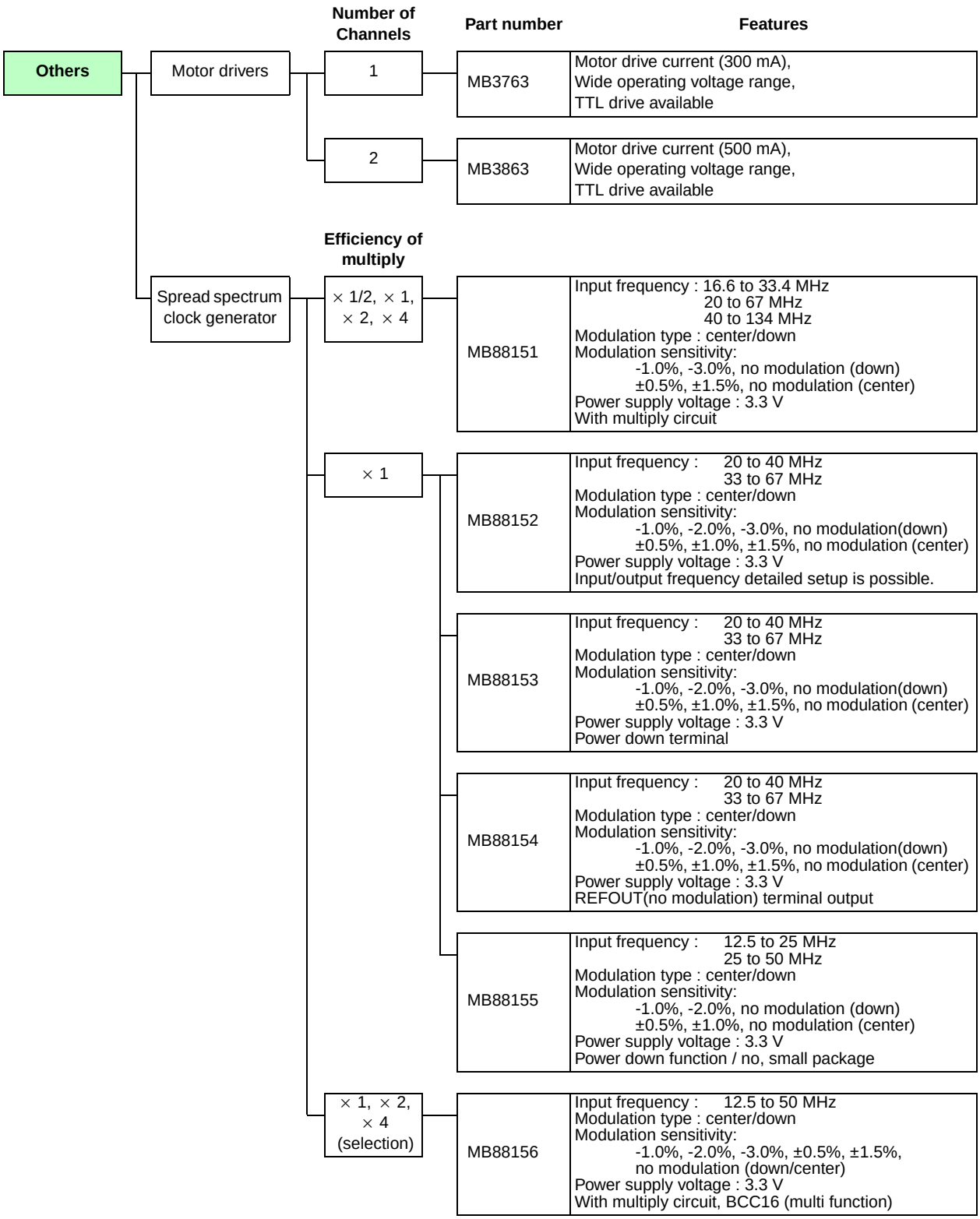
D/A Converter for Digital Tuning Applications

Part number	Function	Settling time (µs) (Max.)	Power consumption (mW) (Typ.)	Non-linearity error (LSB)	Power supply voltage (V)	Package			
						DIP	SOP	SSOP	QFP
MB88346B	12-ch 8-bit D/A converter (internal operational amplifier)	20	14	±1.5	+5±10%	20P	20P	20P	–
MB88346L	12-ch 8-bit D/A converter (internal operational amplifier, low voltage operation)	300	5		+2.7 to +3.6	20P	20P	20P	–
MB88347	8-ch 8-bit D/A converter (internal operational amplifier)	100	9		+5±10%	16P	16P	16P	–
MB88347L	8-ch 8-bit D/A converter (internal operational amplifier, low voltage operation)	200	4.2		+2.7 to +3.6	16P	16P	16P	–
MB88345	24-ch 8-bit D/A converter (internal operational amplifier)	100	27		+5±10%	–	–	–	32P
MB88141 *	12-ch 8-bit D/A converter (compatible with I²C bus, internal operational amplifier)	100	15			24P	24P	24P	–
MB88141A *									–
MB88146A	12-ch 8-bit D/A converter (I/O expander, internal operational amplifier)		14.5		Digital:+2.7 to +5.5 Analog:+5±10%	24P	–	24P	–

Package: P - Plastic

* “Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.”

Others


Number of Channels
Part number
Features
Others
Motor drivers
1
MB3763
Motor drive current (300 mA),
Wide operating voltage range,
TTL drive available
2
MB3863
Motor drive current (500 mA),
Wide operating voltage range,
TTL drive available
Efficiency of multiply
Spread spectrum clock generator
× 1/2, × 1, × 2, × 4
MB88151
Input frequency : 16.6 to 33.4 MHz
20 to 67 MHz
40 to 134 MHz
Modulation type : center/down
Modulation sensitivity:
-1.0%, -3.0%, no modulation (down)
±0.5%, ±1.5%, no modulation (center)
Power supply voltage : 3.3 V
With multiply circuit
× 1
MB88152
Input frequency : 20 to 40 MHz
33 to 67 MHz
Modulation type : center/down
Modulation sensitivity:
-1.0%, -2.0%, -3.0%, no modulation(down)
±0.5%, ±1.0%, ±1.5%, no modulation (center)
Power supply voltage : 3.3 V
Input/output frequency detailed setup is possible.
MB88153
Input frequency : 20 to 40 MHz
33 to 67 MHz
Modulation type : center/down
Modulation sensitivity:
-1.0%, -2.0%, -3.0%, no modulation(down)
±0.5%, ±1.0%, ±1.5%, no modulation (center)
Power supply voltage : 3.3 V
Power down terminal
MB88154
Input frequency : 20 to 40 MHz
33 to 67 MHz
Modulation type : center/down
Modulation sensitivity:
-1.0%, -2.0%, -3.0%, no modulation(down)
±0.5%, ±1.0%, ±1.5%, no modulation (center)
Power supply voltage : 3.3 V
REFOUT(no modulation) terminal output
MB88155
Input frequency : 12.5 to 25 MHz
25 to 50 MHz
Modulation type : center/down
Modulation sensitivity:
-1.0%, -2.0%, no modulation (down)
±0.5%, ±1.0%, no modulation (center)
Power supply voltage : 3.3 V
Power down function / no, small package
× 1, × 2, × 4 (selection)
MB88156
Input frequency : 12.5 to 50 MHz
Modulation type : center/down
Modulation sensitivity:
-1.0%, -2.0%, -3.0%, ±0.5%, ±1.5%,
no modulation (down/center)
Power supply voltage : 3.3 V
With multiply circuit, BCC16 (multi function)

Others

Motor Drivers

Part number	Function	Number of Channels	Output current (mA)	Power supply voltage (V)	Package
					SOP
MB3763	Reversible motor drivers	1	300	+4 to +18	8P
MB3863		2	500	+4 to +36	20P

Package: P - Plastic

Spread spectrum clock generator (SSCG)

Part number	Function	Input frequency (MHz)	Efficiency of multiply	Output frequency (MHz)	Modulation Type	Modulation sensitivity	Other	Package		
								SOP	TSSOP	BCC
MB88151-100	EMI noise reduction PLL (SSCG)	16.6 to 33.4	× 1	16.6 to 33.4	Down or center (selectable)	-1.0%, -3.0% (down) ±0.5%, ±1.5% (center) no modulation	-	8P	-	-
MB88151-200			× 2	33.3 to 66.7						
MB88151-400			× 4	66.6 to 133.4						
MB88151-500			× 1/2	8.3 to 16.7						
MB88152-100		20 to 40 33 to 67 40 to 80 66 to 134	× 1	20 to 40 33 to 67 40 to 80 66 to 134	Down	-1.0%, -3.0%	-	8P	-	-
MB88152-110					Center	±0.5%, ±1.5%				
MB88152-101		20 to 40 33 to 67		20 to 40 33 to 67	Down	-1.0%, -3.0% no modulation				
MB88152-111					Center	±0.5%, ±1.5% no modulation				
MB88152-102		40 to 80 66 to 134		40 to 80 66 to 134	Down	-1.0%, -3.0% no modulation				
MB88152-112					Center	±0.5%, ±1.5% no modulation				
MB88153-100		20 to 40 66 to 134 33 to 67 40 to 80	× 1	20 to 40 66 to 134 33 to 67 40 to 80	Down	-1.0%, no modulation	PD function enable	8P	-	-
MB88153-101						-3.0%, no modulation				
MB88153-110					Center	±0.5%, no modulation				
MB88153-111						±1.5%, no modulation				
MB88154-102		33 to 67	× 1	33 to 67	Down	-1.0%, -2.0%, 3.0%, no modulation	REF output enable	8P	-	-
MB88154-103		20 to 40		20 to 40						
MB88154-112		33 to 67		33 to 67	Center	±0.5%, ±1.0%, ±1.5%, no modulation				
MB88154-113		20 to 40		20 to 40						
MB88155-100		12.5 to 25	× 1	12.5 to 25	Down	-1.0%, -2.0% no modulation	PD function disable	-	8P	-
MB88155-101		25 to 50		25 to 50						
MB88155-102		12.5 to 25		12.5 to 25		-1.0%, -2.0%	PD function enable			
MB88155-103		25 to 50		25 to 50						
MB88155-110		12.5 to 25		12.5 to 25	Center	±0.5%, ±1.0% no modulation	PD function disable			
MB88155-111		25 to 50		25 to 50						
MB88155-112		12.5 to 25		12.5 to 25		±0.5%, ±1.0%	PD function enable			
MB88155-113		25 to 50		25 to 50						
MB88155-400		12.5 to 20	× 4	50 to 80	Down	-1.0%, -2.0% no modulation	PD function disable			
MB88155-402						-1.0%, -2.0%	PD function enable			
MB88155-410					Center	±0.5%, ±1.0% no modulation	PD function disable			
MB88155-412						±0.5%, ±1.0%	PD function enable			
MB88156-000		12.5 to 50 (× 1) 12.5 to 25 (× 2) 12.5 to 20 (× 4)	× 1, × 2, × 4 (selectable)	12.5 to 50 (× 1) 25 to 50 (× 2) 50 to 80 (× 4)	Down/ Center (selectable)	-1.0%, -2.0%, ±0.5%, ±1.0%, no modulation	REF output enable	-	-	16P
MB88156-001							REF output disable			

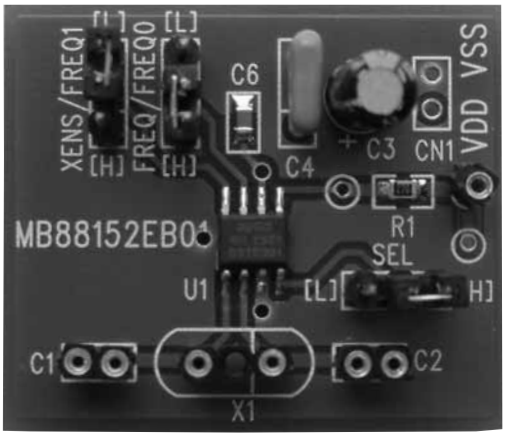
Package: P - Plastic

Others

SSGC Simple Evaluation Board

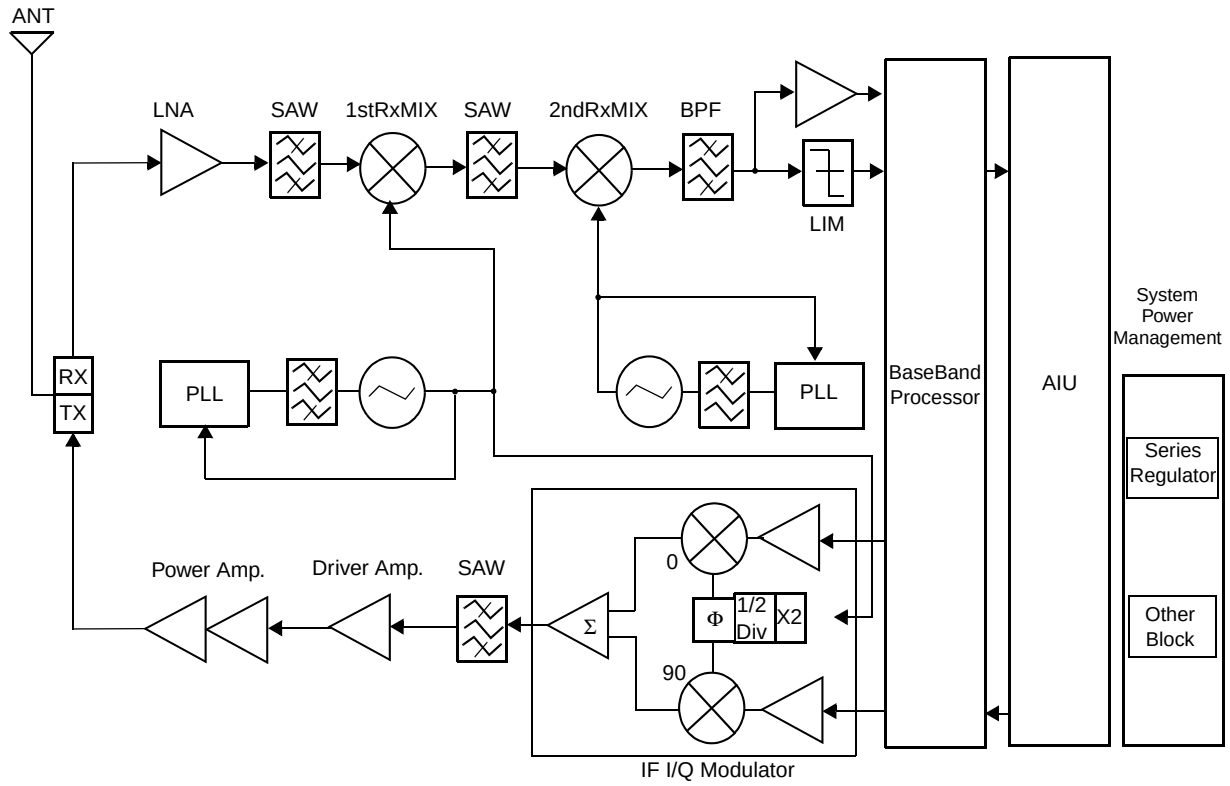
Part number		Remarks	
MB88151	MB88151EB01-100	MB88151-100 mounted	An oscillation vibrator, oscillation stable capacity, and a power supply line are required.
	MB88151EB01-200	MB88151-200 mounted	
	MB88151EB01-400	MB88151-400 mounted	
	MB88151EB01-500	MB88151-500 mounted	
MB88152	MB88152EB01-100	MB88152-100 mounted	
	MB88152EB01-110	MB88152-110 mounted	
	MB88152EB01-101	MB88152-101 mounted	
	MB88152EB01-111	MB88152-111 mounted	
	MB88152EB01-102	MB88152-102 mounted	
	MB88152EB01-112	MB88152-112 mounted	
MB88153	MB88153EB01-100	MB88153-100 mounted	
	MB88153EB01-101	MB88153-101 mounted	
	MB88153EB01-110	MB88153-110 mounted	
	MB88153EB01-111	MB88153-111 mounted	
MB88154	MB88154EB01-102	MB88154-102 mounted	
	MB88154EB01-103	MB88154-103 mounted	
	MB88154EB01-112	MB88154-112 mounted	
	MB88154EB01-113	MB88154-113 mounted	
MB88155	MB88155EB01-100	MB88155-100 mounted	
	MB88155EB01-101	MB88155-101 mounted	
	MB88155EB01-102	MB88155-102 mounted	
	MB88155EB01-103	MB88155-103 mounted	
	MB88155EB01-110	MB88155-110 mounted	
	MB88155EB01-111	MB88155-111 mounted	
	MB88155EB01-112	MB88155-112 mounted	
	MB88155EB01-113	MB88155-113 mounted	
	MB88155EB01-400	MB88155-400 mounted	
	MB88155EB01-402	MB88155-402 mounted	
	MB88155EB01-410	MB88155-410 mounted	
	MB88155EB01-412	MB88155-412 mounted	
MB88156	MB88156EB01-BC16-000	MB88156-000 mounted	
	MB88156EB01-BC16-001	MB88156-001 mounted	

Overview (MB88152EB01-101 : 30 mm × 35 mm)



Communication Equipment (Telephones)

System Configuration of a Digital Cellular Phone

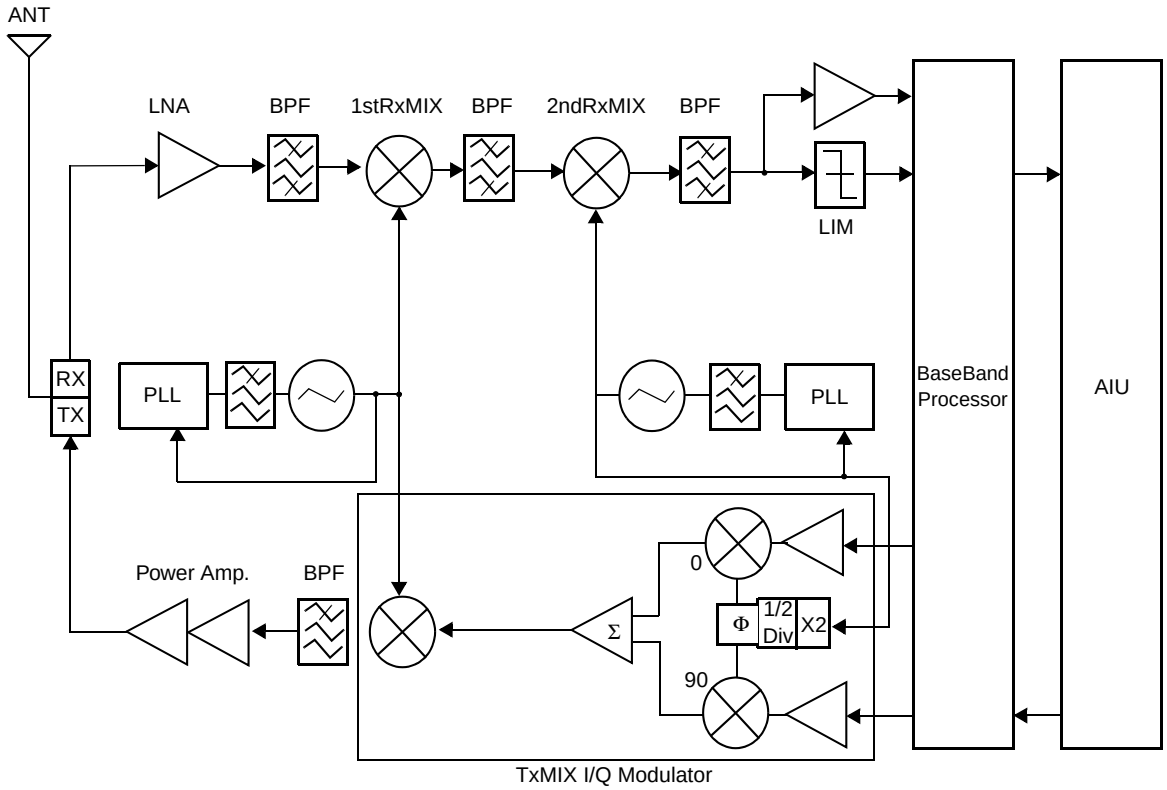


Recommended Semiconductor Products [Digital Cellular]

Part number	Functions
MB15F72UL	PLL frequency synthesizer with an internal prescaler
MB15F73UL	
MB15F78UL	
MB15C100	IF PLL frequency synthesizer semicustom LSI
MB86437	Audio interface unit (AIU)

System Configuration

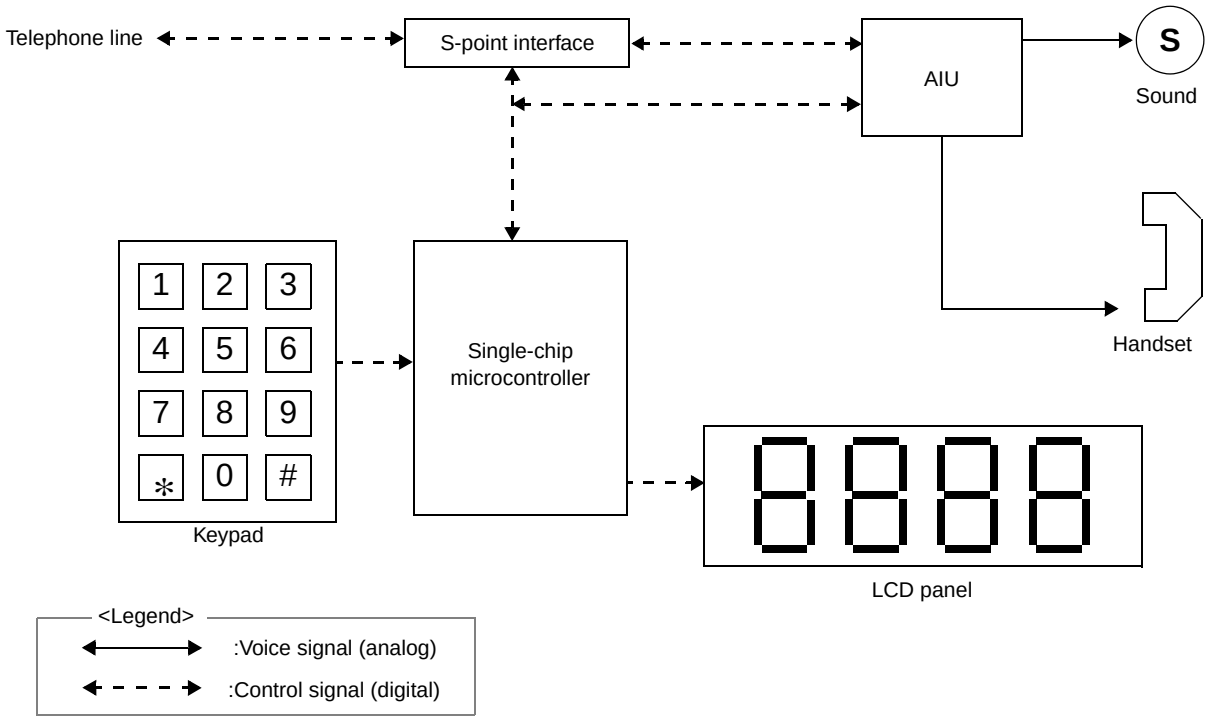
System Configuration of a Digital Cordless Phone



Recommended Semiconductor Products [Digital Cordless]

Part number	Functions
MB15E05SL	PLL frequency synthesizer with an internal prescaler
MB15F73UL	
MB15C100	IF PLL frequency synthesizer semicustom LSI
MB15C101	IF PLL frequency synthesizer

System Configuration of an ISDN Digital Telephone



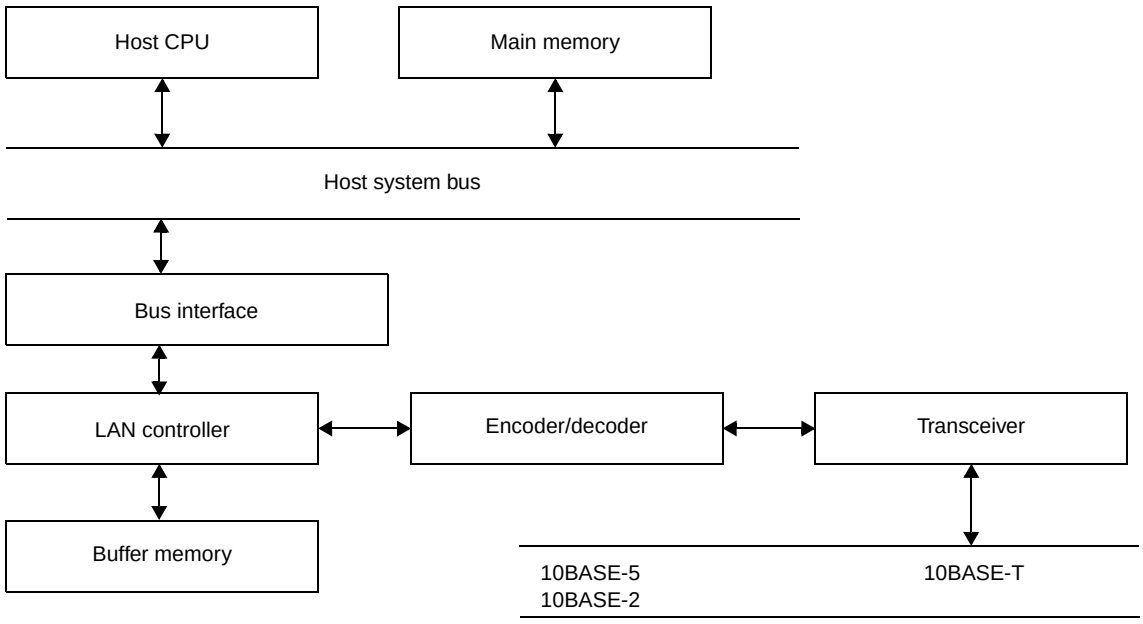
Recommended Semiconductor Products [ISDN Digital Telephone]

Part number	Functions
MB86434	Audio interface unit (AIU)

Communication Control and Communication Networks

LAN (Local Area Network)

Ethernet System Configuration

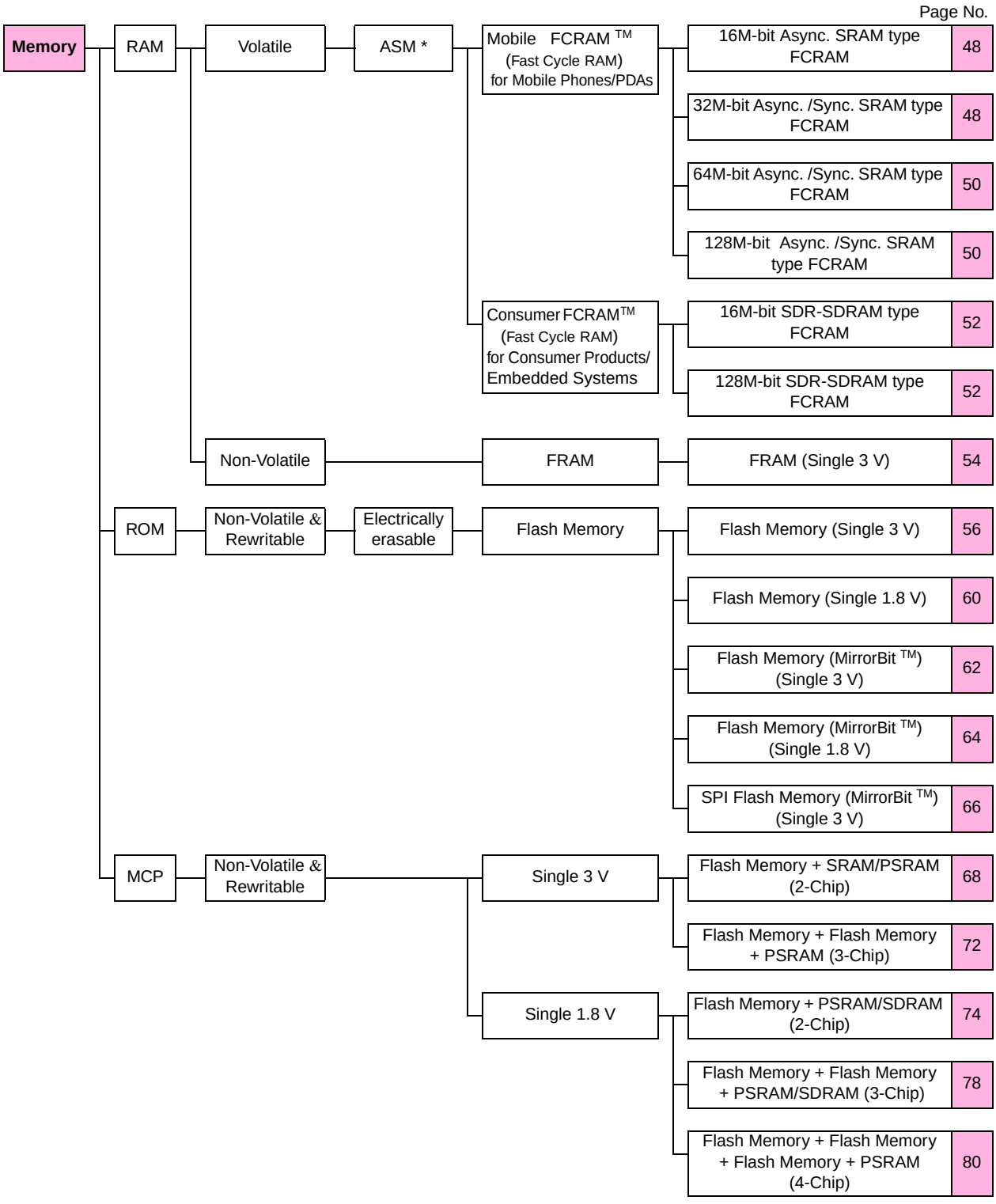


Recommended Semiconductor Products [Ethernet]

Part number	Functions
MB86967	LAN controller, encoder/decoder, transceiver, PCMCIA interface, general-purpose interface

Note: Ethernet is a registered trademark of XEROX Corporation of the USA.

Memory Product Line-up

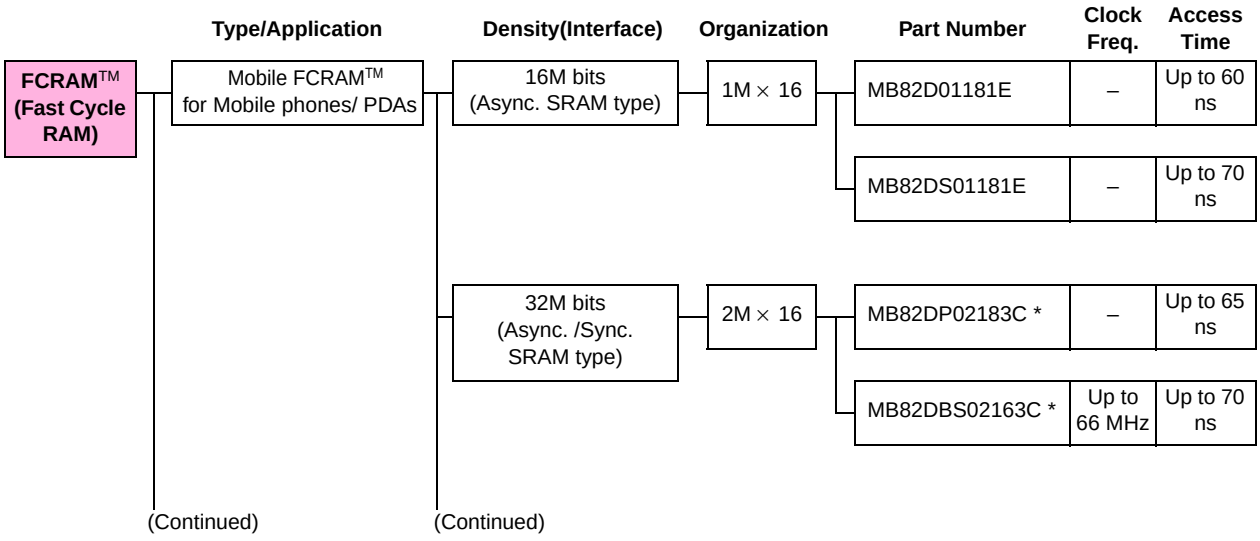


* : ASM =Application Specific Memory

FCRAM is a trademark of Fujitsu Limited.

MirrorBit is a trademark of Spansion LLC.

FCRAM™ (Fast Cycle RAM) (1)



* : Compliance with "COSMORAM (Common Specifications for Mobile RAM) "
COSMORAM is common specifications for pseudo SRAM agreed among Toshiba Corporation Semiconductor Company, NEC Electronics Corporation, and FUJITSU LIMITED.

FCRAM is a trademark of Fujitsu Limited.

Mobile FCRAM™ (Fast Cycle RAM)

- 16M-bit Async. SRAM Type FCRAM

T_A = −30° C to +85° C

Organization (W × b)	Part Number *1	Access Time Max. (ns)	Supply Current Max.			Supply Voltage (V)	Package
			Operating (mA)	Standby (µA)	Power Down (µA)		FBGA
1M × 16	MB82D01181E-60L	60	20	100	10	2.3 to 3.5	48P, *2, *3
	MB82DS01181E-70L	70	20	100	10	1.7 to 1.95	-,*4

*1: Package suffix is not included.
*2: SRAM compatible pin out FBGA (Fine Pitch Ball Grid Array) (Suffix PBN) .
*3: Stacked MCP (Multi Chip Package) parts, in which an Async. SRAM type FCRAM part is packaged with a flash memory part, is also available for mobile phone applications. Chip/wafer (Suffix KTD/WFKT) supply is optional.
*4: Monolithic package option is T.B.D. Chip/wafer (Suffix KTD/WFKT) supply is optional.

- 32M-bit Async. /Sync. SRAM Type FCRAM

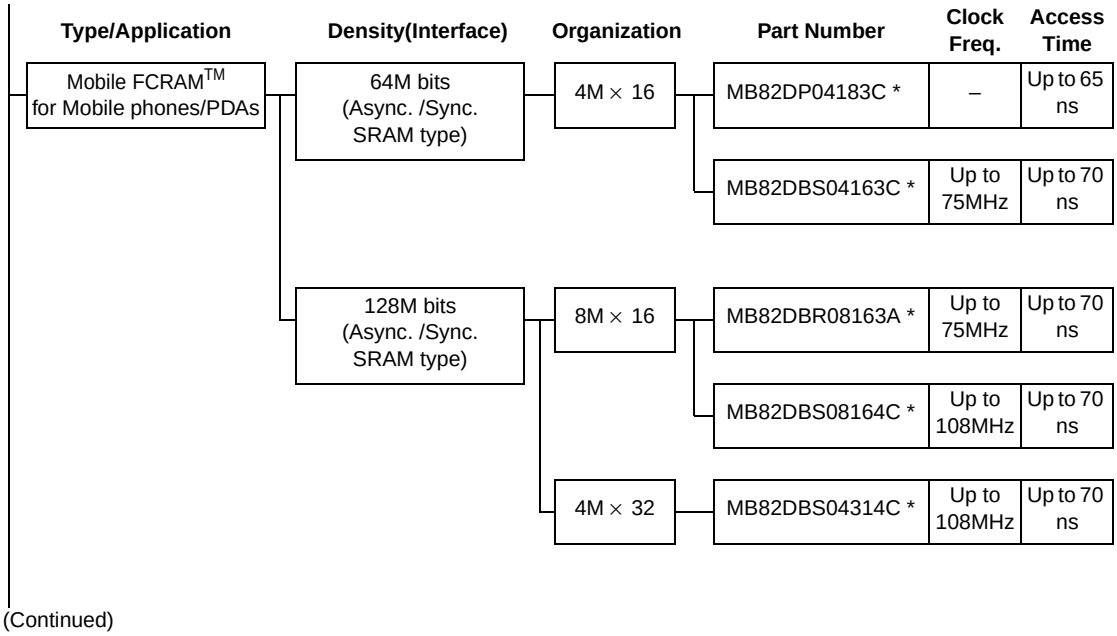
T_A = −30° C to +85° C

Organization (W × b)	Part Number *1	Access Time Max. (ns) *2	Supply Current Max.			Supply Voltage (V)	Package
			Operating (mA)	Standby (µA)	Power Down (µA)		FBGA
2M × 16	MB82DP02183C-65L	65 (20)	30	80	10	2.6 to 3.5	71P,*3,*4
	MB82DBS02163C-70L	70 (20) <12>	30	80	10	1.65 to 1.95	71P,*3,*4

*1: Package suffix is not included.
*2: ( ) : Page Address Access Time, < > : Burst Clock Access Time.
*3: FBGA package in compliance with COSMORAM spec (Suffix PBT).
*4: Stacked MCP (Multi Chip Package) parts, in which an Async. SRAM type FCRAM part is packaged with a flash memory part, is also available for mobile phone applications. Chip/wafer (Suffix KTD/WFKT) supply is optional.

FCRAM™ (Fast Cycle RAM) (2)

(Continued)



Type/Application	Density(Interface)	Organization	Part Number	Clock Freq.	Access Time
Mobile FCRAM™ for Mobile phones/PDAs	64M bits (Async. /Sync. SRAM type)	4M × 16	MB82DP04183C *	–	Up to 65 ns
			MB82DBS04163C *	Up to 75MHz	Up to 70 ns
	128M bits (Async. /Sync. SRAM type)	8M × 16	MB82DBR08163A *	Up to 75MHz	Up to 70 ns
			MB82DBS08164C *	Up to 108MHz	Up to 70 ns
		4M × 32	MB82DBS04314C *	Up to 108MHz	Up to 70 ns

(Continued)

* : Compliance with "COSMORAM (Common Specifications for Mobile RAM) "
COSMORAM is common specifications for pseudo SRAM agreed among Toshiba Corporation Semiconductor Company, NEC Electronics Corporation, and FUJITSU LIMITED.

FCRAM is a trademark of Fujitsu Limited.

FCRAM™ (Fast Cycle RAM) (2)

- 64M-bit Async. /Sync. SRAM Type FCRAM

T_A = -30°C to +85°C

Organization (W × b)	Part Number *1	Access Time Max. (ns) *2	Supply Current Max.			Supply Voltage (V)	Package
			Operating (mA)	Standby (µA) *3	Power Down (µA)		FBGA
4M × 16	MB82DP04183C-65L	65 (20)	40	90	10	2.6 to 3.1	71P, *4, *5
	MB82DBS04163C-70L	70 (20) <10>	35	90	10	1.7 to 1.95	71P, *4, *5

*1: Package suffix is not included.
*2: ( ) : Page Address Access Time, < > : Burst Clock Access Time.
*3: TA ≦ 40°C.
*4: FBGA package in compliance with COSMORAM spec (Suffix PBT) . Production support with monolithic package is T.B.D.
*5: Stacked MCP (Multi Chip Package) parts, in which an Async. SRAM type FCRAM part is packaged with a flash memory part, is also available for mobile phone applications. Chip/wafer (Suffix KTD/WFKT) supply is optional.

- 128M-bit Async. /Sync. SRAM Type FCRAM

T_A = -30°C to +85°C

Organization (W × b)	Part Number *1	Access Time Max. (ns) *2	Supply Current Max.			Supply Voltage (V)	Package
			Operating (mA)	Standby (µA)	Power Down (µA)		FBGA
8M × 16	MB82DBR08163A-70L	70 (20) <11>	35	300	10	Core : 2.6 to 3.1 IO : 1.65 to 1.95	71P, *4, *5
	MB82DBS08164C-70L	70 <6> *3	40	300	10	1.7 to 1.95	115P, *4, *5
4M × 32	MB82DBS04314C-70L	70 <6> *3	50	300	10	1.7 to 1.95	115P, *4, *5

*1: Package suffix is not included.
MB82DBR08163A : with Burst mode (Sync. Type) & Page mode (Async. Type) .
MB82DBS08164C/MB82DBS04314C : with Burst mode (Sync. Type) .
*2: ( ) : Page Address Access Time, < > : Burst Clock Access Time.
*3: Burst Clock Access Time : RL = 6, 7
*4: FBGA (Fine Pitch Ball Grid Array) package in compliance with COSMORAM spec (Suffix PBT) . Production support with monolithic package is T.B.D.
*5: Stacked MCP (Multi Chip Package) parts, in which an Async. SRAM type FCRAM part is packaged with a flash memory part, is also available for mobile phone applications. Chip/wafer (Suffix KTD/WFKT) supply is optional.

FCRAM™ (Fast Cycle RAM) (3)

(Continued)

Type/Application	Density (Interface)	Organization	Part Number	Clock Freq.	Access Time
Consumer FCRAM™ for Consumer Products/ Embedded Systems	16M bits (SDR-SDRAM type)	2 × 512K × 16	MB81ES171625 MB81ES171625-X *	Up to 85 MHz	Up to 10.2 ns
		2 × 256K × 32	MB81ES173225 MB81ES173225-X *	Up to 85 MHz	Up to 10.2 ns
	128M bits (SDR-SDRAM type)	4 × 1M × 32	MB81ES123245	Up to 108 MHz	Up to 7 ns

* : Clock Frequency to 66.7 MHz, Access time to 12 ns

FCRAM is a trademark of Fujitsu Limited.

Consumer FCRAM™ (Fast Cycle RAM)

- 16M-bit SDR-SDRAM Type *1 FCRAM

V_{DD} = +1.65V to +1.95V, T_j = 0°C to +100°C

Organization (Bank × W × b)	Part Number *2	Clock Frequency Max. (MHz)	Clock Period Min. (ns)	Access Time Max. (ns) *3	Supply Current Max. (mA) *4		Shipping style
					Operating	Standby	
2 × 512K × 16	MB81ES171625-12	85	11.7	10.2	30	1	Chip or Wafer
	MB81ES171625-15	66.7	15	12	30	1	
2 × 256K × 32	MB81ES173225-12	85	11.7	10.2	30	1	
	MB81ES173225-15	66.7	15	12	30	1	

V_{DD} = +1.65V to +1.95V, T_j = -40°C to +125°C

Organization (Bank × W × b)	Part Number *2	Clock Frequency Max. (MHz)	Clock Period Min. (ns)	Access Time Max. (ns) *3	Supply Current Max. (mA) *4		Shipping style
					Operating	Standby	
2 × 512K × 16	MB81ES171625-15-X	66.7	15	12	30	1	Chip or Wafer
2 × 256K × 32	MB81ES173225-15-X	66.7	15	12	30	1	

*1: Single Data Rate SDRAM Interface.
*2: Chip/wafer suffix (KTD/WFKT) are not included.
*3: t_{AC}(Max.)
*4: Operating current is I_{DD1} (1 Bank Active) and Standby current is I_{DD2P} (Power Down Mode) .

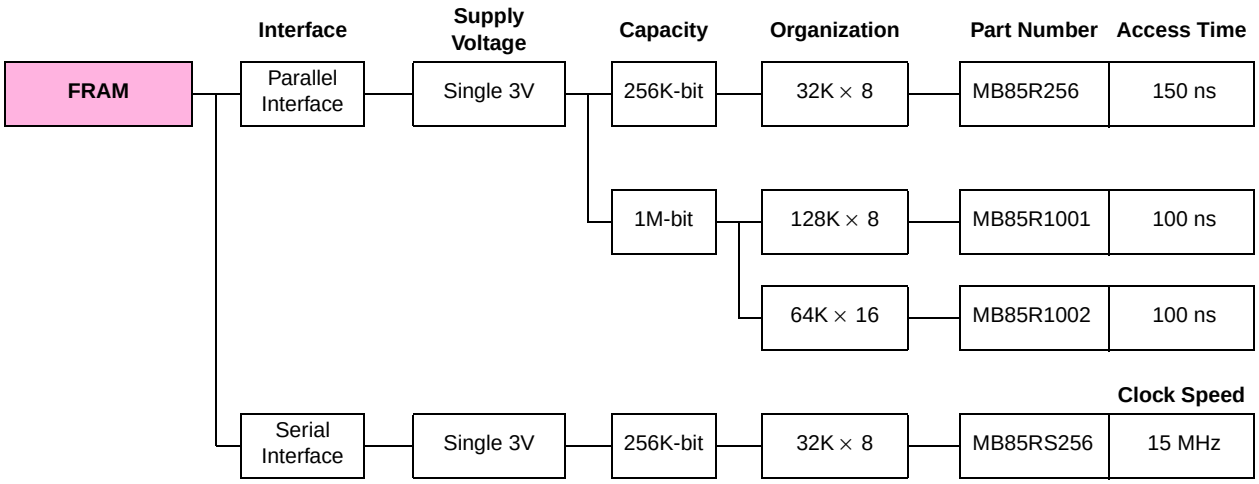
- 128M-bit SDR-SDRAM Type *1 FCRAM

V_{DD} = +1.7V to +1.9V, T_j *6

Organization (Bank × W × b)	Part Number *2	Clock Frequency Max. (MHz)	Clock Period Min. (ns)	Access Time Max. (ns) *3	Supply Current Max. (mA) *4		Shipping style
					Operating	Standby	
4 × 1M × 32	MB81ES123245-10	108	9.2	7	*5	0.5	Chip or Wafer

*1: Single Data Rate SDRAM Interface
*2: Chip/wafer suffix (KTD/WFKT) are not included.
*3: t_{AC}(Max.)
*4: Operating current is I_{DD1} (1 Bank Active) and Standby current is I_{DD2P} (Power Down Mode) .
*5: 60 (Page Length 256) , 45 (Page Length 128) , 35 (Page Length 64)
*6: T_j = -25°C to +95°C

FRAM (Ferroelectric RAM)



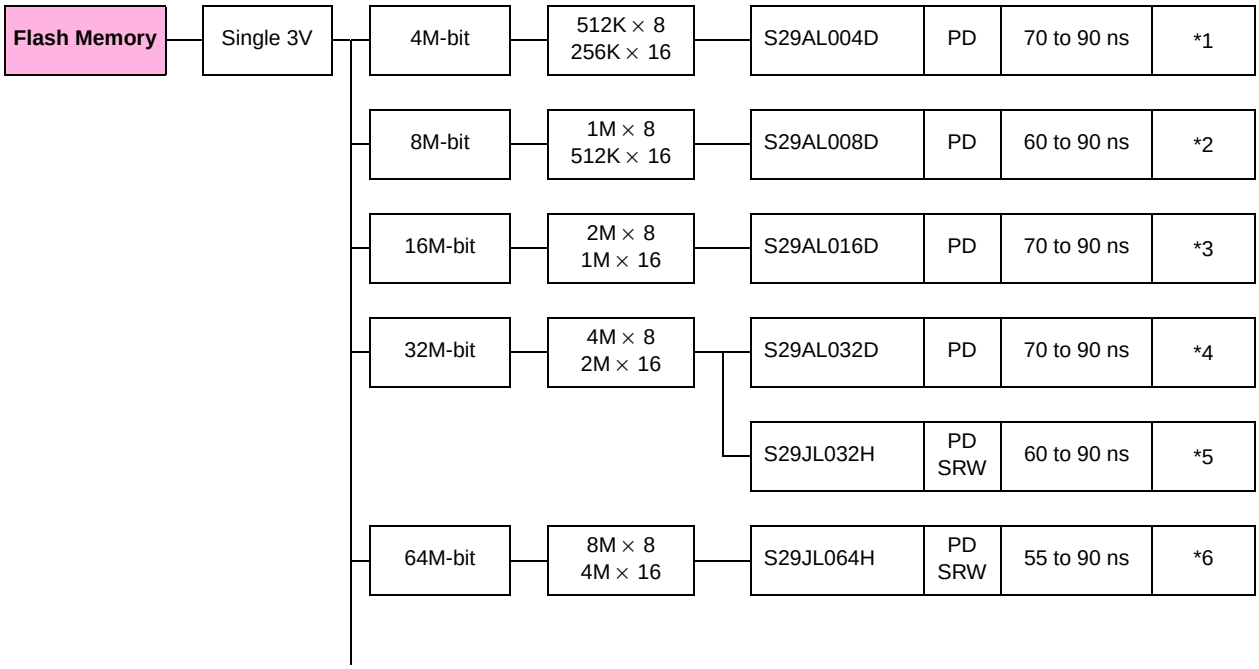
FRAM

Interface	Organization (W × b)	Part Number	Access Time Max. (ns)	Cycle Time Min. (ns)	Clock Speed Max. (MHz)	V_{CC} Current		Supply Voltage (V)	Operating Temperature Range T_A (°C)	Packages		
						Operating (mA)	Standby (μA)			SOP	TSOP	FBGA
Parallel	32K × 8	MB85R256	150	235	–	5	5	3.0 to 3.6	-40 to +85	28P	28P	-
Parallel	128K × 8	MB85R1001	100	200	–	10	10	3.0 to 3.6	-20 to +85	-	48P	-
Parallel	64K × 16	MB85R1002	100	200	–	10	10	3.0 to 3.6	-20 to +85	-	48P	48P
Serial	32K × 8	○ MB85RS256	–	–	15	10	50	3.0 to 3.6	-20 to +85	8P	-	-

Pakage : P –Plastic
○: New released.

Flash Memory (Single 3V) (1)

(Continued)



(Continued)

Variation
PD: Automatic sleep mode
SRW: Simultaneous Read / Write operation (Read-while-program or Read-while-Erase)

MirrorBit is a trademark of Spansion LLC.

*1 : (16Kbytes × 1sectors) + (8Kbytes × 2sectors) + (32Kbytes × 1sector) + (64Kbytes × 7sectors)
*2 : (16Kbytes × 1sectors) + (8Kbytes × 2sectors) + (32Kbytes × 1sector) + (64Kbytes × 15sectors)
*3 : (16Kbytes × 1sectors) + (8Kbytes × 2sectors + (32Kbytes × 1sector) + (64Kbytes × 31sectors)
*4 : (16Kbytes × 1sectors) + (8Kbytes × 2sectors + (32Kbytes × 1sector) + (64Kbytes × 61sectors)
*5 : (8Kbytes × 8sectors) + (64Kbytes × 63sectors)
*6 : (8Kbytes × 16sectors) + (64Kbytes × 126sectors)

Flash memory (Single 3V)

Organization (W × b)	Part Number	Access Time Max. (ns)	Cycle Time Min. (ns)	V_{CC} Current		Supply Voltage (V)	Operating Temperature Range T_A (°C)	Packages		
				Read (mA)	Standby Mode (μA)			TSOP	FBGA	SOP
512K × 8 256K × 16	S29AL004D70 *	70	70	16 (f = 5 MHz)	5	2.7 to 3.6	-40 to +85	48P	48P	44P
	S29AL004D90	90	90							
1M × 8 512K × 16	S29AL008D60 *	60	60	16 (f = 5 MHz)	5	3.0 to 3.6	-40 to +85	48P	48P	44P
	S29AL008D70 *	70	70			2.7 to 3.6				
	S29AL008D90	90	90							
2M × 8 1M × 16	S29AL016D70 *	70	70	16 (f = 5 MHz)	5	2.7 to 3.6	-40 to +85	48P	48P	–
	S29AL016D90	90	90							
4M × 8 2M × 16	S29AL032D70 *	70	70	16 (f = 5 MHz)	5	2.7 to 3.6	-40 to +85	48P	48P	–
	S29AL032D90	90	90							
	S29JL032H60 *	60	60	16 (f = 5 MHz)	5	2.7 to 3.6	-40 to +85	48P	–	–
	S29JL032H70	70	70							
	S29JL032H90	90	90							
8M × 8 4M × 16	S29JL064H55 *	55	55	16 (f = 5 MHz)	5	2.7 to 3.6	-40 to +85	48P	63P	–
	S29JL064H60 *	60	60							
	S29JL064H70	70	70							
	S29JL064H90	90	90							

* : at C_L = 30pF

Package: P-Plastic

Flash Memory (Single 3V) (2)

(Continued)

Capacity	Organization	Part Number	Variation	Access Time	Remarks
32M-bit	2M × 16	S29PL032J	PD SRW PM	From 55 to 70 ns	*1
64M-bit	4M × 16	S29PL064J	PD SRW PM	From 55 to 70 ns	*2
128M-bit	8M × 16	S29PL127J	PD SRW PM	From 55 to 70 ns	*3
		S29PL129J	PD SRW PM	From 55 to 70 ns	*4

Feature
Variation
PD: Automatic sleep mode
SRW: Simultaneous Read / Write operation (Read-while-program or Read-while-Erase)
PM: Page mode

*1: Sector structure - (4 K word ×8 sectors, 32 K word × 7 sectors) + (32 K word × 24 sectors) + (32 K word × 24 sectors) (4 K word × 8 sectors, 32 K word × 7 sectors)
*2: Sector structure - (4 K word × 8 sectors, 32 K word × 15 sectors) + (32 K word × 48 sectors) + (32 K word × 48 sectors) (4 K word × 8 sectors, 32 K word × 15 sectors)
*3: Sector structure - (4 K word × 8 sectors, 32 K word × 31 sectors) + (32 K word × 96 sectors) + (32 K word × 96 sectors) (4 K word × v8 sectors, 32 K word × 31 sectors)
*4: Sector structure - (4 K word × 8 sectors, 32 K word × 31 sectors) + (32 K word × 96 sectors) + (32 K word × 96 sectors) (4 K word × 8 sectors, 32 K word × 31 sectors)

Flash memory (Single 3V)

(Continued)

Organization (W × b)	Part Number	Access Time Max. (ns)	Cycle Time Min. (ns)	V_{CC} Current		Supply Voltage (V)	Operating Temperature Range T_A (°C)	Packages	
				Read (mA)	Standby Mode (μA)			TSOP	FBGA
2M × 16	S29PL032J55BxW	55 (20) *	55 (20) *	30 (f = 5 MHz)	5	Read:2.7 to 3.6 Write:2.7 to 3.6	-25 to +85 -40 to +85	-	48P 56P
	S29PL032J60BxW	60 (25) *	60 (25) *						
	S29PL032J70BxW	70 (30) *	70 (30) *						
4M × 16	S29PL064J55BxW	55 (20) *	55 (20) *	30 (f = 5 MHz)	5	Read:2.7 to 3.6 Write:2.7 to 3.6	-25 to +85 -40 to +85	-	48P 56P
	S29PL064J60BxW	60 (25) *	60 (25) *						
	S29PL064J70BxW	70 (30) *	70 (30) *						
8M × 16	S29PL127J55xxW	55 (20) *	55 (20) *	30 (f = 5 MHz)	5	Read:2.7 to 3.6 Write:2.7 to 3.6	-25 to +85 -40 to +85	56P	64P 80P
	S29PL127J60xxW	60 (25) *	60 (25) *						
	S29PL127J70xxW	70 (30) *	70 (30) *						
	S29PL129J55xxW	55 (20) *	55 (20) *	30 (f = 5 MHz)	5	Read:2.7 to 3.6 Write:2.7 to 3.6	-25 to +85 -40 to +85	56P	64P 80P
	S29PL129J60xxW	60 (25) *	60 (25) *						
	S29PL129J70xxW	70 (30) *	70 (30) *						

C_L = 30pF

*: Page Access

Package: P - Plastic

Flash memory (Single 1.8V)

	Supply Voltage	Capacity	Organization	Part Number	Variation	Access Time	Remarks
Flash Memory	Single 1.8V	64M-bit	4M × 16	S29WS064J	PD BM SRW HM	From 9.1 (80 MHz) to 11.2 ns (66 MHz)	*2
		128M-bit	8M × 16	S29WS128J	PD BM SRW HM	From 9.1 (80 MHz) to 11.2 ns (66 MHz)	*3
				S29WS128K	PD BM SRW HM	From 7.0 (108 MHz) to 13.5 ns (54 MHz)	*4

Feature
T: The boot blocks located in top address area.
B: The boot blocks located in bottom address area.
D: The boot blocks located in top address and bottom address area.

Variation
PD : Automatic sleep mode
SRW: Simultaneous Read / Write operation (Read-while-program or Read-while-Erase)
PM: Page mode
BM: Burst Mode
HM: Hand Shake Mode

*1: Sector structure - (16Kbytes × 1sector) + (8Kbytes × 2sectors)+(32Kbytes × 1sector)+(64Kbytes × 15sectors)
*2: Sector structure - (4Kwords × 16sectors) + (32Kwords × 126sectors)
*3: Sector structure - (4Kwords × 16sectors) + (32Kwords × 254sectors)
*4: Sector structure - (16Kwords × 8sectors) + (32Kwords × 252sectors)

Flash memory (Single 1.8V)

T_A = -40 °C to +85 °C

Organization (W × b)	Part Number	Access Time Max. (ns)	Cycle Time Min. (ns)	Burst Speed (MHz)	V_{CC} Current		Supply Voltage (V)	Packages	
					Read (mA)	Standby Mode (µA)		FBGA	Super CSP
4M × 16	S29WS064J0P	55 *1, 56/11.2 *2	–	66	30 *3, *4	50	1.65 to 1.95	80P	–
	S29WS064J0S	45 *1, 46/9.1 *2		80	36 *3, *4				
8M × 16	S29WS128J0P	55 *1, 56/11.2 *2	–	66	30 *3, *4	50	1.65 to 1.95	84P	–
	S29WS128J0S	45 *1, 46/9.1 *2		80	36 *3, *4				
	S29WS128KBA	45 *1, 45/7.0 *2	–	108	25 *3, *4	50	1.70 to 1.95	80P 84P	–
	S29WS128K0S	45 *1, 45/9.0 *2		80	25 *3, *4				
	S29WS128K0P	55 *1, 55/11.2 *2		66	20 *3, *4				
	S29WS128K0L	55 *1, 55/13.5 *2		54	20 *3, *4				

C_L = 30pF

Package: P-Plastic

*1 : Asynchronous access time

*2 : Synchronous delay time/burst access time

*3 : Burst Read

*4 : Continuous mode

Flash Memory (MirrorBit ™) (Single 3 V)

	Supply Voltage	Capacity	Organization	Part Number	Variation	Access Time	Remarks
Flash Memory MirrorBit ™	Single 3V	16M-bit	2M × 8 1M × 16	S29GL016A	PD PM	from 90 to 100 ns.	*2
		32M-bit	4M × 8 2M × 16	S29GL032A	PD PM	from 90 to 110 ns.	*3
		64M-bit	8M × 8 4M × 16	S29GL064A	PD PM	from 90 to 110 ns.	*4
		128M-bit	16M × 8 8M × 16	S29GL128N	PD PM	from 90 to 110 ns.	*5
		256M-bit	32M × 8 16M × 16	S29GL256N	PD PM	from 90 to 110 ns.	*6
		512M-bit	64M × 8 32M × 16	S29GL512N	PD PM	from 100 to 110 ns.	*7
		1G-bit	128M × 8 64M × 16	S70GL01GN11	PD PM	110 ns.	*8

Variation
PD : Automatic sleep mode
PM: Page mode

MirrorBit is a trademark of Spansion LLC.

*1: 16Kbytes × 1 +8Kbytes × 2 +32Kbytes × 1 +64Kbytes × 31sectors (Byte mode)
8Kword × 1 +4Kword × 2 +16Kword × 1 +32Kword × 31sectors (Word mode)
*2: Uniform sector model : 32Kword (64Kbytes) × 32sectors
Boot sector model : 32Kword (64Kbytes) × 31sectors +4Kword (8Kbytes) × 8sectors
*3: Uniform sector model : 32Kword (64Kbytes) × 64sectors
Boot sector model : 32Kword (64Kbytes) × 63sectors +4Kword (8Kbytes) × 8sectors
*4: Uniform sector model : 32Kword (64Kbytes) × 128sectors
Boot sector model : 32Kword (64Kbytes) × 127sectors +4Kword (8Kbytes) × 8sectors
*5: Sector structure - 64Kword (128Kbytes) × 128sectors
*6: Sector structure - 64Kword (128Kbytes) × 256sectors
*7: Sector structure - 64Kword (128Kbytes) × 512sectors
*8: Sector structure - 64Kword (128Kbytes) × 1024sectors

Flash memory (MirrorBit) (Single 3V)

Organization (W × b)	Part Number	Access Time Max. (ns)	Cycle Time Min. (ns)	V_{CC} Current		Supply Voltage (V)	Operating Temperature Range T_A (°C)	Packages	
				Read (mA)	Standby Mode (μA)			TSOP	FBGA
2M × 8 1M × 16	◎ S29GL016A90	90 (25)	90 (25)	25 (f = 5 MHz)	5	3.0 to 3.6	-40 to +85	48P	48P 64P
	◎ S29GL016A10	100 (30)	100 (30)						
4M × 8 2M × 16	◎ S29GL032A90	90 (25)	90 (25)	25 (f = 5 MHz)	5	3.0 to 3.6	-40 to +85	40P 48P 56P	48P 64P
	◎ S29GL032A10	100 (30)	100 (30)						
	◎ S29GL032A11	110 (30)	110 (30)						
8M × 8 4M × 16	◎ S29GL064A90	90 (25)	90 (25)	25 (f = 5 MHz)	5	3.0 to 3.6	-40 to +85	48P 56P	63P 64P
	◎ S29GL064A10	100 (30)	100 (30)						
	◎ S29GL064A11	110 (30)	110 (30)						
16M × 8 8M × 16	S29GL128N90	90 (25)	90 (25)	50 (f = 5 MHz)	5	3.0 to 3.6	-40 to +85	56P	64P
	S29GL128N10	100 (25)	100 (25)			2.7 to 3.6			
	S29GL128N11	110 (30)	110 (30)						
32M × 8 16M × 16	S29GL256N90	90 (25)	90 (25)	50 (f = 5 MHz)	5	3.0 to 3.6	-40 to +85	56P	64P
	S29GL256N10	100 (25)	100 (25)			2.7 to 3.6			
	S29GL256N11	110 (30)	110 (30)						
64M × 8 32M × 16	S29GL512N10	100 (25)	100 (25)	50 (f = 5 MHz)	5	2.7 to 3.6	-40 to +85	56P	64P
	S29GL512N11	110 (30)	110 (30)						
128M × 8 64M × 16	S70GL01GN11	110 (25)	110 (25)	50 (f = 5 MHz)	5	2.7 to 3.6	-40 to +85	–	64P

◎ : Now planning

C_L = 30pF

Package: P-Plastic

Flash Memory (MirrorBit ™) (Single 1.8 V)

(Continued)

	Supply Voltage	Capacity	Organization	Part Number	Variation	Access Time	Remarks
Flash Memory MirrorBit ™	Single 1.8V	128M-bit	8M × 16	S29WS128N	PD BM SRW HM	from 9 (80 MHz.) to 13.5 ns. (54 MHz.)	*1
		256M-bit	16M × 16	S29WS256N	PD BM SRW HM	from 9 (80 MHz.) to 13.5 ns. (54 MHz.)	*2

Variation
PD : Automatic sleep mode
BM: Burst mode
SRW: Simultaneous Read / Write operation (Read-while-program or Read-while-Erase)
HM: Hand Shake Mode

MirrorBit is a trademark of Spansion LLC.

*1: Sector structure - (16Kwords × 8sectors) + (64Kwords × 126sectors)
*2: Sector structure - (16Kwords × 8sectors) + (64Kwords × 254sectors)

Flash memory (MirrorBit) (Single 1.8V)

Organization (W × b)	Part Number	Access Time Max. (ns)	Burst Speed (MHz)	V_{CC} Current		Supply Voltage (V)	Operating Temperature Range T_A (°C)	Packages
				Read (mA)	Standby Mode (μA)			FBGA
8M × 16	S29WS128N0LBxW	80 *1, 80/13.5 *2	54	36 *3	40	1.70 to 1.95	-25 to +85	84P
	S29WS128N0PBxW	80 *1, 80/11.2 *2	66	42 *3				
	S29WS128N0SBxW	80 *1, 80/9.0 *2	80	48 *3				
16M × 16	S29WS256N0LBxW	80 *1, 80/13.5 *2	54	36 *3	40	1.70 to 1.95	-25 to +85	84P
	S29WS256N0PBxW	80 *1, 80/11.2 *2	66	42 *3				
	S29WS256N0SBxW	80 *1, 80/9.0 *2	80	48 *3				

C_L = 30pF
Package: P-Plastic
*1 : Asynchronous access time
*2 : Synchronous delay time/burst access time
*3 : Burst Read (continuous mode)

Serial Peripheral Interface (MirrorBit™) (Single 3 V)

	Supply Voltage	Capacity	Organization	Part Number	Variation	Access Time	Remarks
Flash Memory MirrorBit ™	Single 3V	4 M-bit	4 M × 1	S25FL004A	SI	50 MHz	*1
		8 M-bit	8 M × 1	S25FL008A	SI	50 MHz	*2
		16 M-bit	16 M × 1	S25FL016A	SI	50 MHz	*3
		64M-bit	64 M × 1	S25FL064A	SI	50 MHz	*4

Variation
SI: Serial interface

*1 : Sector structure - 512 K bytes × 8 sectors
*2 : Sector structure - 512 K bytes × 16 sectors
*3 : Sector structure - 512 K bytes × 32 sectors
*4 : Sector structure - 512 K bytes × 128 sectors

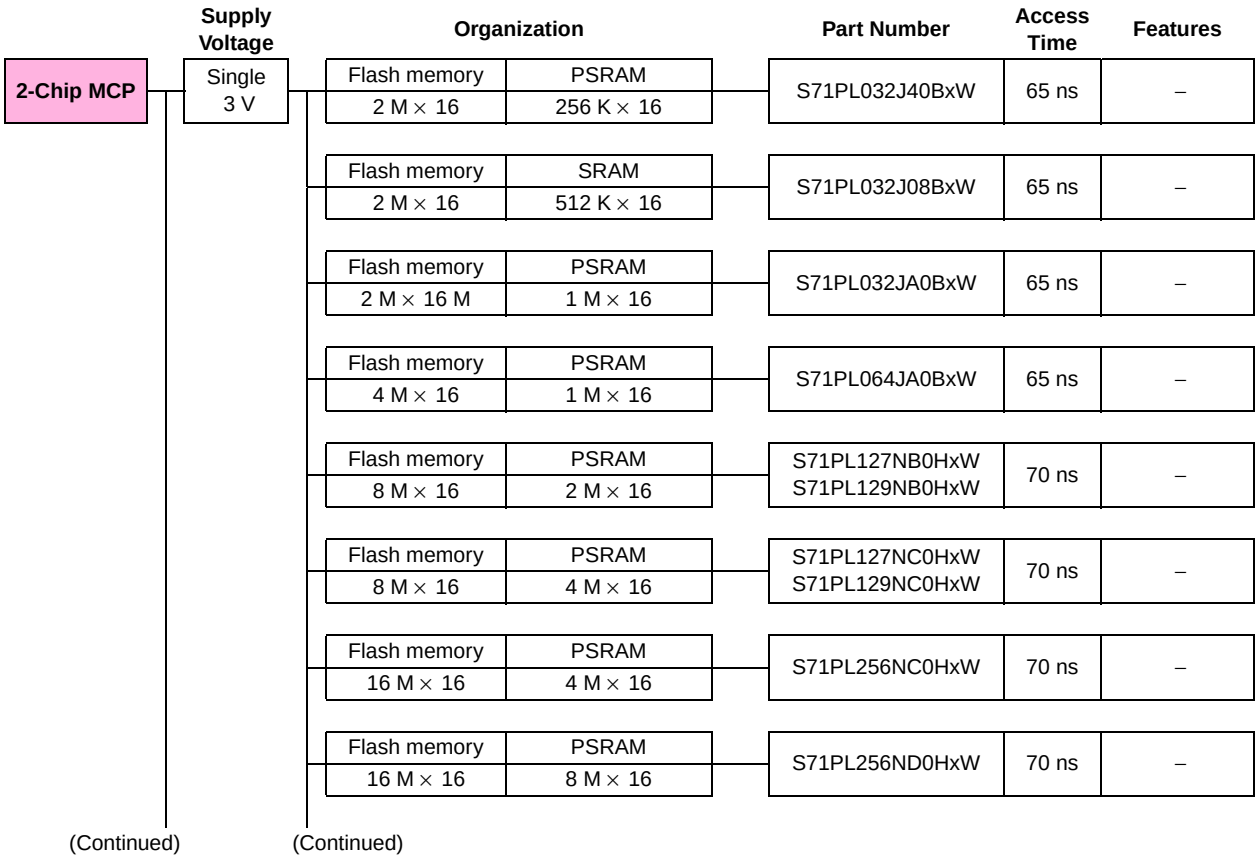
Serial Peripheral Interface (MirrorBit™) (Single 3 V)

Flash memory (MirrorBit) (Single 3 V)

Organization (W × b)	Part Number	Clock speed (MHz)	V_{CC} Current		Supply Voltage (V)	Operating Temperature Range T_A (°C)	Packages	
			Read (mA)	Standby Mode (μA)			SOP	SON
4 M × 1	S25FL004A0L	50	13 (f = 50MHz)	50	2.7 to 3.6	-40 to +85	8SO	8USON
8 M × 1	S25FL008A0L	50	12 (f = 50MHz)	50	2.7 to 3.6	-40 to +85	8SO	8USON
16 M × 1	S25FL016A0L	50	11 (f = 50MHz)	50	2.7 to 3.6	-40 to +85	16SO	8WSON
64 M × 1	S25FL064A0L	50	10 (f = 50MHz)	50	2.7 to 3.6	-40 to +85	16SO	–

C_L = 30pF
Package: P-Plastic

MCP (Multi Chip Package)



2-Chip MCP (Single 3 V)

Part Number	Organization (W × b)	Access Time Max. (ns)	V_{CC} Current		Supply Voltage (V)	Operating Temperature (°C)	Packages
			Read (mA)	Standby Mode (μA)			BGA
S71PL032J40BxW	Flash memory 2 M × 16	65	30 (f = 5 MHz)	5	2.7 to 3.1	-25 to +85	56P
	PSRAM 256 K × 16		22 (f = 10 MHz)	100			
S71PL032J08BxW	Flash memory 2 M × 16	65	30 (f = 5 MHz)	5	2.7 to 3.1	-25 to +85	56P
	SRAM 512 K × 16		25 (f = 10 MHz)	10			
S71PL032JA0BxW	Flash memory 2 M × 16	65	30 (f = 5 MHz)	5	2.7 to 3.1	-25 to +85	56P
	PSRAM 1 M × 16		35	100			
S71PL064JA0BxW	Flash memory 4 M × 16	65	30 (f = 5 MHz)	5	2.7 to 3.1	-25 to +85	56P
	PSRAM 1 M × 16		25	100			
◎ S71PL127NB0HxW ◎ S71PL129NB0HxW	Flash memory 8 M × 16	70	45 (f = 5 MHz)	40	2.7 to 3.1	-25 to +85	64P
	PSRAM 2 M × 16		35	100			
◎ S71PL127NC0HxW ◎ S71PL129NC0HxW	Flash memory 8 M × 16	70	45 (f = 5 MHz)	40	2.7 to 3.1	-25 to +85	64P
	PSRAM 4 M × 16		45	120			
S71PL256NC0HxW	Flash memory 16 M × 16	70	45 (f = 5 MHz)	40	2.7 to 3.1	-25 to +85	84P
	PSRAM 4 M × 16		45	120			
S71PL256ND0HxW	Flash memory 16 M × 16	70	45 (f = 5 MHz)	40	2.7 to 3.1	-25 to +85	84P
	PSRAM 8 M × 16		TBD	TBD			

◎ : Now planning

Package: P-Plastic
Consult the Sales representatives for other products.

MCP (Multi Chip Package)

(Continued) (Continued)

Supply Voltage	Organization		Part Number	Access Time	Features
Single 3 V	Flash memory 1 M × 16	PSRAM 256 K × 16	S71GL016A40BxW	100 ns	–
	Flash memory 2 M × 16	PSRAM 256 K × 16	S71GL032A40BxW	100 ns	–
	Flash memory 2 M × 16 M	SRAM 512 K × 16	S71GL032A08BxW	100 ns	–
	Flash memory 4 M × 16	SRAM 512 K × 16	S71GL064A08BxW	100 ns	–
	Flash memory 4 M × 16	PSRAM 1 M × 16	S71GL064AA0BxW	100 ns	–
	Flash memory 8 M × 16	PSRAM 2 M × 16	S71GL128NB0BxW	90 ns	–
	Flash memory 8 M × 16	PSRAM 4 M × 16	S71GL128NC0BxW	90 ns	–
	Flash memory 16 M × 16	PSRAM 2 M × 16	S71GL256NB0BxW	90 ns	–
	Flash memory 32 M × 16	PSRAM 2 M × 16	S71GL512NB0BxW	100 ns	–

2-Chip MCP (Single 3 V)

Part Number	Organization (W × b)	Access Time Max. (ns)	V_{CC} Current		Supply Voltage (V)	Operating Temperature (°C)	Packages
			Read (mA)	Standby Mode (µA)			BGA
S71GL016A40BxW	Flash memory 1 M × 16	100	25 (f = 5 MHz)	5	2.7 to 3.1	-25 to +85	56P
	PSRAM 256 K × 16		15 (f = 10 MHz)	40			
S71GL032A40BxW	Flash memory 2 M × 16	100	25 (f = 5 MHz)	5	2.7 to 3.1	-25 to +85	56P
	PSRAM 256 K × 16		15 (f = 10 MHz)	40			
S71GL032A08BxW	Flash memory 2 M × 16	100	25 (f = 5 MHz)	5	2.7 to 3.1	-25 to +85	56P
	SRAM 512 K × 16		22	15			
S71GL064A08BxW	Flash memory 4 M × 16	100	25 (f = 5 MHz)	5	2.7 to 3.1	-25 to +85	56P
	SRAM 512 K × 16		22	15			
S71GL064AA0BxW	Flash memory 4 M × 16	100	25 (f = 5 MHz)	5	2.7 to 3.1	-25 to +85	56P
	PSRAM 1 M × 16		20	100			
S71GL128NB0BxW	Flash memory 8 M × 16	90	30 (f = 5 MHz)	5	2.7 to 3.1	-25 to +85	64P
	PSRAM 2 M × 16		20	100			
S71GL128NC0BxW	Flash memory 8 M × 16	90	30 (f = 5 MHz)	5	2.7 to 3.1	-25 to +85	84P
	PSRAM 4 M × 16		TBD	TBD			
S71GL256NB0BxW	Flash memory 16 M × 16	90	30 (f = 5 MHz)	5	2.7 to 3.1	-25 to +85	84P
	PSRAM 2 M × 16		20	100			
S71GL512NB0BxW	Flash memory 32 M × 16	100	30 (f = 5 MHz)	5	2.7 to 3.1	-25 to +85	84P
	PSRAM 2 M × 16		20	100			

Package: P-Plastic
Consult the Sales representatives for other products.

MCP (Multi Chip Package)

	Supply Voltage	Organization			Part Number	Access Time	Features
		Code Flash memory	Data Flash memory	PSRAM			
3-Chip MCP	Single 3 V	8 M × 16	8 M × 16	2 M × 16	S75PL127JBDBxW	65	–
		8 M × 16	16 M × 16	2 M × 16	S75PL127JBEBxW	65	–
		8 M × 16	32 M × 16	2 M × 16	S75PL127JBFBxW	65	–
		8 M × 16	8 M × 16	4 M × 16	S75PL127JCDBxW	65	–
		8 M × 16	16 M × 16	4 M × 16	S75PL127JCEBxW	65	–
		8 M × 16	32 M × 16	4 M × 16	S75PL127JCFBxW	65	–

3-Chip MCP (Single 3 V)

Part Number	Organization (W × b)	Access Time Max. (ns)	V_{CC} Current		Supply Voltage (V)	Operating Temperature (°C)	Packages
			Read (mA)	Standby Mode (μA)			BGA
S75PL127JBDBxW	Code Flash 8 M × 16	65	30 (f = 5 MHz)	5	2.7 to 3.1	-25 to +85	84P
	Data Flash 8 M × 16		50 (f = 5 MHz)	5			
	PSRAM 2 M × 16		35	100			
S75PL127JBEBxW	Code Flash 8 M × 16	65	30 (f = 5 MHz)	5	2.7 to 3.1	-25 to +85	84P
	Data Flash 16M × 16		50 (f = 5 MHz)	5			
	PSRAM 2 M × 16		35	100			
S75PL127JBFBxW	Code Flash 8 M × 16	65	30 (f = 5 MHz)	5	2.7 to 3.1	-25 to +85	84P
	Data Flash 32 M × 16		50 (f = 5 MHz)	5			
	PSRAM 2 M × 16		45	120			
S75PL127JCDBxW	Code Flash 8 M × 16	65	30 (f = 5 MHz)	5	2.7 to 3.1	-25 to +85	84P
	Data Flash 8 M × 16		50 (f = 5 MHz)	5			
	PSRAM 4 M × 16		45	120			
S75PL127JCEBxW	Code Flash 8 M × 16	65	30 (f = 5 MHz)	5	2.7 to 3.1	-25 to +85	84P
	Data Flash 16 M × 16		50 (f = 5 MHz)	5			
	PSRAM 4 M × 16		45	120			
S75PL127JCFBxW	Code Flash 8 M × 16	65	30 (f = 5 MHz)	5	2.7 to 3.1	-25 to +85	84P
	Data Flash 32 M × 16		50 (f = 5 MHz)	5			
	PSRAM 4 M × 16		45	120			

Package: P-Plastic
Consult the Sales representatives for other products.

MCP (Multi Chip Package)

	Supply Voltage	Organization		Part Number	Access Time	Features
2-Chip MCP	Single 1.8 V	Flash memory 4 M × 16	PSRAM 1 M × 16	S71WS064JA0BxW	55 *1 56/11.2 ns *2	–
		Flash memory 4 M × 16	PSRAM 2 M × 16	S71WS064JB0BxW	55 *1 56/11.2 ns *2	–
		Flash memory 8 M × 16	PSRAM 2 M × 16	S71WS128JB0BxW	55 *1 56/11.2 ns *2	–
		Flash memory 8 M × 16	PSRAM 4 M × 16	S71WS128JC0BxW	55 *1 56/11.2 ns *2	–
		Flash memory 8 M × 16	PSRAM 2 M × 16	S71WS128NB0BxW	80 *1 80/9 ns *2	–
		Flash memory 8 M × 16	PSRAM 4 M × 16	S71WS128NC0BxW	80 *1 80/9 ns *2	–
		Flash memory 16 M × 16	PSRAM 4 M × 16	S71WS256NC0BxW	80 *1 80/9 ns *2	–
		Flash memory 16 M × 16	PSRAM 8 M × 16	S71WS256ND0BxW	80 *1 80/9 ns *2	–

(Continued)

(Continued)

*1 : Asynchronous access time
*2 : Synchronous delay time/burst access time

2-Chip MCP (Single 1.8 V)

Part Number	Organization (W × b)	Access Time Max. (ns)	Burst speed (MHz)	V_{CC} Current		Supply Voltage (V)	Operating Temperature (°C)	Packages
				Read (mA)	Standby Mode (μA)			BGA
S71WS064JA0BxW	Flash memory 4 M × 16	55 *1	66	30 *3	50	1.7 to 1.95	-25 to +85	80P
	PSRAM 1 M × 16	56/11.2 *2		30*4	110			
S71WS064JB0BxW	Flash memory 4 M × 16	55 *1	66	30 *3	50	1.7 to 1.95	-25 to +85	80P
	PSRAM 2 M × 16	56/11.2 *2		30*4	110			
S71WS128JB0BxW	Flash memory 8 M × 16	55 *1	66	30 *3	50	1.7 to 1.95	-25 to +85	84P
	PSRAM 2 M × 16	56/11.2 *2		30*4	110			
S71WS128JC0BxW	Flash memory 8 M × 16	55 *1	66	30 *3	50	1.7 to 1.95	-25 to +85	84P
	PSRAM 4 M × 16	56/11.2 *2		30*4	120			
S71WS128NB0BxW	Flash memory 8 M × 16	80 *1 80/9 *2	80 66 54	48 *3	40	1.7 to 1.95	-25 to +85	84P
	PSRAM 2 M × 16	80 *1 80/11.2 *2 80 *1 80/13.5 *2		35 *4	110			
S71WS128NC0BxW	Flash memory 8 M × 16	80 *1 80/9 *2	80 66 54	48 *3	40	1.7 to 1.95	-25 to +85	84P
	PSRAM 4 M × 16	80 *1 80/11.2 *2 80 *1 80/13.5 *2		35 *4	120			
S71WS256NC0BxW	Flash memory 16 M × 16	80 *1 80/9 *2	80 66 54	48 *3	40	1.7 to 1.95	-25 to +85	84P
	PSRAM 4 M × 16	80 *1 80/11.2*2 80* 1 80/13.5 *2		35 *4	120			
S71WS256ND0BxW	Flash memory 16 M × 16	80* 1 80/9 *2	80 66 54	48 *3	40	1.7 to 1.95	-25 to +85	84P
	PSRAM 8 M × 16	80 *1 80/11.2*2 80 *1 80/13.5 *2		40	120			

*1 : Asynchronous access time
*2 : Synchronous delay time/burst access time
*3 : Burst read - at continuous mode
*4 : Initial Access - at burst read
Package: P-Plastic
Consult the Sales representatives for other products.

MCP (Multi Chip Package)

(Continued) (Continued)

Supply Voltage	Organization		Part Number	Access Time	Features
	Flash memory	PSRAM			
Single 1.8 V	4 M × 16	1 M × 16	S71NS064JA0BxFW	65 *1 71/11 ns *2 70*1 87.5/13.5 *2	–
	Flash memory	PSRAM			
	8 M × 16	1 M × 16	S71NS128JA0BxFW	65 *1 71/11 ns *2 70 *1 87.5/13.5 *2	–
	Flash memory	PSRAM			
	8 M × 16	4 M × 16	S71NS128JC0BxFW	65 *1 71/11 ns *2 70 *1 87.5/13.5 *2	–
	Flash memory	PSRAM			
	8 M × 16	1 M × 16	S71NS128NA0BxFW	80 *1 80/9 ns *2 80 *1 80/11 *2	–
	Flash memory	PSRAM			
	8 M × 16	4 M × 16	S71NS128NC0BxFW	80 *1 80/9 ns *2 80 *1 80/11 *2	–
	Flash memory	SDRAM			
	16 M × 16	8 M × 16	S72WS256ND0BxW	80 *1 80/13.5 *2	–
	Flash memory	SDRAM			
	16 M × 16	8 M × 16	S73WS256ND0BxW	80 *1 80/13.5 *2	–

*1 : Asynchronous access time
*2 : Synchronous delay time/burst access time

2-Chip MCP (Single 1.8 V)

Part Number	Organization (W × b)	Access Time Max. (ns)	Burst speed (MHz)	V_{CC} Current		Supply Voltage (V)	Operating Temperature (°C)	Packages
				Read (mA)	Standby Mode (μA)			BGA
S71NS064JA0BxFW	Flash memory 4 M × 16	65 *1 71/11 *2	66 54	30	40	1.7 to 1.95	-25 to +85	44P
	PSRAM 1 M × 16	70 *1 87.5/13.5 *2		25	60			
S71NS128JA0BxFW	Flash memory 8 M × 16	65 *1 71/11 *2	66 54	30	40	1.7 to 1.95	-25 to +85	48P
	PSRAM 1 M × 16	70 *1 87.5/13.5 *2		25	60			
S71NS128JC0BxFW	Flash memory 8 M × 16	65 *1 71/11 *2	66 54	30	40	1.7 to 1.95	-25 to +85	60P
	PSRAM 4 M × 16	70 *1 87.5/13.5 *2		35 *4	120			
S71NS128NA0BxFW	Flash memory 8 M × 16	80 *1 80/9 *2	80 66	42 *3	70	1.7 to 1.95	-25 to +85	44P
	PSRAM 1 M × 16	80 *1 80/11 *2		25	60			
S71NS128NC0BxFW	Flash memory 8 M × 16	80 *1 80/9 *2	80 66 54	42 *3	70	1.7 to 1.95	-25 to +85	56P
	PSRAM 4 M × 16	80 *1 80/11 *2 80 *1 80/13.5 *2		35 *4	120			
S72WS256ND0BxW	Flash memory 16 M × 16	80 *1 80/13.5 *2	54	36 *3	40	1.7 to 1.95	-25 to +85	137P
	SDRAM 8 M × 16			50	300			
S73WS256ND0BxW	Flash memory 16 M × 16	80 *1 80/13.5 *2	54	36 *3	40	1.7 to 1.95	-25 to +85	137P
	SDRAM 8 M × 16			50	300			

*1 : Asynchronous access time
*2 : Synchronous delay time/burst access time
*3 : At continuous mode
*4 : At initial Access
Package: P-Plastic
Consult the Sales representatives for other products.

MCP (Multi Chip Package)

	Supply Voltage	Organization			Part Number	Access Time	Features
3-Chip MCP	Single 1.8V	Flash memory 16 M × 16	Flash memory 16 M × 16	PSRAM 4 M × 16	S71WS512NC0BxW	80 *1 80/9 ns *2	–
		Flash memory 16 M × 16	Flash memory 16 M × 16	PSRAM 8 M × 16	S71WS512ND0BxW	80 *1 80/9 ns *2	–
		Flash memory 16 M × 16	Flash memory 16 M × 16	SDRAM 8 M × 16	S72WS256NDEBxW	80 *1 80/13.5 *2	–
					S73WS256NDEBxW	80 *1 80/13.5 *2	–
		Flash memory 16 M × 16	Flash memory 16 M × 16	SDRAM 16 M × 16	S72WS256NEEBxW	80 *1 80/13.5 *2	–
					S73WS256NEEBxW	80 *1 80/13.5 *2	–

*1 : Asynchronous access time
*2 : Synchronous delay time/burst access time

3-Chip MCP (Single 1.8 V)

Part Number	Organization (W × b)	Access Time Max. (ns)	Burst speed (MHz)	V_{CC} Current		Supply Voltage (V)	Operating Temperature (°C)	Packages
				Read (mA)	Standby Mode (μA)			BGA
S71WS512NC0BxW	Flash memory 16 M × 16	80 *1 80/ 9 *2	80 66 54	48 *3	40	1.7 to 1.95	-25 to +85	84P
	Flash memory 16 M × 16	80 *1 80/11. 2 *2		48 *3	40			
	PSRAM 4 M × 16	80 *1 80/13.5 *2		35 *4	120			
S71WS512ND0BxW	Flash memory 16 M × 16	80 *1 80/9 *2	80 66 54	48 *3	40	1.7 to 1.95	-25 to +85	84P
	Flash memory 16 M × 16	80 *1 80/11.2 *2		48 *3	40			
	PSRAM 8 M × 16	80 *1 80/13.5 *2		40	120			
S72WS256NDEBxW	Flash memory 16 M × 16	80 *1 80/13.5 *2	54	36 *3	40	1.7 to 1.95	-25 to +85	137P
	Flash memory 16 M × 16			36 *3	40			
	SDRAM 8 M × 16			30*4	110			
S73WS256NDEBxW	Flash memory 16 M × 16	80 *1 80/13.5 *2	54	36 *3	40	1.7 to 1.95	-25 to +85	137P
	Flash memory 16 M × 16			36 *3	40			
	SDRAM 8 M × 16			30*4	110			
S72WS256NEEBxW	Flash memory 16 M × 16	80 *1 80/13.5 *2	54	36 *3	40	1.7 to 1.95	-25 to +85	137P
	Flash memory 16 M × 16			36 *3	40			
	SDRAM 16 M × 16			35 *4	120			
S73WS256NEEBxW	Flash memory 16 M × 16	80 *1 80/13.5 *2	54	36 *3	40	1.7 to 1.95	-25 to +85	137P
	Flash memory 16 M × 16			36 *3	40			
	SDRAM 16 M × 16			35 *4	120			

*1 : Asynchronous access time
*2 : Synchronous delay time/burst access time
*3 : At continuous mode
*4 : At initial Access
Package: P-Plastic

MCP (Multi Chip Package)

	Supply Voltage	Organization				Part Number	Access Time	Features
4-Chip MCP	Single 1.8V	Flash memory	Flash memory	Flash memory	PSRAM	S75WS256NDFBxW	80 *1 80/9 ns *2	–
		16 M × 16	16 M × 16	16 M × 16	8 M × 16			

*1 : Asynchronous access time
*2 : Synchronous delay time/burst access time

4-Chip MCP (Single 1.8 V)

Part Number	Organization (W × b)	Access Time Max. (ns)	Burst speed (MHz)	V_{CC} Current		Supply Voltage (V)	Operating Temperature (°C)	Packages
				Read (mA)	Standby Mode (μA)			BGA
S75WS256NDFBxW	Flash memory 16 M × 16	80 *1	80 66 54	48 *3	40	1.7 to 1.95	-25 to +85	84P
	Flash memory 16 M × 16	80/9 *2						
	Flash memory 16 M × 16	80 *1						
	PSRAM 8 M × 16	80/11.2 *2						
		80 *1		35 *4	120			
		80/13.5 *2						

*1 : Asynchronous access time
*2 : Synchronous delay time/burst access time
*3 : Continuous modeéû
*4 : Initial Accesséû
Package: P-Plastic

Products Scheduled to be out of Production

The productions listed below are scheduled to go out of production.
If you are considering the use in the new applications, select the other series of products

FCRAM

Part number	Description
MB82D01161-85 MB82D01161-85L	16Mbit Async. SRAM Type FCRAM
MB82D01161-90 MB82D01161-90L	
MB82D01171A-80 MB82D01171A-80L MB82D01171A-80LL	
MB82D01171A-85 MB82D01171A-85L MB82D01171A-85LL	
MB82D01171A-90 MB82D01171A-90L MB82D01171A-90LL	
MB82D01171B-60L MB82D01171B-60LL	
MB82D01171B-70L MB82D01171B-70LL	
MB82D02172A-70 MB82D02172A-70L	32Mbit Async. SRAM Type FCRAM
MB82D02172A-80 MB82D02172A-80L	
MB82D04172-65 MB82D04172-65L	64Mbit Async. SRAM Type FCRAM
MB82D04172-75 MB82D04172-75L	
MB82DBS04163B-70 MB82DBS04163B-70L	64Mbit Async./Sync. SRAM Type FCRAM
MB82DP04183B-65 MB82DP04183B-65L	
MB82DBR08163-70 MB82DBR08163-70L	128Mbit Async./Sync. SRAM Type FCRAM
MB81E161622-10 MB81E161622-10-X	16Mbit SDR-SDRAM Type FCRAM
MB81E161622-12 MB81E161622-12-X	
MB811L323229-12 MB811L323229-18	32Mbit SDR-SDRAM Type FCRAM

Flash memory/MCP

Part number	Description
MBM29DL400TC-55 MBM29DL400BC-55	4Mbit simultaneous Read/Write operation (SRW) Flash memory
MBM29DL400TC-70 MBM29DL400BC-70	
MBM29DL400TC-90 MBM29DL400BC-90	
S29GL032M90 S29GL032M10 S29GL032M11	32M/64M/128M/256Mbit page mod Flash memory
S29GL064M90 S29GL064M10 S29GL064M11	
S29GL128M90 S29GL128M10	
S29GL256M10 S29GL256M11	
MBM29BS32LF-18 MBM29BT32LF-18	32Mbit simultaneous Read/Write operation (SRW) burst mode Flash memory
MBM29BS32LF-25 MBM29BT32LF-25	
S29WS064N0L S29WS064N0P S29WS064N0S	64Mbit simultaneous Read/Write operation (SRW) burst mode Flash memory
S71WS256JD0BFW	3-Stacked MCP (Single 1.8 V)
S71WS512NE0BFW	4-Stacked MCP (Single 1.8 V)

FUJITSU Semicustom Products

Semicustom Products					Page No.
	Standard cell	CMOS	CS101 series	More than 91,000,000 (on-chip) gates with on-chip RAM, ROM, ADC/DAC	84
			CS91 series	More than 48,000,000 (on-chip) gates with on-chip RAM, ROM, Multipliers, ADC/DAC	85
			CS86 series	More than 40,000,000 (on-chip) gates with on-chip RAM, ROM, FIFO, Delay Line, ADC/DAC	86
			CS81 series	More than 40,000,000 (on-chip) gates, 11 ps/gate with on-chip RAM, ROM, Multipliers, ADC/DAC	87
			CS71 series	More than 10,000,000 gates (on chip), 29 ps/gate with on-chip RAM, ROM, Multipliers, ADC/DAC	88
			CS66 series	More than 1,700,000 (on-chip) gates, 98 ps/gate with on-chip RAM, ROM, Multipliers, ADC/DAC	89
	Macro-embedded type cell arrays	CMOS	CE81 series	Maximum of 34,000,000 (on chip) gates, 12 ps/gate with on-chip RAM, ROM, Multipliers, ADC/DAC	91
			CE77 series	Maximum of 10,000,000 (on chip) gates, 33 ps/gate with on-chip RAM, ROM, FIFO, Delay Line	92
			CE71 series	Maximum of 8,096,000 (on chip) gates, 29 ps/gate with on-chip RAM, ROM, Multipliers, ADC/DAC	94
			CE66 series	Maximum of 1,138,000 (on-chip) gates, 98 ps/gate with on-chip RAM, ROM, Multipliers, ADC/DAC.	96
			CE61 series	Maximum of 2,025,000 (on chip) gates, 85 ps/gate with on-chip RAM/ROM, Multipliers, ADC/DAC	98
			CE46 series	Maximum of 198,000 (on chip) gates, 300 ps/gate with on-chip RAM, ROM, FIFO	101
	Gate arrays	Sea-of-Gate CMOS	CG61 series	Maximum of 1,568,000 (on chip) gates, 85 ps/gate with on-chip RAM, Analog PLL embedment is possible in some frames	102
			CG47 series	Maximum of 55,000 (on chip) gates, 300 ps/gate with on-chip RAM, FIFO	104
			CG46 series	Maximum of 198,000 (on chip) gates, 300 ps/gate with on-chip RAM, FIFO	105
	AccelArray ™	CMOS	CA91 series	More than 6,000,000 (on-chip) gates, 4,550,000bit SRAM, 3.125 Gbps high-speeds interface macros	106
	IF PLL Frequency Synthesizer	CMOS	MB15C100 series	For IF PLL frequency synthesizers Operating frequency: Up to 500 MHz	107

AccelArray is a trademark of Fujitsu Limited, Japan.

CS101 Series

Features

Optimum gate count	: Maximum of 91,000,000 gates
Technology	: 90 nm Si-gate CMOS
	6- to 10-metal layers. Low-k (low permittivity) inter-layer insulation film material is used for all layers.
	3 types of transistors (low leak, standard, high speed) can be mixed on a chip. The design rules comply with industry standard processes.
Supply voltage	: +1.2 V ±0.1 V (normal)
Junction temperature range	: -40 to +125 °C (normal)
Gate delay time	: tpd = 12 ps (1.2 V, Inverter, F/O = 1)
Gate power consumption	: Pd = 2.7 nW/MHz/BC (1.2 V, Inverter, F/O = 1)

Reduced chip sized realized by I/O with pad.
Supports a wide range of cell sets (from low power versions to high speed versions)
Compliance with industry standard design rules enables non-Fujitsu commercial macros to be easily incorporated.
Compiled cells (RAM/ROM and others)
Ultra high-speed interface macro (up to 10 GBps)
Special interfaces (LVDS, SSTL_2 and others)
Supports use of industry standard libraries (. LIB)
Uses industry standard tools and supports the optimum tools for the application.
High reliability design estimation in the early stage of physical design realized by physical prototyping tool.
Layout synthesis with optimized timing realized by physical synthesis tools.
Hierarchical design environment for supporting large-scale circuits.
High accuracy design environment considering drop in power supply voltages, signal noise, delay penalty, and crosstalk.
I/O design environment (power line design, assignment and selection of I/Os, package selection) considering noise.
Support for static timing sign-off
Support for memory (RAM/ROM) BIST
Support for boundary SCAN
Support for LOGIC BIST
Support for transition delay test

Optimum of package lineup : TEBGA, FBGA, PBGA, FC-BGA

Note: Some items are in preparation.

CS91 Series

Features

Optimum gate count : Maximum of 48,000,000 gates
Technology : 0.11 µm Si-gate CMOS, 5- to 8-layer wiring (Copper is used as wire material) , Low-k Inter-layer material
(Inter-layer material that has low permittivity)
Support for 5 types of cell sets that differ in speed, integration, and power consumption.
These cell sets can be mixed on a chip.
Supply voltage : +1.2 V ±0.1 V (normal)
Junction temperature range : -40 to +125 °C
Gate delay time : tpd = 16 ps (1.2 V, Inverter, F/O = 1)
Gate power consumption : Pd = 6.6 nW/MHz (1.2 V, Inverter, F/O = 1)
Ultra high-speed interface macro (622 to 780 Mbps, 2.5 to 3.125 Gbps, 10 Gbps)
Special interfaces: P-CML, LVDS, PCI, USB, SSTL, HSTL, T-LVTTL, and others
Buffer cells for crystal oscillation circuits.
IP macros: CPU (ARM9, ARM7TDMI) , DSP, PCI, IEEE1394, USB, IrDA, PLL, ADC, DAC, and others
Compiled cells (RAM/ROM/multiplier and others)
Uses industry standard tools and supports the optimum tools for the application.
Short-term development using a physical prototyping tool.
Hierarchical design environment for supporting large-scale circuits.
Support for Signal Integrity, EMI noise reduction
Support for High resolution RC extraction base delay calcuration environment
Support for optimization environment of power supply wire
Support for static timing sign-off
Support for memory (RAM/ROM) BIST
Support for boundary SCAN
Support for LOGIC BIST
Support for transition delay test
A variety of package options : FC-BGA (Max. 2116 pin), EBGA, HQFP, FBGA and others

Note: Some items are in preparation.

CS86 Series

Features

Optimum gate count	: Maximum of 40,000,000 gates		
Technology	: 0.18 µm Si-gate CMOS, 4- to 6-layer wiring		
	Support for three types of internal cell sets (ultra high-speed, standard, low-leak)		
	Capable of integrating a mixture of standard transistor cell and ultra high-speed process/cell, and mixture of standard transistor cell and low leak process/cell on a single chip		
Supply voltage	: +1.8 V ±0.15V (normal) to +1.1V ±0.1V		
Gate delay time	: tpd = 88 ps	(standard	: 1.8 V, 2NAND, F/O = 2, standard load)
	tpd = 70 ps	(ultra high-speed	: 1.8 V, 2NAND, F/O = 2, standard load)
	tpd = 136 ps	(low-leak	: 1.8 V, 2NAND, F/O = 2, standard load)
Leakage Current	: 0.023 nW	(standard	: 1.8 V, 2NAND, F/O = 0, no load)
	3.922 nW	(ultra high-speed	: 1.8 V, 2NAND, F/O = 0, no load)
	0.0067 nW	(low-leak	: 1.8 V, 2NAND, F/O = 0, no load)
Gate power consumption	: 40.1 nW/MHz	(standard	: 1.8 V, 2NAND, F/O = 1, 4Grid)
	42.7 nW/MHz	(ultra high-speed	: 1.8 V, 2NAND, F/O = 1, 4Grid)
	38.3 nW/MHz	(low-leak	: 1.8 V, 2NAND, F/O = 1, 4Grid)
Junction temperature range	: -40 to +125 °C		

Output buffer cells with noise reduction circuits
Inputs with on-chip input pull-up/pull-down resistors and bidirectional buffer cells.
Buffer cells for crystal oscillation circuits.

Special interfaces	: SSTL2, PCI, P-CML, T-LVTTL, USB2.0, IEEE1394, and others
IP macros	: CPU (FR-V, ARM9,and others), DSP, PCI, IEEE1394, USB2.0, IrDA, PLL, ADC, DAC, and others

Compiled cells (RAM/ROM/FIFO/Delay line, and others)
Configurable internal bus circuits
Advanced for hardware/software co-design environment
Short-term development using a physical synthesis tool
Low-power dissipation using a low power synthesis tool
Short-term development using a timing driven layout tool
Hierarchical design environment for supporting large-scale circuits
Supprt for signal Integrity
Suppor for memory (RAM, ROM) SCAN
Suppor for memory (RAM) BIST
Suppor for boundary SCAN
Support for path delay test
A variety of package options (QFP, TQFP, LQFP, HQFP, PBGA, FBGA, FLGA, EBGA)

Note: Some items are in preparation.

Packages

The table below lists the available package types.

Type	Pin Count	Material
QFP	176, 208, 240	Plastics
TQFP	100, 120	Plastics
LQFP	144, 176, 208, 256	Plastics
HQFP	208, 240, 256, 304	Plastics
PBGA	256, 352, 420	Plastics
FBGA	112, 144, 168, 176, 192, 224, 272, 288, 240, 304, 368	Plastics
FLGA	144, 176, 208, 224, 288	Plastics
EBGA	660	Plastics

Note: This list contains packages under planning. Contact Fujitsu for the availability.

CS81 Series

Features
Optimum gate count : Maximum of 40,000,000 gates
Technology : 0.18 µm Si-gate CMOS, 3- to 6-layer wiring
Capable of integrating a mixture of high-speed processes and cells on a single chip
Supply voltage : +1.8 V ±0.15V (normal) to +1.1V ±0.1V
Gate delay time : tpd = 11 ps (1.8 V, Inverter, F/O = 1)
Gate power consumption : 5nW/MHz/BC (1.1V, 2NAND, F/O = 1)
Junction temperature range : -40 to +125 °C
Ultra high-speed interface macro (622 to 780 Mbps, 2.5 to 3.125 Gbps)
Output buffer cells with noise reduction circuits
Inputs with on-chip input pull-up/pull-down resistors (33 kΩ typical) and bidirectional buffer cells.
Buffer cells for crystal oscillation circuits.
Special interfaces: P-CML, LVDS, PCI, AGP, USB, SDRAM-I/F, SSTL, and others
IP macros: CPU, DSP, PCI, IEEE1394, USB, IrDA, PLL, ADC, DAC, and others
Compiled cells (RAM/ROM/multiplier, and others)
Configurable internal bus circuits
Advanced for hardware/software co-design environment
Short-term development using a timing driven layout tool
Support for static timing sign-off
Dramatically reducing the time for generating test vectors for timing verification and the simulation time
Hierarchical design environment for supporting large-scale circuits
Simulation (before layout) considering the input through rate and high resolution RC extraction base delay calculation (after layout), supporting development with minimized timing trouble after trial manufacture.
Supprt for signal Integrity, EMI noise reduction
Suppor for memory (RAM, ROM) SCAN
Suppor for memory (RAM) BIST
Suppor for boundary SCAN
Support for At-Speed test on internal circuits
Support for path delay test
Support for transition delay test
A variety of package options (TQFP, HQFP, EBGA, FBGA, TAB-BGA, FC-BGA, LQFP)

Note: Some items are in preparation.

Packages

The table below lists the available package types.

Type	Pin Count	Material
TAB-BGA	304, 352, 480 560, 660, 720	Plastics
EBGA	576, 660, 672	Plastics
HQFP	208, 240, 256, 304	Plastics
TQFP	100, 120	Plastics
LQFP	144, 176, 208	Plastics
FBGA	288	Plastics
FC-BGA	1089, 1225, 1369, 1681, 1849, 2116	Plastics, Ceramic

Note: This list contains packages under planning. Contact Fujitsu for the availability.

CS71 Series

Features

Optimum gate count : Maximum of 10,000,000 gates
Technology : 0.25 µm Si-gate CMOS, 3- to 4-layer metal wiring
Supply voltage : +2.5 V ± 0.2 V (normal) to +1.5 V ± 0.1 V
(5 V TTL interface is available if 5 V tolerant I/O is adopted. some frames are under development.)
Gate delay time : t_{pd} = 32 ps (Inverter cell high speed type, F/O = 1, No load)
Gate power consumption : 0.044 µW/MHz (F/O = 1, no load)
Junction temperature range : -40 to +125 °C
High-load driving capability : I_{OL} = 2 mA/4 mA/8 mA/12 mA mixable.

Output buffer cells with noise reduction circuits
Inputs with on-chip input pull-up/pull-down resistors (25 kΩ typical) and bidirectional buffer cells.
Buffer cells for crystal oscillation circuits.
Special interfaces (P-CML, LVDS, SDRAM-I/F, SSTL, and others)
IP macros (SPARClite, FR40, F²MC16LX, PCI, IEEE1394, USB, IrDA, PLL, ADC/DAC, and others)
Compiled cells (RAM/ROM/multipliers, and others)
Configurable internal bus circuits
Advanced for hardware/software co-design environment
Linking floor plan tools and logic synthesis tools allows automatic optimization of the circuits using the floor plan information. The Clock Driven Design Method (Cadence "CT-Gen") clock tree synthesis tools using the floor plan information are also available. Using the floor plan information in the pre-layout stage would eliminate the problems of setup after layout or timing problems for hold, significantly reducing the time to market.
Supports the static timing sign off using the Synopsys CAD tool PrimeTime. This contributes to the considerable reduction of time required for test vector creation for timing verification and the simulation time.
Simulation (before layout) considering the input through rate and detailed RC delay calculation (after layout), supporting development with minimized timing trouble after trial manufacture.
Support for memory (RAM, ROM) SCAN
Support for memory (RAM) BIST
Support for boundary SCAN
A variety of package options (SQFP, LQFP, HQFP, PBGA, EBGA, TAB-BGA, FBGA)

Note: Some items are in preparation.

Packages

The table below lists the available package types.

Type	Pin count	Material
SQFP	176, 208, 240	Plastics
LQFP	144, 176, 208, 256	Plastics
HQFP	208, 240, 256, 304	Plastics
PBGA	256, 352, 420	Plastics
EBGA	352, 420, 576, 660, 672	Plastics
TAB-BGA	304, 352, 480, 560, 660, 720	Plastics
FBGA	144, 176, 224, 288	Plastics

Note: This list contains packages under planning. Contact Fujitsu for the availability.

CS66 Series

Features

Optimum gate count	: Maximum of 1,700,000 gates
Technology	: 0.35 µm Si-gate, 3- to 4-layer metal wiring
Supply voltage	: +3.3 V ± 0.3 V (normal) to +2.0 V ± 0.1 V +5.0 V ± 10% (only for external interface; when internal requirements is 3.3 V) +3.3 V ± 10% (only for external interface; when internal requirements is 3.3 to 2.0 V)
Gate delay time	: t_{pd} = 91 ps (high-speed type, F/O = 2, standard load)
Gate power consumption	: 0.29 µW/MHz (F/O = 2, standard load)
Junction temperature range	: -40 to +125°C
High-load driving capability	: I_{OL} = 2 mA/4mA/8mA/12mA/24mA mixable.

Output buffer cells with noise reduction circuits
On-chip input pull-up/pull-down resistors (50 kΩ typical)
Buffer cells for crystal oscillation circuits.
Configurable internal bus circuits
Highly integrated RAM/ROM/multipliers mountable; arbitrary words/bits configurable.
Clock skew layout design method (Cadence "CT-Gen") based on the floor plan information minimizes post-layout circuit modification, reducing turnaround time for development.
Simulation (before layout) considering the input through rate and detailed RC delay calculation (after layout), supporting development with minimized timing trouble after trial manufacture.
Special interface (T-LVTTL and SDRAM-I/F, and others)
Analog PLL
Analog circuits (ADC, DAC, OPAMP and others)
Macros for system ASICs (CPU core, CPU peripheral, operation macro, and others)
Support for DFF scan test with MUX
Support for memory (RAM/ROM) scan
Support for memory (RAM) BIST
Support for boundary SCAN

Note: Some items are in preparation.

Number of gates used in each package

The table below lists the available package types and athe reference number of gates used.

CS66 (P-frame)

Package and pin count		0 2000K 4000K 6000K 8000K 10000K 12000K 14000K 16000K
TQFP	100	1579K
LQFP	100	1579K
	144	1579K
	176	1579K
	208	1305K
QFP	120	1579K
	144	1579K
	160	1579K
	176	1579K
	208	1579K
	240	1579K
	256	1579K
HQFP	208	1579K
	240	1579K
	256	1579K
	304	1579K
PBGA	256	1579K
	352	1579K
FBGA	112	639K
	144	639K
	168	835K
	176	1305K
	192	1579K
	224	1579K
	288	1579K

Note: This list contains packages under planning.

Standard Cell

CS66 (S-frame)

Package and pin count		0 100K 200K 300K 400K 500K 600K 700K 800K 900K
TQFP	100	158K
LQFP	100	158K
	144	158K
	208	433K
QFP	120	158K
	144	158K
	160	228K
	176	228K
	208	358K
	240	545K
HQFP	208	358K
	240	545K
	256	545K
PBGA	256	545K
	352	807K
FBGA	112	192K
	144	228K
	168	433K
	176	228K
	192	289K
	224	433K
	288	807K

Note: This list contains packages under planning.

CE81 Series

Features

High Integration : Maximum of 34,000,000 BCs
Technology : 0.18 µm Si-gate CMOS, 4- to 5-layer wiring
Supply voltage : +1.8 V ±0.15 V (normal) to +1.1 V ±0.1 V
Gate delay time : tpd = 12 ps (1.8V, Inverter, F/O = 1)
Gate power consumption : 8nW/MHz/BC (1.1V, 2NAND, F/O = 1)
Junction temperature range : -40 to +125 °C
Output buffer cells with noise reduction circuits
Inputs with on-chip input pull-up/pull-down resistors (33 kΩ typical) and bidirectional buffer cells.
Buffer cells for crystal oscillation circuits.
Special interfaces: P-CML, LVDS, PCI, AGP, USB, SDRAM-I/F, SSTL, and others
IP macros: CPU, DSP, PCI, IEEE1394, USB, IrDA, PLL, ADC, DAC, and others
Compiled cells (RAM/ROM/multipliers, and others)
Configurable internal bus circuits
Advanced for hardware/software co-design environment
Short-term development using a timing driven layout tool
Support for static timing sign-off
Dramatically reducing the time for generating test vectors for timing verification and the simulation time.
Hierarchical design environment for supporting large-scale circuits
Support for optimization environment of power supply wire
Simulation (before layout) considering of the input through rate and high resolution RC extraction base delay calculation (after layout), supporting development with minimized timing trouble after trial manufacture.
Support for Signal Integrity
Support for memory (RAM, ROM) SCAN
Support for memory (RAM) BIST
Support for boundary SCAN
Support for At-Speed test on internal circuits
Support for path delay test
Support for transition delay test
A variety of package options (TQFP, HQFP, EBGA, FBGA, TAB-BGA, LQFP)
Note: Some items are in preparation.

Number of gates used in package

The table below lists the available package types and athe reference number of gates used.

Package and pin count		0 2000K 4000K 6000K 8000K 10000K 12000K 14000K 16000K
TAB-BGA	304	891K
	352	1254K
	480	1905K
	560	2689K
	660	3609K
	720	9129K
EBGA	576	5982K
	660	9805K
	672	7952K
HQFP	208	1098K
	240	2085K
	256	3764K
	304	15158K
	304	4712K
TQFP	100	514K
	120	514K
LQFP	144	722K
	176	722K
	208	1098K
FBGA	288	4712K

Note: This list contains packages under planning.

CE77 Series

Features

High integration	: Maximum of 10,000,000 BCs
Technology	: 0.25 µm Si-gate CMOS, 3- to 4-layer wiring
Supply voltage	: +2.5 V ± 0.2 V (normal) to +1.5 V ± 0.1 V
Junction temperature range	: -40 to +125° C
Gate delay time	: t_{pd} = 33 ps (2.5 V, Inverter, F/O = 1, No load)
Gate power consumption	: 0.02 µW/MHz (1.5 V, Inverter, F/O = 1, No load)
High-load driving capability	: I_{OL} = 2mA/4mA/8mA/12mA mixable.

Output buffer cells with noise reduction circuits
Inputs with on-chip input pull-up/pull-down resistors (25 kΩ typical) and bidirectional buffer cells.
Buffer cells for crystal oscillation circuits.
Special interfaces (P-CML, LVDS, T-LVTTL, SSTL, PCI, USB, GTL+, and others)
IP macros (CPU, PCI, USB, IrDA, PLL, DAC, ADC, and others)
Compiled cells (RAM/ROM/FIFO/DelayLine, and others)
Configurable internal bus circuits
Advanced for hardware/software co-design environment
Short-term development using a timing driven layout tool
Hierarchical design environment for supporting large-scale circuits
Support for static timing sign-off
Dramatically reducing the time for generating test vectors for timing verification and the simulation time.
Simulation (before layout) considering the input through rate and detailed RC delay calculation (after layout), supporting development with minimized timing trouble after trial manufacture.
Support for memory (RAM, ROM) SCAN
Support for memory (RAM) BIST
Support for boundary SCAN
Support for path delay test
A variety of package options (SQFP, LQFP, HQFP, FBGA, PBGA)

Note: Some items are in preparation.

Number of gates used in each package

The table below lists the available package types and athe reference number of gates used.
CE77 (V-Frame)

Package and pin count		0 1000k 2000k 3000k 4000k 5000k 6000k 7000k 8000k 9000k	Material
SQFP	176	274k	P
	208	803k	P
	240	965k	P
HQFP	208	1776k	P
	240	2276k	P
	256	1776k	P
	304	7128k	P
PBGA	256	618k	P

P: Plastic
Note: This list contains packages under planning.

CE77 (T-Frame)

Package and pin count		0 500K 1000K 1500K 2000K 2500K 3000K 3500K 4000K 4500K 5000K	Material
LQFP	144	976 K	P
	176	744 K	P
	208	1375 K	P
	256	1841 K	P
HQFP	208	1375 K	P
	240	1609 K	P
	256	2109 K	P
	304	4538 K	P
FBGA	144	461 K	P
	176	646 K	P
	224	1375 K	P
	288	2109 K	P
PBGA	256	1841 K	P
	352	2678 K	P
	420	3789 K	P

P: Plastic
Note: This list contains packages under planning.

CE71 Series

Features

High integration	: Maximum of 8,000,000 BCs
Technology	: 0.25 µm Si-gate CMOS, 3- to 4-layer metal wiring
Supply voltage	: +2.5 V ± 0.2 V (normal) to +1.5 V ± 0.1 V (5 V TTL interface is available if 5 V tolerant I/O is adopted. Some frames are under development.)
Gate delay time	: t_{pd} = 29 ps (2.5 V, Inverter, F/O = 1, No load)
Gate power consumption	: 0.060 µW/MHz (F/O = 1, No load)
Junction temperature range	: -40 to +125°C
High-load driving capability	: I_{OL} = 2 mA/4 mA/8 mA/12 mA mixable.

Output buffer cells with noise reduction circuits
Inputs with on-chip input pull-up/pull-down resistors (25 kΩ typical) and bidirectional buffer cells.
Buffer cells for crystal oscillation circuits.
Special interfaces (P-CML, LVDS, SDRAM-I/F, SSTL, and others)
IP macros (SPARClite, FR40, F²MC16LX, PCI, IEEE1394, USB, IrDA, PLL, ADC/DAC, and others)
Compiled cells (RAM/ROM/multipliers, and others)
Configurable internal bus circuits
Advanced for hardware/software co-design environment
Linking floor plan tools and logic synthesis tools allows automatic optimization of the circuits using the floor plan information. The Clock Driven Design Method (CDDM) clock tree synthesis tools using the floor plan information are also available. Using the floor plan information in the pre-layout stage would eliminate the problems of setup after layout or timing problems for hold, significantly reducing the time to market.
Supports the static timing sign off using the Synopsys CAD tool Prime Time. This contributes to the considerable reduction of time required for test vector creation for timing verification and the simulation time.
Simulation (before layout) considering the input through rate and detailed RC delay calculation (after layout), supporting development with minimized timing trouble after trial manufacture.
Suppor for memory (RAM, ROM) SCAN
Support for memory (RAM) BIST
Support for boundary SCAN
A variety of package options (SQFP, LQFP, HQFP, PBGA, EBGA, TAB-BGA, FBGA)

Note: Some items are in preparation.

Number of gates used in each package

The table below lists the available package types and athe reference number of gates used.
CE71 (J-Frame)

Package and pin count		0 — 1000 K — 2000 K — 3000 K — 4000 K — 5000 K	Material
SQFP	176	203 K	P
	208	592 K	P
	240	714 K	P
HQFP	208	1313 K	P
	240	1681 K	P
	256	1313 K	P
	304	5345 K	P
PBGA	256	457 K	P
EBGA	352	991 K	P
	420	1313 K	P
	576	1986 K	P
	660	5345 K	P
	672	2673 K	P

P: Plastic
Note: This list contains packages under planning.

CE71 (L-Frame)

Package and pin count		0 1000 K 2000 K 3000 K 4000 K 5000 K	Material
TAB-BGA	304	310 K	P
	352	672 K	P
	480	672 K	P
	560	2279 K	P
	660	1284 K	P
	720	3278 K	P

Note: This list contains packages under planning.
P: Plastic

CE71 (T-Frame)

Package and pin count		0 1000 K 2000 K 3000 K 4000 K 5000 K	Material
LQFP	144	341 K	P
	176	477 K	P
	208	1014 K	P
	256	1358 K	P
HQFP	208	1014 K	P
	240	1188 K	P
	256	1559 K	P
	304	3349 K	P
FBGA	144	341 K	P
	176	477 K	P
	224	1014 K	P
	288	1559 K	P
PBGA	256	1358 K	P
	352	1976 K	P
	420	2794 K	P

Note: This list contains packages under planning.
P: Plastic

CE66 Series

Features

High integration	: Maximum of 1,138,000 BCs
Technology	: 0.35 μm Si-gate, 3- to 4-layer metal wiring
Supply voltage	: +3.3 V ± 0.3 V (normal) to +2.0 V ± 0.1 V +5.0 V ± 10% (only for external interface; when internal requirements is 3.3 V) +3.3 V ± 10% (only for external interface; when internal requirements is 3.3 to 2.0 V)
Gate delay time	: t_{pd} = 98 ps (high-speed type, F/O = 2, standard load)
Gate power consumption	: 0.29 μW/MHz (F/O = 2, standard load)
Junction temperature range	: - 40 to 125° C
High-load driving capability	: I_{OL} = 2 mA/4mA/8mA/12mA/24mA mixable.

Output buffer cells with noise reduction circuits
On-chip input pull-up/pull-down resistors (50 kΩ typical)
Buffer cells dedicated to crystal oscillator
Configurable internal bus circuits
Highly integrated RAM/ROM/multipliers mountable; arbitrary words/bits configurable.
Clock skew layout design method (CDDM) based on the floor plan information minimizes post-layout circuit modification, reducing turnaround time for development.
Simulation (before layout) considering the input through rate and detailed RC delay calculation (after layout), supporting development with minimized timing trouble after trial manufacture.
Special interfaces (T-LVTTL and SDRAM-I/F, and others)
Analog PLL
Analog circuits (ADC, DAC, OPAMP and others)
Macros for system ASICs (CPU core, CPU peripheral, operational macros, and others)
Support for DFF scan test with MUX
Support for memory (RAM/ROM) SCAN
Support for memory (RAM) BIST
Support for boundary SCAN

Note: Some items are in preparation.

Number of gates used in each package

The table below lists the available package types and athe reference number of gates used.

CE66 (P-frame)

Package and pin count		0 100K 200K 300K 400K 500K 600K 700K 800K 900K 1000K 1100K 1200K
TQFP	100	1138K
LQFP	100	1138K
	144	1138K
	176	1138K
	208	939K
QFP	120	1138K
	144	1138K
	160	1138K
	176	1138K
	208	1138K
	240	1138K
	256	1138K
HQFP	208	1138K
	240	1138K
	256	1138K
	304	1138K
PBGA	256	1138K
	352	1138K
FBGA	112	459K
	144	459K
	168	601K
	176	939K
	192	1138K
	224	1138K
	288	1138K

Note: This list contains packages under planning.

CE66 (S-frame)

Package and pin count		0 50K 100K 150K 200K 250K 300K 350K 400K 450K 500K 550K 600K
TQFP	100	112K
LQFP	100	112K
	144	112K
	208	311K
QFP	120	112K
	144	112K
	160	163K
	176	163K
	208	256K
	240	390K
HQFP	208	256K
	240	390K
	256	390K
PBGA	256	390K
	352	579K
FBGA	112	136K
	144	163K
	168	311K
	176	163K
	192	206K
	224	311K
	288	579K

Note: This list contains packages under planning.

CE61 Series

Features

High Integration	: Maximum of 2,000,000 BCs
Technology	: 0. 35 µm Si-gate 3-layer metal wiring/4-layer metal wiring (There are restrictions applicable frames)
Basic circuit (basic cell)	: 2-input NAND/2-input NOR gates
Supply voltage	: +3.3 V ± 0.3 V (normal) to +2.0 V ± 0.1 V High voltage tolerant transistor for I/O; interface provided for 5 V devices (Also requiring a 5 V power supply for interface with 5 V devices)
Gate delay time	: High-speed type, t_{pd} = 85 ps (2-input NAND, F/O = 2, standard load)
Junction temperature range	: 0 to +100° C
High-load driving capability	: I_{OL} = 2 mA/4 mA/8 mA/12 mA/24 mA mixable.
Power consumption	: Reduced to 50% to 20% (over the Fujitsu CE51 Series)

Output buffer cells with noise reduction circuits
On-chip input pull-up/pull-down resistors (Typ. 50kΩ)
Buffer cells for crystal oscillation circuits.
Configurable internal bus circuits
Super high-integration RAM and ROM available. Compilable bit/word configuration
Clock skew reduction layout design technique (CDDM) employed to minimize circuit modification after layout, reducing TAT
Simulation (before layout) considering the input through rate and detailed RC delay calculation (after layout), supporting development with minimized timing trouble after trial manufacture.
Supporting high speed interfaces [P-CML (200 MHz transmission), LVDS (250 MHz transmission), and SDRAM I/F, PCI,5 V tolerant, USB, IEEE 1284]
PLL circuits
Analog circuits (ADC, DAC)
Macros for system ASICs (CPU core and CPU peripheral and operational macros, and others)
Supporting tests (for function/DC) using DFF scan with MUX
Supporting the test for RAM BIST, RAM SCAN and ROM SCAN
Supporting the Boundary SCAN
Now under preparation on for a narrow-pitch pad technology and high-pin count BGA packages to be added to the current lineup
Variety of package options to optimize any gate size

Note: Some items are in preparation.

Number of gates used in each package)

The table below lists the available package types and athe reference number of gates used."

CE61 (F10 to F80)

Package and pin count		0 100K 200K 300K 400K 500K 600K 700K 800K 900K 1000K 1100K 1200K 1300K	Material
QFP	64	86K	P
	80	86K	P
	100	86K	P
	120	86K	P
	144	593K	P
	160	1317K	P
	160	981K	C
	176	593K	P
	176	1317K	C
	208	1317K	P
	208	1317K	C
	240	981K	P
	240	981K	C
	256	1317K	C
	256	593K	P
	304	1317K	C
LQFP	64	86K	P
	80	86K	P
	100	86K	P
HQFP	208	1317K	P
	240	981K	P
	256	1317K	P
	304	981K	P
BGA	256	593K	P
	352	981K	P
	420	981K	P
PGA	256	1317K	C
	299	1317K	C
	361	981K	C
	401	1317K	C

P : Plastic C : Ceramic

Note: This list contains packages under planning.

Macro-Embedded Type Cell Arrays

CE61 (E7 to E71)

Package and pin count		0 100K 200K 300K 400K 500K 600K 700K 800K 900K 1000K 1100K	Material
QFP	120	509K	P
	144	509K	P
	160	747K	P
	176	509K	P
	208	747K	P
	240	747K	P
	256	747K	P
LQFP	64	78K	P
	80	128K	P
	100	128K	P
HQFP	208	1029K	P
	240	1029K	P
	256	1029K	P
	304	1029K	P
BGA	256	391K	P
	352	391K	P
	420	509K	P
	576	747K	P
	672	1029K	P

P : Plastic
Note: This list contains packages under planning.

CE46 Series

Features

High integration	: Maximum of 198,000 BCs	
Technology	: 0.65 µm Si-gate CMOS, 2-layer metal wiring	
Basic circuit (Basic cell)	: 2-input NAND/2-input NOR gates	
Gate delay time	: Standard gate	tpd = 360 ps (2-input NAND, standard load, V_{DD} = 5 V)
		tpd = 520 ps (2-input NAND, standard load, V_{DD} = 3.3 V)
	Power gate	tdp = 300 ps (2-input NAND, standard load, V_{DD} = 5 V)
		tpd = 430 ps (2-input NAND, standard load, V_{DD} = 3.3 V)
Output driving capability	: I_{OL} = 2 mA/4 mA/6 mA/12 mA mixable (3.3 V output buffer)	
	I_{OL} = 3.2 mA/8 mA/12 mA/24 mA mixable (5.0 V output buffer)	
Supply voltage	: [Single power supply]	5 V ± 5% (normal), 3.3 V ± 0.3 V (optional)
	[Dual power supply]	Internal domain: 3.3 V ± 0.3 V, 5 V ± 5% (cannot be mixed)
	I/O: 3.3 V ± 0.3 V, 5 V ± 5% (mixable)	

Interface can be provided between the two power supplies.
Can be configured for 3 V systems or 5 V systems (mixable)
Using 3.3 V internal supply voltage allows low-power consumption
Detailed RC delay calculation minimized timing trouble after trial manufacture.
On-chip input pull-up/pull-down resistor
Output buffer cells with noise reduction circuits, buffer cells for crystal oscillation circuits
Internal bus circuit configurable
Standard cell macros: RAM, ROM, 1H delay line, FIFO memory
Using the clock skew reduction layout design method (CDDM) minimized the circuit modification after layout, reducing the time to market
Support for ATG (Automatic Test Generation) based on scan design
Support for HISCAN (automatic scan generation)
(Note that mixture of dual power supply and HISCAN is not allowed)
Simplified interface: CAD-to-CAD interface uses special language for logic data(FLDL) and test data(FTDL).
Integrated development tools

Number of gates used in each package

The table below lists the available package types and athe reference number of gates used.

Package and pin count		Number of gates used (BC): 0 10K 20K 30K 40K 50K 60K 70K 80K 90K 100K
SSOP	30	5K
LQFP	48	10K
	64	42K
	80	42K
	100	71K
	120	71K
	144	71K
	176	54K
	208	54K
TQFP	64	5K
	100	71K
QFP	44	5K
	64	71K
	80	71K
	100	71K
	120	89K
	144	89K
	160	89K
	176	89K
	208	89K
	240	89K
	256	89K

Note: This list contains packages under planning.

CG61 Series (Analog PLL embedment is possible in some frames)

Features

High Integration	: 1,560,000 BCs
Technology	: 0. 35 μm Si-gate CMOS, 3-layer metal wiring
Basic circuit (basic cell)	: 2-input NAND/2-input NOR gates
Supply voltage	: +3.3 V ± 0.3 V (normal) to +2.0 V ± 0.1 V (5 V TTL interface is possible when 5 V tolerant I/Os are used.)
Gate delay time	: t_{pd} = 85 ps (3.3 V, 2-input NAND, F/O = 2, standard load)
Gate power dissipation	: 0.24 μW/MHz (2.0 V, 2-input NAND, F/O = 2, standard load)
Junction temperature range	: 0 to +100 °C
High-load driving capability	: I_{OL} = 2 mA/4 mA/8 mA/12 mA/24 mA mixable

Output buffer cells with noise reduction circuits
On-chip input pull-up/pull-down resistors (Typ. 50 kΩ <at 3.3 V>)
Buffer cells for crystal oscillation circuits
Configurable internal bus circuits
Compiled RAM can be embedded. Compilable bit/word configuration
An analog PLL can be embedded in CG61P only.
Clock skew reduction layout design technique (CDDM) employed to minimize circuit modification after layout, reducing TAT
Simulation (before layout) considering the input through rate and detailed RC delay calculation (after layout), supporting development with minimized timing trouble after trial manufacture.
Supporting high speed interfaces (T-LVTTL, P-CML, LVDS, SDRAM I/F)
Supporting tests using DFF scan with MUX
Supporting the test for RAM BIST and RAM SCAN

Number of gates used in each package

The table below lists the available package types and athe reference number of gates used.

Package and pin count		0 100K 200K 300K 400K 500K 600K 700K 800K 900K	Material
LQFP	120	222K	P
	144	222K	P
QFP	120	395K	P
	144	395K	P
	160	580K	P
	176	395K	P
	208	580K	P
	240	580K	P
	256	580K	P
HQFP	208	802K	P
	240	580K	P
	256	580K	P
	304	802K	P
BGA	420	395K	P
	576	580K	P
	672	802K	P

P: plastic
Note: This list contains packages under planning.

CG 61P (The frame which can use Analog PLL))

Package and pin count		0 20K 40K 60K 80K 100K 120K 140K 160K 180K 200K	Material
LQFP	48	48K	P
	64	88K	P
	80	188K	P
	100	188K	P
	120	188K	P
	144	188K	P
	176	188K	P
	208	188K	P
QFP	240	188K	P
	256	188K	P
TQFP	120	188K	P
BCC	48	88K	P
	64	88K	P

P: plastic
Note: This list contains packages under planning.

CG47 Series

Features

High integration : Maximum 55,000 BCs (on chip)
Technology : 0.65 µm Si-gate CMOS, 2-layer metal wiring
Gate delay time : 300ps (power type 2-input NAND, standard load)
Supply voltage : [Single power supply] +5 V ± 5%(normal), +3.3 V ± 0.3 V (normal)
[Dual power supply] Internal domain: +3.3 V ± 0.3 V, +5 V ± 5% (cannot be mixed)
I/O: +3.3 V ± 0.3 V, +5 V ± 5% (can be mixed)

Interface enabled between dual power sources
Low power consumption enabled by operating internal supply voltage at 3.3V.
Delay time estimation by detailed time equations
Detailed time equations can be used for the estimation of delay time closer to that of actual devices.
Buffer cells for crystal oscillations circuits
Supports separate low frequency (32 kHz), and high frequency (1 to 40MHz) buffers, and oscillator stop function.
Supporting output open drain cell and input fail safe cells
Compiled cells include single port RAM, dual port RAM, and FIFO memory.
Note: The type of the RAM that can be used is specified depending on the internal power supply when the RAM is a single-port RAM.
HISCAN (scan circuit automatic generation function)
HISCAN is supported with single power supply, but dual power supply specifications and HISCAN are mutually exclusive.
Simple interface
CAD-to-CAD interface uses special language for logic data (FLDL) and test data (FTDL).
Integrated development tools

Number of gates used in each package

The table below lists the available package types and athe reference number of gates used.

Package and pin count		0 5K 10K 15K 20K 25K 30K 35K 40K 45K 50K
SSOP	30	2K
LQFP	48	11K
	64	21K
	80	33K
	100	33K
	120	33K
	144	33K
	176	33K
	208	33K
QFP	64	21K
	80	21K
	100	21K
	120	21K
	240	33K
TQFP	100	33K
BCC	48	21K
	64	31K
	80	31K

Note: This list contains packages under planning.

CG46 Series

Features

High integration	: Maximum 198,084 BCs (on chip)
Technology	: 0.65 µm Si-gate CMOS, 2-layer metal wiring
Basic circuit (basic cell)	: 2-input NAND/2-input NOR gates
Input level	: TTL/CMOS level mixable
Supply voltage	: +5 V ± 5% (normal) +3.3 V ± 0.3 V (optional)
Gate delay time	: Standard gate tpd = 360 ps (2-input NAND, standard load) Power gate tpd = 300 ps (2-input NAND, standard load)
Operating temperature	: 0 to +70° C
High-load driving capability	: I_{OL} = 3.2 mA/8 mA/12 mA/24 mA mixable

Output buffer cells with noise reduction circuits
On-chip input pull-up/pull-down resistors (Typ. 50 kΩ)
Buffer cells for crystal oscillations circuits
Configurable internal bus circuits
RAM and FIFO memory allowing arbitrary bit/word configuration
Clock skew reduction layout design technique (CDDM) employed to minimize circuit modification after layout, reducing the period of time for development
Delailed RC delay calculation minimized timing trouble after trial manufacture.
Support for ATG (Automatic Test Generation) based on scan design
Support for HISCAN (automatic scan generation)
Simplified interface: CAD-to-CAD interface uses special language for logic data (FLDL) and test data (FTDL) .
Integrated development tools

Number of gates used in each package

The table below lists the available package types and the reference number of gates used.

Package and pin count		Number of gates used (BC): 0 10K 20K 30K 40K 50K 60K 70K 80K 90K 100K
SSOP	30	5K
LQFP	48	10K
	64	42K
	80	42K
	100	65K
	120	65K
	144	65K
	176	50K
	208	50K
TQFP	64	5K
	100	65K
QFP	44	5K
	64	65K
	80	65K
	100	65K
	120	89K
	144	89K
	160	89K
	176	89K
	208	89K
	240	89K
	256	89K

Note: This list contains packages under planning.

AccelArray ™

CA91 Series

Features

Optimum gate Count : Maximum of 6,000,000 gates
Technology : 0.11 µm Si-gate CMOS, 6- to 7-metal layers (Copper is used as wire material),
Low-k inter-layer material (inter-layer material that has low permittivity) ,area bump.
Supply voltage :1.2 V ± 0.1 V/2.5 V ± 0.2 V
(Dual power supply. Needs 1.5 V power supply during using HTSL.)
Junction temperature range : -40 to +125 °C
Maximum operating frequency : 333 MHz (internal circuit)
High-speed, large scale ASIC produced in short development time :TAT = One third compared with Standard Cell ASIC (target value) .
Higher precision of layaout/timing estimation achieved by introduction of physical synthesis tools (Amplify® AccelArray™).
Uses an architecture that simplifies physical design tasks.
Pre-designed common masters with IR-drop free.
Pre-designed test circuit insertion to reduce test synthesis tasks.
Uses a dedicated timing-driven layout tool to reduce development time.
Support for Signal Integrity (Verification is unnecessary for global clock trees.)
Internal cells support high-speed operation
High-speed interface/macro (200 Mbps/400 Mbps DDR interface, 2.5 Gbps PCI-Express, 3.125 Gbps XAUI, etc.)
Special interfaces : P-CML, LVDS, PCI, HSTL, SSTL-2, etc.
IP macros : PLL, SRAM (maximum of 4,550,000bits) , ARM9
8channel clock supply system incorporating a PLL.
Support for Memory-BIST/Bounday-SCAN
Package : FC-BGA (729 pin to 1681 pin)
Note : Some items are in preparation

MB15C100 Series

Features

n (constant) in the divide-by-n counter can be any integer by customizing mask in accordance with applications.
Fixed value of n allows the elimination of external setting of values.
Low supply current: 1.2 mA (Vcc = 3 V, 300 MHz in looking state)
Allows versatile selection of charge pumps to meet wide applications (high-speed sync charge pump, output current ± 6 mA, low sensitivity charge pump, output current ±1.5 mA)
Mountable on super-miniature package
Time-to-market 4 weeks (normal)

Product line-up

Part number	Vcc	Icc	Operating Maximum frequency	Prescaler divide ratio	Comparison main counter divide ratio (N)	Swallow counter divide ratio (A)	Reference counter divide ratio (R)
MB15C100	2.4 to 3.6 V	1.2 mA*1	380MHz*2 (2.4 to 3.0V) 300MHz*2 (2.4 to 3.6V) 500MHz*3 (2.4 to 3.6V)	8/9, 16/17 or 32/33	Any value between divide-by-5 and divide-by-4095	Any value between divide-by-0 and divide-by-31	Any value between divide-by-5 and divide-by-4095

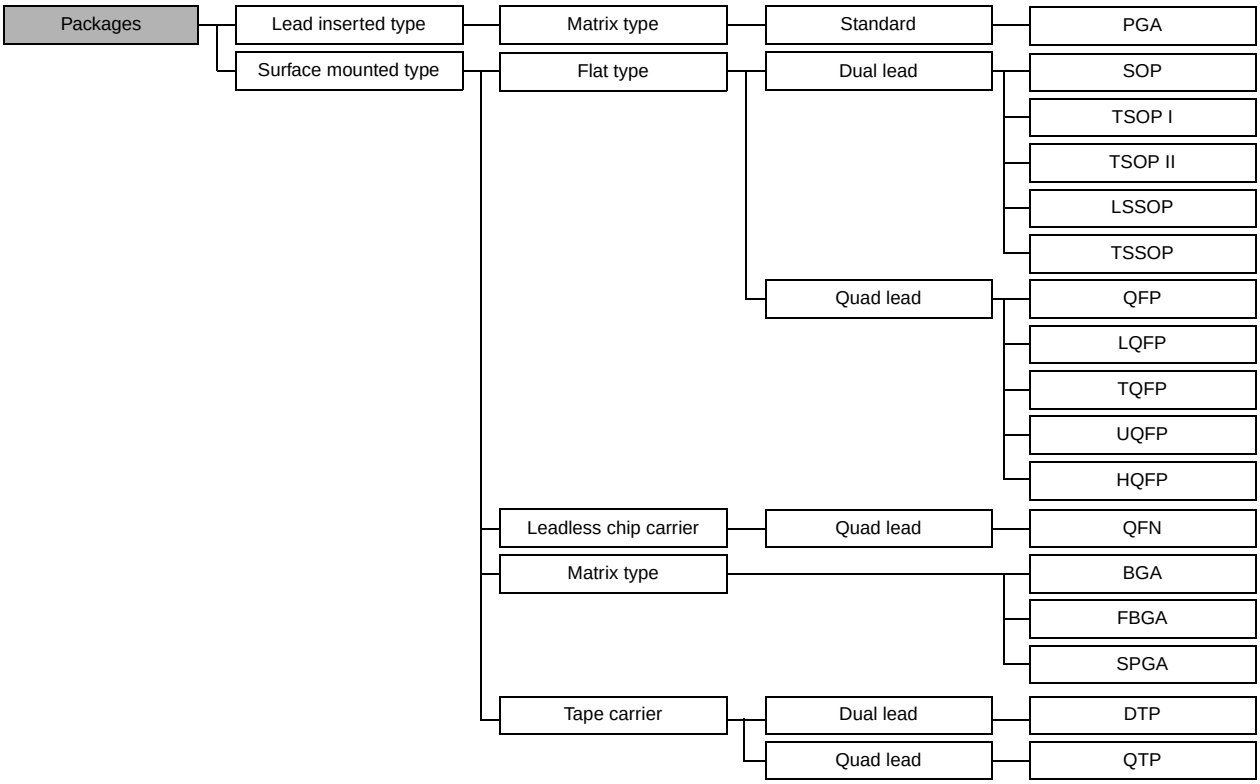
*1: 300 MHz in looking state, Vcc = 3 V
*2: Input sensitivity: -10 to +2 dBm
*3: Input sensitivity: -5 to +2 dBm

Package

MB15C100 series: SSOP-8, BCC-16 (S-Type)

■ Package Line-up

The packages are classified as follows, according to form, material, and the mounting methods for which they are suited.



Package Line-up

Name of package	Description	Lead pitch (mm)
PGA	Pin Grid Array Package	1.27/2.54
SOP	Small Outline Package (straight lead) Small Outline L-Leaded Package	1.27
SOL*2	Small Outline L-Leaded Package (JEDEC*1)	1.27
SSOP	Shrink Small Outline L-Leaded Package	0.65/0.80/1.00
TSOP (I)	Thin Small Outline L-Leaded Package (I)	0.50/0.55/0.60
TSOP (II)	Thin Small Outline L-Leaded Package (II)	0.50/0.80/1.00/1.27
SON	Small Outline Non-Leaded Package	0.50/1.00
QFP	Quad Flat Package (straight lead) Quad Flat L-Leaded Package	0.40/0.50/0.65/0.80/1.00
LQFP*2	Low-Profile Quad Flat L-Leaded Package	0.40/0.50/0.65/0.80
TQFP	Thin Quad Flat L-Leaded Package	0.40/0.50
HQFP	QFP with Heat Sink	0.40/0.50/0.65
LCC*2	Leadless Chip Carrier	1.016/1.27
QFN	Quad Flat Non-Leaded Package	
BGA	Ball Grid Array	1.27/1.0
FBGA	Fine pitch Ball Grid Array	0.8/0.75/0.65/0.5
DTP	Dual Tape Carrier Package	—
QTP	Quad Tape Carrier Package	—

*1: Joint Electron Device Engineering Council

*2: Package name used by Fujitsu